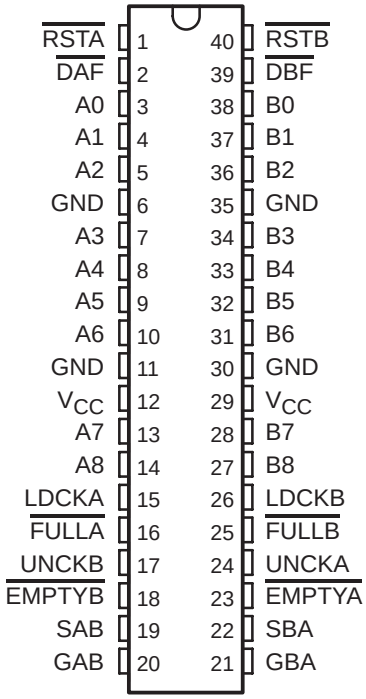
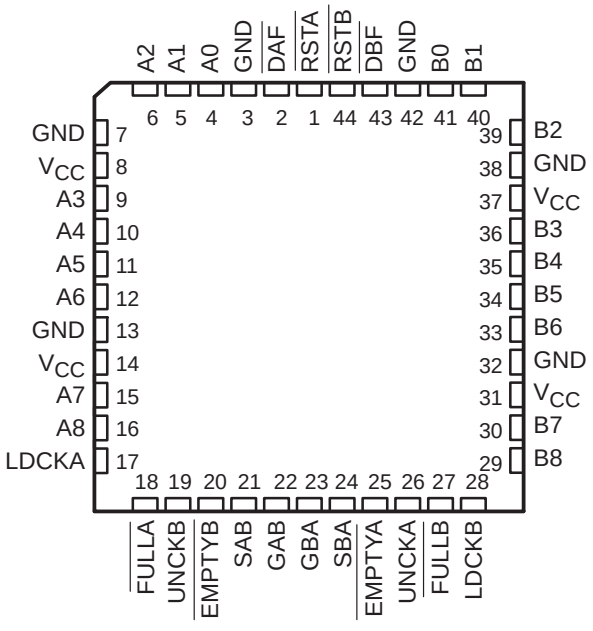
- **Independent Asychronous Inputs and Outputs**
- **Bidirectional**
- **32 Words by 9 Bits**
- **Programmable Depth**
- **Data Rates from 0 to 40 MHz**
- **Fall-Through Time . . . 22 ns Typ**
- **3-State Outputs**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

This 576-bit memory uses advanced low-power Schottky IMPACT-X™ technology and features high speed and fast fall-through times. It consists of two FIFOs organized as 32 words by 9 bits each.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

The SN74ALS2238 consists of bus-transceiver circuits, two 32 × 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enables GAB and GBA are provided to control the transceiver functions. The SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low level selects real-time data and a high selects stored data. Eight fundamental bus-management functions can be performed as shown in Figure 1.

Data on the A or B data bus, or both, is written into the FIFOs on a low-to-high transition at the load clock (LDCKA or LDCKB) input and is read out on a low-to-high transition at the unload clock (UNCKA or UNCKB) input. The memory is full when the number of words clocked in exceeds, by the defined depth, the number of words clocked out.

When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

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description (continued)

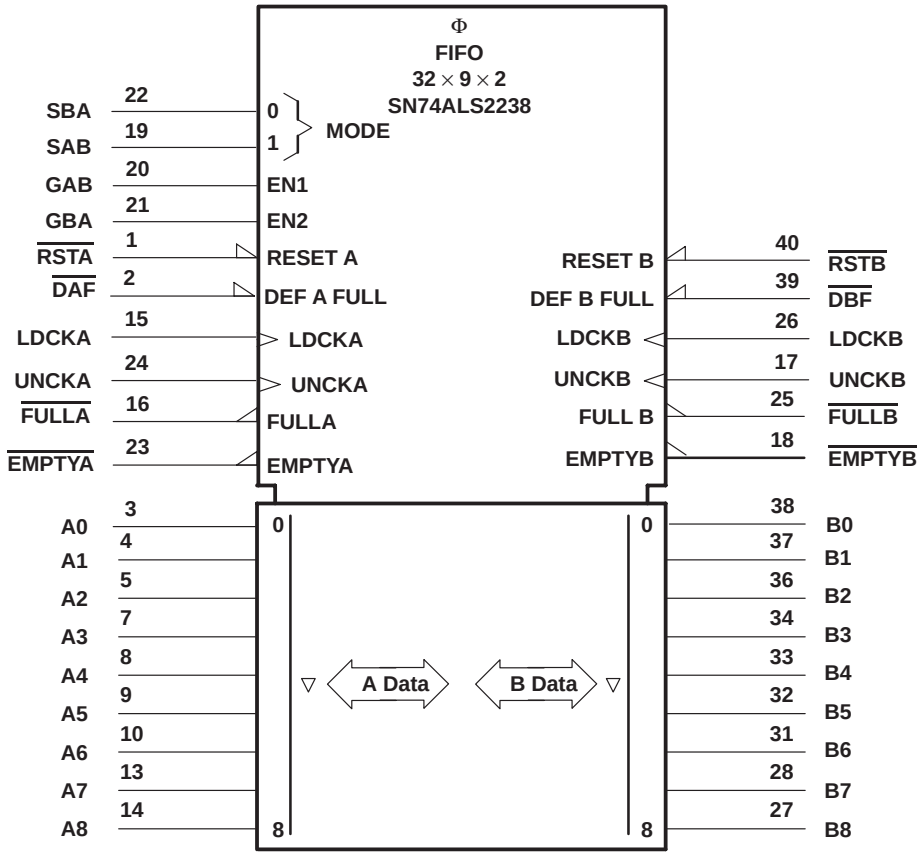
Status of the FIFO memories is monitored by the $\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$, $\overline{\text{EMPTYA}}$, and $\overline{\text{EMPTYB}}$ output flags. The $\overline{\text{FULLA}}$ and $\overline{\text{FULLB}}$ are definable full flags. A high-to-low transition on $\overline{\text{DAF}}$ stores the binary value of A0 through A4 into a register for use as the value of X. A high-to-low transition on $\overline{\text{DBF}}$ stores the binary value of B0 through B4 into a register for use as the value of Y. In this way, the depth of either FIFO can be defined to be one to 32 words deep. The value of X and Y must be defined after power up or the stored value of X and Y will be ambiguous. The $\overline{\text{FULLA}}$ and $\overline{\text{FULLB}}$ outputs are low when their corresponding memories are full and high when the memories are not full.

The $\overline{\text{EMPTYA}}$ and $\overline{\text{EMPTYB}}$ outputs are low when their corresponding memories are empty and high when they are not empty. The status flag outputs are always active.

A low-level pulse on the $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ inputs resets the control pointers on FIFO A or FIFO B and also sets $\overline{\text{EMPTYA}}$ low and $\overline{\text{FULLA}}$ high or $\overline{\text{EMPTYB}}$ low and $\overline{\text{FULLB}}$ high. The outputs are not reset to any specific logic levels. With $\overline{\text{DAF}}$ at a low level, a low-level pulse on $\overline{\text{RSTA}}$ sets FIFO A to a depth of 32 − X, where X is the value stored above. With $\overline{\text{DAF}}$ at a high level, a low level pulse on $\overline{\text{RSTA}}$ sets FIFO A to a depth of 32 words. The depth of FIFO B is set in a similar manner. The first low-to-high transition on LDCKA or LDCKB, either after a reset pulse or from an empty condition, will cause $\overline{\text{EMPTYA}}$ or $\overline{\text{EMPTYB}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

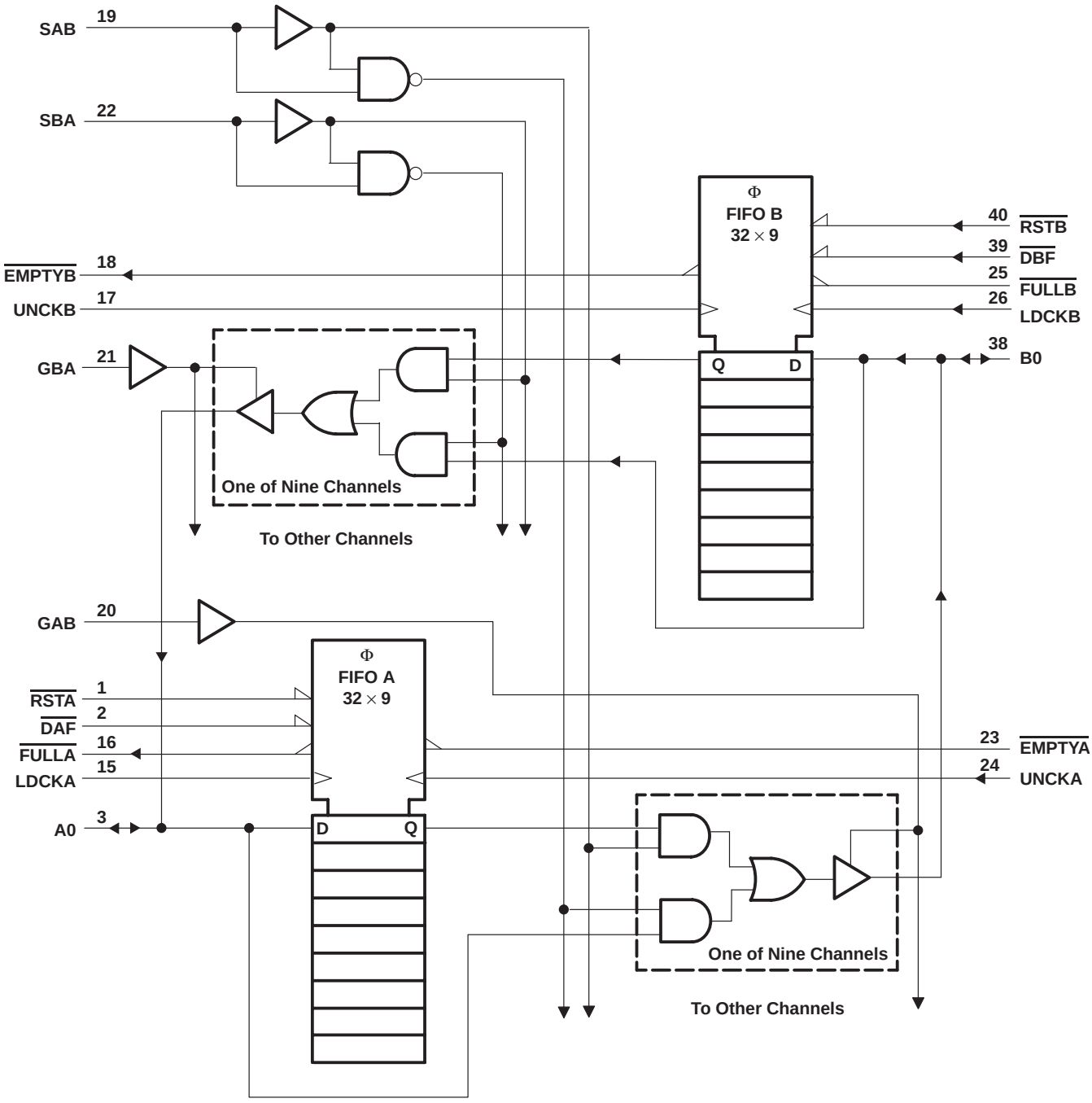
The SN74ALS2238 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)



Pin numbers shown are for the N package.

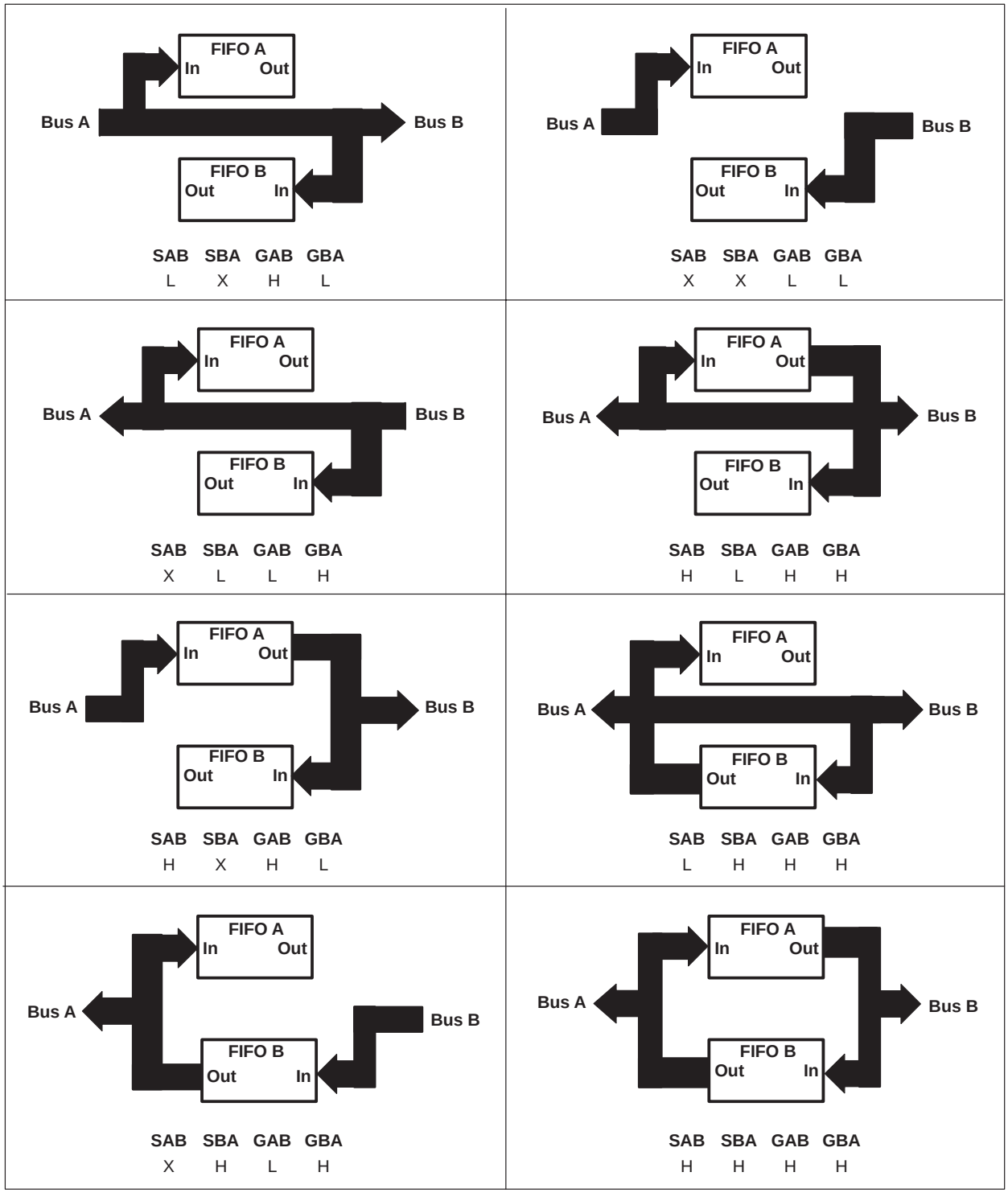
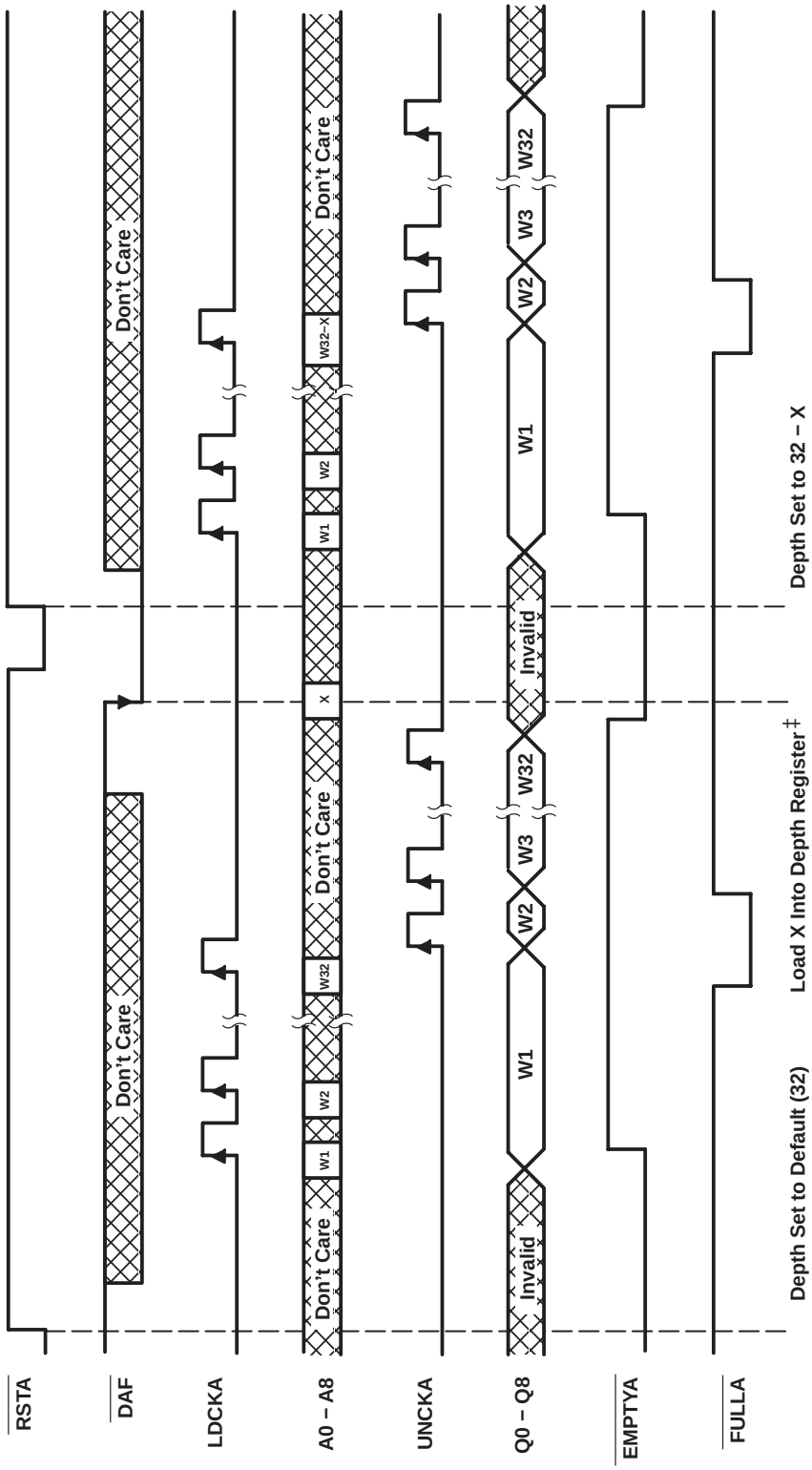


Figure 1. Bus-Management Functions

timing diagram for FIFO A†



† Operation of FIFO B is identical to that of FIFO A.
‡ X includes A0 through A4 only. A5 through A8 are ignored.

SELECT-MODE CONTROL TABLE

CONTROL		OPERATION	
SAB	SBA	A BUS	B BUS
L	L	Real-time B to A bus	Real-time A to B bus
L	H	FIFO B to A bus	Real-time A to B bus
H	L	Real-time B to A bus	FIFO A to B bus
H	H	FIFO B to A bus	FIFO A to B bus

OUTPUT-ENABLE CONTROL TABLE

CONTROL		OPERATION	
GAB	GBA	A BUS	B BUS
H	H	A bus enabled	B bus enabled
L	H	A bus enabled	Isolation/input to B bus
H	L	Isolation/input to A bus	B bus enabled
L	L	Isolation/input to A bus	Isolation/input to B bus

programming procedure for depth of FIFO A†

Program:

Step 1. With $\overline{\text{RSTA}}$ at a high level, take $\overline{\text{DAF}}$ from a high level to a low level. The high-to-low transition on $\overline{\text{DAF}}$ stores the binary value of A0−A4 for use as the value of X in defining the depth of FIFO A.

Step 2. With $\overline{\text{DAF}}$ held low, pulse the $\overline{\text{RSTA}}$ signal low. On the low-to-high transition of $\overline{\text{RSTA}}$, FIFO A is set to a depth of 32 − X, where X is the value of A0−A4 stored above.

Step 3. To redefine the depth of FIFO A to 32 words, hold $\overline{\text{DAF}}$ at a high level and pulse the $\overline{\text{RSTA}}$ signal low.

† The programming procedures used to define the depth of FIFO B are the same as the procedure above.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Maximum junction temperature . . . . . 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	A or B ports			−15	mA
		Status flags			−0.4	
I_{OL}	Low-level output current	A or B ports			24	mA
		Status flags			8	
f_{clock}	Clock frequency	LDCKA or LDCKB	0		40	MHz
		UNCKA or UNCKB	0		40	
t_w	Pulse duration	$\overline{RSTA}$ or $\overline{RSTB}$ low	17			ns
		LDCKA or LDCKB low	12.5			
		LDCKA or LDCKB high	10			
		UNCKA or UNCKB low	12.5			
		UNCKA or UNCKB high	10			
		$\overline{DAF}$ or $\overline{DBF}$ high	10			
t_{su}	Setup time	Data before LDCKA or LDCKB↑	7			ns
		Define depth: D4 − D0 before $\overline{DAF}$ or $\overline{DBF}$↓	6			
		Define depth: $\overline{DAF}$ or $\overline{DBF}$↓ before $\overline{RSTA}$ or $\overline{RSTB}$↑	45			
		Define depth (32): $\overline{DAF}$ or $\overline{DBF}$ high before $\overline{RSTA}$ or $\overline{RSTB}$↑	32			
		LDCKA or LDCKB (inactive) before $\overline{RSTA}$ or $\overline{RSTB}$↑	5			
t_h	Hold time	Data after LDCKA or LDCKB↑	3			ns
		Define depth: D4 − D0 after $\overline{DAF}$ or $\overline{DBF}$↓	4			
		Define depth: $\overline{DAF}$ or $\overline{DBF}$ low after $\overline{RSTA}$ or $\overline{RSTB}$↑	0			
		Define depth (32): $\overline{DAF}$ or $\overline{DBF}$ high after $\overline{RSTA}$ or $\overline{RSTB}$↑	0			
		LDCKA or LDCKB (inactive) after $\overline{RSTA}$ or $\overline{RSTB}$↑	5			
T_A	Operating free-air temperature		0		70	°C

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCKA or LDCKB and UNCKA or UNCKB clock inputs. Any excessive noise or glitching on the clock inputs (which violates the V_{IL}, V_{IH}, or minimum pulse duration limits) can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	A or B ports	V_{CC} = 4.5 V,	I_{OH} = − 2 mA	V_{CC}−2			
		V_{CC} = 4.5 V,	I_{OH} = − 3 mA	2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_I	$\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports					0.2	
I_{IH}	$\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports‡					40	
I_{IL}	$\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LCKA, LDCKB, UNCKA, UNCKB	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
	A or B ports‡					−0.4	
I_O§	A or B ports‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−130	mA
	Status flags			−15		−100	
I_{CC}		V_{CC} = 5.5 V			190	350	mA

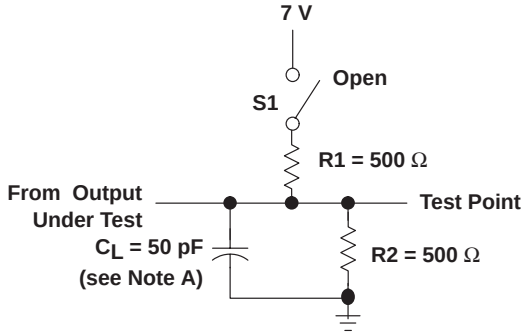
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the offstate output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
f_{max}	LDCK, UNCK		40			MHz
t_{pd}	LDCKA↑, LDCKB↑	B, A	7	22	33	ns
	UNCKA↑, UNCKB↑		7	20	29	
t_{PLH}	LDCKA↑, LDCKB↑	$\overline{EMPTYA}$, $\overline{EMPTYB}$	5	12	22	ns
t_{PHL}	UNCKA↑, UNCKB↑		5	12	22	
t_{PHL}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	$\overline{EMPTYA}$, $\overline{EMPTYB}$	5	12	22	ns
t_{PHL}	LDCKA↑, LDCKB↑	$\overline{FULLA}$, $\overline{FULLB}$	5	12	22	ns
t_{PLH}	UNCKA↑, UNCKB↑	$\overline{FULLA}$, $\overline{FULLB}$	5	12	23	ns
	$\overline{RSTA}$↓, $\overline{RSTB}$↓		6	15	28	
t_{pd}	SAB, SBA‡	B, A	2	11	18	ns
	A/B		2	8	15	
t_{en}	GBA, GAB	A, B	2	6	15	ns
t_{dis}	GBA, GAB	A, B	1	5	12	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

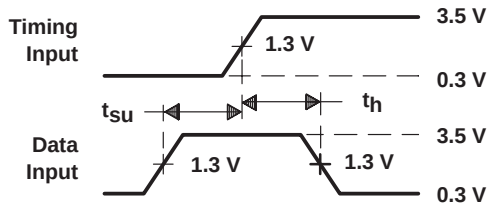
PARAMETER MEASUREMENT INFORMATION



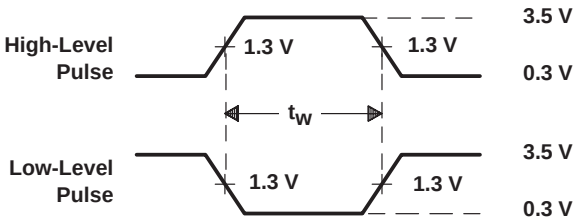
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

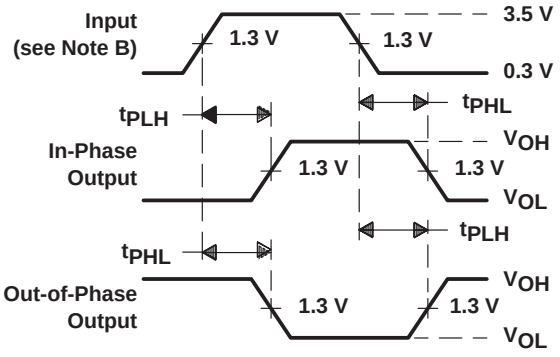
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



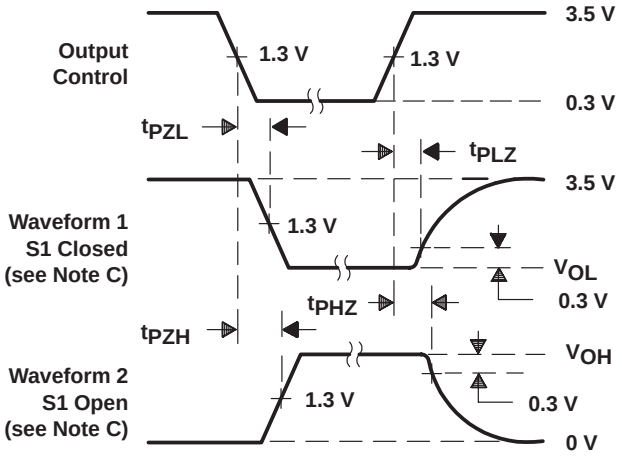
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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