

Document Title

4Mx4 bit Dynamic RAM with Fast Page Mode

Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0A	Initial Draft	June 14,2002	Preliminary
0B	Chang working range from $V_{CC}=1.9V\sim 2.4V$ to $V_{CC}=1.9V\sim 2.7V$, $V_{IH}=1.4V$ to $V_{IH}=1.6V$	July 31,2002	

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4M x 4 (16-MBIT) DYNAMIC RAM WITH FAST PAGE MODE

FEATURES

- Fast Page Mode Access Cycle
- TTL compatible inputs and outputs
- Refresh Interval:
 - 2,048 cycles/32 ms
 - 4,096 cycles/64 ms
- Refresh Mode: $\overline{\text{RAS}}$ -Only, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ (CBR), and Hidden
- JEDEC standard pinout
- Single power supply: 1.9V – 2.7V

DESCRIPTION

The *ICSI* 44052/44054 Series is a 4,194,304 x 4-bit high-performance CMOS Dynamic Random Access Memory. The Fast Page Mode allows 2,048 or 4,096 random accesses within a single row with access cycle time as short as 20 ns per 4-bit word.

These features make the 44052/44054 Series ideally suited for digital signal processing, and low power portable audio applications.

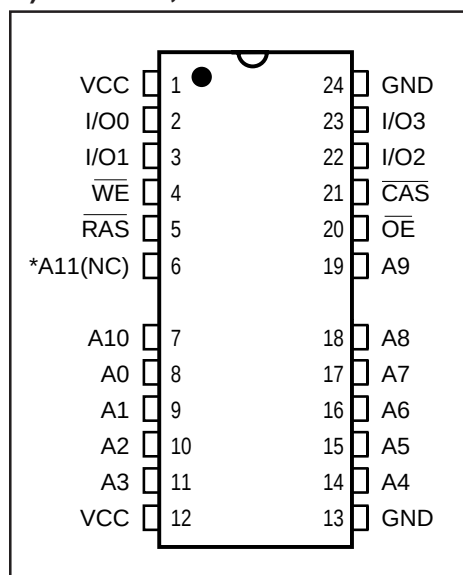
The 44052/44054 Series is packaged in a 26-pin 300mil SOJ and a 26 pin TSOP-2

KEY TIMING PARAMETERS

Parameter	-70	-100	Unit
RAS Access Time (t_{RAC})	70	100	ns
CAS Access Time (t_{CAC})	20	25	ns
Column Address Access Time (t_{AA})	35	50	ns
Fast Page Mode Cycle Time (t_{PC})	45	60	ns
Read/Write Cycle Time (t_{RC})	130	180	ns

PIN CONFIGURATION

24 (26) Pin SOJ, TSOP-2

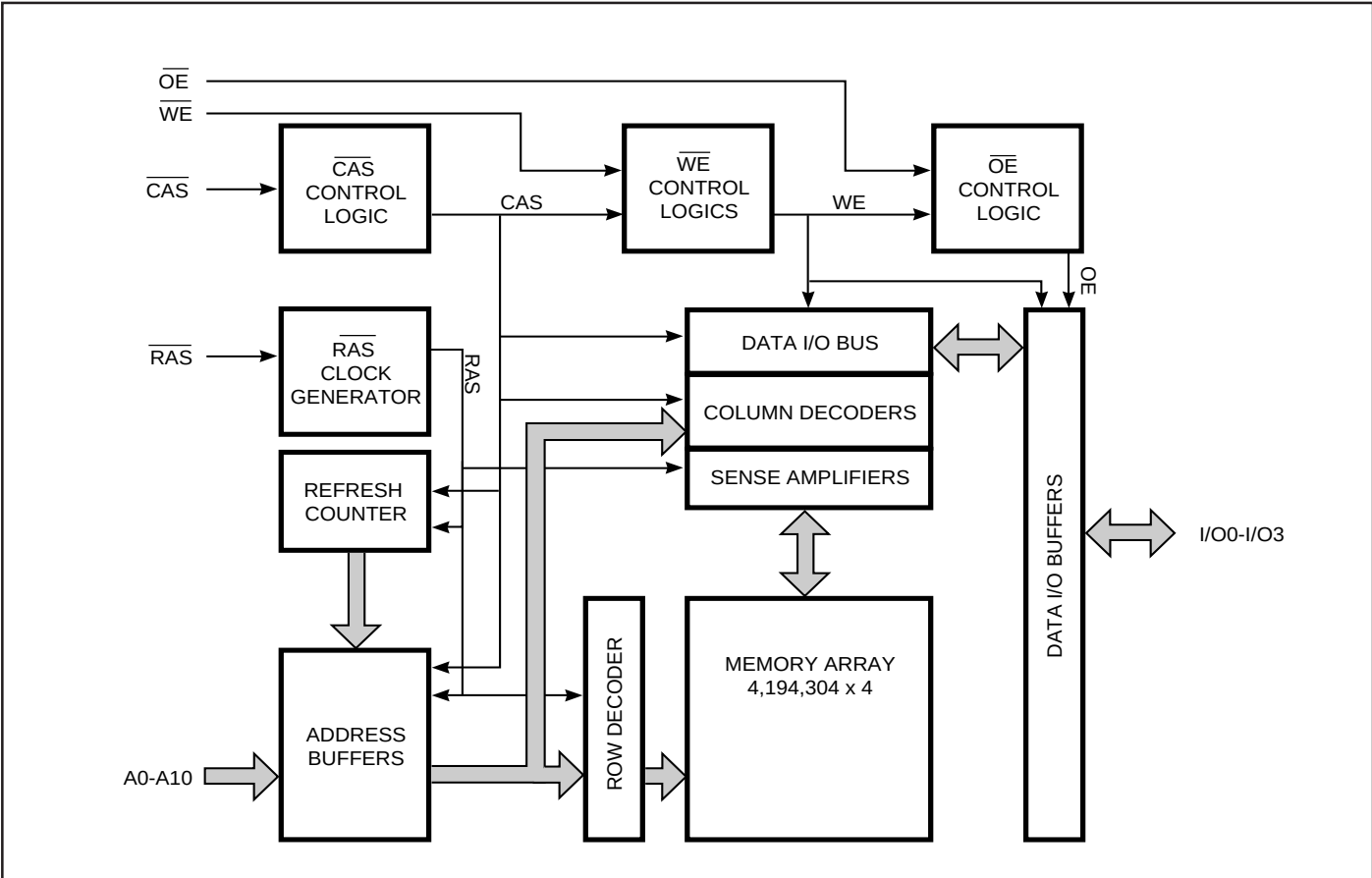


PIN DESCRIPTIONS

A0-A11	Address Inputs (4K Refresh)
A0-A10	Address Inputs (2K Refresh)
I/O0-3	Data Inputs/Outputs
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
Vcc	Power
GND	Ground

*A11 is NC for 2K Refresh devices.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Function	RAS	CAS	WE	OE	Address tr/tc	I/O
Standby	H	H	X	X	X	High-Z
Read	L	L	H	L	ROW/COL	DoUT
Write: Word (Early Write)	L	L	L	X	ROW/COL	DiN
Read-Write	L	L	H→L	L→H	ROW/COL	DoUT, DiN
Hidden Refresh	Read	L→H→L	L	H	ROW/COL	DoUT
	Write ⁽¹⁾	L→H→L	L	L	ROW/COL	DiN
RAS-Only Refresh	L	H	X	X	ROW/NA	High-Z
CBR Refresh	H→L	L	X	X	X	High-Z

Note:

1. EARLY WRITE only.

Functional Description

The IC41SV44052 and IC41LV44054 are CMOS DRAMs optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 11 or 12 address bits. These are entered 11 bits (A0-A10) at a time for the 2K refresh device or 12 bits (A0-A11) at a time for the 4K refresh device. The row address is latched by the Row Address Strobe (RAS). The column address is latched by the Column Address Strobe (CAS). $\overline{\text{RAS}}$ is used to latch the first nine bits and $\overline{\text{CAS}}$ is used the latter ten bits.

Memory Cycle

A memory cycle is initiated by bring $\overline{\text{RAS}}$ LOW and it is terminated by returning both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH. To ensure proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. A new cycle must not be initiated until the minimum precharge time t_{RP} , t_{CP} has elapsed.

Read Cycle

A read cycle is initiated by the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{OE}}$, whichever occurs last, while holding $\overline{\text{WE}}$ HIGH. The column address must be held for a minimum time specified by t_{AR} . Data Out becomes valid only when t_{RAC} , t_{AA} , t_{CAC} and t_{OEA} are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

Write Cycle

A write cycle is initiated by the falling edge of $\overline{\text{CAS}}$ and $\overline{\text{WE}}$, whichever occurs last. The input data must be valid at or before the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$, whichever occurs last.

Refresh Cycle

To retain data, 2,048 refresh cycles are required in each 32 ms period, or 4,096 refresh cycles are required in each 64ms period. There are two ways to refresh the memory:

1. By clocking each of the 2,048 row addresses (A0 through A10) or 4096 row addresses (A0 through A11) with $\overline{\text{RAS}}$ at least once every 32 ms or 64ms respectively. Any read, write, read-modify-write or $\overline{\text{RAS}}$ -only cycle refreshes the addressed row.
2. Using a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh is activated by the falling edge of $\overline{\text{RAS}}$, while holding $\overline{\text{CAS}}$ LOW. In $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle, an internal 11(12)-bit counter provides the row addresses and the external address inputs are ignored.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

Power-On

After application of the V_{CC} supply, an initial pause of 200 μs is required followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ signal).

During power-on, it is recommended that $\overline{\text{RAS}}$ track with V_{CC} or be held at a valid V_{IH} to avoid current surges.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameters	Rating	Unit
V _T	Voltage on Any Pin Relative to GND	−0.5 to +3.0	V
V _{CC}	Supply Voltage	−0.5 to +3.0	V
I _{OUT}	Output Current	50	mA
P _D	Power Dissipation	0.2	W
T _A	Commercial Operation Temperature	−10 to +70	°C
T _{STG}	Storage Temperature	−55 to +125	°C

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	1.9	2.7	V
V _{IH}	Input High Voltage	1.6	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	−0.3	0.6	V
T _A	Commercial Ambient Temperature	−10	70	°C

CAPACITANCE^(1,2)

Symbol	Parameter	Max.	Unit
C _{IN1}	Input Capacitance: A0-A10	5	pF
C _{IN2}	Input Capacitance: RAS, CAS, WE, OE	7	pF
C _{IO}	Data Input/Output Capacitance: I/O0-I/O3	7	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz.

ELECTRICAL CHARACTERISTICS⁽¹⁾

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed	Min.	Max.	Unit
I _{IL}	Input Leakage Current	Any input $0V \leq V_{IN} \leq V_{CC}$ Other inputs not under test = 0V		-5	5	μA
I _{IO}	Output Leakage Current	Output is disabled (Hi-Z) $0V \leq V_{OUT} \leq V_{CC}$		-5	5	μA
V _{OH}	Output High Voltage Level	I _{OH} = -2.0 mA		1.6	-	V
V _{OL}	Output Low Voltage Level	I _{OL} = 2 mA		-	0.8	V
I _{CC1}	Standby Current: TTL	$\overline{RAS}, \overline{CAS} \geq V_{IH}$		-	1	mA
I _{CC2}	Standby Current: CMOS	$\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2V$			0.5	mA
I _{CC3}	Operating Current: Random Read/Write ^(2,3,4) Average Power Supply Current	$\overline{RAS}, \overline{CAS}$, Address Cycling, t _{RC} = t _{RC} (min.)	-70 -100	- -	60 50	mA
I _{CC4}	Operating Current: Fast Page Mode ^(2,3,4) Average Power Supply Current	$\overline{RAS} = V_{IL}, \overline{CAS} \geq V_{IH}$ t _{RC} = t _{RC} (min.)	-70 -100	- -	45 35	mA
I _{CC5}	Refresh Current: $\overline{RAS}$ -Only ^(2,3) Average Power Supply Current	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH}$ t _{RC} = t _{RC} (min.)	-70 -100	- -	60 50	mA
I _{CC6}	Refresh Current: CBR ^(2,3,5) Average Power Supply Current	$\overline{RAS}, \overline{CAS}$ Cycling t _{RC} = t _{RC} (min.)	-70 -100	- -	60 50	mA

Notes:

1. An initial pause of 200 μs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ -Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each Fast page cycle.
5. Enables on-chip refresh and address counters.

AC CHARACTERISTICS^(1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-70		-100		Units
		Min.	Max.	Min.	Max.	
t _{RC}	Random READ or WRITE Cycle Time	130	–	180	–	ns
t _{RAC}	Access Time from $\overline{\text{RAS}}$ ^(6, 7)	–	70	–	100	ns
t _{CAC}	Access Time from $\overline{\text{CAS}}$ ^(6, 8, 15)	–	20	–	25	ns
t _{AA}	Access Time from Column-Address ⁽⁶⁾	–	35	–	50	ns
t _{RAS}	$\overline{\text{RAS}}$ Pulse Width	70	10K	100	10K	ns
t _{RP}	$\overline{\text{RAS}}$ Precharge Time	50	–	70	–	ns
t _{CAS}	$\overline{\text{CAS}}$ Pulse Width ⁽²³⁾	20	10K	25	10K	ns
t _{CP}	$\overline{\text{CAS}}$ Precharge Time ⁽⁹⁾	10	–	10	–	ns
t _{CSH}	$\overline{\text{CAS}}$ Hold Time ⁽²¹⁾	70	–	100	–	ns
t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time ^(10, 20)	20	50	25	75	ns
t _{ASR}	Row-Address Setup Time	0	–	0	–	ns
t _{RAH}	Row-Address Hold Time	10	–	15	–	ns
t _{ASC}	Column-Address Setup Time ⁽²⁰⁾	0	–	0	–	ns
t _{CAH}	Column-Address Hold Time ⁽²⁰⁾	15	–	20	–	ns
t _{AR}	Column-Address Hold Time (referenced to $\overline{\text{RAS}}$)	70	–	100	–	ns
t _{RAD}	$\overline{\text{RAS}}$ to Column-Address Delay Time ⁽¹¹⁾	15	35	20	50	ns
t _{RAL}	Column-Address to $\overline{\text{RAS}}$ Lead Time	35	–	50	–	ns
t _{RPC}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	5	–	5	–	ns
t _{RSH}	$\overline{\text{RAS}}$ Hold Time	20	–	25	–	ns
t _{CLZ}	$\overline{\text{CAS}}$ to Output in Low-Z ^(15, 24)	3	–	3	–	ns
t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time ⁽²¹⁾	5	–	5	–	ns
t _{OD}	Output Disable Time ^(19, 24)	3	20	3	25	ns
t _{OE}	Output Enable Time ^(15, 16)	–	20	–	25	ns
t _{OES}	OE LOW to $\overline{\text{CAS}}$ HIGH Setup Time	5	–	5	–	ns
t _{RCS}	Read Command Setup Time ^(17, 20)	0	–	0	–	ns
t _{RRH}	Read Command Hold Time (referenced to $\overline{\text{RAS}}$) ⁽¹²⁾	0	–	0	–	ns
t _{RCH}	Read Command Hold Time (referenced to $\overline{\text{CAS}}$) ^(12, 17, 21)	0	–	0	–	ns
t _{WCH}	Write Command Hold Time ⁽¹⁷⁾	10	–	15	–	ns
t _{WCR}	Write Command Hold Time (referenced to $\overline{\text{RAS}}$) ⁽¹⁷⁾	70	–	100	–	ns
t _{WP}	Write Command Pulse Width ⁽¹⁷⁾	10	–	15	–	ns
t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time ⁽¹⁷⁾	20	–	25	–	ns
t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time ^(17, 21)	20	–	25	–	ns
t _{WCS}	Write Command Setup Time ^(14, 17, 20)	0	–	0	–	ns
t _{DHR}	Data-in Hold Time (referenced to $\overline{\text{RAS}}$)	50	–	60	–	ns

AC CHARACTERISTICS (Continued)^(1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-70		-100		Units
		Min.	Max.	Min.	Max.	
t _{ACH}	Column-Address Setup Time to $\overline{\text{CAS}}$ Precharge during WRITE Cycle	15	–	15	–	ns
t _{OEH}	$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$ during READ-MODIFY-WRITE cycle ⁽¹⁸⁾	20	–	25	–	ns
t _{DS}	Data-In Setup Time ^(15, 22)	0	–	0	–	ns
t _{DH}	Data-In Hold Time ^(15, 22)	15	–	20	–	ns
t _{RWC}	READ-MODIFY-WRITE Cycle Time	185	–	240	–	ns
t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time during READ-MODIFY-WRITE Cycle ⁽¹⁴⁾	100	–	130	–	ns
t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time ^(14, 20)	45	–	55	–	ns
t _{AWD}	Column-Address to $\overline{\text{WE}}$ Delay Time ⁽¹⁴⁾	60	–	85	–	ns
t _{PC}	Fast Page Mode READ or WRITE Cycle Time	45	–	60	–	ns
t _{RASP}	Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	70	100K	100	100K	ns
t _{CPA}	Access Time from $\overline{\text{CAS}}$ Precharge ⁽¹⁵⁾	–	40	–	55	ns
t _{PRWC}	Fast Page Mode READ WRITE Cycle Time	100	–	120	–	ns
t _{OFF}	Output Buffer Turn-Off Delay from $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$ ^(13,15,19, 24)	3	15	3	15	ns
t _{CSR}	$\overline{\text{CAS}}$ Setup Time (CBR REFRESH) ^(20, 25)	5	–	5	–	ns
t _{CHR}	$\overline{\text{CAS}}$ Hold Time (CBR REFRESH) ^(21, 25)	10	–	10	–	ns
t _{ORD}	$\overline{\text{OE}}$ Setup Time prior to $\overline{\text{RAS}}$ during HIDDEN REFRESH Cycle	0	–	0	–	ns
t _{REF}	Auto Refresh Period 2,048 Cycles	–	32	–	32	ms
	Auto Refresh Period 4,096 Cycles	–	64	–	64	ms
t _r	Transition Time (Rise or Fall) ^(2, 3)	3	50	3	50	ns

AC TEST CONDITIONS

Output load: One TTL Load and 100 pF

Input timing reference levels: $V_{IH} = 1.6V$, $V_{IL} = 0.6V$

Output timing reference levels: $V_{OH} = 1.6V$, $V_{OL} = 0.8V$

Notes:

1. An initial pause of 200 μ s is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycle ($\overline{\text{RAS}}$ -Only or CBR) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. If CAS and $\overline{\text{RAS}} = V_{\text{IH}}$, data output is High-Z.
5. If $\text{CAS} = V_{\text{IL}}$, data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{MAX})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
8. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{MAX})$.
9. If CAS is LOW at the falling edge of $\overline{\text{RAS}}$, data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, CAS and $\overline{\text{RAS}}$ must be pulsed for t_{CP} .
10. Operation with the $t_{\text{RCD}} (\text{MAX})$ limit ensures that $t_{\text{RAC}} (\text{MAX})$ can be met. $t_{\text{RCD}} (\text{MAX})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{\text{RCD}} (\text{MAX})$ limit, access time is controlled exclusively by t_{CAC} .
11. Operation within the $t_{\text{RAD}} (\text{MAX})$ limit ensures that $t_{\text{RCD}} (\text{MAX})$ can be met. $t_{\text{RAD}} (\text{MAX})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{\text{RAD}} (\text{MAX})$ limit, access time is controlled exclusively by t_{AA} .
12. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
13. $t_{\text{OFF}} (\text{MAX})$ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL} .
14. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{MIN})$, the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD}} (\text{MIN})$, $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{MIN})$ and $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{MIN})$, the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until CAS and $\overline{\text{RAS}}$ or $\overline{\text{OE}}$ go back to V_{IH}) is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after CAS goes LOW result in a LATE WRITE ($\overline{\text{OE}}$ -controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding CAS input.
16. During a READ cycle, if $\overline{\text{OE}}$ is LOW then taken HIGH before CAS goes HIGH, I/O goes open. If $\overline{\text{OE}}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as $\overline{\text{WE}}$ going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if CAS remains LOW and $\overline{\text{OE}}$ is taken back to LOW after t_{OEH} is met.
19. The I/Os are in open during READ cycles once t_{OD} or t_{OFF} occur.
20. Determined by falling edge of CAS .
21. Determined by rising edge of CAS .
22. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. CAS must meet minimum pulse width.
24. The 3 ns minimum is a parameter guaranteed by design.
25. Enables on-chip refresh and address counters.

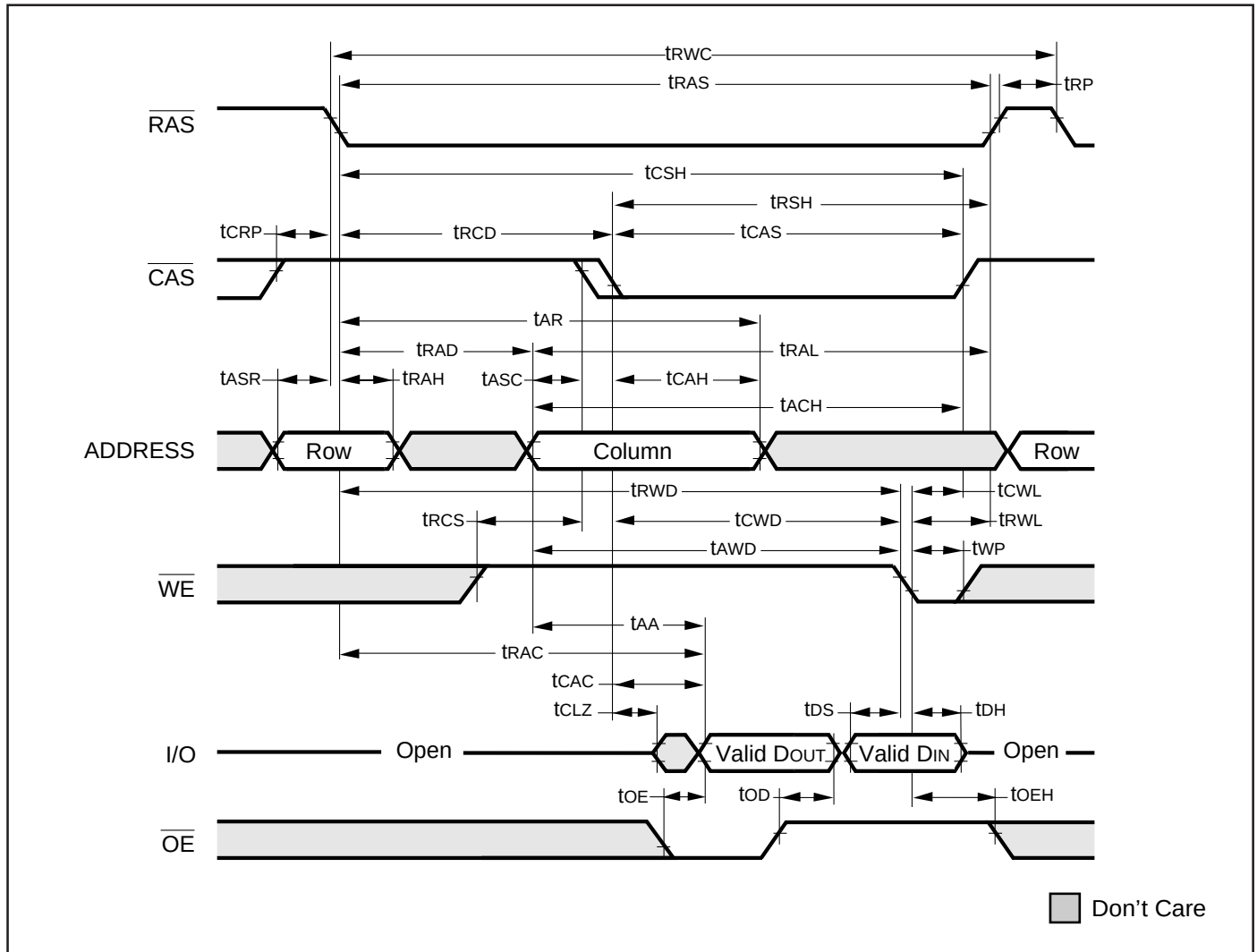
The diagram illustrates the timing relationships for a 2D DRAM array. The signals and their timing parameters are as follows:

- RAS**: Row Address Strobe. Timing parameters include t_{RC} (Row Cycle Time), t_{RAS} (Row Address Strobe Pulse Width), t_{RP} (Row Precharge Time), t_{CRP} (Row Precharge Delay), t_{RSH} (Row Strobe to Column Strobe Delay), and t_{RRH} (Row Strobe to Row Precharge Delay).
- CAS**: Column Address Strobe. Timing parameters include t_{CSH} (Column Strobe Pulse Width), t_{RCD} (Row to Column Delay), t_{CAS} (Column Address Strobe Pulse Width), and t_{RRH} (Row Strobe to Row Precharge Delay).
- ADDRESS**: Data Address. Timing parameters include t_{ASR} (Address Setup Time), t_{RAH} (Row Address Hold Time), t_{ASC} (Address Setup to Column Strobe Delay), t_{AL} (Address Hold to Column Strobe Delay), t_{CAH} (Column Address Hold Time), and t_{AR} (Row Address to Row Strobe Delay).
- WE**: Write Enable. Timing parameters include t_{RCS} (Row Strobe to Column Strobe Delay), t_{RCH} (Row Strobe to Row Precharge Delay), t_{AA} (Write Enable to Row Address Strobe Delay), t_{RAC} (Write Enable to Row Address Strobe Delay), t_{CAC} (Write Enable to Column Address Strobe Delay), and t_{CLZ} (Write Enable to Column Address Strobe Delay).
- I/O**: Data Input/Output. Timing parameters include t_{OE} (Output Enable Pulse Width), t_{OD} (Output Disable Delay), t_{OES} (Output Enable to Output Disable Delay), and $t_{OFF(1)}$ (Output Disable Delay).
- OE**: Output Enable. Timing parameters include t_{OE} (Output Enable Pulse Width), t_{OD} (Output Disable Delay), and t_{OES} (Output Enable to Output Disable Delay).

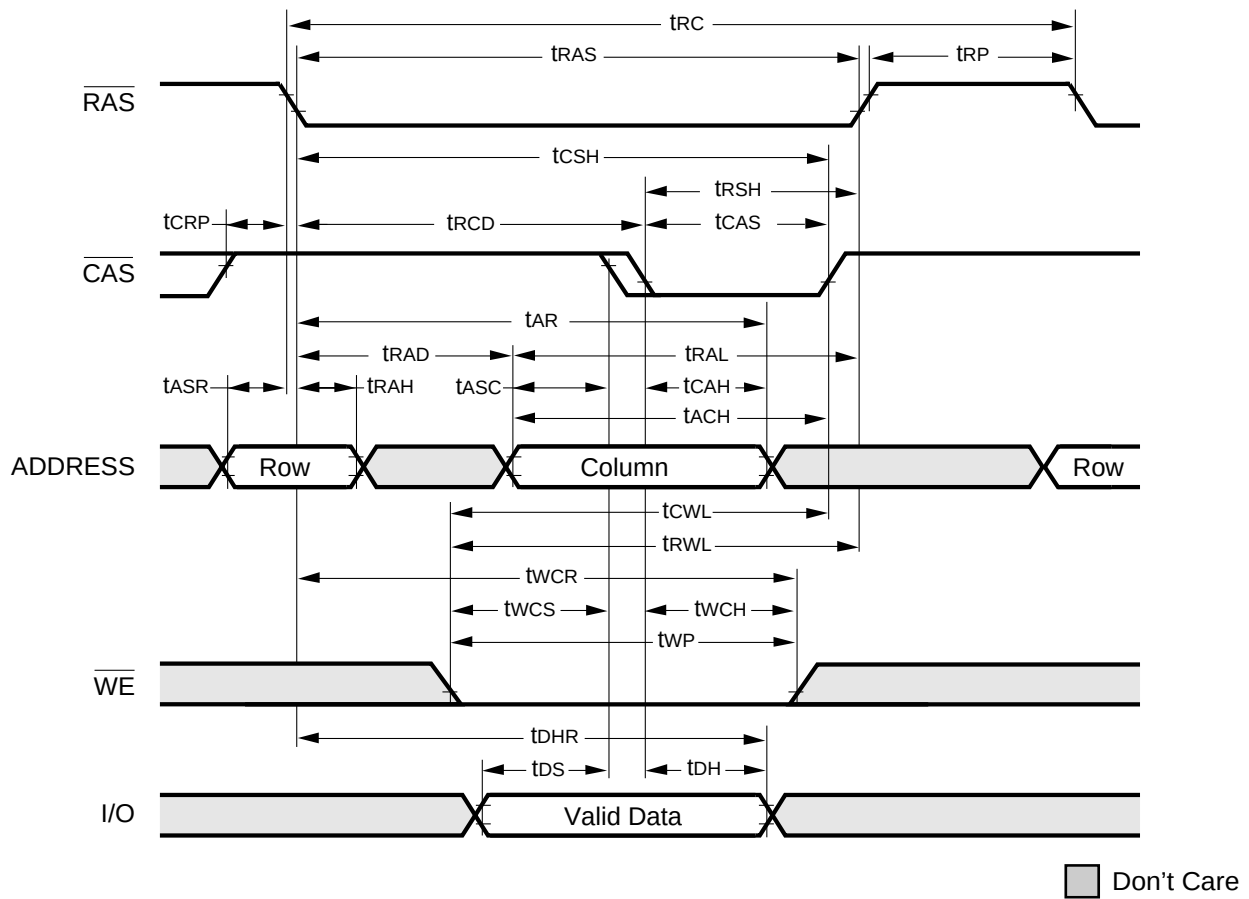
The diagram also shows the data flow from the I/O bus to the memory array, with the data being valid during the output enable period. The "Don't Care" region is indicated by a shaded area.

1. toff is referenced from rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.

READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)



EARLY WRITE CYCLE ($\overline{OE}$ = DON'T CARE)



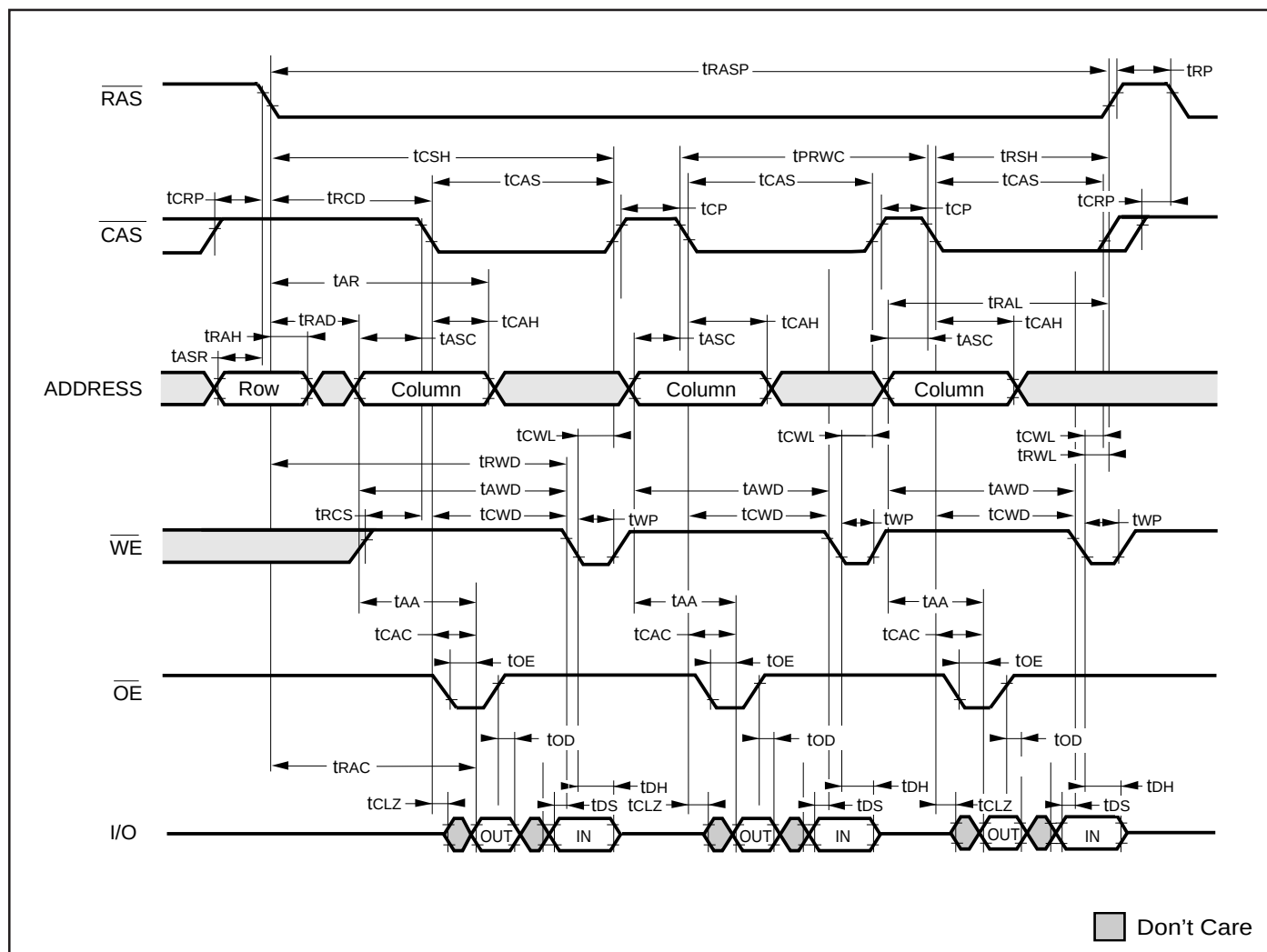
The diagram illustrates the timing relationships for a memory device. The signals shown are RAS, CAS, ADDRESS, WE, OE, and I/O. The ADDRESS signal is divided into Row and Column phases. The WE (Write Enable) signal is active low. The OE (Output Enable) signal is active low. The I/O signal is shown with data output (OUT) during the Row and Column phases. Various timing parameters are indicated by arrows and labels, such as tRASP (RAS pulse width), tCRP (CAS to RAS precharge), tRCD (RAS to CAS delay), tCAS (CAS pulse width), tPC (CAS to RAS precharge), tRSH (RAS to CAS setup), tTAR (RAS to ADDRESS delay), tTRAH (RAS to ADDRESS hold), tTRAD (RAS to ADDRESS delay), tTASC (RAS to ADDRESS setup), tTCAH (RAS to ADDRESS hold), tTAL (RAS to ADDRESS delay), tTCAH (RAS to ADDRESS hold), tTCS (RAS to CAS setup), tTAA (RAS to ADDRESS delay), tTAC (RAS to ADDRESS delay), tTOE (RAS to ADDRESS delay), tTRAC (RAS to ADDRESS delay), tTCLZ (RAS to ADDRESS delay), tTOD (RAS to ADDRESS delay), and tTRP (RAS pulse width).

The diagram illustrates the timing relationships for a memory device. The signals shown are $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, ADDRESS, $\overline{\text{WE}}$, $\overline{\text{OE}}$, and I/O. The ADDRESS signal is divided into Row and Column phases. The I/O signal is divided into Valid DIN and Valid DOUT phases. The timing parameters are defined as follows:

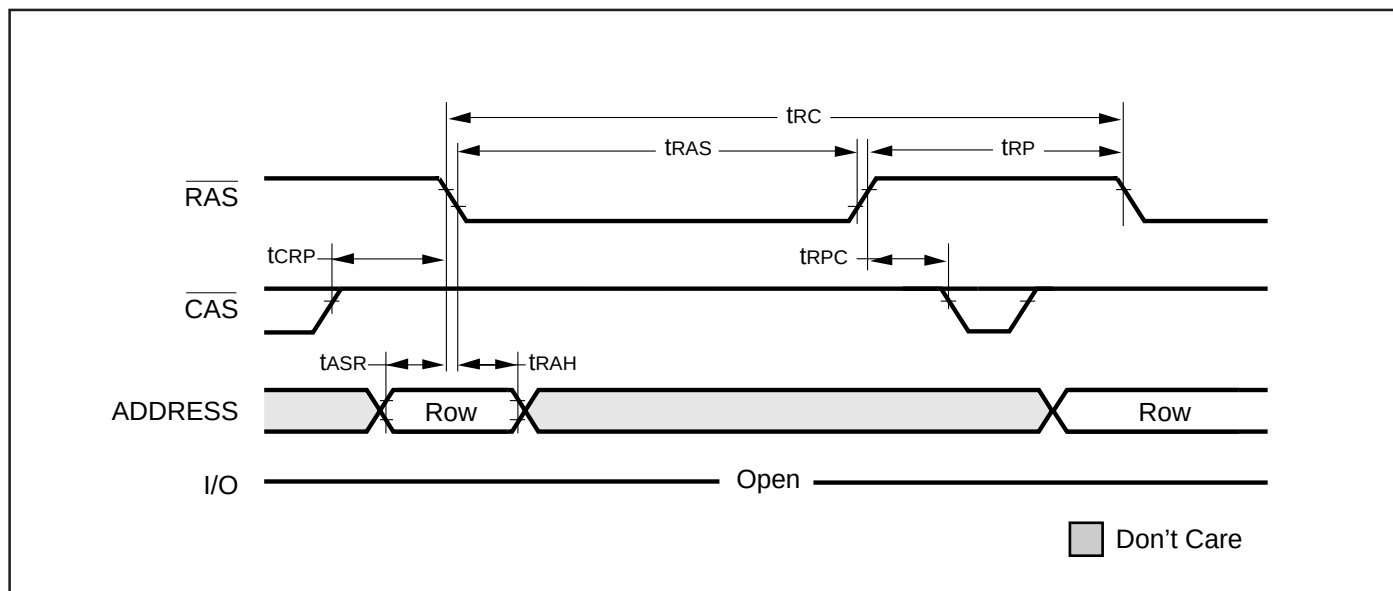
- t_{RASP} : RAS pulse width
- t_{CRP} : CAS to RAS setup time
- t_{RCD} : RAS to CAS delay
- t_{CAS} : CAS pulse width
- t_{CP} : CAS to RAS setup time
- t_{PC} : RAS to CAS delay
- t_{RSH} : RAS to CAS delay
- t_{CAS} : CAS pulse width
- t_{CRP} : CAS to RAS setup time
- t_{AR} : Address to RAS delay
- t_{RAH} : Address to RAS delay
- t_{ASR} : Address to RAS delay
- t_{RAD} : Address to RAS delay
- t_{ASC} : Address to RAS delay
- t_{CAH} : Address to RAS delay
- t_{CWL} : Column write latency
- t_{wCS} : Column write setup time
- t_{wCH} : Column write hold time
- t_{wP} : Column write pulse width
- t_{wCR} : Column write recovery time
- t_{DHR} : Data hold time
- t_{DS} : Data setup time
- t_{DH} : Data hold time
- t_{DQ} : Data output delay

Legend: Don't Care

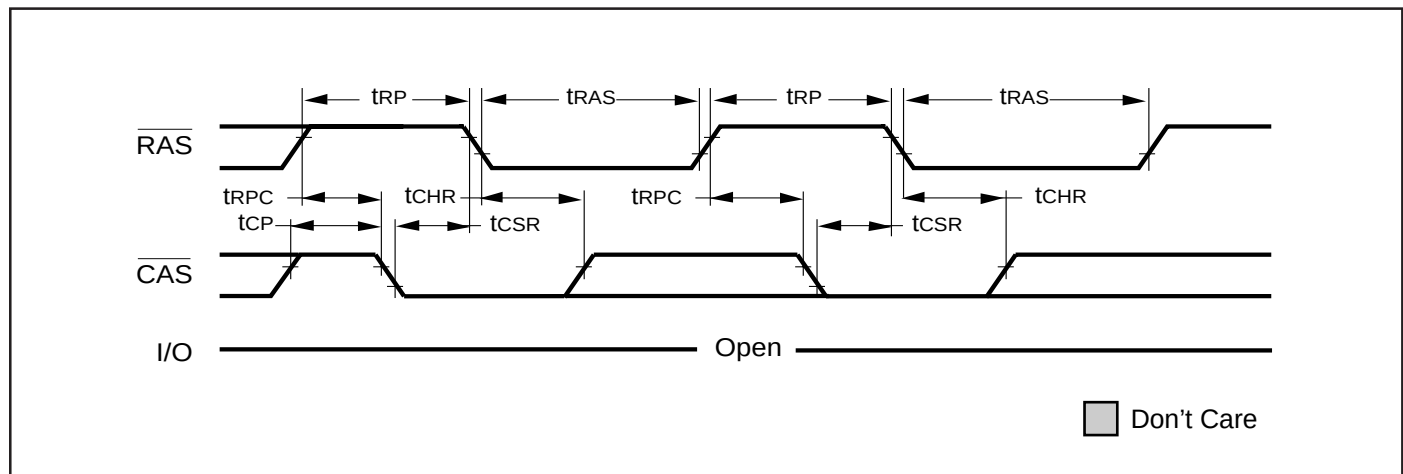
FAST PAGE MODE READ WRITE CYCLE (LATE WRITE AND READ-MODIFY-WRITE CYCLE)



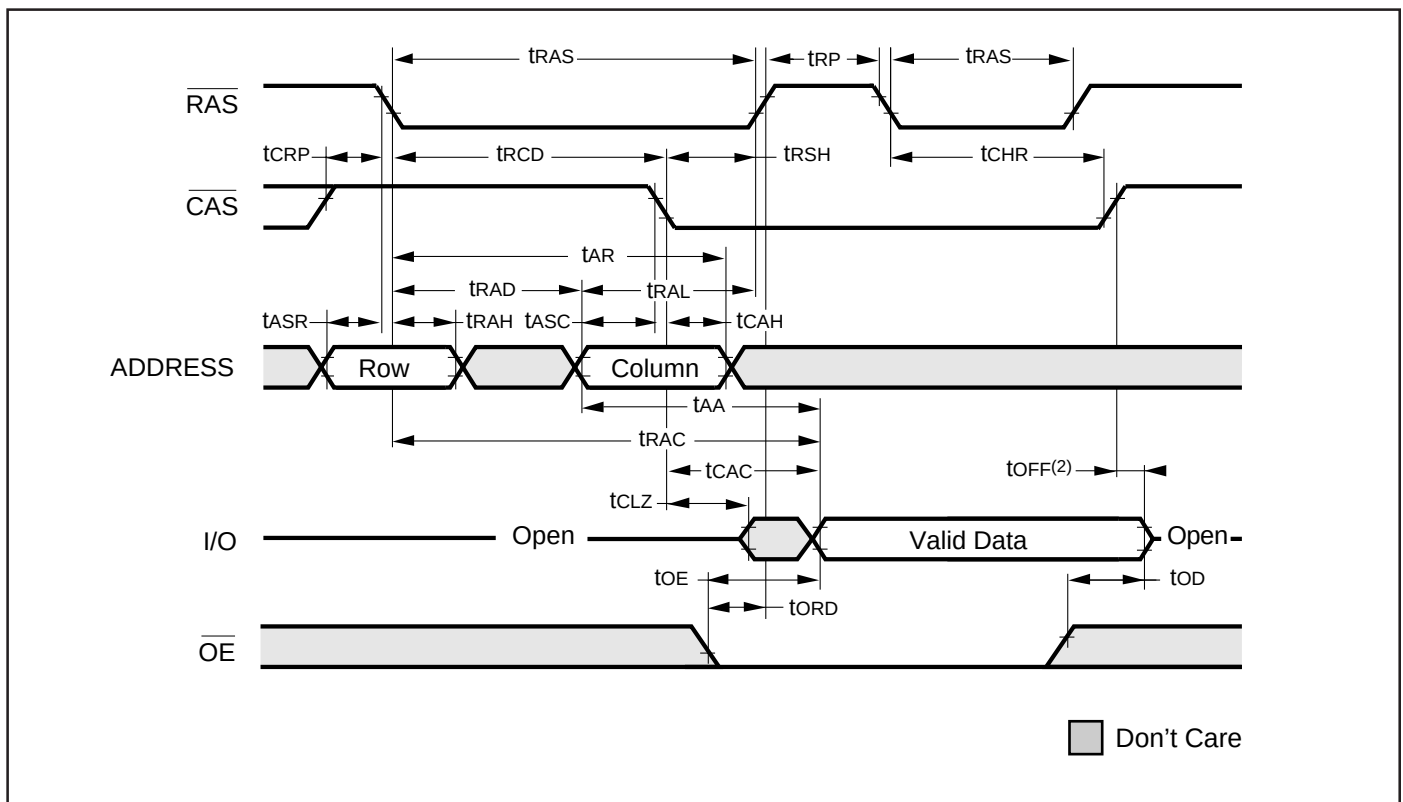
RAS-ONLY REFRESH CYCLE ($\overline{OE}$, $\overline{WE}$ = DON'T CARE)



CBR REFRESH CYCLE (Addresses; $\overline{WE}$, $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE⁽¹⁾ ($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



Notes:

1. A Hidden Refresh may also be performed after a Write Cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
2. t_{OFF} is referenced from rising edge of RAS or CAS, whichever occurs last.

ORDERING INFORMATION

Commercial Range: -10°C to 70°C

Voltage: 2.2V

Speed (ns)	Order Part No.	Package
70	IC41SV44052-70J	300mil SOJ
70	IC41SV44052-70T	300mil TSOP-2
70	IC41SV44052-70JG	300mil SOJ Pb-free
70	IC41SV44052-70TG	300mil TSOP-2 Pb-free
100	IC41SV44052-100J	300mil SOJ
100	IC41SV44052-100T	300mil TSOP-2
100	IC41SV44052-100JG	300mil SOJ Pb-free
100	IC41SV44052-100TG	300mil TSOP-2 Pb-free

Speed (ns)	Order Part No.	Package
70	IC41SV44054-70J	300mil SOJ
70	IC41SV44054-70T	300mil TSOP-2
70	IC41SV44054-70JG	300mil SOJ Pb-free
70	IC41SV44054-70TG	300mil TSOP-2 Pb-free
100	IC41SV44054-100J	300mil SOJ
100	IC41SV44054-100T	300mil TSOP-2
100	IC41SV44054-100JG	300mil SOJ Pb-free
100	IC41SV44054-100TG	300mil TSOP-2 Pb-free



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