PRELIMINARY

CY7C1399D

256K (32K x 8) Static RAM

Features

- **Pin- and function-compatible with CY7C1399B**
- **Single 3.3V power supply**
- **Ideal for low-voltage cache memory applications**
- **High speed**
  - **— t_{AA} = 8 ns**
- **Low active power**
  - **— I_{CC} = 60 mA @ 10 ns**
- **Low CMOS standby power**
  - **— I_{SB2} = 1.2 mA (“L” Version only)**
- **Data Retention at 2.0V**
- **Available in 28-SOJ and 28-TSOP I Pb-Free packages**

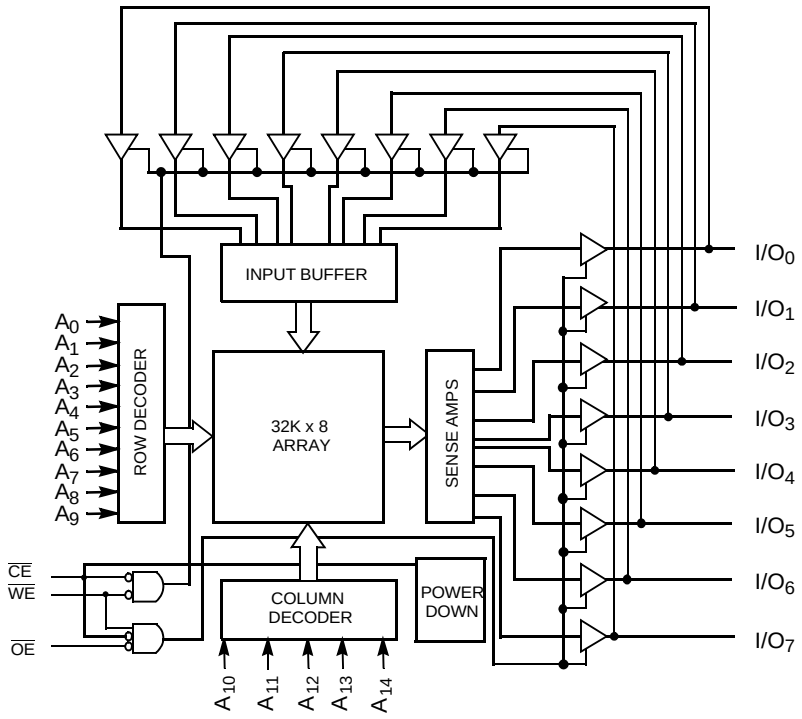
Functional Description[1]

The CY7C1399D is a high-performance 3.3V CMOS Static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and active LOW Output Enable ($\overline{OE}$) and tri-state drivers. The device has an automatic power-down feature, reducing the power consumption when deselected.

An active LOW Write Enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

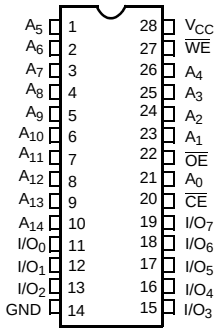
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable ($\overline{WE}$) is HIGH. The CY7C1399D is available in 28-pin standard 300-mil-wide SOJ and TSOP Type I Pb-Free packages.

Logic Block Diagram



Pin Configurations

SOJ
Top View



Note:

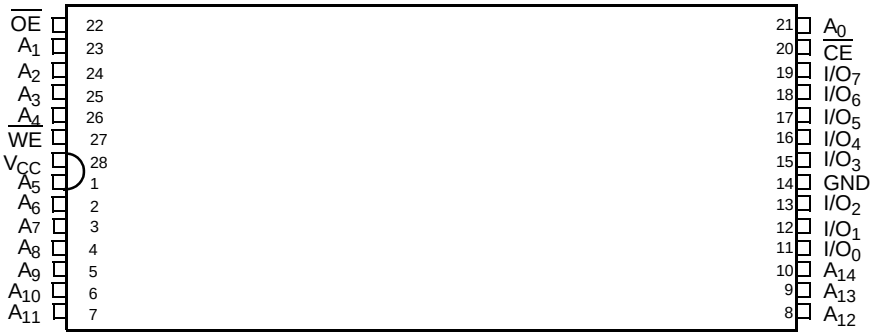
1. For guidelines on SRAM system design, please refer to the ‘System Design Guidelines’ Cypress application note, available on the internet at www.cypress.com.

Selection Guide

		1399D-10	1399D-12	1399D-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current		60	50	40	mA
Maximum CMOS Standby Current		3.0	3.0	3.0	mA
	L	1.2	1.2	1.2	

Pin Configuration

TSOP I
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[2] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[2] ..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ±300 mV
Industrial	–40°C to +85°C	3.3V ±300 mV

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C1399D-10 Min.	7C1399D-10 Max.	7C1399D-12 Min.	7C1399D-12 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[2]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current			–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$			60		50	mA
I_{SB1}	Automatic CE Power-down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH}, or V_{IN} ≤ V_{IL}, f = f_{MAX}			10		10	mA
			L		10		10	mA
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs[4]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, WE ≥ V_{CC} – 0.3V or WE ≤ 0.3V, f = f_{MAX}			3.0		3.0	mA
			L		1.2		1.2	mA

Parameter	Description	Test Conditions		7C1399D-15 Min.	7C1399D-15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage			–0.3	0.8	V
I_{IX}	Input Load Current			–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–1	+1	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$			40	mA
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH}, or V_{IN} ≤ V_{IL}, f = f_{MAX}			10	mA
			L		10	mA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs[4]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC}–0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, WE≥V_{CC}–0.3V or WE≤ 0.3V, f=f_{MAX}			3.0	mA
			L		1.2	mA

Notes:
2. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 2V for pulse durations of less than 20 ns.
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Device draws low standby current regardless of switching on the addresses.
5. Tested initially and after any design or process changes that may affect these parameters.

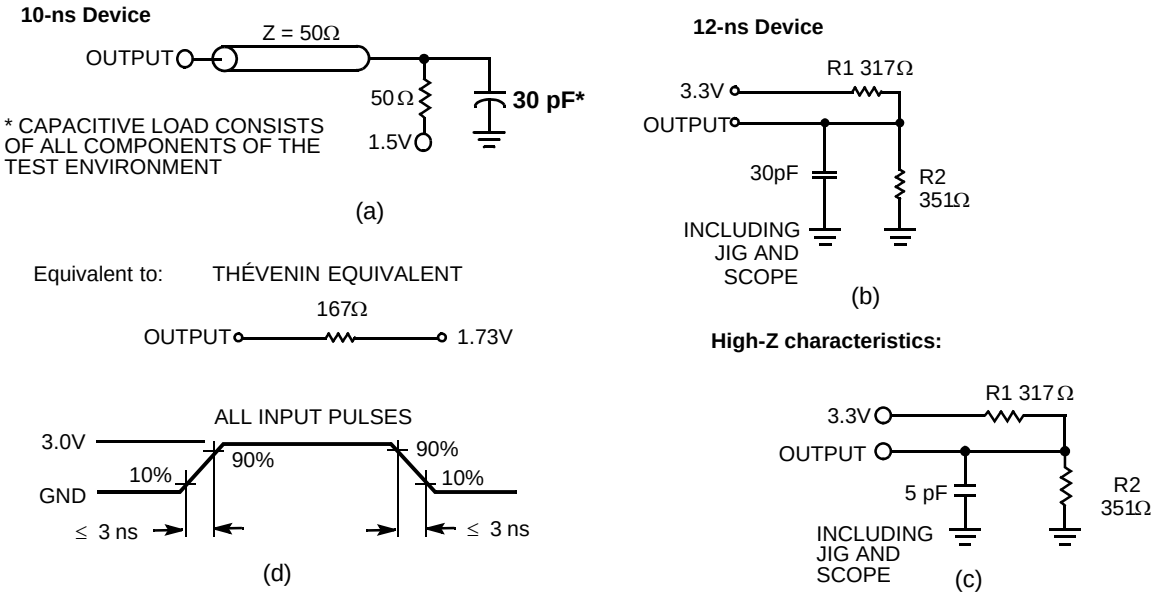
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	5	pF
C_{IN}: Controls			6	pF
C_{OUT}	Output Capacitance		6	pF

Thermal Resistance[5]

Parameter	Description	Test Conditions	All – Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[5]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[5]		TBD	°C/W

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range [7]

Parameter	Description	1399D-10		1399D-12		1399D-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{power}[6]	V_{CC}(typical) to the first access	100		100		100		µs
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		5		5		6	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		ns

Notes:
6. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and capacitance C_L = 30 pF.

Switching Characteristics Over the Operating Range (continued)[7]

Parameter	Description	1399D-10		1399D-12		1399D-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		5		6		7	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15	ns
Write Cycle[10, 11]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		8		10		ns
t_{AW}	Address Set-Up to Write End	7		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		10		ns
t_{SD}	Data Set-Up to Write End	5		7		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[10]		7		7		7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		ns

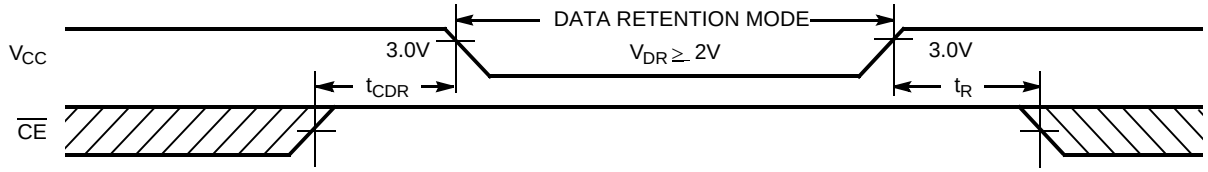
Notes:

8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, t_{HZWE} are specified with C_L = 5 pF as in AC Test Loads. Transition is measured ±200 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics (Over the Operating Range)

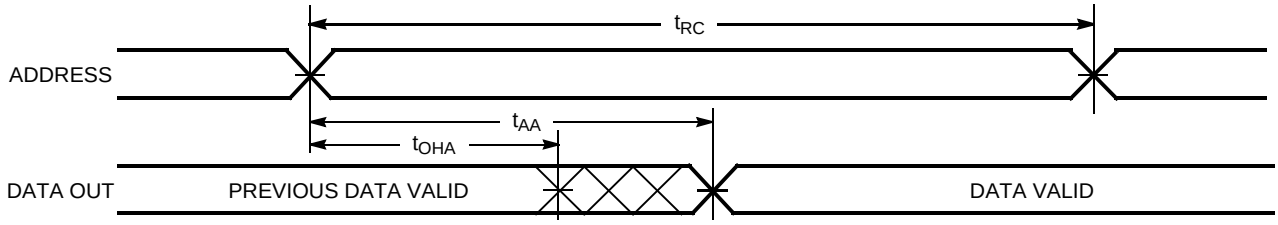
Parameter	Description		Conditions	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	Non-L, Com'l / Ind'l	$\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		3	mA
		L-Version Only			1.2	mA
t_{CDR} [5]	Chip Deselect to Data Retention Time			0		ns
t_R [12]	Operation Recovery Time			t_{RC}		ns

Data Retention Waveform

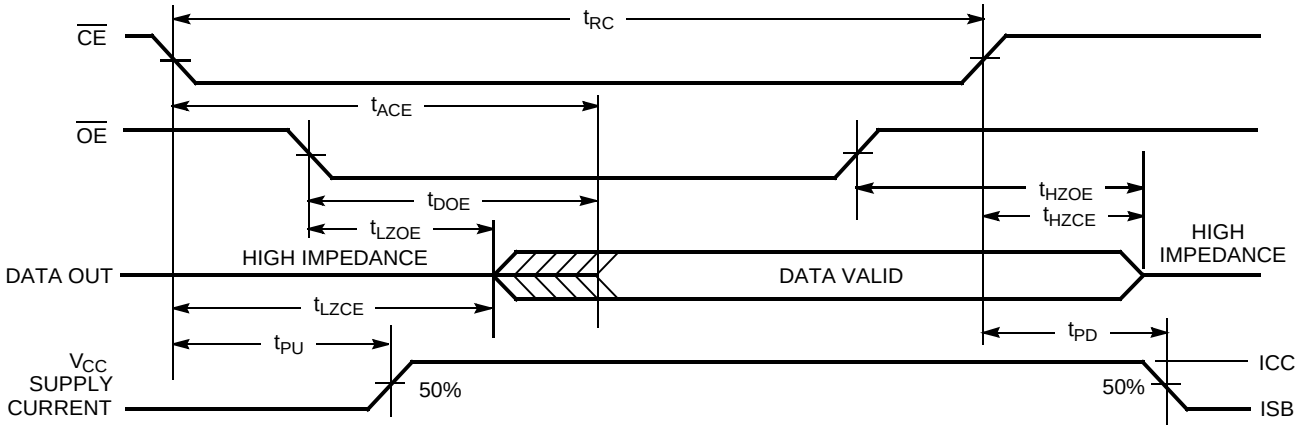


Switching Waveforms

Read Cycle No. 1 [13, 14]



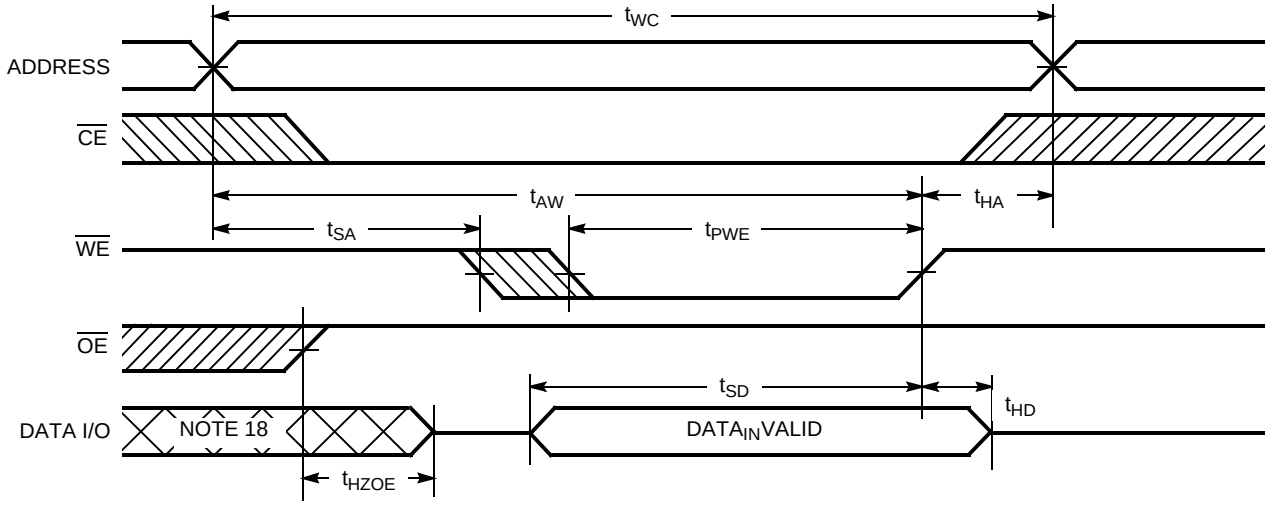
Read Cycle No. 2 [14, 15]



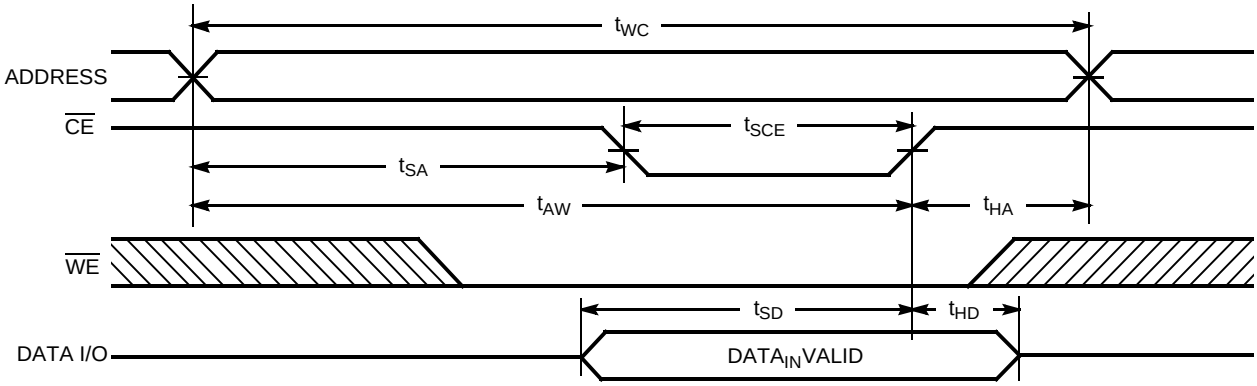
Notes:
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50\ \mu s$ or stable at $V_{CC(min.)} \geq 50\ \mu s$.
13. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
14. $\overline{WE}$ is HIGH for read cycle.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

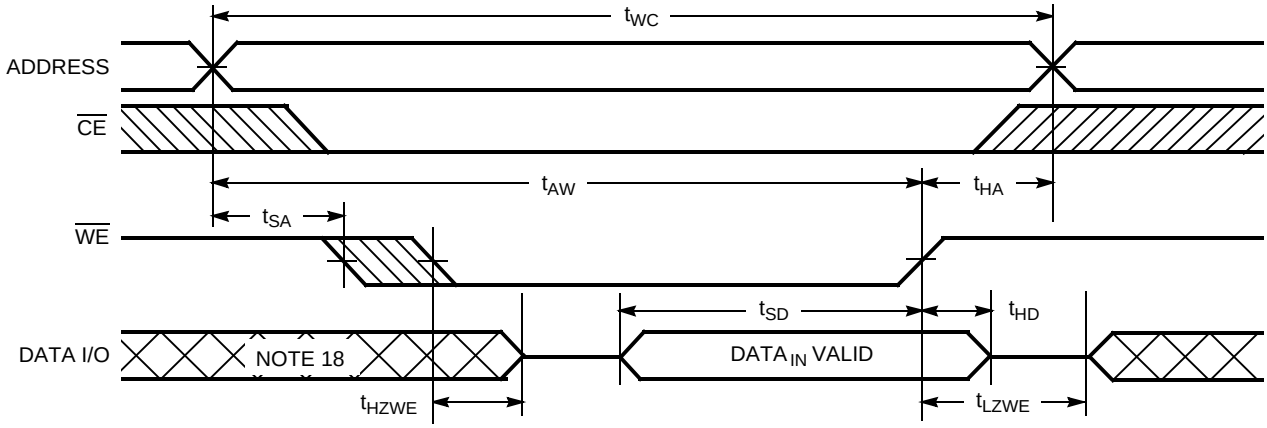
Write Cycle No. 1 (WE Controlled)[10, 16, 17]



Write Cycle No. 2 (CE Controlled)[10, 16, 17]



Write Cycle No. 3 (WE Controlled, OE LOW)[11, 17]



Notes:
16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
18. During this period, the I/Os are in the output state and input signals should not be applied.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

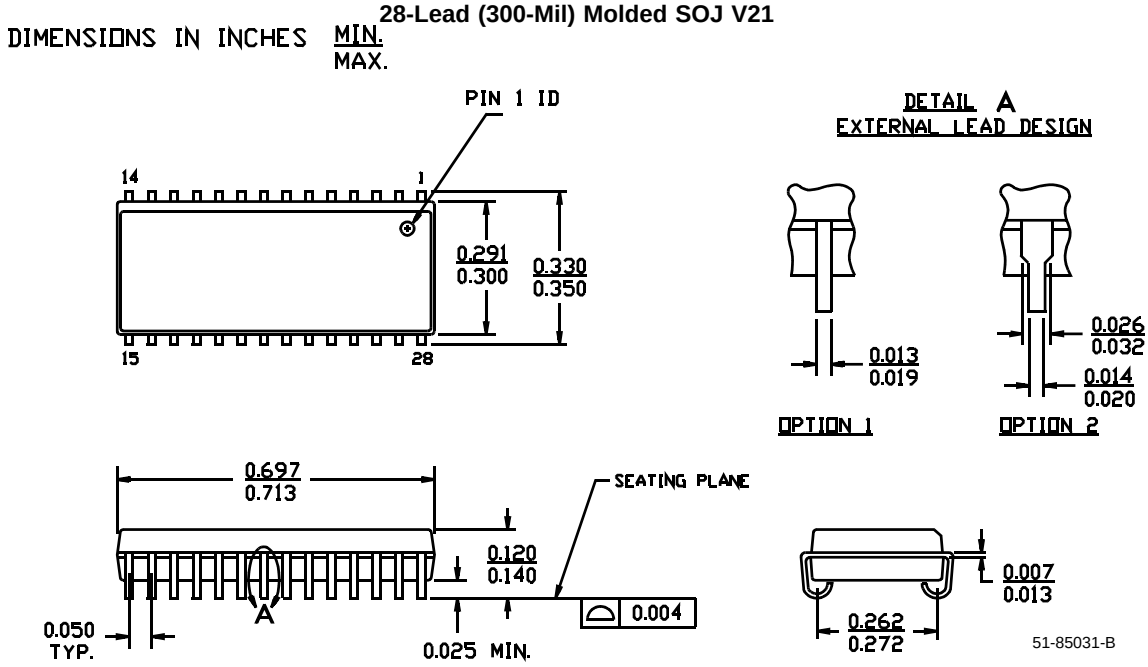
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1399D-10VXC	V21	28-Lead Molded SOJ (Pb-Free)	Commercial
	CY7C1399D-10ZXC	Z28	28-Lead Thin Small Outline Package (Pb-Free)	
	CY7C1399DL-10VXC	V21	28-Lead Molded SOJ (Pb-Free)	
	CY7C1399DL-10ZXC	Z28	28-Lead Thin Small Outline Package (Pb-Free)	
	CY7C1399D-10VXI	V21	28-Lead Molded SOJ (Pb-Free)	Industrial
	CY7C1399D-10ZXI	Z28	28-Lead Thin Small Outline Package (Pb-Free)	
	CY7C1399DL-10VXI	V21	28-Lead Molded SOJ (Pb-Free)	Industrial
	CY7C1399DL-10ZXI	Z28	28-Lead Thin Small Outline Package (Pb-Free)	
12	CY7C1399D-12VXC	V21	28-Lead Molded SOJ (Pb-Free)	Commercial
	CY7C1399D-12ZXC	Z28	28-Lead Thin Small Outline Package (Pb-Free)	
	CY7C1399DL-12VXC	V21	28-Lead Molded SOJ (Pb-Free)	
	CY7C1399DL-12ZXC	Z28	28-Lead Thin Small Outline Package (Pb-Free)	
	CY7C1399D-12VXI	V21	28-Lead Molded SOJ (Pb-Free)	Industrial
	CY7C1399D-12ZXI	Z28	28-Lead Thin Small Outline Package (Pb-Free)	
	CY7C1399DL-12VXI	V21	28-Lead Molded SOJ (Pb-Free)	Industrial
	CY7C1399DL-12ZXI	Z28	28-Lead Thin Small Outline Package (Pb-Free)	
15	CY7C1399D-15VXC	V21	28-Lead Molded SOJ (Pb-Free)	Commercial
	CY7C1399D-15ZXC	Z28	28-Lead Thin Small Outline Package (Pb-Free)	
	CY7C1399DL-15VXC	V21	28-Lead Molded SOJ (Pb-Free)	
	CY7C1399DL-15ZXC	Z28	28-Lead Thin Small Outline Package (Pb-Free)	
	CY7C1399D-15VXI	V21	28-Lead Molded SOJ (Pb-Free)	Industrial
	CY7C1399D-15ZXI	Z28	28-Lead Thin Small Outline Package (Pb-Free)	
	CY7C1399DL-15VXI	V21	28-Lead Molded SOJ (Pb-Free)	Industrial
	CY7C1399DL-15ZXI	Z28	28-Lead Thin Small Outline Package (Pb-Free)	

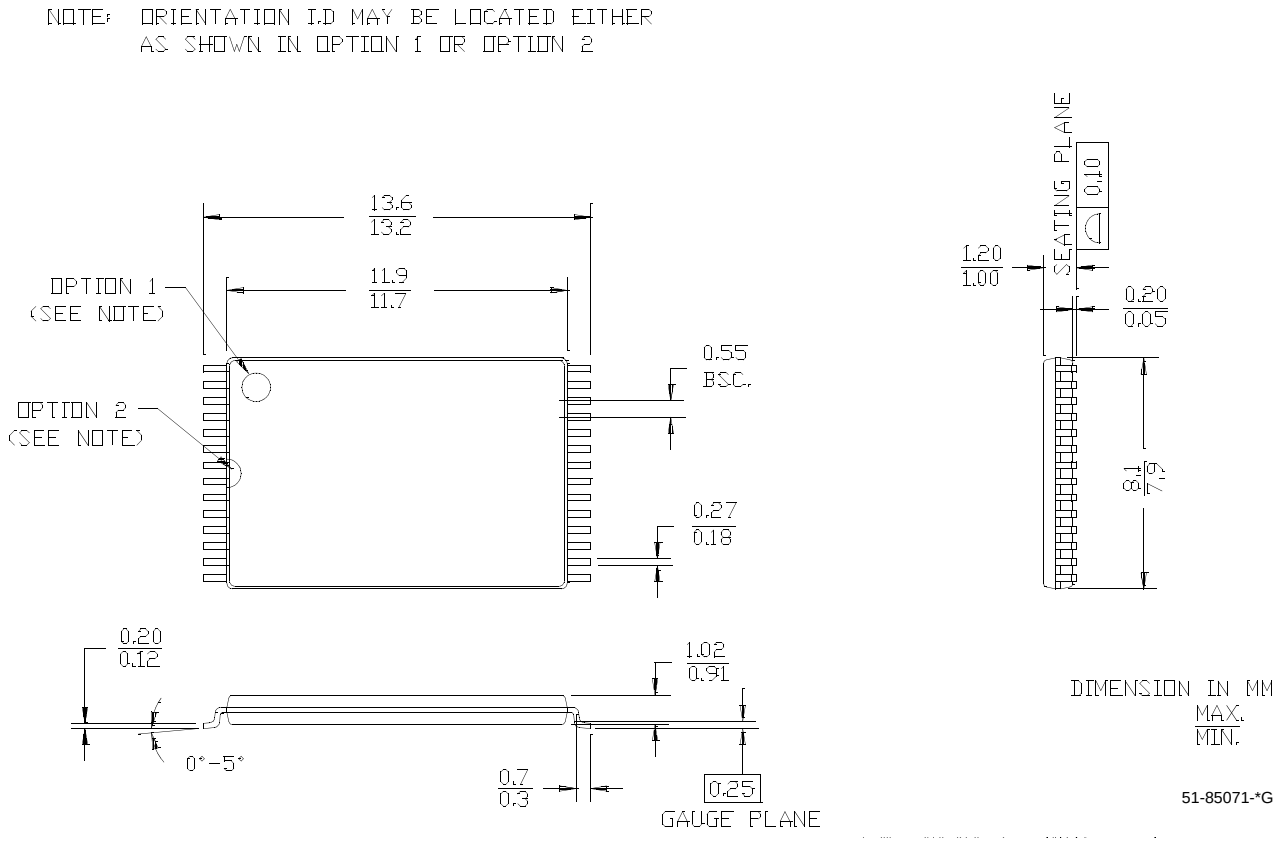
Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams

28-Lead (300-Mil) Molded SOJ V21



28-Lead Thin Small Outline Package Type 1 (8x13.4 mm) Z28



Document History Page

Document Title: CY7C1399D 256K (32K x 8) Static RAM (Preliminary) Document Number: 38-05467				
REV.	**Ecn No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233722	See ECN	RKF	DC parameters are modified as per EROS (Spec # 01-2165) Pb-free offering in the 'ordering information
*B	262950	See ECN	RKF	Added T_{power} Spec in Switching Characteristics table Shaded Ordering Information
*C	307594	See ECN	RKF	Reduced Speed bins to -10, -12 and -15 ns