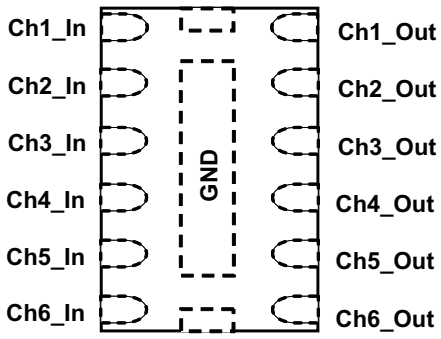
SIX-CHANNEL EMI FILTER FOR LCD DISPLAY/KEYPAD APPLICATION

Check for Samples: TPD6F002

FEATURES

- **Six-Channel EMI Filtering for Data Ports**
- **Robust ESD Protection Exceeds IEC61000-4-2 (Level 4)**
  - **±15-kV Human-Body Model (HBM)**
  - **±20-kV IEC 61000-4-2 Contact Discharge**
  - **±30-kV IEC 61000-4-2 Air-Gap Discharge**
- **Pi-Style (C-R-C) Filter Configuration ($R = 100\ \Omega$, $C_{TOTAL} = 34$ pF)**
- **Less than 20-nA Leakage Current Across Temperature and Process Variation**
  - **-35 dB Insertion Loss at 800 MHz**
  - **-57 dB Crosstalk Attenuation at 100 MHz**
  - **-35 dB Insertion Loss at 800 MHz**
  - **-3 dB Bandwidth 100 MHz**
- **Space-Saving SON Package (3 mm × 1.35 mm) and Flow-Through Pin Mapping Provides Optimum Filter Performance**

DSV PACKAGE
(TOP VIEW)



APPLICATIONS

- **LCD Display Interface**
- **Keypad**
- **SVGA Video Connections**
- **Memory Interface**

DESCRIPTION/ORDERING INFORMATION

The TPD6F002 is a six-channel EMI filter in a space-saving DSV package. This low-pass filter array reduces EMI emissions and provides system-level ESD protection at the data ports. Because of its small package and easy-to-use pin assignments, this device is suitable for a wide array of applications such as mobile handsets, PDAs, video consoles, notebook computers, etc. In particular, the TPD6F002 is ideal for EMI filtering and protecting data lines from ESD at the LCD display, keypad, and memory interfaces. The pi-style (C-R-C) filter provides at least 35 dB attenuation in the carrier frequency range.

The TPD6F002 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. This filter includes ESD protection circuitry that prevents damage to the application when subjected to ESD up to IEC 61000-4-2 ±20 kV Contact ESD and ±30 kV Air-Gap ESD.

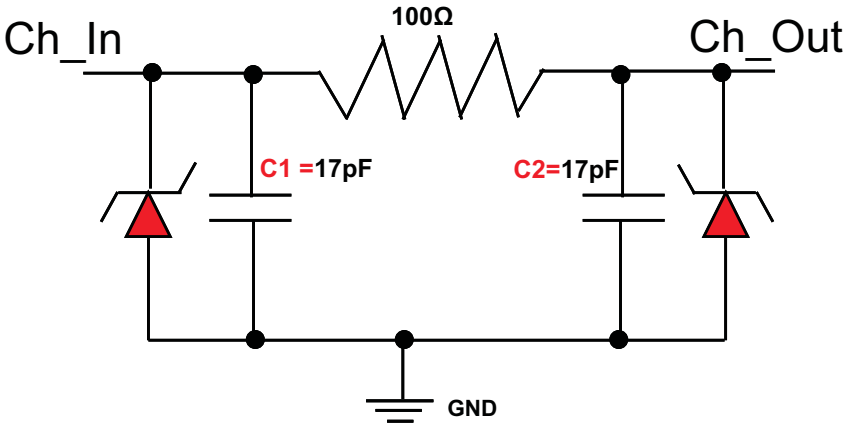
The TPD6F002 is specified for –40°C to 85°C operation.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)	PACKAGE DIMENSION	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	0.5-mm pitch SON – DSV	Length = 3 mm, Width = 1.35 mm, Pitch = 0.5 mm, Height = 0.75 mm)	TPD6F002DSVR	YM3NS

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

EQUIVALENT SCHEMATIC REPRESENTATION



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	IO to GND		6	V
T_{stg}	Storage temperature range	–65	150	°C
T_J	Junction temperature		150	°C
	Lead temperature (soldering, 10 s)		300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{BR}	DC breakdown voltage	I_{IO} = 10 µA	6			V
R	Resistance		85	100	115	Ω
C	Capacitance (C1 or C2)	V_{IO} = 2.5 V		17		pF
I_{IO}	Channel leakage current	V_{IO} = 3.3 V		1	20	nA
f_C	Cut-off frequency	Z_{SOURCE} = 50 Ω, Z_{LOAD} = 50 Ω		100		MHz

(1) Typical values are at T_A = 25°C.

ESD PROTECTION

PARAMETER	TYP	UNIT
HBM	±15	kV
IEC 61000-4-2 Contact Discharge	±20	kV
IEC 61000-4-2 Air-Gap Discharge	±30	kV

TYPICAL OPERATING CHARACTERISTCS

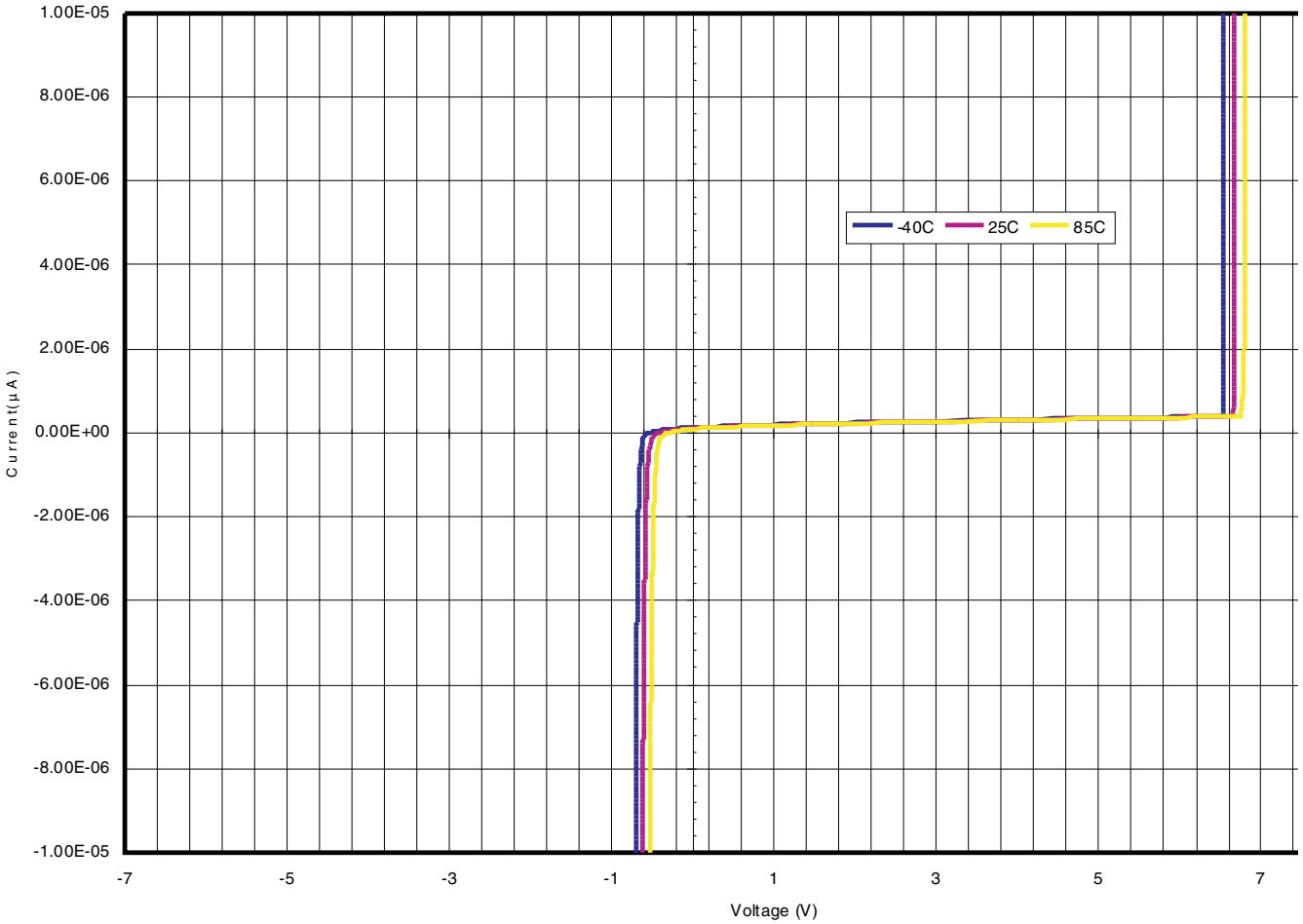


Figure 1. DC Voltage-Current Sweep across Input, Output Pins

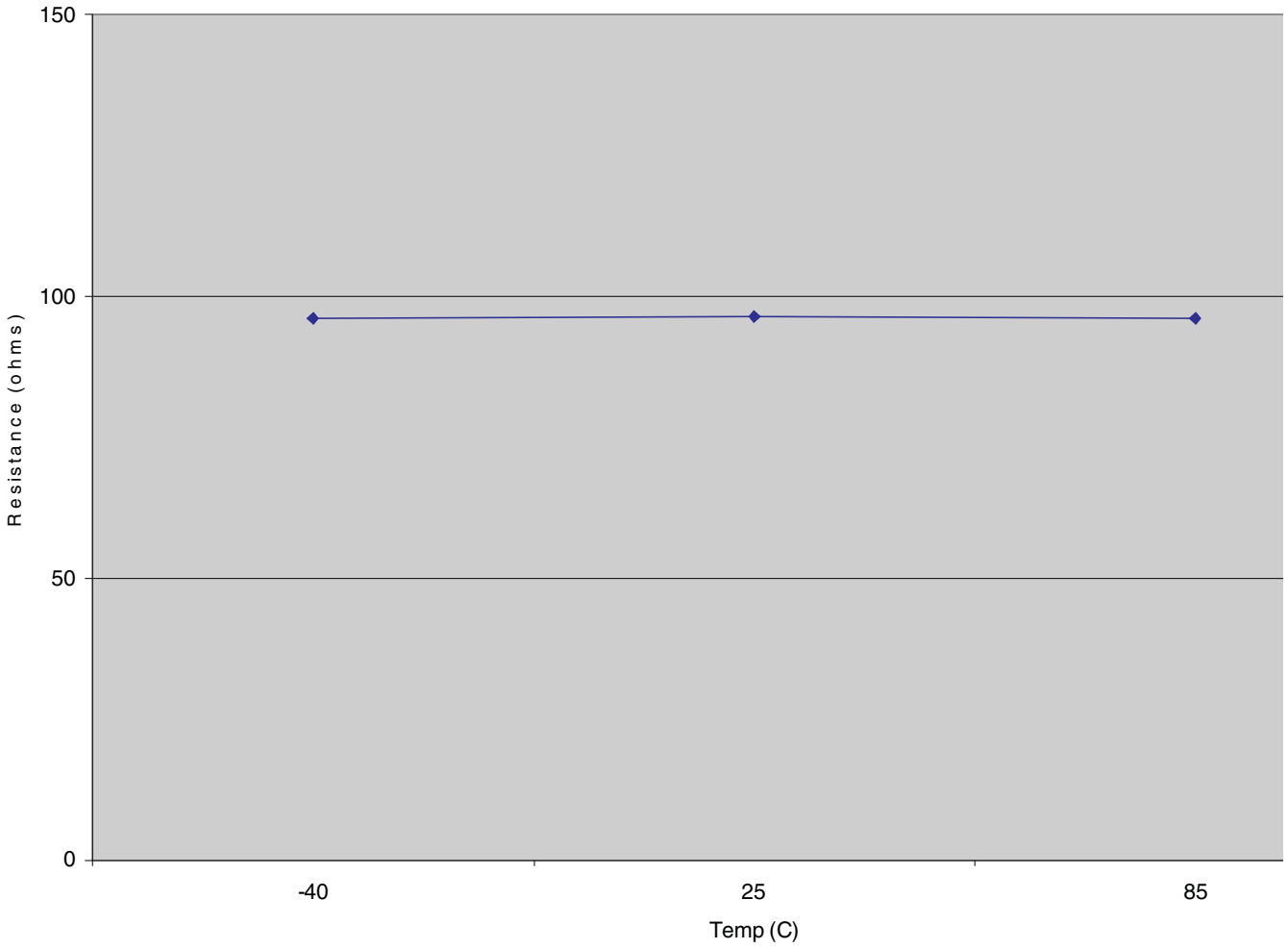


Figure 2. Series Resistance vs Temperature

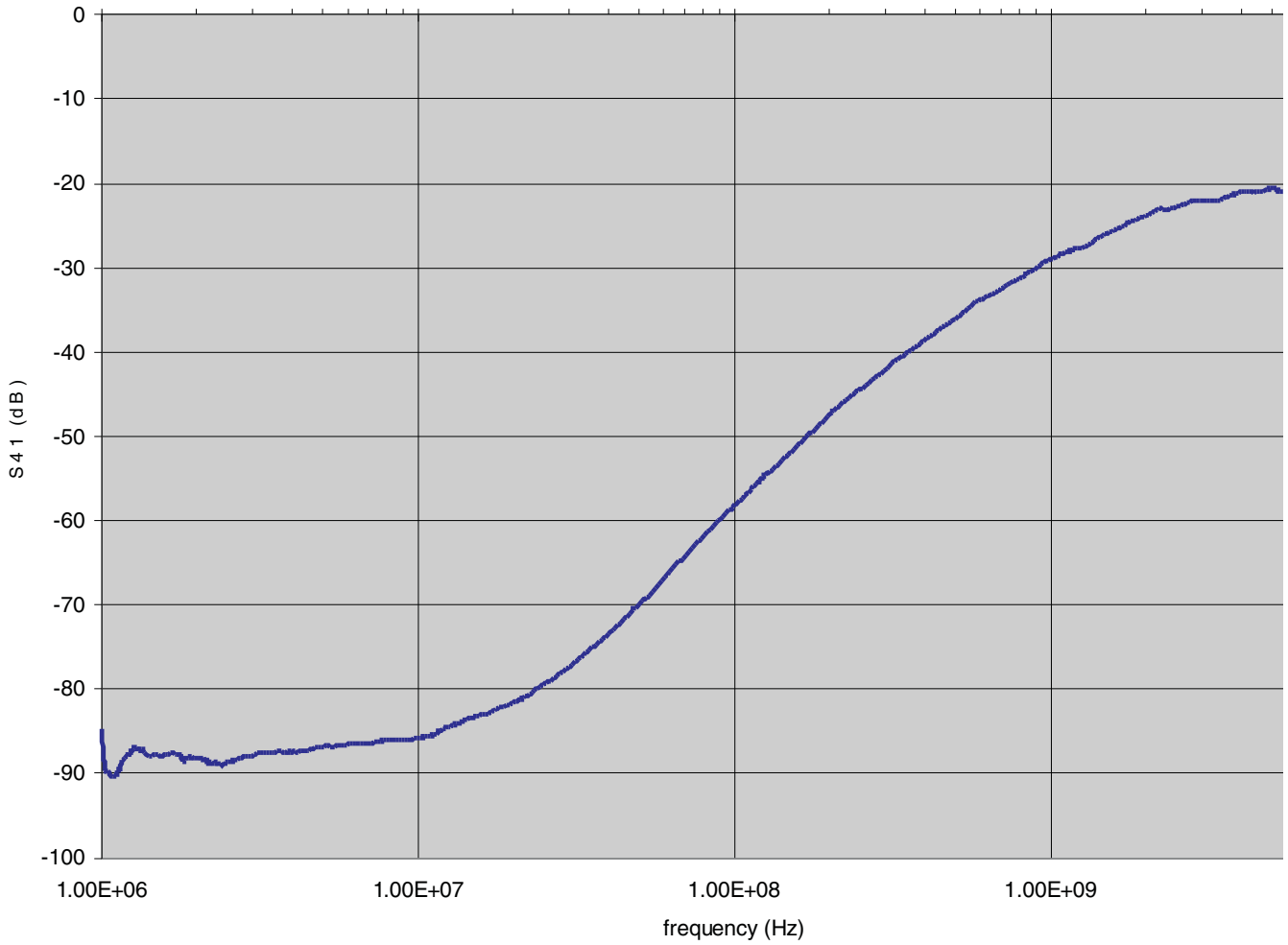


Figure 3. Channel-to-Channel Crosstalk

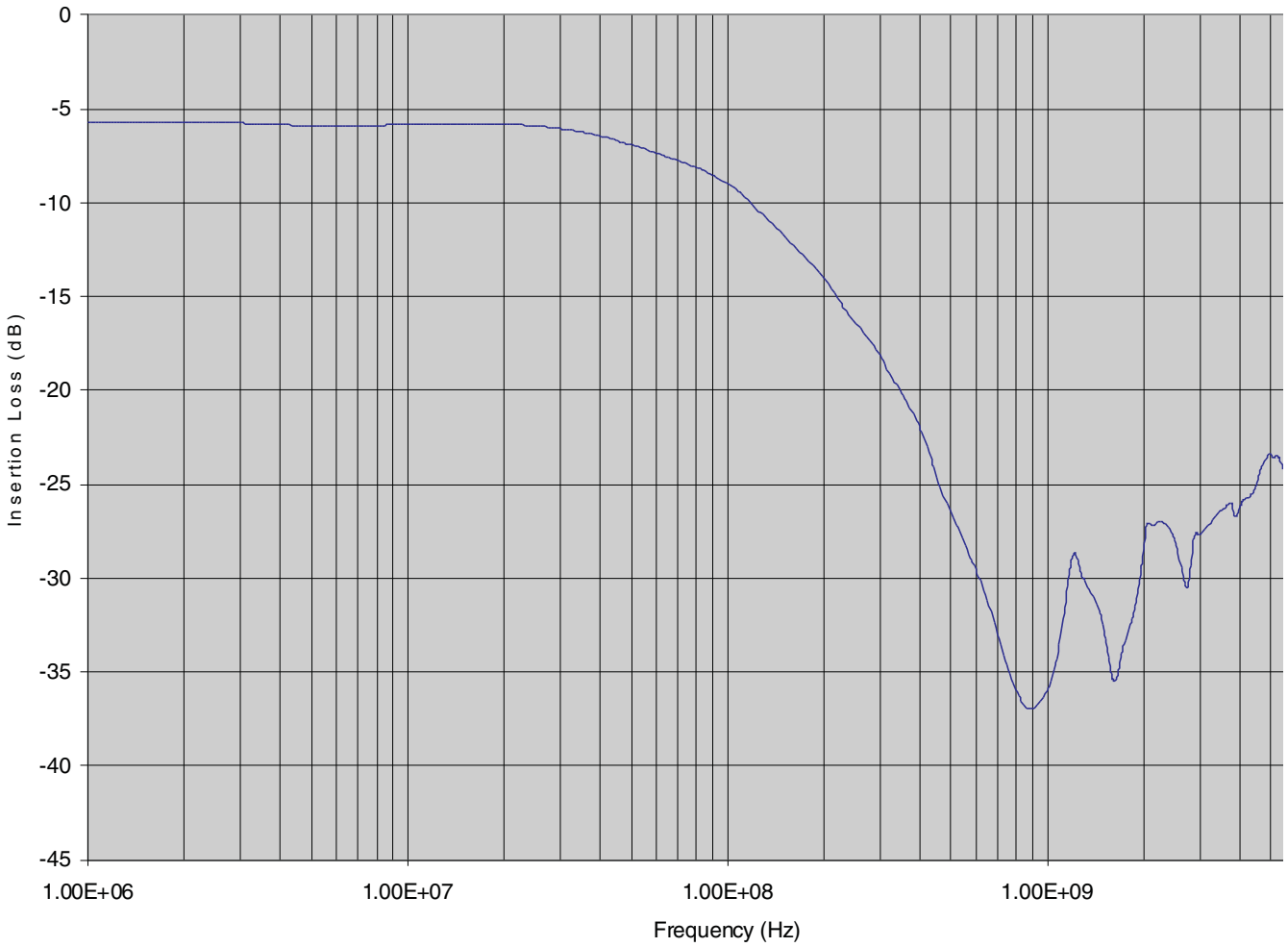


Figure 4. TPD6F002 Typical Insertion-loss Characteristics (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

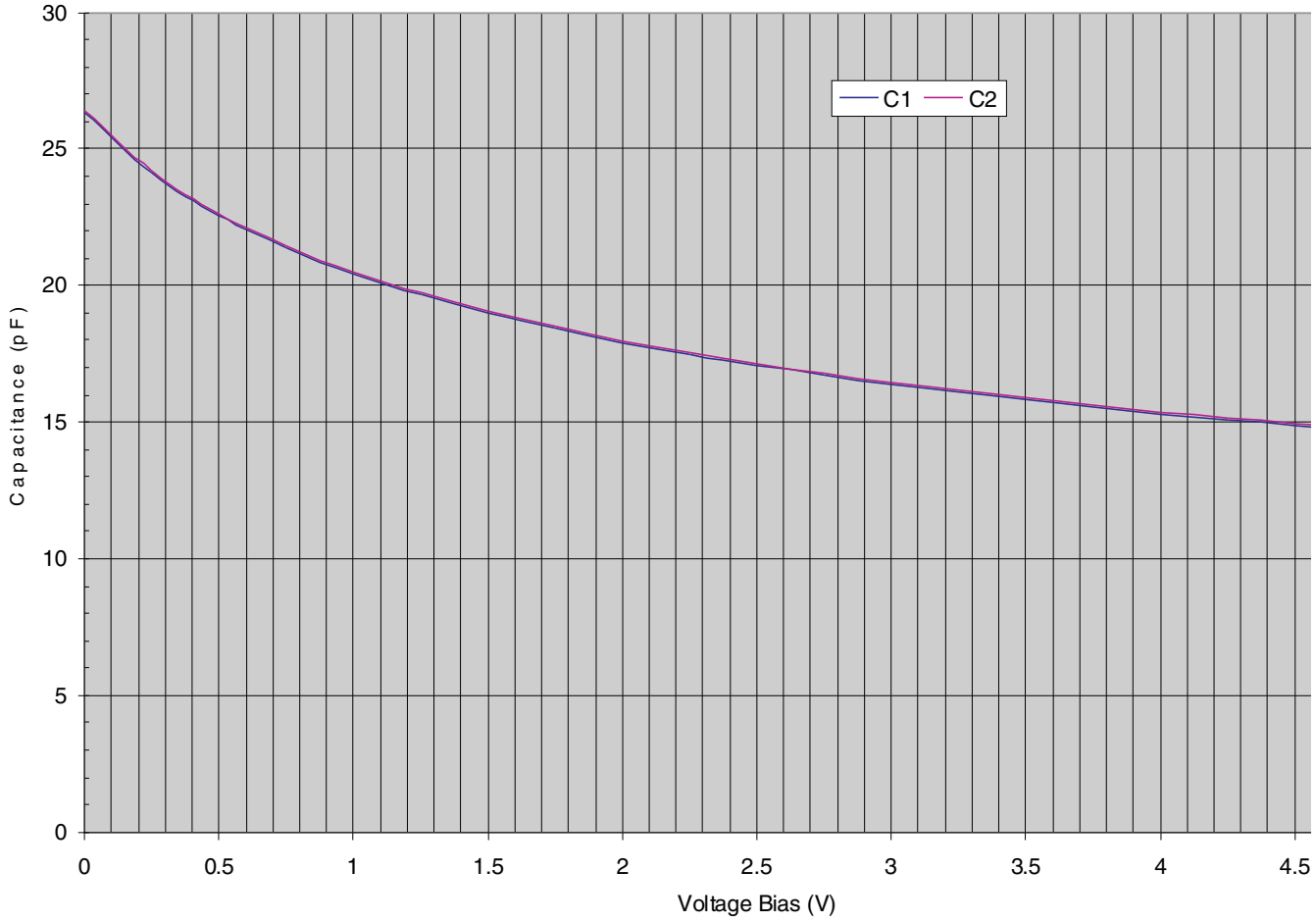


Figure 5. Capacitance (C1 or C2) vs. Bias Voltage

PACKAGING INFORMATION

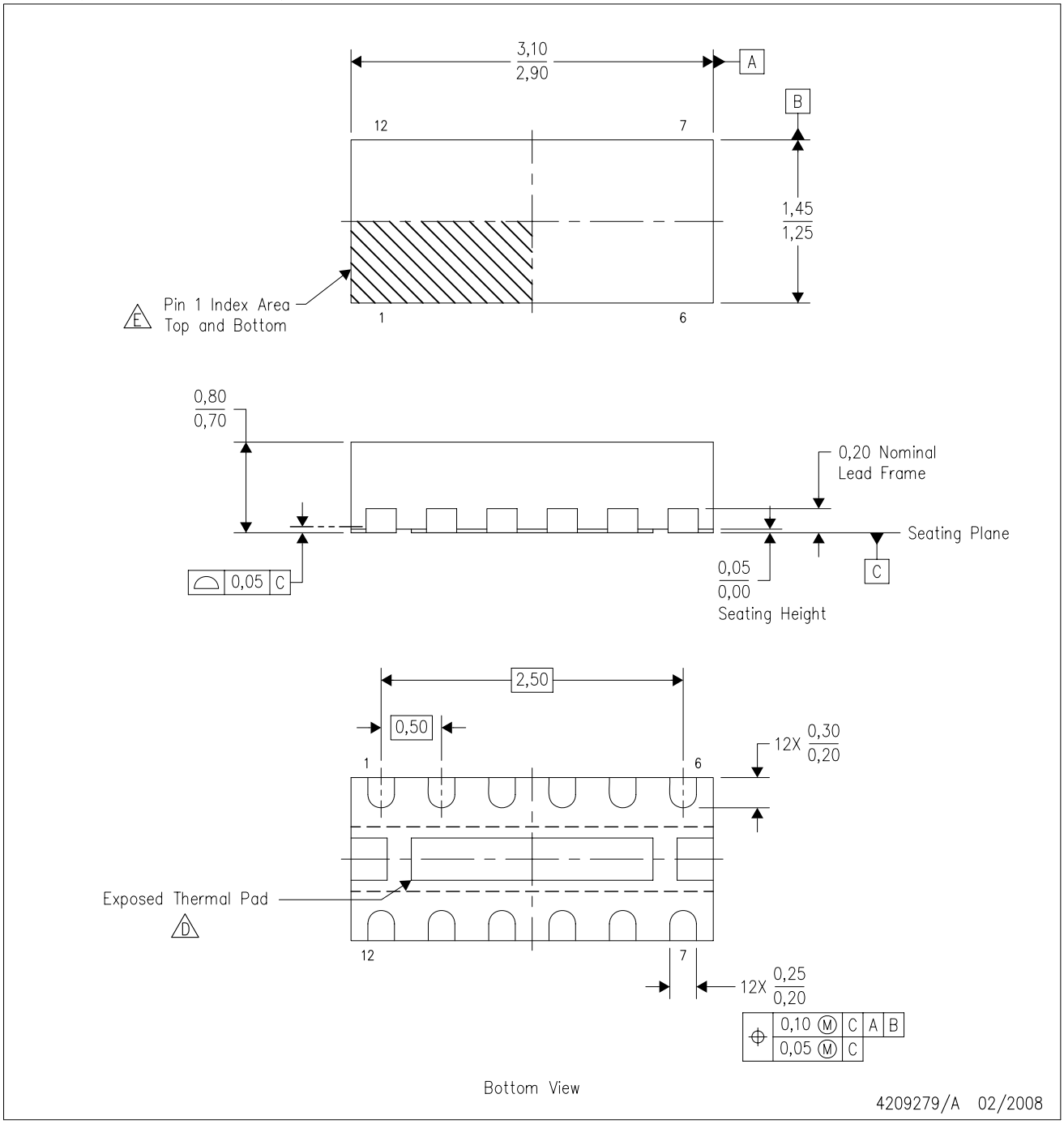
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPD6F002DSVR	ACTIVE	SON	DSV	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DSV (R–PDSO–N12) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

THERMAL PAD MECHANICAL DATA

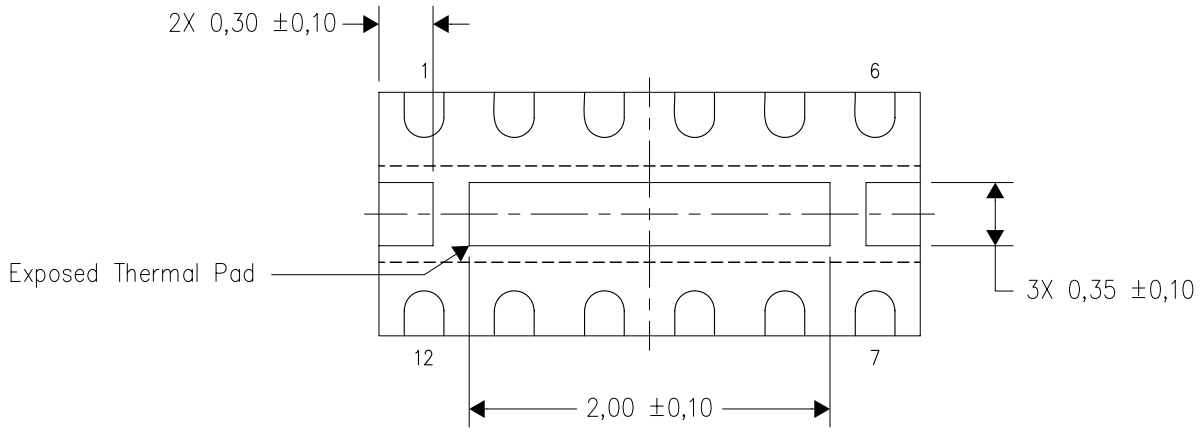
DSV (R–PDSO–N12)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

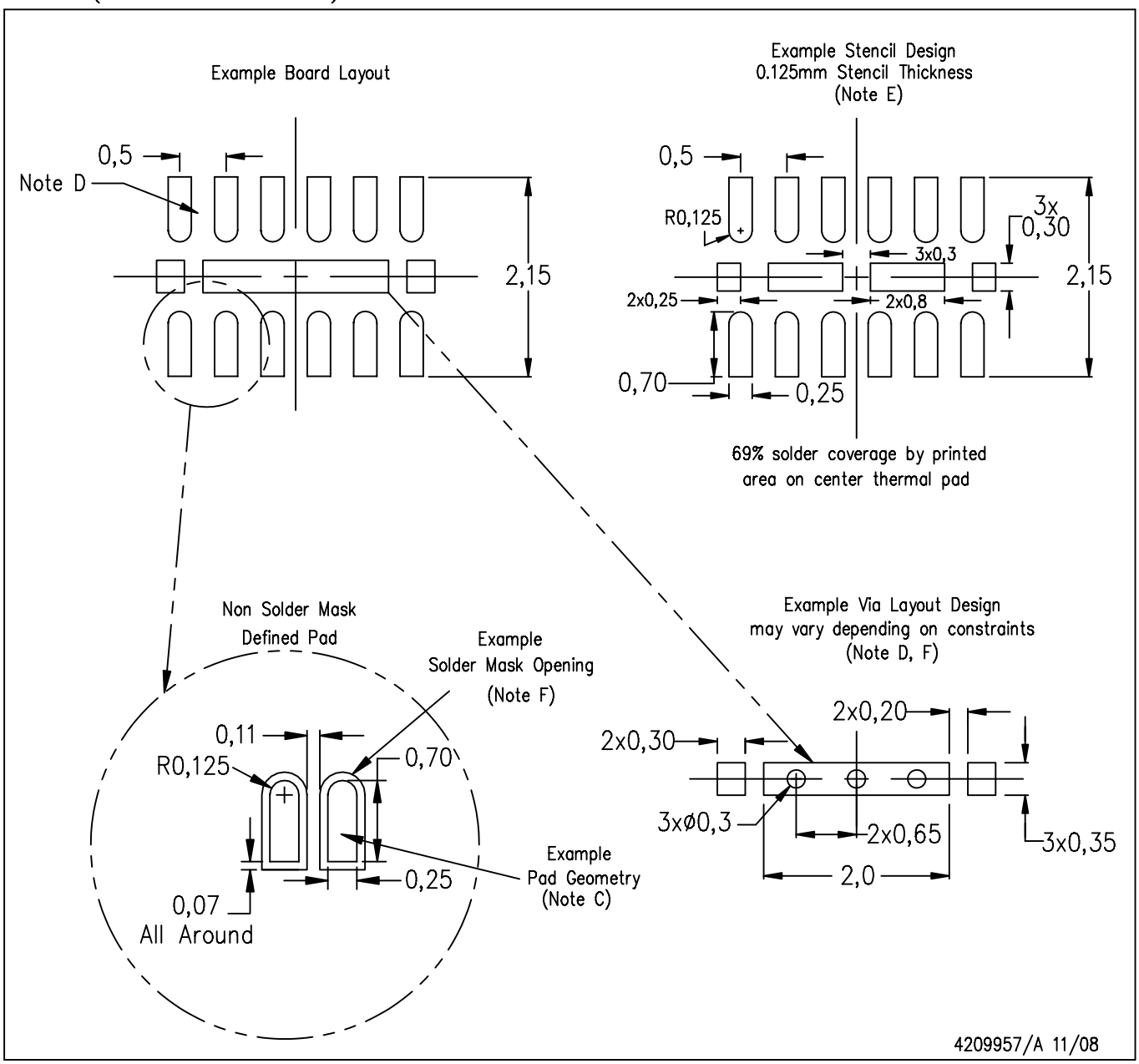


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DSV (R–PDSO–N12)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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