

74FST3251

8:1 Multiplexer/ Demultiplexer Bus Switch

The ON Semiconductor 74FST3251 is an 8:1, high performance multiplexer/demultiplexer bus switch. The device is CMOS TTL compatible when operating between 4 and 5.5 Volts. The device exhibits extremely low R_{ON} and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

Features

- $R_{ON} < 4 \Omega$ Typical
- Less Than 0.25 ns–Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- All Popular Packages: QSOP–16, TSSOP–16, SOIC–16
- All Devices in Package TSSOP are Inherently Pb–Free*

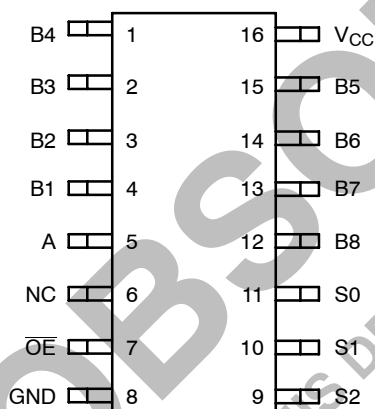


Figure 1. QSOP/SSOP/TSSOP
TOP VIEW

TRUTH TABLE

Inputs				Function
OE	S2	S1	S0	
L	L	L	L	A Port = B1 Port
L	L	L	H	A Port = B2 Port
L	L	H	L	A Port = B3 Port
L	L	H	H	A Port = B4 Port
L	H	L	L	A Port = B5 Port
L	H	L	H	A Port = B6 Port
L	H	H	L	A Port = B7 Port
L	H	H	H	A Port = B8 Port
H	X	X	X	Disconnect

NOTE: H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



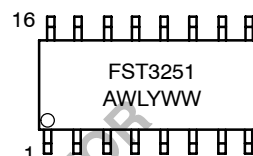
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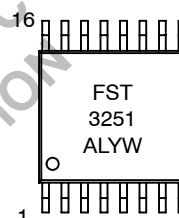
MARKING DIAGRAMS



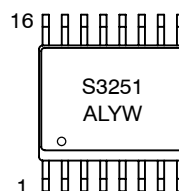
SOIC–16
D SUFFIX
CASE 751B



TSSOP–16
DT SUFFIX
CASE 948F



QSOP–16
QS SUFFIX
CASE 492



A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week

PIN NAMES

Pin	Description
$\overline{OE}_1, \overline{OE}_2$	Bus Switch Enables
S0, S1	Select Inputs
A	Bus A
B1, B2, B3, B4	Bus B

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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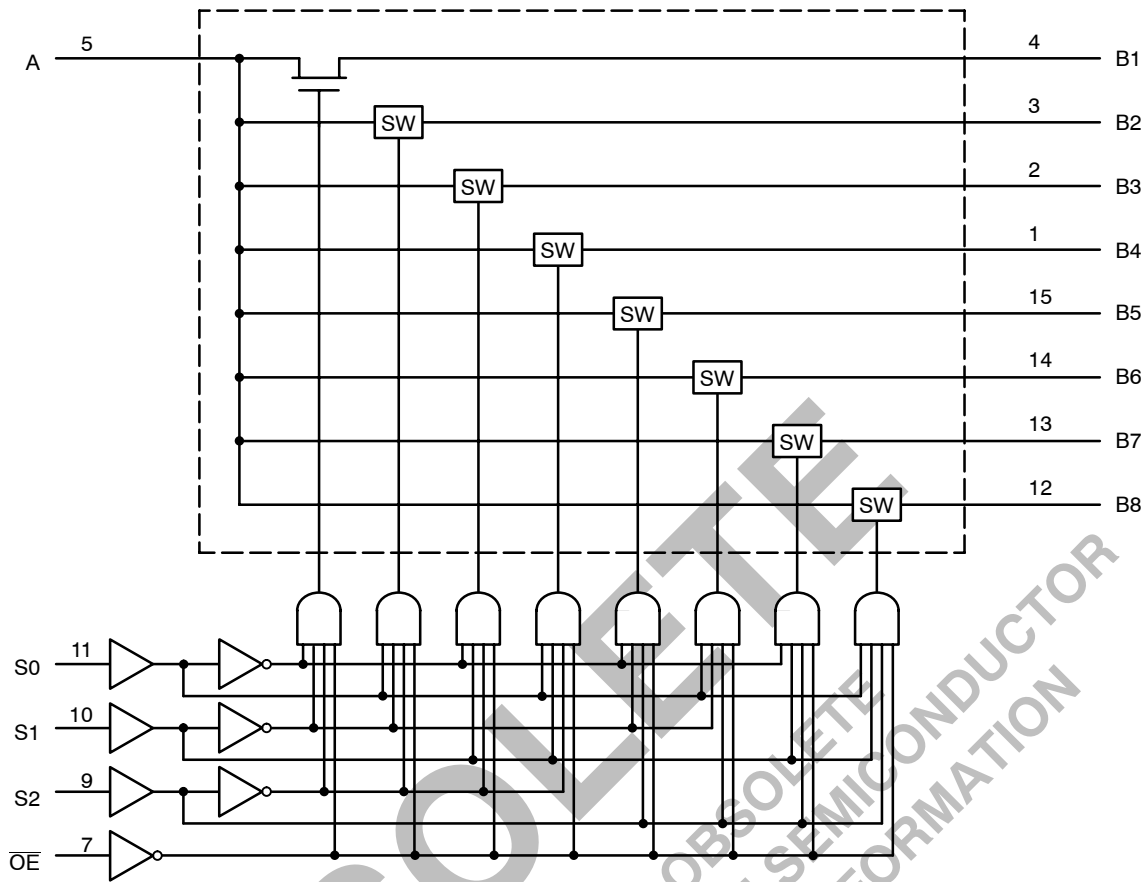


Figure 2. Logic Diagram

ORDERING INFORMATION

Device Order Number	Package	Shipping [†]
74FST3251D	SOIC-16	48 Units / Rail
74FST3251DR2	SOIC-16	1000 Units / Tape & Reel
74FST3251DT	TSSOP-16* (Pb-Free)	96 Units / Rail
74FST3251DTR2	TSSOP-16* (Pb-Free)	2500 Units / Tape & Reel
74FST3251QS	QSOP-16	96 Units / Rail
74FST3251QSR	QSOP-16	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	- 0.5 to + 7.0	V
V_I	DC Input Voltage	- 0.5 to + 7.0	V
V_O	DC Output Voltage	- 0.5 to + 7.0	V
I_{IK}	DC Input Diode Current $V_I < GND$	- 50	mA
I_{OK}	DC Output Diode Current $V_O < GND$	- 50	mA
I_O	DC Output Sink Current	128	mA
I_{CC}	DC Supply Current per Supply Pin	± 100	mA
I_{GND}	DC Ground Current per Ground Pin	± 100	mA
T_{STG}	Storage Temperature Range	- 65 to + 150	$^{\circ}C$
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	$^{\circ}C$
T_J	Junction Temperature Under Bias	+ 150	$^{\circ}C$
θ_{JA}	Thermal Resistance SOIC TSSOP QSOP	125 170 200	$^{\circ}C/W$
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 200 N/A	V
$I_{Latchup}$	Latchup Performance Above V_{CC} and Below GND at 85 $^{\circ}C$ (Note 4)	± 500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage Operating, Data Retention Only	4.0	5.5	V
V_I	Input Voltage (Note)	0	5.5	V
V_O	Output Voltage (HIGH or LOW State)	0	5.5	V
T_A	Operating Free-Air Temperature	- 40	+ 85	$^{\circ}C$
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate Switch I/O Switch Control Input $V_{CC} = 5.0 V \pm 0.5 V$	0	DC 5	ns/V

5. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C			Unit
				Min	Typ*	Max	
V _{IK}	Clamp Diode Resistance	I _{IN} = -18mA	4.5			-1.2	V
V _{IH}	High-Level Input Voltage		4.0 to 5.5	2.0			V
V _{IL}	Low-Level Input Voltage		4.0 to 5.5			0.8	V
I _I	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5 V	5.5			±1.0	μA
I _{OZ}	OFF-STATE Leakage Current	0 ≤ A, B ≤ V _{CC}	5.5			±1.0	μA
R _{ON}	Switch On Resistance (Note 6)	V _{IN} = 0 V, I _{IN} = 64 mA	4.5		4	7	Ω
		V _{IN} = 0 V, I _{IN} = 30 mA	4.5		4	7	
		V _{IN} = 2.4 V, I _{IN} = 15 mA	4.5		8	15	
		V _{IN} = 2.4 V, I _{IN} = 15 mA	4.0		11	20	
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND, I _{OUT} = 0	5.5			3	μA
ΔI _{CC}	Increase In I _{CC} per Input	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5			2.5	mA

*Typical values are at V_{CC} = 5.0 V and T_A = 25°C.

6. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	T _A = -40°C to +85°C C _L = 50 pF, R _U = R _D = 500 Ω				Unit
			V _{CC} = 4.5-5.5 V		V _{CC} = 4.0 V		
			Min	Max	Min	Max	
t _{PHL} , t _{PLH}	Prop Delay Bus to Bus (Note 7)	V _I = OPEN		0.25		0.25	ns
	Prop Delay, Select to Bus A		1.0	6.3		6.9	
t _{PZH} , t _{PZL}	Output Enable Time, Select to Bus B	V _I = 7 V for t _{pZL}	1.0	6.0		6.5	ns
	Output Enable Time, I _{OE} to Bus A, B	V _I = OPEN for t _{pZH}	1.0	6.0		6.5	
t _{PHZ} , t _{PLZ}	Output Disable Time, Select to Bus B	V _I = 7 V for t _{pLZ}	1.0	5.8		6.5	ns
	Output Disable Time, I _{OE} to Bus A, B	V _I = OPEN for t _{pHZ}	1.0	5.8		6.5	

7. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

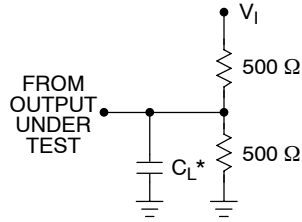
CAPACITANCE (Note 8)

Symbol	Parameter	Conditions	Typ	Max	Unit
C _{IN}	Control Pin Input Capacitance	V _{CC} = 5.0 V	3		pF
C _{I/O}	A Port Input/Output Capacitance	V _{CC} , $\overline{OE}$ = 5.0 V	13		pF
C _{I/O}	B Port Input/Output Capacitance	V _{CC} , $\overline{OE}$ = 5.0 V	5		pF

8. T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

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AC Loading and Waveforms



NOTES:

1. Input driven by 50 Ω source terminated in 50 Ω .
 2. C_L includes load and stray capacitance.
- * $C_L = 50$ pF

Figure 3. AC Test Circuit

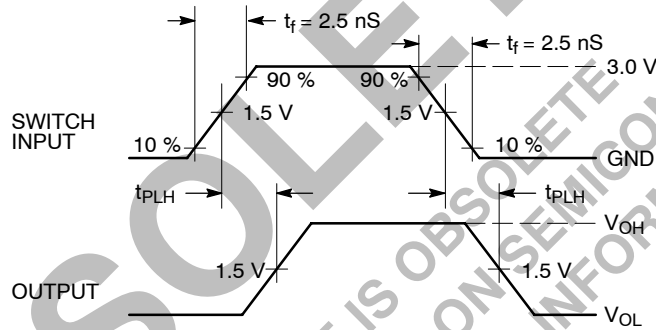


Figure 4. Propagation Delays

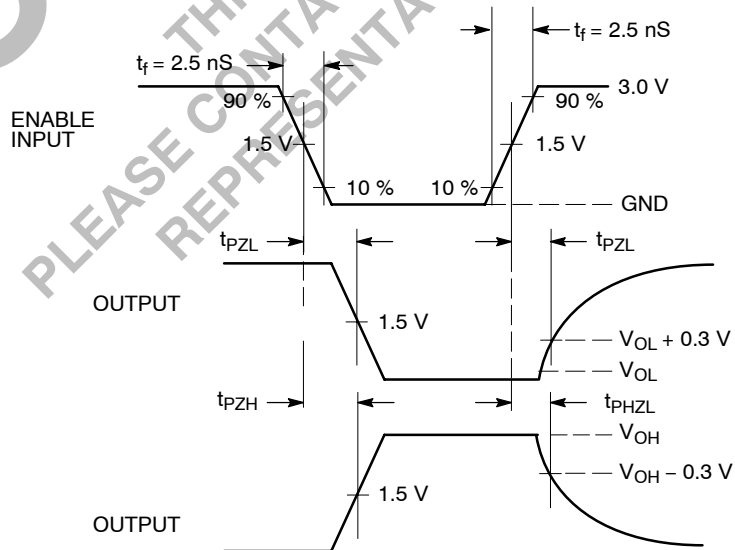
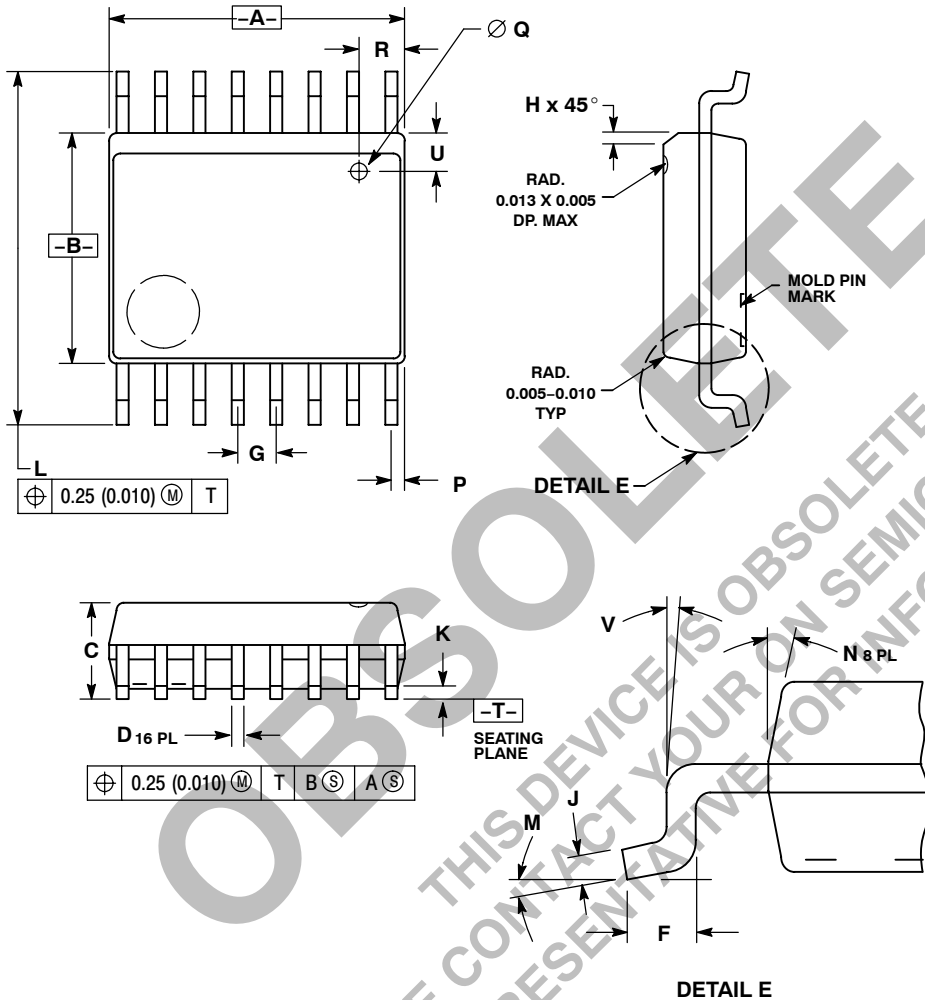


Figure 5. Enable/Disable Delays

PACKAGE DIMENSIONS

QSOP-16
QS SUFFIX
CASE 492-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
4. PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER SIDE.
5. BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

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