RICOH

R1272S Series

34 V Input Synchronous Step-down DC / DC Controller

NO.EA-351-210910

OUTLINE

The R1272S is a step-down DC/DC controller which can generate an output voltage of 0.7 V to 5.3 V by driving external high- / low-side NMOSs. By the adoption of a unique current mode PWM architecture without an external current sense resistor, the R1272S can make up a stable DC/DC converter with high-efficiency even if adding low Ron MOSFETs and a low DCR inductor externally. And, by the frequency characteristics optimization with using external phase compensation capacitor, the R1272S can achieve a high-speed response to variations of input voltage and load current. The user-settable oscillation frequency is adjustable over a range of 250 kHz to 1 MHz(1) by external resistors, and also can be synchronized to an external clock.
Output Voltage Control Methods have three operating modes: Forced PWM mode, PLL_PWM mode, and PWM/VFM Auto-switching mode. These modes are selectable according to conditions of the MODE pin. Especially, the PWM/VFM Auto-switching mode can improve efficiency under light load conditions.
The R1272S can minimize the output voltage drop caused by an input voltage drop at cranking, with reducing the operating frequency (the lowest possible limit is a quarter of the frequency) so that the off-duty is reduced.
Protection functions include a current limit function, an UVLO (Under Voltage Lock Out) function, an OVP (Over Voltage Protection) function, a soft-start function, a low-inductor current shutdown function, and so on. Also, a power good function provides the status of output with using a power good (PGOOD) pin.
For EMI reduction, SSCG (Spread-Spectrum Clock Generator) for diffused oscillation frequency at the PWM operation is optionally available. The R1272S is available in HSOP-18 package.

FEATURES

- Operating Voltage (Maximum Rating) ····· 4.0 V to 34 V (36 V)
- Operating Temperature Range ····· -40°C ≤ Ta ≤ 105°C
  (Usable in high-temperature environment)
- Start-up Voltage ····· 4.5 V
- Output Voltage ····· 0.7 V to 5.3 V
- Feedback Voltage Tolerance ····· 0.64 V ± 1%
- Consumption Current at No Load (at VFM mode) ····· Typ.15 μA
- Adjustable Oscillation Frequency(1) ····· 250 kHz to 1 MHz
- Synchronizable Clock Frequency(1) ····· 250 kHz to 1 MHz
- Spreading Rate for SSCG ····· Typ. ±3.6%
- Minimum On-Time ····· Typ.100 ns
- Minimum Off-Time ····· Typ.120 ns (at regulation mode)
  At dropout, actual minimum off-time is reduced.
- Adjustable Soft-start Time(2) ····· Typ.500 μs
- Pre-bias Start-up
- Anti-phase Clock Output
- Thermal Shutdown Function ····· Tj = 160ºC (Typ.)

(1) The adjustable oscillation frequency range becomes 250 kHz ≤ f_{OSC} ≤ 600 kHz when 0.7 V ≤ V_{OUT} < 1.35V.
(2) 500 μs (Typ.) as a lower limit with using an external capacitor. Otherwise, available the tracking function through the application of an external voltage.

- Under Voltage Lockout (UVLO) Function ····· Typ. 3.3 V
- Over Voltage Detection (OVD) Function ····· FB pin voltage (V_{FB}) + 10% (Typ.)
  Detection/Release Hysteresis ····· FB pin voltage (V_{FB}) x 3% (Typ.)
- Under Voltage Detection (UVD) Function ····· FB pin voltage (V_{FB}) - 10% (Typ.)
  Detection/Release Hysteresis ····· FB pin voltage (V_{FB}) x 3% (Typ.)
- Over-current Protection ····· Hiccup-mode / Latch mode
- Selectable Current Limit Threshold ····· 50 mV / 70 mV / 100 mV
- Power Good Output ····· NMOS Open-drain Output
- Package ····· HSOP-18

APPLICATIONS

- Power source for digital home appliances such as digital TV, DVD players.
- Power source for office equipment such as printers and fax machines.
- Power source for mobile communication equipment, cameras and video instruments.
- Power source for high voltage battery-powered equipment.

SELECTION GUIDE

The function and setting for the ICs are selectable at the user's request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1272SxxyA-E2-FE	HSOP-18	1,000	Yes	Yes

xx : Select the combination of processing and function.

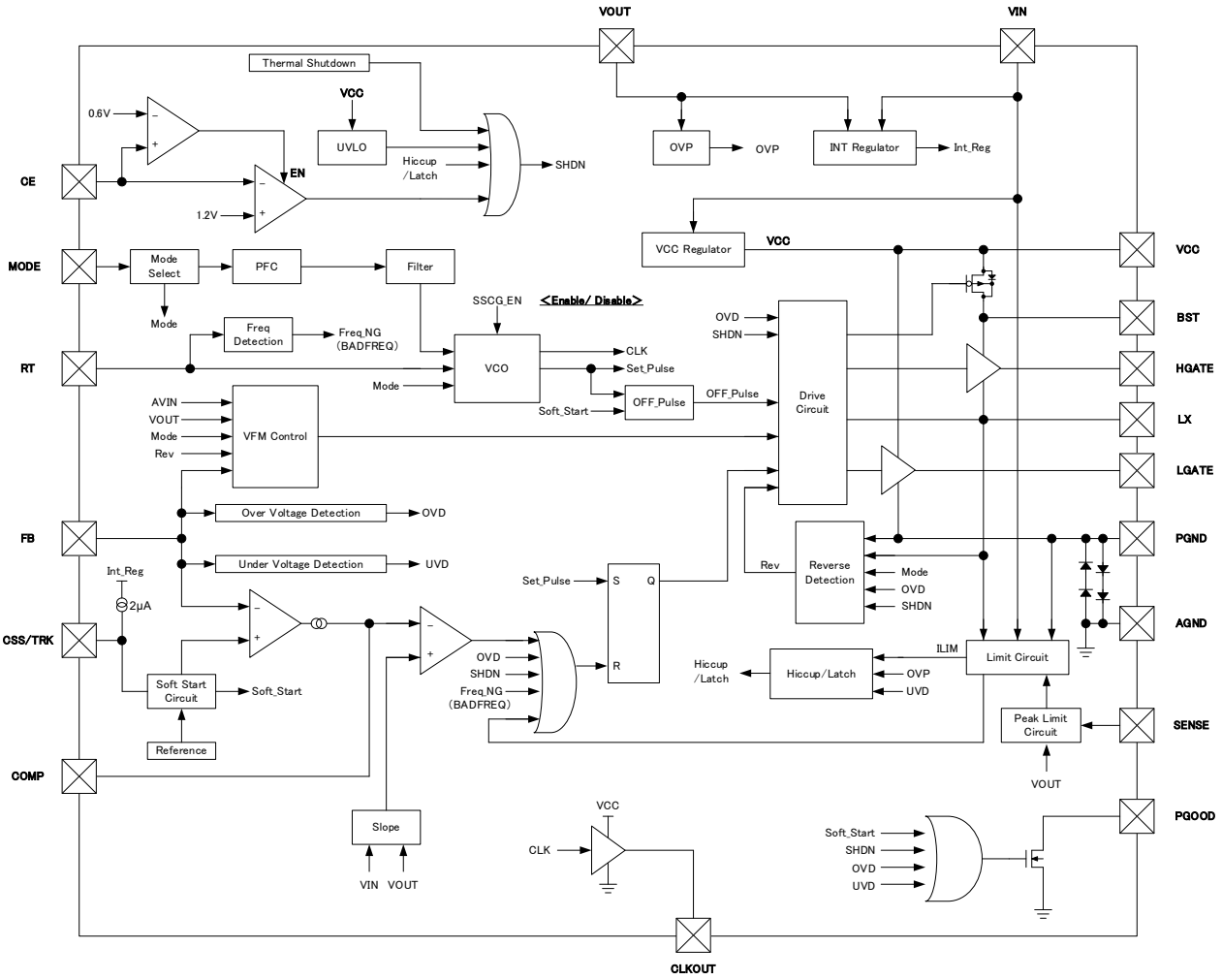
xx	Over Current Protection	SSCG	Output Voltage Range
00	Non-latch type hiccup mode	Disable	3.15 V < V_{OUT} ≤ 5.3 V
01	Latch mode	Disable	3.15 V < V_{OUT} ≤ 5.3 V
03	Latch mode	Enable	3.15 V < V_{OUT} ≤ 5.3 V
10	Non-latch type hiccup mode	Disable	0.7 V ≤ V_{OUT} ≤ 3.15 V
11	Latch mode	Disable	0.7 V ≤ V_{OUT} ≤ 3.15 V
13	Latch mode	Enable	0.7 V ≤ V_{OUT} ≤ 3.15 V

If required a version with SSCG function, please contact our sales offices.

y : Select the current limit threshold voltage.

y	Set Voltage for Current Limit Threshold (Typ.)	Reverse Current Detection Value (Typ.)
1	50 mV	25mV
2	70 mV	35mV
3	100 mV	50mV

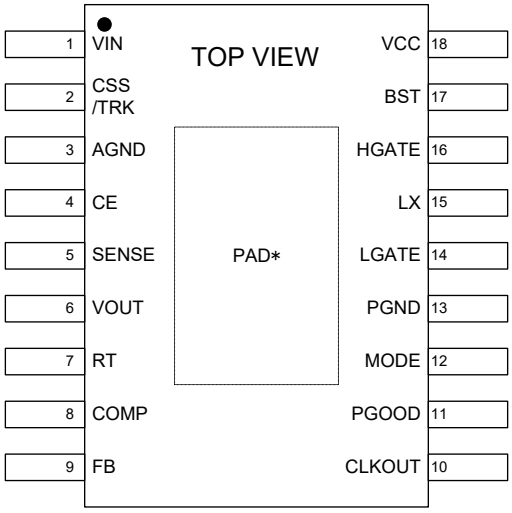
BLOCK DIAGRAMS



R1272SxxxA

PIN DESCRIPTIONS

HSOP-18

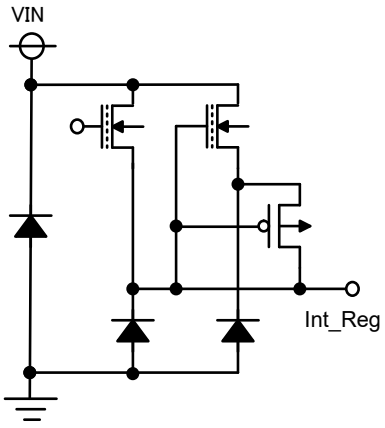


HSOP-18 Pin Description

Pin No.	Pin Name	Description
1	VIN	Power supply pin
2	CSS/TRK	Soft-start adjustment pin
3	AGND	Analog GND pin
4	CE	Chip enable pin (Active ”H”)
5	SENSE	Sense pin for inductor current
6	VOUT	Output voltage feedback input pin
7	RT	Oscillation adjustment pin
8	COMP	Capacitor connecting pin for phase compensation of error amplifier
9	FB	Feedback input pin to the error amplifier
10	CLKOUT	Clock output pin
11	PGOOD	Power-good output pin
12	MODE	Mode-set input pin
13	PGND	Power GND pin
14	LGATE	L-side FET control pin
15	LX	Switchingpin
16	HGATE	H-side FET control pin
17	BST	Boostrap pin
18	VCC	VCC output pin

∗ The tab on the bottom of the package must be electrically connected to GND (substrate level) when mounted on the board.

INTERNAL EQUIVALENT CIRCUIT FOR EACH PIN



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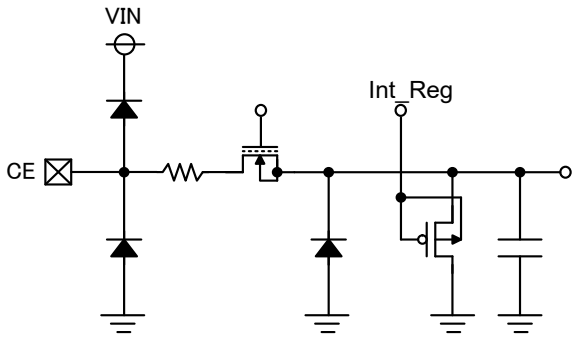

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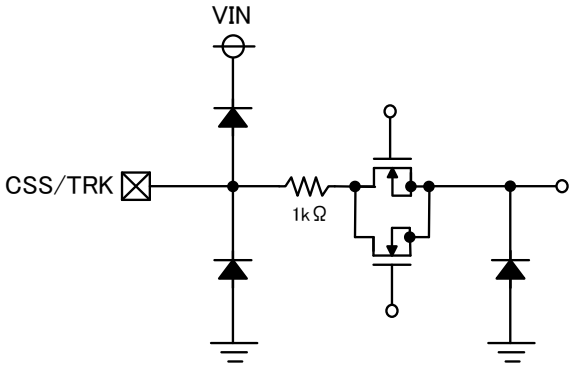

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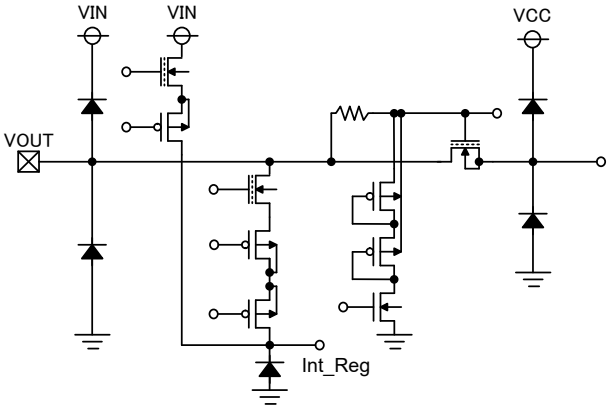

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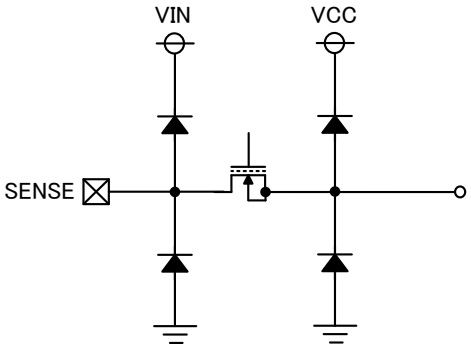

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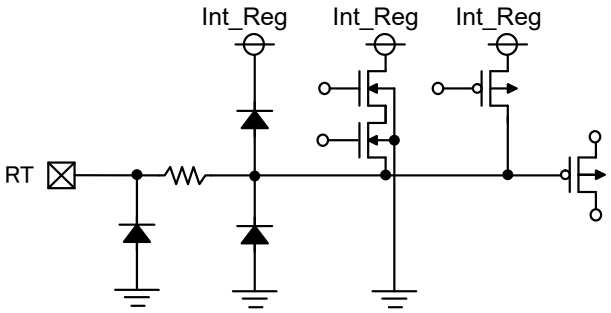

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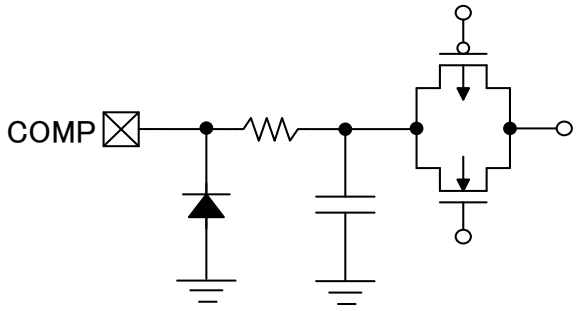

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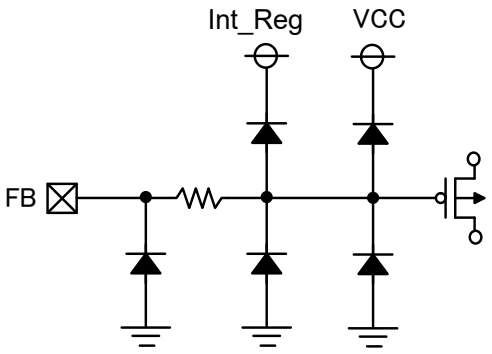

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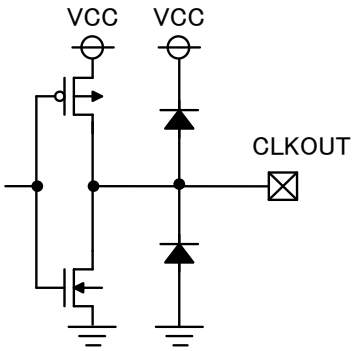

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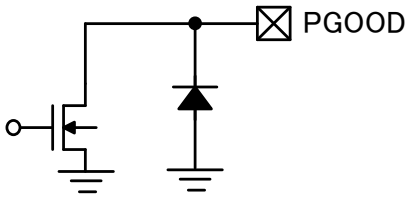

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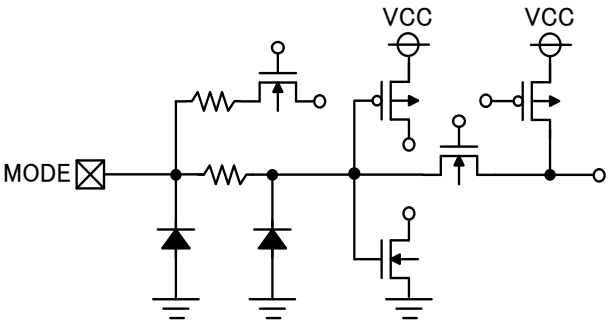

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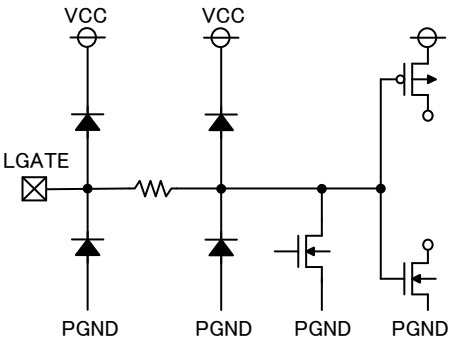

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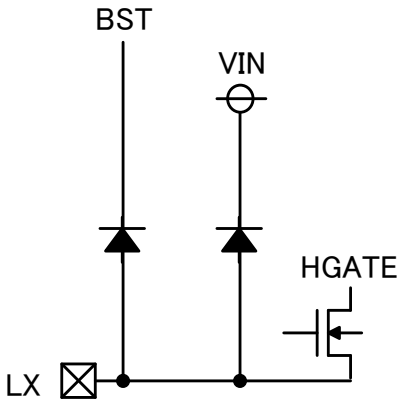

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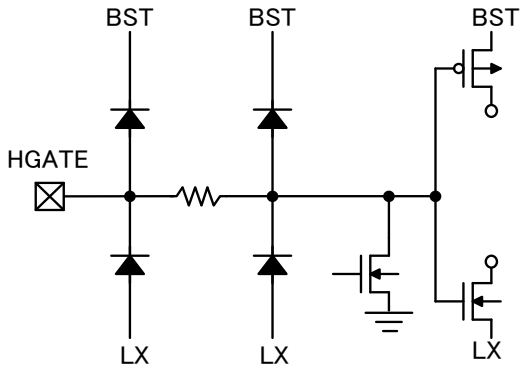

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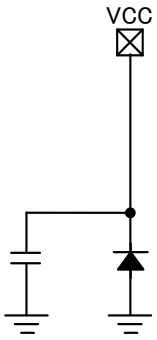

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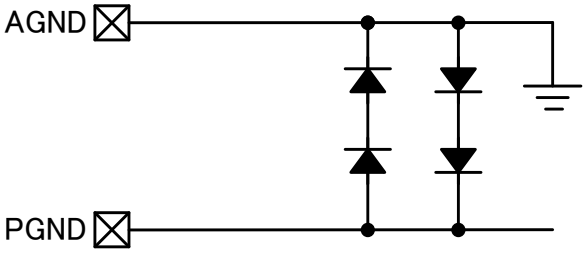


< AGND-PGND Pins >

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{IN}	VIN pin voltage	-0.3 to 36	V
V_{CE}	CE pin voltage	-0.3 to 36	V
V_{CSS}/V_{TRK}	CSS/TRK pin voltage	-0.3 to 3	V
V_{OUT}	VOUTpin voltage	-0.3 to 6	V
V_{SENSE}	SENSEpin voltage	-0.3 to 6	V
V_{RT}	RT pin voltage	-0.3 to 3	V
V_{COMP}	COMP pin voltage(1)	-0.3 to 6	V
V_{FB}	FB pin voltage	-0.3 to 3	V
V_{CC}	VCC pin voltage	-0.3 to 6	V
	Output current for VCC pin	Internally limited	mA
V_{BST}	BST pin voltage	LX-0.3 to LX+6	V
V_{HGATE}	HGATE pin voltage	LX-0.3 to BST	V
V_{LX}	LX pin voltage(2)	-0.3 to 36	V
V_{LGATE}	LGATE pin voltage(1)	-0.3 to 6	V
V_{MODE}	MODE pin voltage	-0.3 to 6	V
V_{PGOOD}	PGOOD pin voltage	-0.3 to 6	V
V_{CLKOUT}	CLKOUT pin voltage(1)	-0.3 to 6	V
P_D	Power Dissipation(3) (HSOP-18, JEDEC STD.51-7 Test Land Pattern)	3100	mW
Tj	Junction Temperature	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field.
The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	4.0 to 34	V
Ta	Operating Temperature Range	−40 to 105	°C
V_{OUT}	Output Voltage Range	0.7 to 5.3	V

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) The pin voltage must be prevented from exceeding V_{CC} +0.3V.
(2) The pin voltage must be prevented from exceeding V_{IN} +0.3V.
(3) Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, CE = V_{IN}, unless otherwise specified.

The specifications surrounded by [ ] are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1272SxxxA (Ta = 25°C)

Symbol	Item		Conditions	Min.	Typ.	Max.	Unit
V_{START}	Start-up Voltage					[4.5]	V
V_{CC}	VCC Pin Voltage (VCC–AGND)		V_{FB} = 0.672 V	[4.9]	5.1	[5.3]	V
$I_{STANDBY}$	Standby Current		V_{IN} = 34 V, CE = 0 V		3	[20]	µA
I_{VIN1}	VIN Consumption Current 1 at Switching Stop in PWM mode	R1272S0xx	V_{FB} = 0.672 V, MODE = 5 V, V_{OUT} = SENSE = LX = 5 V		1.0	[1.3]	mA
		R1272S1xx	V_{FB} = 0.672 V, MODE = 5 V, V_{OUT} = SENSE = 1.5 V, LX = 5 V		1.6	[1.9]	
I_{VIN2}	VIN Consumption Current 2 at Switching Stop in VFM mode	R1272S0xx	V_{FB} = 0.672 V, MODE = 0 V V_{OUT} = SENSE = LX = 5 V		15	[75]	µA
		R1272S1xx	V_{FB} = 0.672V, MODE = 0 V V_{OUT} = SENSE = 1.5 V, LX = 5 V		45	[145]	
V_{UVLO2}	UVLO Threshold Voltage		V_{CC} Rising	[3.85]	4.0	[4.2]	V
V_{UVLO1}			V_{CC} Falling	[3.1]	3.3	[3.4]	V
V_{FB}	FB Voltage Accuracy		Ta = 25°C	0.6336	0.64	0.6464	V
			-40°C ≤ Ta ≤ 105°C	[0.6272]		[0.6528]	
f_{OSC0}	Oscillation Frequency 0		RT = 135 kΩ	[225]	250	[275]	kHz
f_{OSC1}	Oscillation Frequency 1		RT = 32 kΩ	[900]	1000	[1100]	kHz
t_{OFF}	Minimum OFF Time		V_{IN} = 5 V, V_{OUT} = 5 V		120	[190]	ns
t_{ON}	Minimum ON Time				100	[120]	ns
f_{SYNC}	Synchronizing Frequency		f_{OSC} as the reference	[fosc×0.5]		[fosc×1.5]	kHz
				[250]		[1000]	
t_{SS1}	Soft-start Time 1		CSS / TRK = OPEN	[0.4]		[0.75]	ms
t_{SS2}	Soft-start Time 2		C_{SS} = 4.7 nF	[1.4]		[2.0]	ms
I_{TSS}	Charge Current for Soft-start Pin		CSS / TRK = 0 V	[1.8]	2	[2.2]	µA
V_{SSEND}	CSS/TRK Pin Voltage at End of Soft-start			[V_{FB}]	V_{FB} +0.03	[V_{FB}+0.06]	V
R_{DIS_CSS}	Discharge Resistance for CSS/TRK Pin		V_{IN} = 4.5 V, CE = 0 V, CSS / TRK = 3 V	[2.0]	3.0	[5.0]	kΩ
$R_{UPHGATE}$	On-resistance of Pull-up Transistor (HGATE Pin)		(BST – LX) = 5 V, I_{HGATE} = -100 mA		2.5	[5.0]	Ω

V_{IN} = 12 V, CE = V_{IN}, unless otherwise specified.

The specifications surrounded by [ ] are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1272SxxxA Continued (Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
$R_{DOWNHGATE}$	On-resistance of Pull-down Transistor (HGATE Pin)	(BST – LX) = 5 V, I_{HGATE} = 100 mA		1.5	3.5	Ω
$R_{UPLGATE}$	On-resistance of Pull-up Transistor (LGATE Pin)	(VCC – PGND) = 5 V, I_{LGATE} = -100 mA		4.0	7.0	Ω
$R_{DOWNLGATE}$	On-resistance of Pull-down Transistor (LGATE Pin)	(VCC – PGND) = 5 V, I_{LGATE} = 100 mA		1.5	3.5	Ω
V_{ILIMIT}	Current Limit Threshold Voltage (SENSE – VOUT)	R1272Sxx1x	40	50	60	mV
		R1272Sxx2x	60	70	80	mV
		R1272Sxx3x	90	100	110	mV
$V_{IREVLIMIT}$	Reverse Current Sense Threshold (SENSE – VOUT)	MODE = H/CLK R1272Sxx1x	-35	-25	-15	mV
		MODE = H/CLK R1272Sxx2x	-45	-35	-25	mV
		MODE = H/CLK R1272Sxx3x	-60	-50	-40	mV
$V_{LXSHORTL}$	LX Short to GND Detector Threshold Voltage (VIN – LX)		0.345	0.43	0.520	V
$V_{LXSHORTH}$	LX Short to VCC Detector Threshold Voltage (LX – PGND)		0.330	0.43	0.515	V
V_{CEH}	CE "High" Input Voltage		1.27			V
V_{CEL}	CE "Low" Input Voltage				1.14	V
I_{CEH}	CE "High" Input Current	CE = 34 V	0.20		2.45	µA
I_{CEL}	CE "Low" Input Current	CE = 0 V	-1.00	0	1.00	µA
I_{FBH}	FB "High" Input Current	V_{FB} = 3 V	-0.10		0.10	µA
I_{FBL}	FB "Low" Input Current	V_{FB} = 0 V	-0.10		0.10	µA
V_{MODEH}	MODE "High" Input Voltage		1.33			V
V_{MODEL}	MODE "Low" Input Voltage				0.74	V
I_{MODEH}	MODE "High" Input Current	MODE = 6 V	1.00		6.60	µA
I_{MODEL}	MODE "Low" Input Current	MODE = 0 V	-1.00	0	1.00	µA
$V_{CLKOUTH}$	CLKOUT Pin "High" Output Voltage	CLKOUT = Hi-z	4.7		V_{CC}	V
$V_{CLKOUTL}$	CLKOUT Pin "Low" Output Voltage	CLKOUT = Hi-z	0		0.1	V
T_{TSD}	Thermal Shutdown Threshold Temperature	Ta Rising	150	160		°C
T_{TSR}		Ta Falling	125	140		°C

V_{IN} = 12 V, CE = V_{IN}, unless otherwise specified.

The specifications surrounded by [ ] are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1272SxxxA Continued (Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
$V_{PGOODOFF}$	PGOOD "Low" Output Voltage	V_{IN} = 4.0 V, PGOOD = 1 mA		0.26	[0.54]	V
$I_{PGOODOFF}$	PGOOD Pin Leakage Current	V_{IN} = 34 V, PGOOD = 6 V	[-0.10]	0	[0.10]	μA
V_{FBOVD1}	FB Pin OVD Threshold Voltage	V_{FB} Rising	[0.680]	V_{FB}×1.10	[0.740]	V
V_{FBOVD2}		V_{FB} Falling	[0.664]	V_{FB}×1.07	[0.712]	V
V_{FBUVD1}	FB Pin UVD Threshold Voltage	V_{FB} Falling	[0.556]	V_{FB}×0.90	[0.604]	V
V_{FBUVD2}		V_{FB} Rising	[0.574]	V_{FB}×0.93	[0.628]	V
gm (EA)	Trans Conductance Amplifier	COMP = 1.5 V	[0.35]	1	[1.55]	mS

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

OPERATING DESCRIPTIONS

MODE Pin Function

The R1272S operating mode is switched among the forced PWM mode, PWM/VFM auto-switching mode and PLL_PWM mode, by a voltage or a pulse applied to MODE pin. The forced PWM mode is selected when the voltage of the MODE pin is more than 1.33 V, and the PWM works regardless of a load current. The PWM/VFM auto-switching mode is selected when it is less than 0.74 V, and control is switched between a PWM mode and a VFM mode depending on the load current.
See *Forced PWM mode and VFM mode* for details. And see *Frequency Synchronization Function* for the operation on connecting an external clock.

Frequency Synchronization Function

The R1272S can synchronize to the external clock being inputted via the MODE pin, with using a PLL (Phase-locked loop). The forced PWM mode is selected during synchronization. The external clock with a pulse-width of 100 ns or more is required. The allowable range of oscillation frequency is 0.5 to 1.5 times of the set frequency(1), and the operating guaranteed frequency is in the 250 kHz to 1 MHz range(2). The R1272S can synchronize to the external clock even if the soft-start works. That is, the R1272S executes the soft-start and the synchronization functions at a time if having started up while inputting an external clock to the MODE pin. When the maxduty or the duty_over state is caused by reduction in differential between input and output voltages, the device runs at asynchronous to the MODE pin, and it operates in the frequency reduced until one-fourth of the external clock frequency. Likewise, the CLKOUT pin becomes asynchronous to the MODE pin. If making synchronization to the MODE pin, take notice in use under a reduced input voltage.

Duty_over Function

When the input voltage is reduced at cranking, the operating frequency is reduced until one-fourth of the set frequency with being linearly proportional to time in order to maintain the output voltage. Exploiting the ON duty to exceed the maxduty value at normal operation can make the differential between input and output voltages small.

PGOOD (Power Good) Output Function

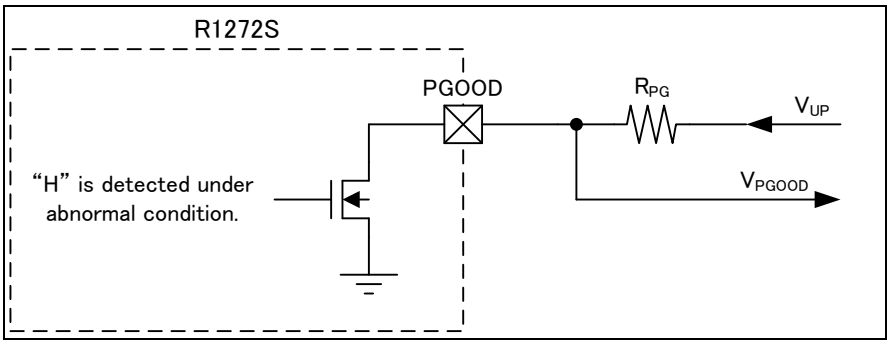
The power good function with using a NMOS open drain output pin can detect the following states of the R1272S. The NMOS turns on and the PGOOD pin becomes “Low” when detecting them. After the R1272S returns to their original state, the NMOS turns off and the PGOOD pin outputs “High” (PGOOD Input Voltage: V_{UP}).

- CE = “L” (Shut down)
- UVLO (Shut down)
- Thermal Shutdown
- Soft-start time

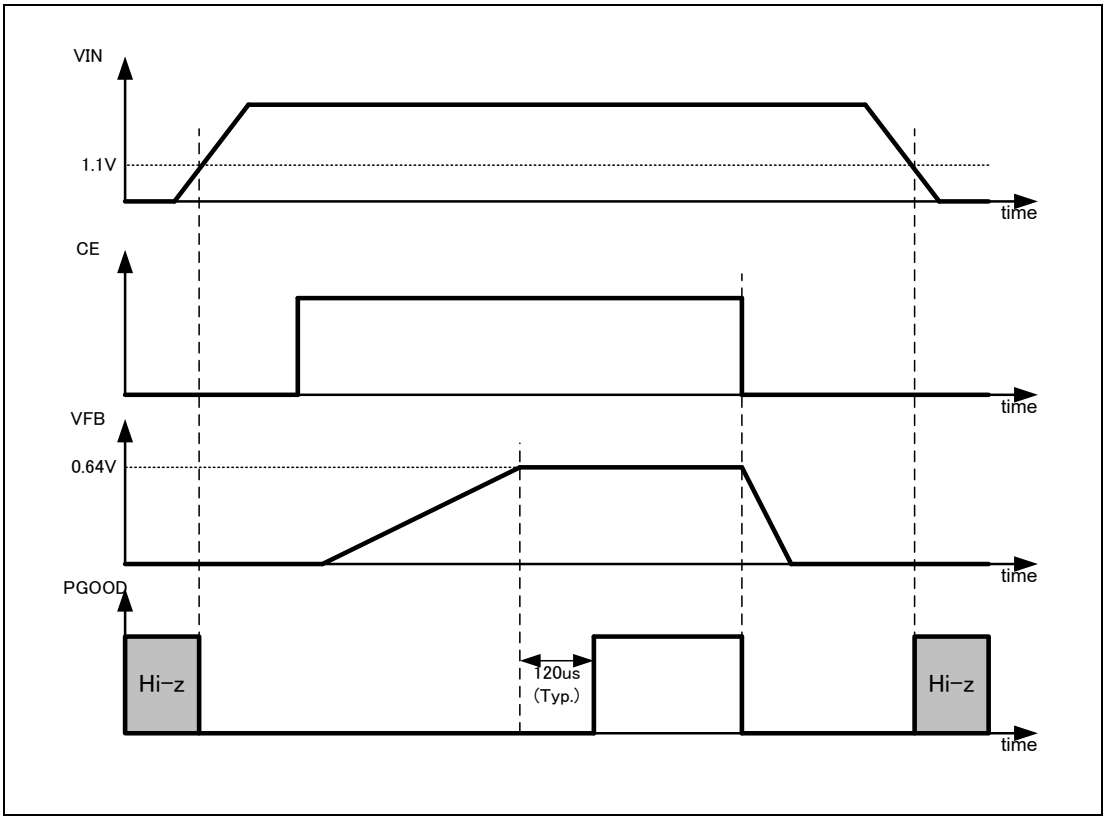
(1) See *Oscillation Frequency Setting* for details of the set frequency.
(2) The adjustable oscillation frequency range becomes 250 kHz ≤ f_{OSC} ≤ 600 kHz when 0.7 V ≤ V_{OUT} < 1.35V.

・at UVD Threshold Voltage Detection
・at OVD Threshold Voltage Detection
・at hiccup-type Protection (when hiccup mode is selected)
・at latch-type Protection (when latch mode is selected)

The PGOOD pin is designed to become 0.54 V or less in “Low” level when the current floating to the PGOOD pin is 1 mA. The use of the PGOOD input voltage (V_{UP}) of 5.5 V or less and the pull-up resistor (RPG) of 10 kΩ to 100 kΩ are recommended. If not using the PGOOD pin, connect it to “Open” or “GND”.



PGOOD Output Pin Connecting Diagram



Rising / Falling Sequence of Power Good Circuit

Under Voltage Detection (UVD)

The UVD function indirectly monitors the output voltage with using the FB pin. The PGOOD pin outputs “L” when the UVD detector threshold is 90% (Typ.) of V_{FB} and V_{FB} is less than the UVD detector threshold for more than 30 µs (Typ.). When V_{FB} is over 93% (Typ.) of 0.64 V, the PGOOD pin outputs “H” after delay time (Typ.120 µs.). And, the hiccup- / latch-type overcurrent protection works when detecting an overcurrent, an LX power supply protection, or an over voltage protection during the UVD detection.

Over Voltage Detection (OVD)

The OVD function indirectly monitors the output voltage with using the FB pin. Switching stops even if the internal circuit is active state, when detecting the over voltage of V_{FB}. The PGOOD pin outputs “L” when the OVD detector threshold is 110% (Typ.) of V_{FB} and V_{FB} is over the OVD detector threshold for more than 30 µs (Typ.). When V_{FB} is under 107% (Typ.) of V_{FB}, which is the OVD released voltage, the PGOOD pin outputs “H” after delay time (Typ.120 µs.). Then, switching is controlled by normal operation. The over voltage protection works when an error is caused by a feedback resistor in peripheral circuits for the FB pin.

Over Voltage Protection (OVP)

The OVP function monitors the voltage of VOUT pin to reduce an over voltage, when an error is caused in peripheral circuits for the FB pin. Switching stops even if the internal circuit is active state, when V_{OUT} is over the OVP detector threshold. When V_{OUT} is under the OVP detector threshold, switching is controlled by normal operation. If the UVD for FB pin occur during the OVP detect state, an error will occur and hiccup- / latch-type protection will work. However, the operation under this function is not guaranteed because the OVP detector threshold is set to the absolute maximum rating and more for the VOUT pin.

LX Power Supply (VIN Short) / GND (GND Short) Protection

In addition to normal current limit, the R1272S provides the LX power supply / GND short protection to monitor the voltage between the FET’s drain and source. Since the current limit function is controlled with an external inductor’s DCR or a sense resistance, the current limit function cannot work when a through-current is flowed through the FET and when an overcurrent is generated by shorting the LX pin to VDD/GND. The detecting current is determined by LX shot to VDD/GND detector threshold voltage (FET_On-resistance x Current, Typ.0.43 V).

Hiccup-type / Latch-type Overcurrent Protection

The hiccup-type / latch-type overcurrent protection can work under the operating conditions that is the UVD can function during the current limit or OVP and the LX GND short protection. The latch-type protection can release the circuit by setting the CE pin to “L” or by reducing V_{IN} to be less than the UVLO detector threshold, when the output is latched off. The hiccup type protection stops switching releases the circuit after the protection delay time (Typ. 3.5 ms). Since this protection is auto-release, the CE pin switching of “L” / “H” is unnecessary. And, damage due to the overheating might not be caused because the term to release is long. When the output is shorted to GND, switching of “ON” / “OFF” is repeated until the shorting is released.

Current Limit Function

The current limit function can be to limit the current by the peak current method to turn the high-side FET off that the potential differences is over the current limit threshold voltage. The threshold voltage is selectable among 50 mV / 70 mV / 100 mV. And, the two following detection methods can be selected by external components connected.

A. Detecting Method with R_{SENSE}

The current limit value is detected with the voltage across the inductor that a sense resistance is connected in series. By connecting a resistance with low level of variation, the current limit with high accuracy can achieve. As a result, be caution that the power loss is caused from the current and R_{SENSE}. The peak current in the current limit inductor can be calculated by the following equation.

Peak current in Current limit inductor (A) = Current limit threshold voltage (mV) / R_{SENSE} (mΩ)

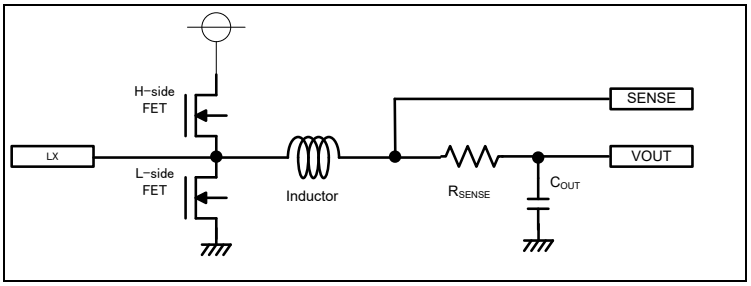


Figure A Detection with Sense Resistance

B. Detecting Method with DCR of Inductor

The current limit value is detected with the DCR of the inductor. The reduction of the loss is minimized since the inductor is in no need of a resistance. But, the SENSE pin requires to connect a resistor and a capacitor to each end of the inductor. Because a constant slope is caused depending on the inductance and the capacitance. Factors causing the poor accuracy of current limit value include the variation in production of the inductor's DCR and the temperature characteristics. R_S and C_S can be calculated by the following equation.

Peak current in Current limit inductor (A) = Current limit threshold voltage (mV) / Inductor's DCR (mΩ)
C_S = L / (DCR x R_S)

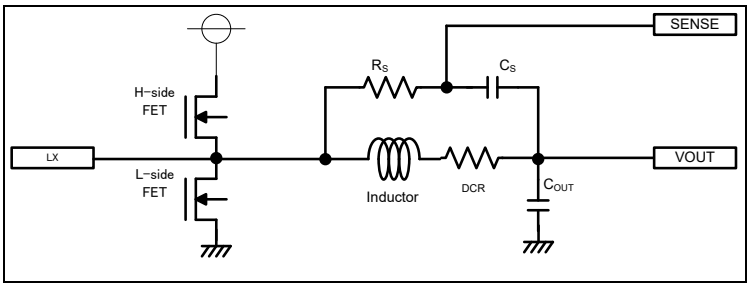


Figure B Detecting with Inductor's DCR

Output Voltage Setting

The output voltage (V_{OUT}) can be set by adjustable values of R_{TOP} and R_{BOT}. The value of V_{OUT} can be calculated by Equation 1 :

$$V_{OUT} = V_{FB} \times (R_{TOP} + R_{BOT}) / R_{BOT} \quad \cdots\cdots \text{Equation1}$$

For example, when setting V_{OUT} = 3.3 V and setting R_{BOT} = 22 kΩ, R_{TOP} can be calculated by substituting them to Equation 1. As a result of the expanding Equation 2, R_{TOP} can be set to 91.4 kΩ.
To make 91.4 kΩ with using the E24 type resistors, the connecting use of 91 kΩ and 0.39 kΩ resistors in series is required. If the tolerance level of the set output voltage is wide, using a resistor of 91 kΩ to R_{TOP} can reduce the number of components.

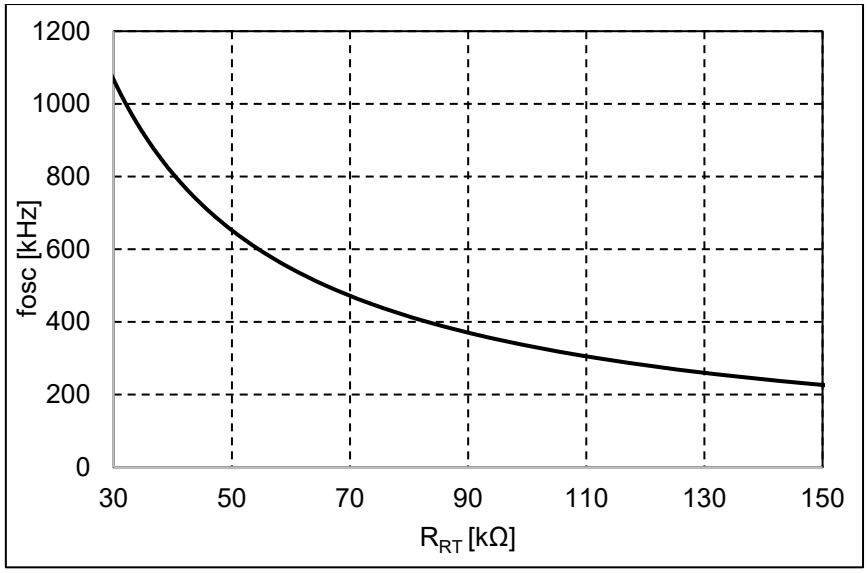
$$R_{TOP} = (3.3\ V / 0.64\ V - 1) \times 22\ k\Omega$$
$$= 91.4\ k\Omega \quad \cdots\cdots \text{Equation2}$$

As to R1272S00x, R1272S01x and R1272S03x, R_{TOP} and R_{BOT} should be selected to meet the required output voltage (V_{OUT}) > 2.91 V with a variation in resistance taken into account.

Oscillation Frequency Setting

Connecting the oscillation frequency setting resistor (R_{RT}) between the RT pin and GND can control the oscillation frequency in the range of 250 kHz to 1 MHz(1). For example, using the resistor of 66 kΩ can set the frequency of about 500 kHz.
The Electrical Characteristics guarantees the oscillation frequency under the conditions stated below for f_{OSC0} (at R_{RT} = 135 kΩ) and f_{OSC1} (at R_{RT} = 32 kΩ).

(1) The adjustable oscillation frequency range becomes 250 kHz ≤ f_{OSC} ≤ 600 kHz when 0.7 V ≤ V_{OUT} < 1.35V.



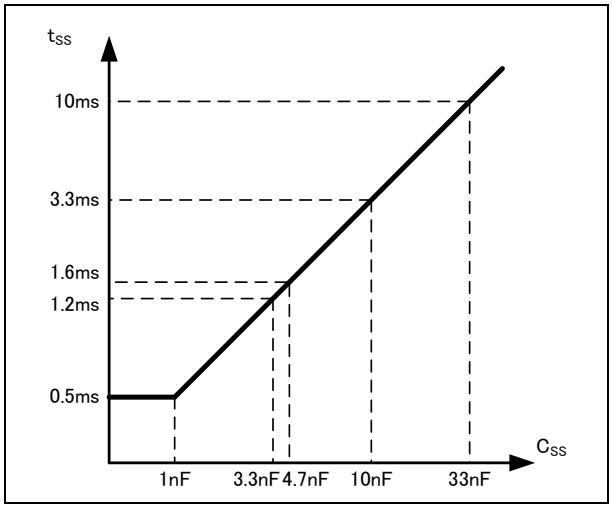
R_{RT} [kΩ] = 41993 x f_{OSC} [kHz] ^ (-1.039)

R1272S001A Oscillation Frequency Setting Resistor (R_{RT}) vs. Oscillation Frequency (f_{OSC})

Soft-start Function

The soft-start time is a time between a rising edge (“H” level) of the CE pin and the timing when the output voltage reaches the set output voltage. Connecting a capacitor (C_{SS}) to the CSS / TRK pin can adjust the soft-start time (t_{SS}) – provided the internal soft-start time of 500 µs (Typ.) as a lower limit. The adjustable soft-start time (t_{SS2}) is 1.6 ms (Typ.) when connecting an external capacitor of 4.7 nF with the charging current of 2.0 µA (Typ.). If not required to adjust the soft-start time, set the CSS / TRK pin to “Open” to enable the internal soft-start time (t_{SS1}) of 500 µs (Typ.). If connecting a large capacitor to an output signal, the overcurrent protection or the LX GND short protection might run. To avoid these protections caused by starting abruptly when reducing the amount of power current, soft-start time must be set as long as possible.

Each of soft-start time (tss1/ tss2) is guaranteed under the conditions described in the chapter of “Electrical Characteristics”.

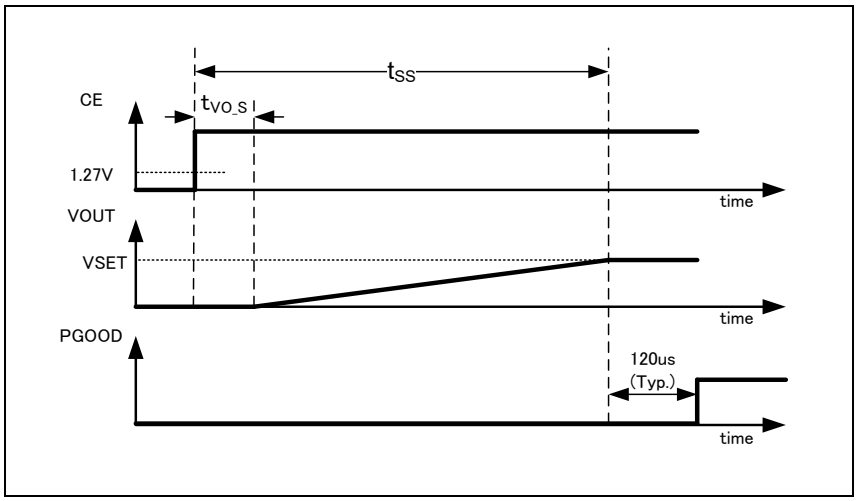


C_{SS} [nF] = (t_{SS} - t_{VO_S}) / 0.64 × 2.0

t_{SS}: Soft-start time (ms)

t_{VO_S}: Time period from CE = "H" to VOUT's rising (Typ. 0.160 ms)

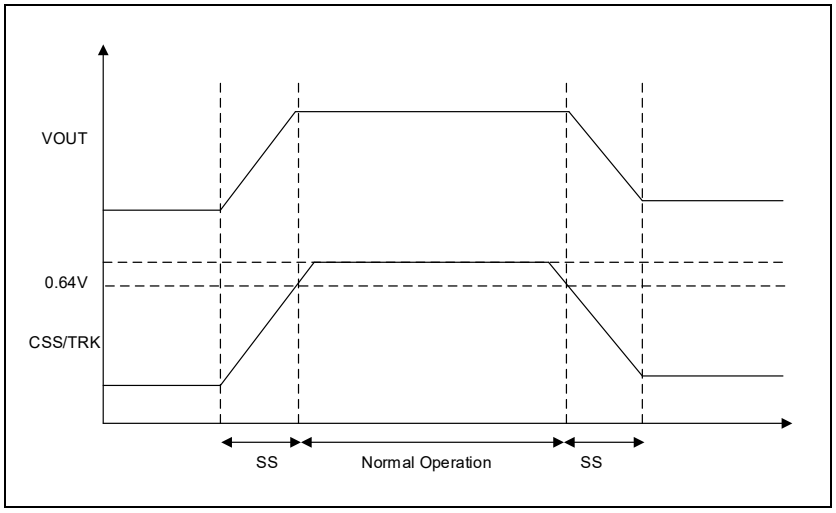
Soft-start Time Adjustable Capacitor (C_{SS}) vs. Soft-start Time (t_{SS})



Soft-start Sequence

Tracking Function

Applying an external tracking voltage to the CSS / TRK pin can control the soft-start sequence – provided that the lowest internal soft-start time is limited to 500 µs (Typ.). Since V_{FB} becomes nearly equal to $V_{CSS/TRK}$ at tracking, the complex start timing and soft-start can be easily designed. The available voltage at tracking is between 0 V and 0.64 V. If the tracking voltage is over 0.64 V, the internal reference voltage of 0.64 V is enabled. Also, an arbitrary falling waveform can be generated by reducing $V_{CSS/TRK}$ to 0.64 V (Typ.) or less, because the R1272S supports both of up- and down- tracking.



Tracking Sequence

Min. ON-time

The min. ON time (Max. 120 ns), which is determined in the R1272S internal circuit, is a minimum time to turn high-side FET on. The R1272S cannot generate a pulse width less than the min. ON time. Therefore, settings of the output set voltage and the oscillator frequency are required so that the minimum step-down ratio [V_{OUT}/V_{IN} x (1 / f_{OSC})] does not stay below 120ns. If staying below 120 ns, the pulse skipping will operate to stabilize the output voltage. However, the ripple current and the output voltage ripple will be larger.

Min. OFF-time

By the adoption of bootstrap method, the high-side FET, which is used as the R1272S internal circuit for the min. OFF time, is used a NMOS. The voltage sufficient to drive the high-side FET must be charged. Therefore, the min. OFF time is determined from the required time to charge the voltage. By the adoption of the frequency's reduction method by one-quarter of a set value (Min.), if the input-output difference voltage becomes small or load transients are caused, the OFF period can be caused once in four-cycle period of normal cycle. As a result, the min. OFF time becomes 30 ns (Typ.) substantially, and the maximum duty cycle can be improved.

Through-current Protection

The HGATE pin voltage (V_{HGATE}) and the LGATE pin voltage (V_{LGATE}) are monitored to protect a through-type current caused by an external FET. In the case of turning-on the low-side FET, after a difference between V_{HGATE} - LX pin voltage (V_{LX}) becomes 1V or less, increasing V_{LGATE} can prevent not to turn on both of the high-side and low-side FETs at a time and thereby prevent the through-current. In the case of turning-on the high-side FET, after a difference between V_{LGATE} - GND (PGND pin voltage) becomes 1 V or less, increasing a difference between V_{HGATE} - V_{LX} can prevent the through-current.

Reverse Current Limit Function

The reverse current limit function works when the output voltage is pulled up more than the set output voltage by shorting. When the current is over the threshold current to detect the reverse current, the LGATE pin becomes to “L” to control the reverse current. As with the current limit value, the reverse current limit value is determined by the voltage between the VOUT pin and the SENSE pin. The detector threshold is one half of the current limit value.

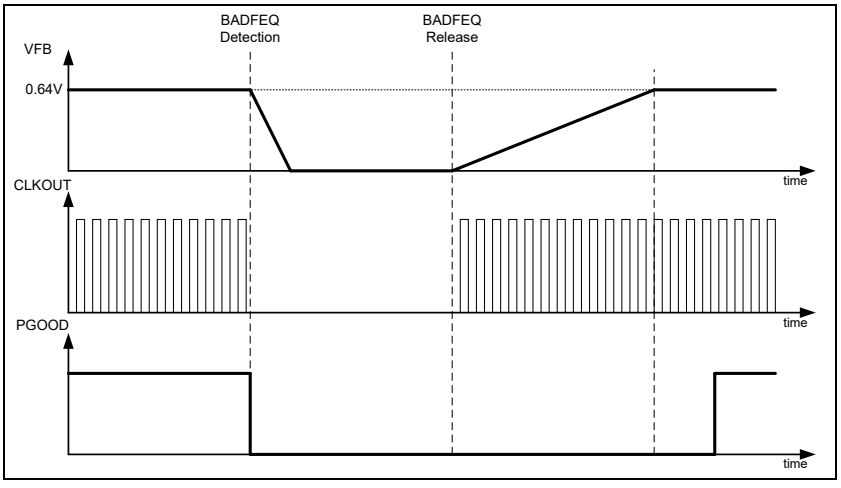
SSCG (Spread Spectrum Clock Generator)

The SSCG function works for EMI reduction at the PWM mode. This function is enabled in the R1272S03xA/13xA.

This function makes EMI waveforms decrease in amplitude to generate a ramp waveform within approximately ±3.6% (Typ.) of the oscillator frequency (f_{OSC}). The modulation cycle is f_{OSC} / 128. At the VFM mode, the SSCG is disabled.

Bad Frequency (BADFREQ) Protection

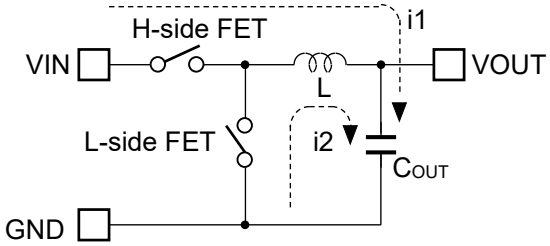
If a current equivalent to 2 MHz (Typ.) or more or 125 kHz (Typ.) or less is applied to the RT pin when the resistor of the RT pin is in open / short, the R1272S will stop switching to protect the IC and will cause the internal state to transition to its state before the soft-start. The CLKOUT pin is fixed to “L” while the bad frequency as above is detected. The R1272S will restart under the normal control from the state of soft-start when recover after the abnormal condition.



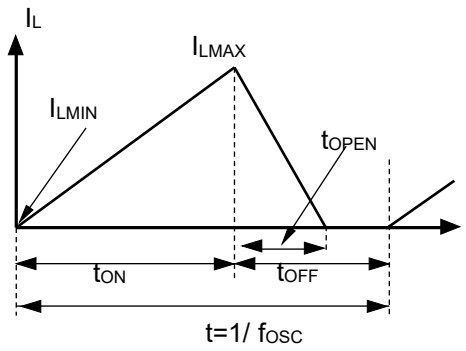
BADFREQ Detection / Release Sequence

Operation of Step-down Converter

A basic step-down DC/DC converter circuit is illustrated in the following figures. This DC/DC converter charges energy in the inductor when the high-side FET turns on, and discharges the energy from the inductor when the high-side FET turns off and controls with less energy loss, so that a lower output voltage than the input voltage is obtained.



Basic Circuit



Current Through Inductor

Step1. The high-side FET turns on and current IL (= i1) flows, and energy is charged into C_{OUT}. At this moment, I_L increases from I_{LMIN} (= 0) to reach I_{LMAX} in proportion to the on-time period (ton) of the high-side FET turns on and current I_L (= i1) flows, and energy is charged into C_{OUT}. At this moment, I_L increases from I_{LMIN} (= 0) to reach I_{LMAX} in proportion to the on-time period (t_{ON}) of the high-side FET.

Step2. When the high-side FET turns off, the low-side FET turns on in order to maintain I_L at I_{LMAX}, and current I_L (= i2) flows.

Step3. When MODE = L (VFM/PWM Auto-switching mode),
I_L (= i2) decreases gradually and reaches $I_L = I_{LMIN} = 0$ after a time period of t_{OPEN}, and the low-side FET turns off. This case is called as discontinuous mode. The VFM mode is switched if go to the discontinuous mode. If the output current is increased, a time period of t_{OFF} runs out prior to reach of $I_L = I_{LMIN} = 0$. The result is that the high-side FET turns on and the low-side FET turns off in the next cycle. This case is called continuous mode.
When MODE = H (Forced PWM mode), MODE = External Clock (PLL_PWM mode),
Since the continuous mode works at all time, the low-side FET turns on until going to the next cycle. That is, the low-side FET must keep “On” to meet $I_L = I_{LMIN} < 0$, when reaches $I_L = I_{LMIN} = 0$ after a time period of t_{OPEN}.

In the PWM mode, the output voltage is maintained constant by controlling t_{ON} with the constant switching frequency (f_{OSC}).

Forced PWM Mode and VFM Mode

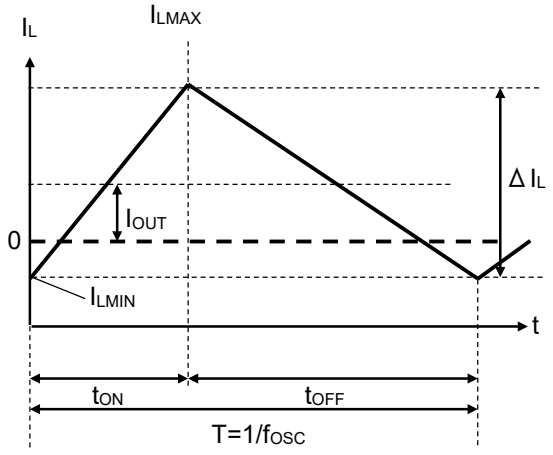
The output voltage control methods are selectable between the PWM / VFM Auto-switching mode and the forced PWM mode by using the MODE pin.

Forced PWM Mode

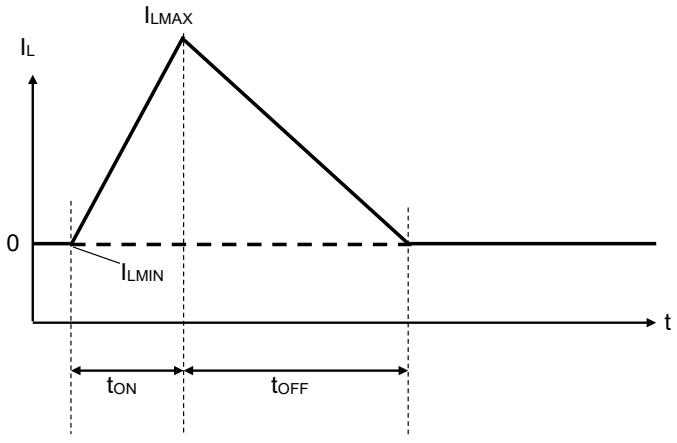
Forced PWM mode is selected when setting the MODE pin to “H”. This mode can reduce the output noise, since the frequency is fixed during light load conditions. Thus, I_{LMIN} becomes less than "0" when I_{OUT} is less than $\Delta I_L/2$. That is, the electric charge, which is charged to C_{OUT}, is discharged via FET for the durations – when I_L reaches “0” from I_{LMIN} during the t_{ON} periods and when I_L reaches I_{LMIN} from “0” during t_{OFF} periods.
But, pulses are skipped to prevent the overvoltage when high-side FET is set to ON under the condition that the output voltage being more than the set output voltage.

VFM Mode

PWM / VFM Auto-switching mode is selected when setting the MODE pin to “L”. This mode can automatically switch from PWM to VFM to achieve a high-efficiency during light load conditions. By the VFM mode architecture, the high-side FET is turned on for t_{ON} x 1.54 (typ.) at the PWM mode under the same condition as the VFM mode when the VFB pin voltage drops below the internal reference voltage (Typ.0.64 V). After the On-time, the high-side FET is turned off and the low-side FET is turned on. When the inductor current of 0 A is detected, the low-side FET is turned off and the switching operation is stopped (Both of hi- and low-side FETs are OFF). The switching operation restarts when the VFB pin voltage becomes less than 0.64 V.
The On-time at the PWM mode is determined by a resistance, input and output voltages, which are connected to the RT pin. Refer to “*Calculation of VFM Ripple”* for detailed description on the On-time at the VFM mode.



Forced PWM Mode



VFM Mode

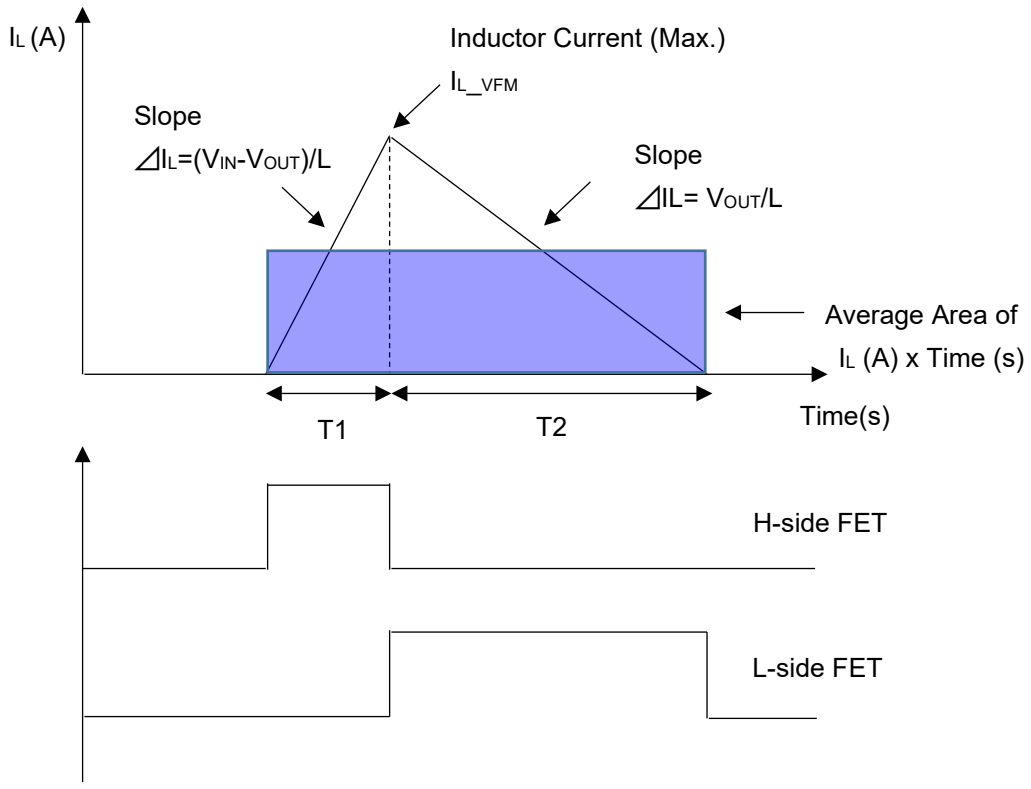
Calculation of VFM Ripple

Calculation example of output ripple voltage (V_{OUT_VFM}) is described. V_{OUT_VFM} can be calculated by Equation 1. And, the maximum value of inductor current (I_{L_VFM}) can be calculated by Equation 2.

$$V_{OUT\_VFM} = R_{COUT\_ESR} \times (I_{L\_VFM}) + C_{OEF\_TON\_VFM} \times (I_{L\_VFM} / 2) / f_{OSC} / C_{OUT\_EFF} \cdots\cdots \text{Equation1}$$

$$I_{L\_VFM} = ((V_{IN} - V_{OUT}) / L) \times C_{OEF\_TON\_VFM} \times V_{OUT} / V_{IN} / f_{OSC} \cdots\cdots \text{Equation 2}$$

V_{OUT_VFM} : Output ripple
R_{COUT_ESR} : ESR of output capacitor
I_{L_VFM} : Maximum current of inductor
$C_{OEF\_TON\_VFM}$: Scaling factor of On-time - Typ.1.54X (Design value)
$(V_{IN}-V_{OUT}) / L$: Slope of inductor current
$C_{OEF\_TON\_VFM} \times V_{OUT} / V_{IN} / f_{OSC}$: On-time



Inductor Current Waveform at VFM Mode

Output voltage can be calculated by the following simple equation.

$V_{OUT} = I \times T/C$

I : Current, C : Capacitance, T : Time

Since I is represented by *1/2 x* I_{L_VFM} as the average current, the time of current passing at the VFM mode can be expressed by the following equation.

$T = C_{OEF\_TON\_VFM} / f_{OSC}$

And, the output ripple voltage (V_{OUT_VFM}) is superimposed a voltage for ESR × I, and Equation 1 is determined. But, ESR is so small that it may be ignored if ceramic capacitors are connected in parallel.

The amount of charge to the output capacitor can be calculated by Equation 3.

(High-side FET On-time (T1) + Low-side FET On-time (T2)) × Average amount of current

…… Equation3

Then, T1 and T2 can be calculated by the following equations, and the time of current passing can be determined.

$T1 = C_{OEF\_TON\_VFM} / f_{OSC} \times V_{OUT} / V_{IN}$…… (On-time at VFM)
$T2 = (V_{IN}/V_{OUT}-1) \times T1$ ($0 = I_{L\_VFM} – V_{OUT}/L \times T2$)

$T = T1 + T2$
$= V_{IN} /V_{OUT} \times T1$
$= C_{OEF\_TON\_VFM} / f_{OSC}$

And then, the amount of charge can be determined as Equation 4.

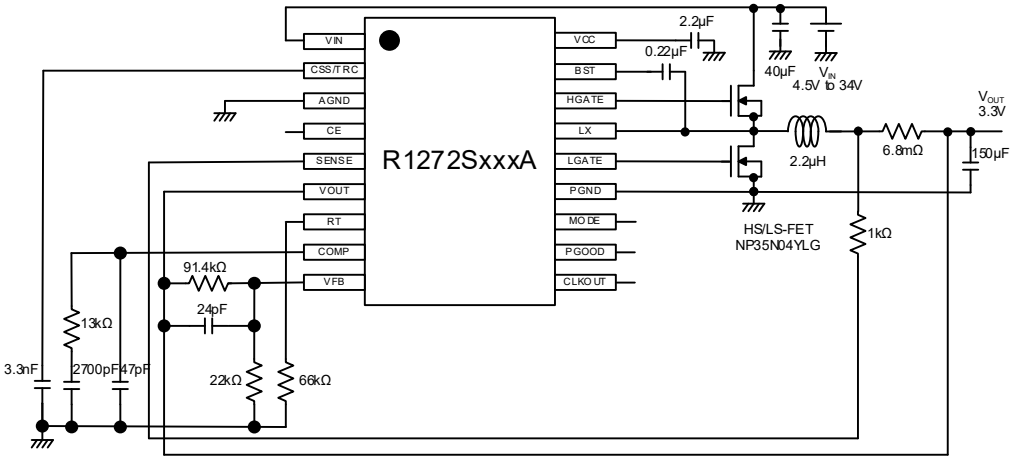
$T \times I_{L\_VFM} /2 = C_{OEF\_TON\_VFM} / f_{OSC} \times I_{L\_VFM} /2$ …… Equation 4

With using above-equations, the output ripple voltage (V_{OUT_VFM}) can be calculated by Equation 5.

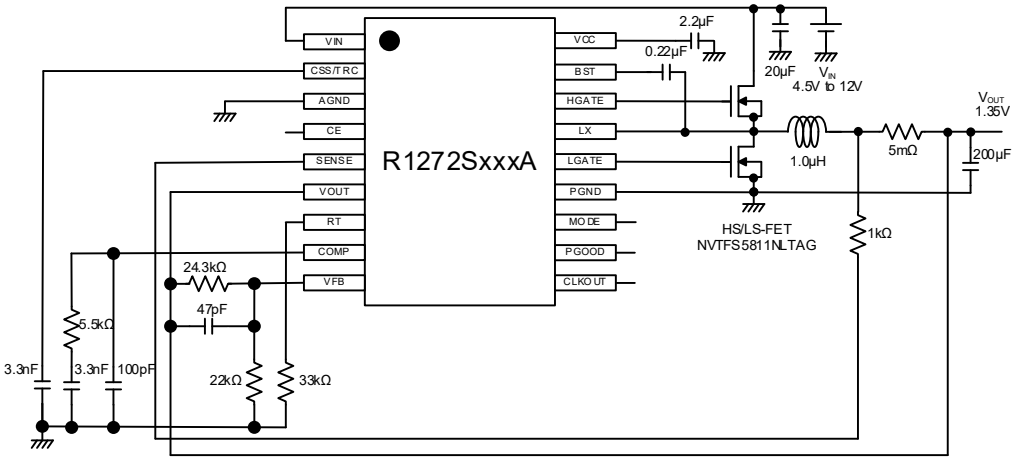
$V = IT/C = C_{OEF\_TON\_VFM} / f_{OSC} \times I_{L\_VFM} / 2 / C_{OUT\_EFF}$ …… Equation 5

APPLICATION INFORMAITON

Typical Application Circuit



R1272SxxxA Typical Application Circuit at 500 kHz



R1272SxxxA Typical Application Circuit at 1MHz

Selection of External Components

External components and its value required for R1272S are described. Each value is reference value at initial. Since inductor's variations and output capacitor's effective value may lead a drift of phase characteristics, adjustment to a unity-gain and phase characteristics may be required by evaluation on the actual unit.

1. Determination of Requirements

Determine the frequency, the output capacitor, and the input voltage required. For reference values, parameters listed in the following table will be used to explain each equation.

Parameter	Value
Output Voltage (V_{OUT})	3.3 V
Output Current (I_{OUT})	10 A
Input Voltage (V_{IN})	12 V
Input Voltage Range	8 V to 16 V
Frequency (f_{OSC})	500 kHz
ESR of Output Capacitor (R_{COUT_ESR})	3 mΩ

2. Selection of Unity-gain frequency (f_{UNITY})

The unity-gain frequency (f_{UNITY}) is determined by the frequency that the loop gain becomes "1" (zero dB). It is recommended to select within the range of one-sixth to one-tenth of the oscillator frequency (f_{OSC}). Since the f_{UNITY} determines the transient response, the higher the f_{UNITY}, the faster response is achieved, but the phase margin will be tight. Therefore, it is required that the f_{UNITY} can secure the adequate stability. As for the reference, the f_{UNITY} is set to 70 kHz.

3. Selection of Inductor

After the input and the output voltages are determined, a ripple current (ΔI_L) for the inductor current is determined by an inductance (L) and an oscillator frequency (f_{OSC}). The ripple current (ΔI_L) can be calculated by Equation 1.

$$\Delta I_L = (V_{OUT} / L / f_{OSC}) \times (1 - V_{OUT} / V_{IN\_MAX}) \quad \text{Equation 1}$$

V_{IN_MAX} : Maximum input voltage

The core loss in the inductor and the ripple current of the output voltage become small when the ripple current (ΔI_L) is small. But, a large inductance is required as shown by Equation 1. The inductance can be calculated by Equation 2 when a reference value of ΔI_L assumes 30% of I_{OUT} is appropriate value.

$$L = (V_{OUT} / \Delta I_L / f_{OSC}) \times (1 - V_{OUT} / V_{IN\_MAX}) \quad \text{Equation 2}$$
$$= (V_{OUT} / (I_{OUT} \times 0.3) / f_{OSC}) \times (1 - V_{OUT} / V_{IN\_MAX})$$

The inductance can be calculated by substituting each parameter to Equation 2.

L = (3.3 V / 3 A / 500 kHz) x (1-3.3 V / 16 V)
= 1.75 µH

When selecting the inductor of 2.2µH as an approximate value of the above calculated value, ΔI_L can be shown as below.

ΔI_L = (3.3 V / 2.2 µH / 500 kHz) x (1-3.3 V / 16 V)
= 2.38 A

4. Setting of Output Capacitance

The output capacitance (C_{OUT}) must be set to meet the following conditions.

■ Calculation based on phase margin

To secure the adequate stability, it is recommended that the pole frequency (f_{P_OUT}) is set to become equal or below one-fourteenth of the unity-gain frequency. The pole frequency (f_{P_OUT}) can be calculated by Equation 3.

$$f_{P\_OUT} = 1/(2 \times \pi \times C_{OUT\_EFF} \times ((R_{OUT\_MIN} \times 2 \times \pi \times f_{OSC} \times L) / (R_{OUT\_MIN} + 2 \times \pi \times f_{OSC} \times L) + R_{COUT\_ESR})) \quad \cdots\cdots\cdots\cdots \text{Equation 3}$$

C_{OUT_EFF} : Output capacitance (effective value)
R_{OUT_MIN} : Output resistance at maximum output current
$R_{OUT\_MIN} = V_{OUT} / I_{OUT}$
= 3.3 V / 10 A
= 0.33 Ω

Equation 4 can be expressed by substituting $f_{P\_OUT} = f_{UNITY} / 14$ to Equation 3.

$$C_{OUT\_EFF} = 14 / (2 \times \pi \times f_{UNITY} \times ((R_{OUT\_MIN} \times 2 \times \pi \times f_{OSC} \times L) / (R_{OUT\_MIN} + 2 \times \pi \times f_{OSC} \times L) + R_{COUT\_ESR})) \quad \cdots\cdots\cdots\cdots \text{Equation 4}$$

Then, the output capacitance (effective value) can be calculated by substituting each parameter to Equation 4.

C_{OUT_EFF} = 14 / (2 × π ×70kHz×((0.33Ω × 2 × π × 500 kHz × 2.2 µH) / (0.33Ω+ 2 × π × 500kHz × 2.2µH)+3mΩ))
= 100.1 µF

It is recommended that the output capacitance is set to become equal or over the effective value calculated by Equation 4.

The output capacitance (effective value), which is derated depending on the DC voltage applied, can be calculated by Equation 5. Refer to "*Capacitor Manufacture's Datasheet"* for details about derating.

$$C_{OUT\_EFF} = C_{OUT\_SET} \times (V_{CO\_AB} - V_{OUT}) / V_{CO\_AB} \quad \cdots\cdots \text{Equation 5}$$

C_{OUT_SET} : Output capacitor's spec
V_{CO_AB} : Capacitor's voltage rating

With using Equation 5, the effective value is calculated to become 100.1 µF or more. The output voltage (C_{OUT}) can be shown as below when V_{CO_AB} is 10 V.

$C_{OUT\_SET} > C_{OUT\_EFF} / ((V_{CO\_AB} - V_{OUT}) / V_{CO\_AB})$
$C_{OUT\_SET} > 100.1\mu F / ((10 - 3.3) / 10)$
$C_{OUT} > 149.4\ \mu F$

As the calculated result, C_{OUT} selects a capacitor of 150 µF (the effective value is 100.5 µF).

■ Calculation based on ripple at VFM mode

With using the calculated value of C_{OUT}, the amount of ripple at the VFM mode can be shown as Equations 6 and Equation 7.

$$I_{L\_VFM} = ((V_{IN\_MAX}-V_{OUT}) / L) \times C_{OEF\_TON\_VFM} \times V_{OUT} / V_{IN\_MAX} / f_{OSC} \quad \cdots\cdots \text{Equation 6}$$

$$V_{OUT\_VFM} = R_{COUT\_ESR} \times (I_{L\_VFM}) + C_{OEF\_TON\_VFM} \times (I_{L\_VFM} / 2) / f_{OSC} / C_{OUT\_EFF} \quad \cdots\cdots \text{Equation 7}$$

I_{L_VFM} : Maximum current of inductor
$C_{OEF\_TON\_VFM}$: On-time scaling (multiples of PWM_ON time)
V_{OUT_VFM} : Maximum output ripple

$C_{OEF\_TON\_VFM}$ can be calculated by 1.54 times (Typ.) as the design value. The ripple value can be calculated by substituting each parameter to Equations 6 and Equation 7.

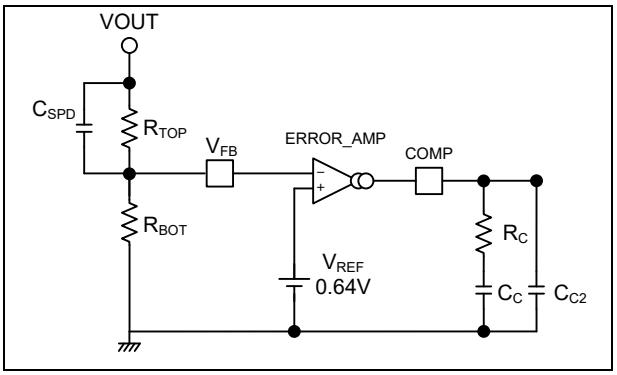
$I_{L\_VFM} = ((16\ V - 3.3\ V) / 2.2\ \mu H) \times 1.54 \times 3.3\ V / 16\ V / 500\ kHz$
$= 3.67\ A$
$V_{OUT\_VFM} = 3\ m\Omega \times 3.67\ A + 1.54 \times (3.67\ A / 2) / 500\ kHz / 100.5\ \mu F$
$= 67.2\ mV$

V_{OUT_VFM} must be set to become the target ripple value or less. If V_{OUT_VFM} is over the target value, the output capacitance must be calculated by Equation 8.

$$C_{OUT\_EFF} = 1.54 \times (I_{L\_VFM} / 2) / f_{OSC} / (V_{OUT\_VFM} - R_{COUT\_ESR} \times (I_{L\_VFM})) \quad \cdots\cdots \text{Equation 8}$$

5. Designation of Phase Compensation

Since the current amplifier for the voltage feedback is output via the COMP pin, the phase compensation is achieved with using external components. The phase compensation is able to secure stable operation with using an external ceramic capacitor and the phase compensation circuit.



Connection Example for External Phase Compensation Circuit

■ Calculation of R_C

The phase compensation resistance (R_C) to set the calculated unity-gain frequency can be calculated by Equation 9.

$$R_C = 2 \times \pi \times f_{UNITY} \times V_{OUT} \times C_{OUT\_EFF} / (g_{m\_ea} \times V_{REF} \times g_{m\_pwr}) \quad \cdots\cdots \text{Equation 9}$$

g_{m_ea} : Error amplifier of g_m
V_{REF} : Reference voltage (0.64 V)
g_{m_pwr} : power level of g_m

$g_{m\_pwr} \times \Delta V_S = \Delta I_L$

$g_{m\_ea} / \Delta V_S = 0.05 \times 10 \text{ ^ } (-6) \times f_{OSC} / V_{OUT}$

$$g_{m\_ea} \times g_{m\_pwr} = 0.05 \times 10 \text{ ^ } (-6) \times \Delta I_L \times f_{OSC} / V_{OUT} \quad \cdots\cdots \text{Equation 10}$$

ΔV_S : Output amplitude of the slope circuit

R_C can be calculated by substituting Equation 10 to Equation 9.

$R_C = 2 \times \pi \times f_{UNITY} \times V_{OUT} \times C_{OUT\_EFF} / (V_{REF} \times 0.05 \times 10 \text{ ^ } (-6) \times \Delta I_L \times f_{OSC} / V_{OUT})$
$= 2 \times \pi \times 70 \text{ kHz} \times 3.3 \text{ V} \times 100.5 \text{ µF} / (0.64 \times 0.05 \times 10 \text{ ^ } (-6) \times 2.38\text{A} \times 500 \text{ kHz} / 3.3 \text{ V})$
$= 12.63 \fallingdotseq 13 \text{ kΩ}$

■ Calculation of C_C

C_C must be calculated by Equation 11 so that the zero frequency of the error amplifier meets the highest pole frequency (f_{P_OUT}). Then, f_{P_OUT} = 5.0 kHz is determined by calculation of Equation 3.

$$C_C = 1 / (2 \times \pi \times R_C \times f_{P\_OUT}) \quad \text{Equation 11}$$
$$= 1/ (2 \times 3.14 \times 13\ k\Omega \times 5.0\ kHz)$$
$$= 2.45 \fallingdotseq 2.7\ nF$$

■ Calculation of C_{C2}

C_{C2} can be calculated by two different calculation methods to vary from the zero frequency (f_{Z_ESR}) depending on the ESR of a capacitor. f_{Z_ESR} can be calculated by Equation 12.

$$f_{Z\_ESR} = 1 / (2 \times \pi \times R_{COUT\_ESR} \times C_{OUT\_EFF}) \quad \text{Equation 12}$$
$$= 528\ kHz$$

[When the zero frequency is lower than f_{OSC} / 2]

C_{C2} sets the pole to f_{Z_ESR}.

$$C_{C2} = R_{COUT\_ESR} \times C_{OUT\_EFF} / R_C \quad \text{Equation 13}$$

[When the zero frequency is higher f_{OSC} / 2]

C_{C2} sets the pole to f_{OSC} / 2 so as to be a noise filter for the COMP pin.

$$f_{OSC} / 2 = 1 / (2 \times \pi \times R_C \times C_{C2})$$
$$C_{C2} = 2 / (2 \times \pi \times R_C \times f_{OSC}) \quad \text{Equation 14}$$

In the reference example, C_{C2} is used as the noise filter for the COMP pin because of being higher than f_{OSC}/2.

$$C_{C2} = 49 \fallingdotseq 47\ pF$$

■ Calculation of C_{SPD}

C_{SPD} sets the zero frequency to meet the unity-gain frequency.

$$R_{TOP} = R_{BOT} \times (V_{OUT} / V_{REF} - 1)$$
$$C_{SPD} = 1 / (2 \times \pi \times f_{UNITY} \times R_{TOP}) \quad \text{Equation 15}$$

When R_{BOT} = 22 kΩ,

$$R_{TOP} = 22\ k \times (3.3\ V / 0.64\ V - 1)$$
$$= 91.4\ k\Omega$$

$$C_{SPD} = 1 / (2 \times \pi \times 70\ kHz \times 91.4\ k\Omega)$$
$$= 24.8 \fallingdotseq 27\ pF$$

Cautions in Selecting External Components

Inductor

- Choose an inductor that has small DC resistance, has sufficient allowable current and is hard to cause magnetic saturation. The inductance value must be determined with consideration of load current under the actual condition. If the inductance value of an inductor is extremely small, the peak current of LX may increase along with the load current. As a result, the current limit circuit may start to operate when the peak current of LX reaches to “LX limit current”.

Capacitor

- Choose a capacitor that has a sufficient margin to the drive voltage ratings with consideration of the DC bias characteristics and the temperature characteristics.
- The use of a ceramic capacitor for CIN is recommended. If combined use of a ceramic and an electrolyte capacitors, the stable operation will improve since the margin becomes bigger. Choose the electrolyte capacitor with the lowest possible ESR with consideration of the allowable ripple current rating (I_{RMS}). I_{RMS} can be calculated by the following equation.

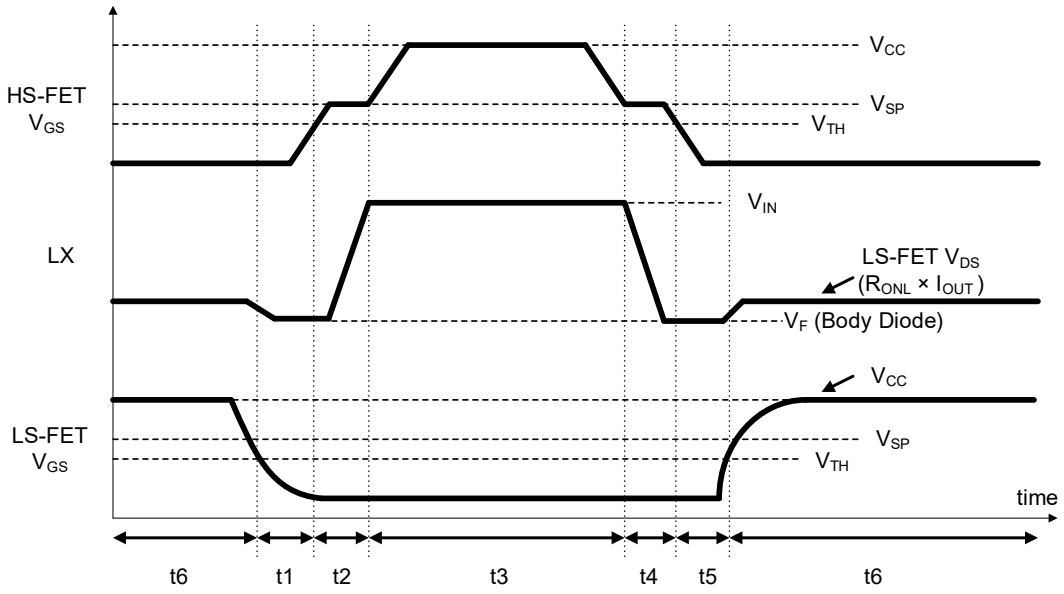
  $I_{RMS} \fallingdotseq I_{OUT} / V_{IN} \times \sqrt{\{ V_{OUT} \times (V_{IN} - V_{OUT}) \}}$

FET

- Gate – Source Voltage
  When considering variations in production and margin, a FET with a withstand voltage of 10 V or more is recommended despite the 5 V high and low driver.
- Gate Threshold Voltage
  Choose a FET with the threshold voltage between 1.0 V (Min.) and 3.4 V (Max.) with consideration of variations in production and margin.
- Drain Current
  Choose a FET having a sufficient margin with consideration of peak current and limit current.
- Connection of Body Diode for Source Current
  Choose a diode with the withstand current over the reverse limit current rating. The R1272S reverse current value becomes one-half of the normal limit current value.
- Input Capacitor (C_{ISS})
  As an index of performance, C_{ISS}: 3800pF
- On-resistance (R_{DS} (on)) & All Gate Capacitance (Qg)
  Choose a FET with the lowest possible characteristics because having an influence on efficiency. Generally, a high-performance FET is rated that R_{DS} x Qq (performance figure) is small.
- Since test specifications vary with FET makers, it is necessary to confirm the application with the R1272S implemented on a board system.

FET Losses

The FET total loss is calculated by the sum of the switching losses when the high side and the low side FETs turning-on / off and the conduction losses by the FET's on-resistance. If the total loss become larger than expected, the external FET must be selected with consideration of the on-resistance, the switching losses and the package's power dissipation. The following figure shows the timing chart of the high side / low side FETs at normal switching. The loss at each delay time can be calculated as follows.



DC / DC Converter Basic Switching Timing Chart

t1 (t5):

For the duration between the low side FET's turn-off and the high side FET's turn-on, the loss occurs to supply a current from the body diode on the low side FET. Likewise, for the duration between the high side FET's turn-off and the low side FET's turn-on, the loss occurs. The losses (P_{DEAD}) for t1 and t5 can be calculated by the following equation.

$$P_{DEAD} = V_F \times I_{OUT} \times f_{OSC} \times (t_{DEAD1} + t_{DEAD5})$$

V_F: The forward voltage of a body-diode

t_{DEAD1}: The delay time from the instant when the gate-source voltage (V_{GS}) falls below the threshold voltage (V_{TH}) on the low side FET to the instant when V_{GS} exceeds V_{TH} on the high side FET.

T_{DEAD5}: The delay time from the instant when V_{GS} falls below V_{TH} on the high side FET to the instant when V_{GS} exceeds V_{TH} on the low side FET.

t2 (t4):

Since the drain-source voltage (V_{DS}) is equal to V_{IN} when the high side FET turns on/off after delay time (t_{DEAD1} / t_{DEAD5}), the source current and the output current (I_{OUT}) become equal. Therefore, a large loss occurs. The losses (P_{SW}) at turn-on / off can be calculated by the following equation.

$$P_{SW} = 1/2 \times V_{IN} \times I_{OUT} \times f_{OSC} \times (t_{RISE} + t_{FALL})$$

t_{RISE}: A duration between the gate voltage rising start time from the threshold voltage and the end of stabilized voltage (V_{SP}) on the high side FET.

T_{FALL}: A duration between the start time of the gate voltage stabilizing and the falling time below the threshold voltage on the high side FET.

For the stabilized duration, V_{GS} of the high side FET remains constant roughly since the gate charge current is used to charge C_{GD}. And, the reverse recovery loss (P_{RR}) occurs to recover the body diode of the low side FET when the high side FET turns on. Refer to *the FET datasheet* for information about the electric charge (Qrr) required for recovery.

$$P_{RR} = V_{IN} \times Qrr \times f_{OSC}$$

And, the power (P_{GH}, P_{GL}) for electric charge of the FET' gate and the power (P_{OSSH}, P_{OSSL}) for electric charge of the FET's output capacity occur. Each power can be calculated by following equations. Refer to *the FET datasheet* for detailed values.

$$P_{GH} = Q_{GH} \times V_{CC} \times f_{OSC}$$
$$P_{GL} = Q_{GL} \times V_{CC} \times f_{OSC}$$
$$P_{OSSH} = 1/2 \times C_{OSSH} \times (V_{IN})^2 \times f_{OSC}$$
$$P_{OSSL} = 1/2 \times C_{OSSL} \times (V_{IN})^2 \times f_{OSC}$$

V_{CC}: VCC pin voltage

Q_{GH}, Q_{GL}: Gate electric charge quantity for High- /Low- side FETs

C_{OSSH}, C_{OSSL}: Drain-gate capacity + Drain-source capacity for High- /Low- side FETs

t3 (t6):

For the duration of t3, the conduction loss of the high side FET (P_{HS}(on)) occurs. For the duration of t6, the conduction loss of the low side FET (P_{LS}(on)) occurs. Each loss can be calculated by the following equation. ON duty is closely analogous to V_{OUT} / V_{IN}.

$I_{RMS} = \sqrt{}\ (((I_{OUT})^2 + (I_{P-P})^2 / 12))$

P_{HS} (on) = $(I_{RMS})^2 \times R_{ONH} \times V_{OUT} / V_{IN}$

P_{LS} (on) =$(I_{RMS})^2 \times R_{ONL} \times (1-V_{OUT} / V_{IN})$

I_{RMS}: FET's rms current

I_{P-P}: FET's peak current amplitude

R_{ONH}, R_{ONL}: On-resistance for High- /Low- side FETs

Since the conduction loss depends on the duty, the loss varies with step-down ratio. When the step-down ratio is large and the ON duty is small, the loss of the low side FET becomes larger, and when the ratio is small, the loss of the high side FET becomes larger. From above equations, each loss of the high side and the low side FETs can be calculated by the following equations.

$P_{HS} = P_{HS}$ (on) + P_{SW} + P_{RR} + P_{GH} + P_{OSSH}

$P_{LS} = P_{LS}$ (on) + P_{GL} + P_{OSSL} + P_{DEAD}

As is evident from these equations, the switching loss becomes predominant when the input voltage and the frequency are high, and the conduction loss conversely becomes predominant when they are low.

TECHNICAL NOTES

The performance of power source circuits using this IC largely depends on peripheral circuits. When selecting the peripheral components, please consider the conditions of use. Do not allow each component, PCB pattern or the IC to exceed their respected rated values (voltage, current, and power) when designing the peripheral circuits.

- External components must be connected as close as possible to the Ics and make wiring as short as possible. Especially, the capacitor connected in between VIN pin and GND pin must be wiring the shortest. If their impedance is high, internal voltage of the IC may shift by the switching current, and the operating may be unstable. Make the power supply and GND lines sufficient.

- Place a capacitor (C_{OUT}) to keep a distance between C_{IN} and C_{OUT} in order to avoid the high-frequency noise by input.

- AGND and PGND for the controller must be wired to the GND line at the low impedance point of the same layer with C_{IN} and C_{OUT}.

- Place a capacitor (C_{BST}) as close as possible to the LX pin and the BST pin. If controlling slew rate for EMI, a resistor (R_{BST}) should be in series between the BST pin and the capacitor (C_{BST}), but not be in series to FET for HGATE and LGATE pins. Because connecting the resistor in series to the FET becomes a cause of a through-current.

- The tab on the bottom of the HSOP-18 package must be connected to GND when mounted on the board. To improve thermal dissipation on the multilayer board, set via to release the heat to the other layer in the connecting part of the tab on the bottom. Likewise, thermal dissipation for FET is required.

- The NC pin must be set to “Open”.

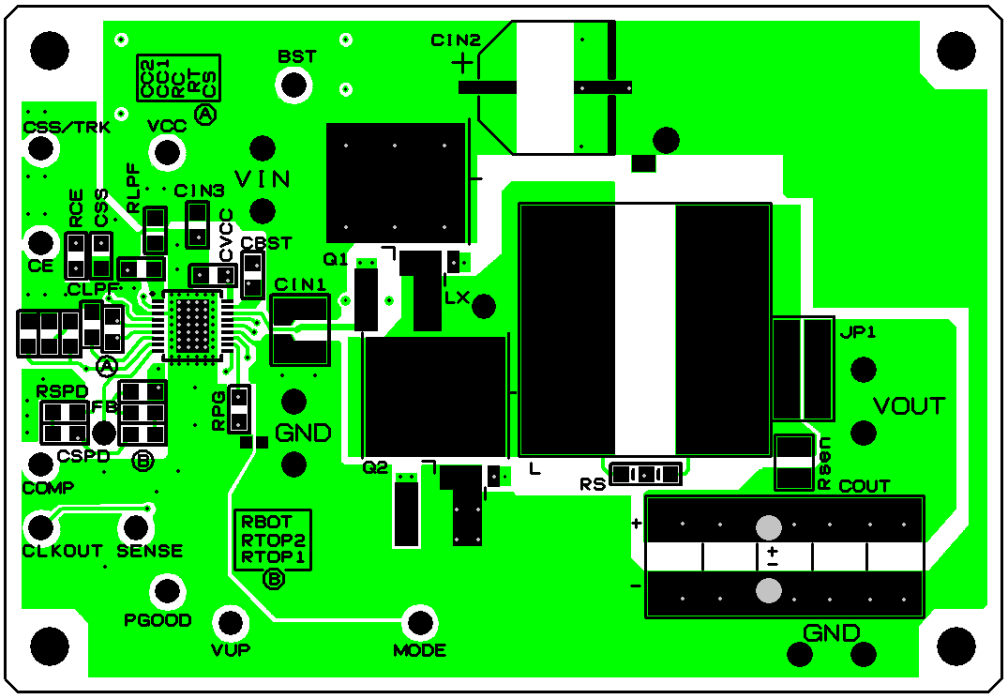
- The MODE pin requires the H / L voltages with the high stability when the forced PWM mode (MODE = “H”) or the VFM mode (MODE = “L”) is enabled. If the voltage with the high stability cannot be applied, connection to the VCC pin as “H” level or the AGND pin as “L” level is recommended. If connecting to the PGND pin as noisy, a malfunction may occur. Avoid the use of the MODE pin being “Open”.

- If V_{OUT} is a minus potential, the setup cannot occur.

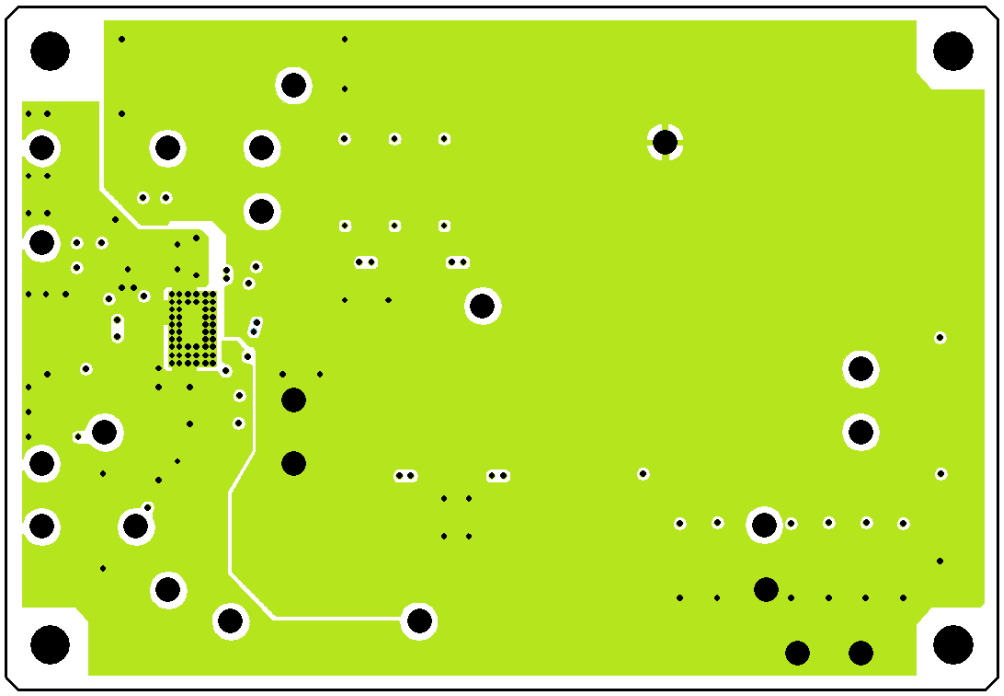
- The power for the controller and for the high-side FET must be used on the same power supply, since the internal slope compensation is applied as the power supply voltage of the high-side FET is equal to the controller’s. If applying the other power supply voltage, the controller will become unstable owing to the inappropriate slope compensation.

Reference PCB Layouts

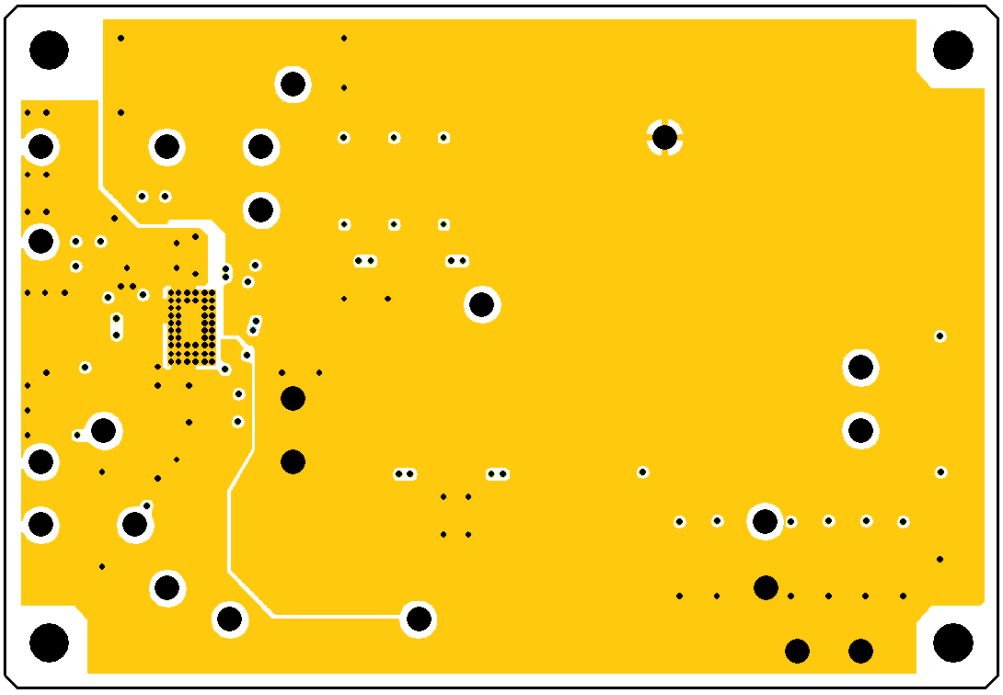
R1272SxxxA PCB Layouts



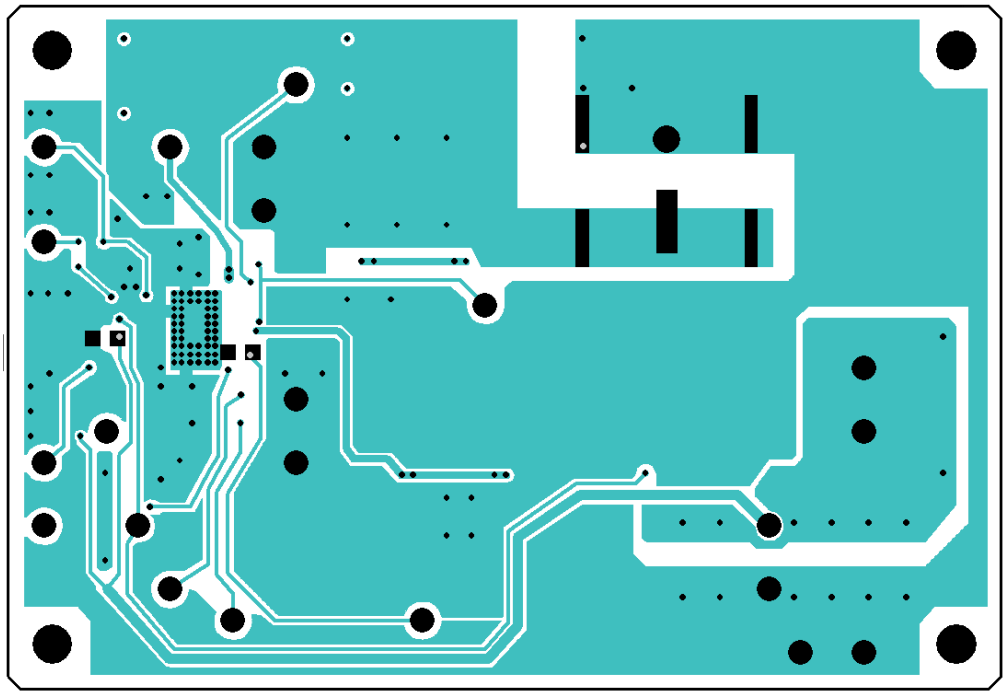
PCB Layout − 1st Layer (Top Layer)



PCB Layout − 2nd Layer



PCB Layout − 3rd Layer

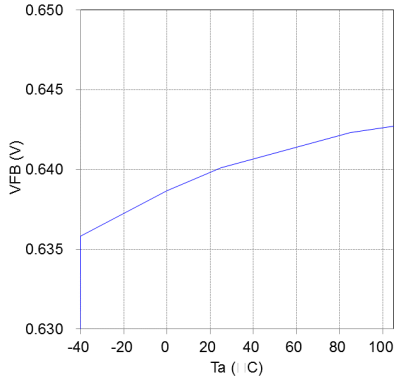


PCB Layout − 4th Layer (Bottom Layer)

TYPICAL CHARACTERISTICS

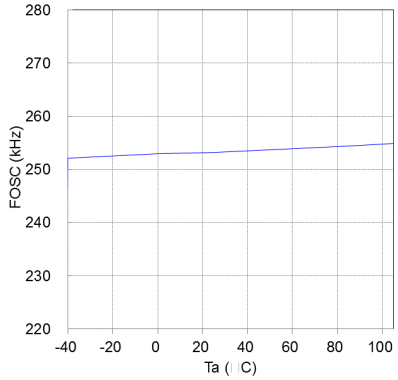
Typical Characteristics are intended to be used as reference data, they are not guaranteed.

1) FB Voltage vs. Temperature

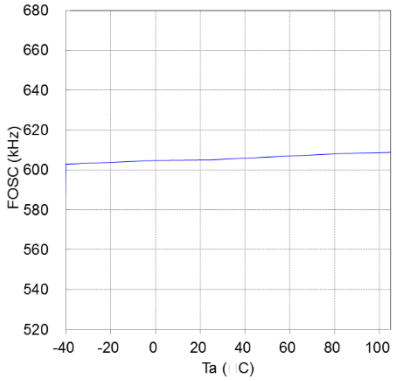


2) Oscillation Frequency vs. Temperature

250kHz (RT = 135 kΩ)

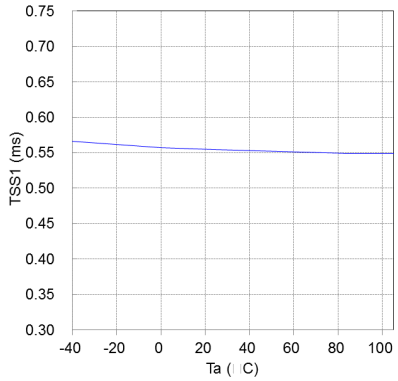


600 kHz (RT = 55 kΩ)

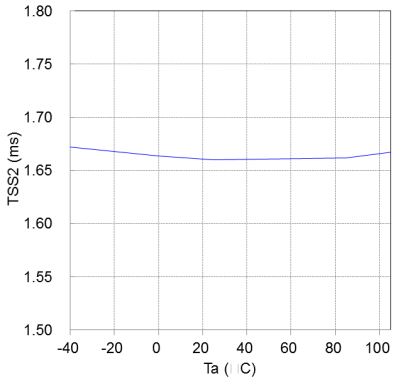


3) Soft-start time 1 vs. Temperature

Fixed soft-start time
(C_{SS} = Open)

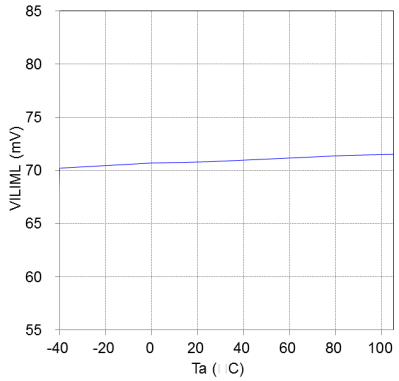


Adjustable soft-start time
(C_{SS} = 4.7 nF)

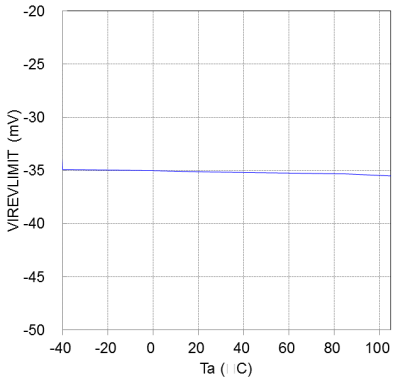


4) Current limit threshold voltage vs. Temperature

Current limit threshold voltage
(R1272Sxx2x)

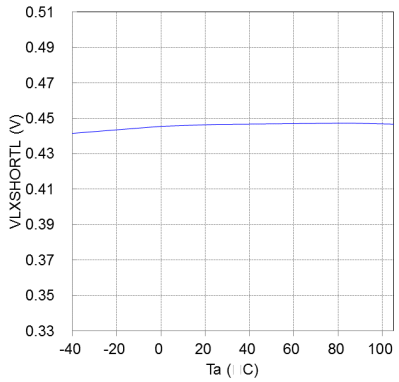


Overcurrent limit threshold voltage
(R1272Sxx2x)

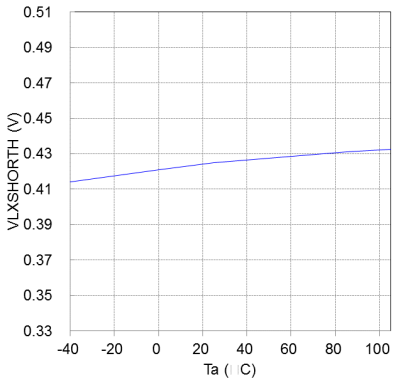


5) LX GND/VIN short threshold voltage vs. Temperature

LX GND short threshold voltage
(VIN-LX)

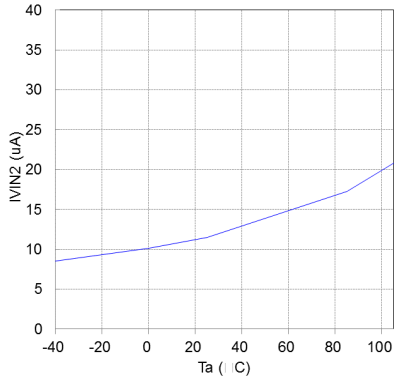


LX VIN short threshold voltage
(LX-PGND)

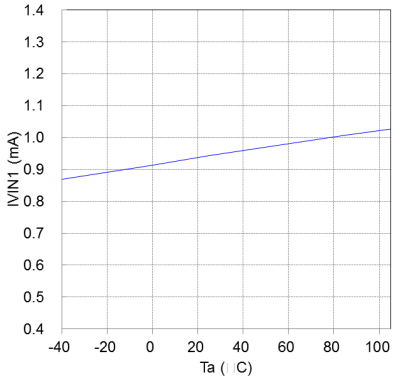


6) Current consumption vs. Temperature

Current consumption (VFM)
(V_{IN} = 12 V)

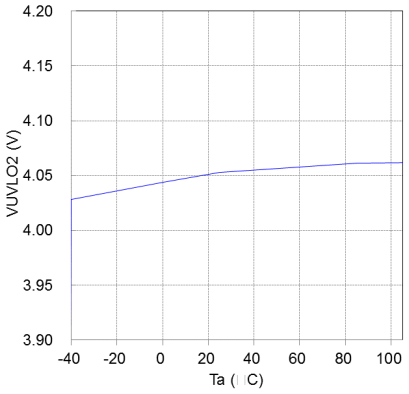


Current consumption (PWM)
(V_{IN} = 12 V)

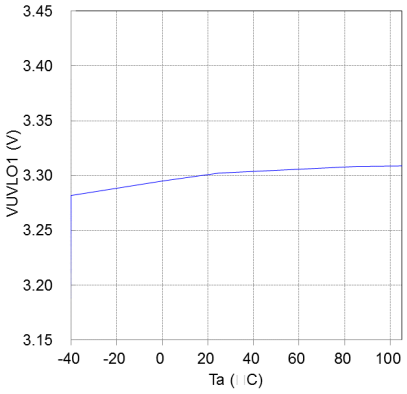


7) UVLO vs. Temperature

UVLO release voltage

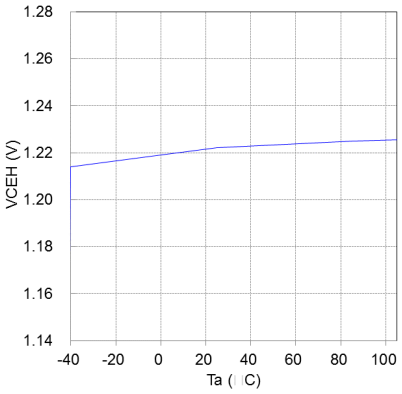


UVLO threshold voltage

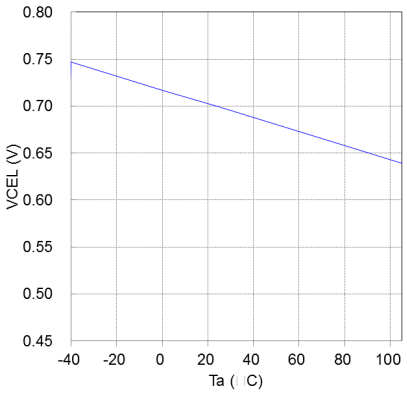


8) CE input voltage vs. Temperature

CE "H" input voltage

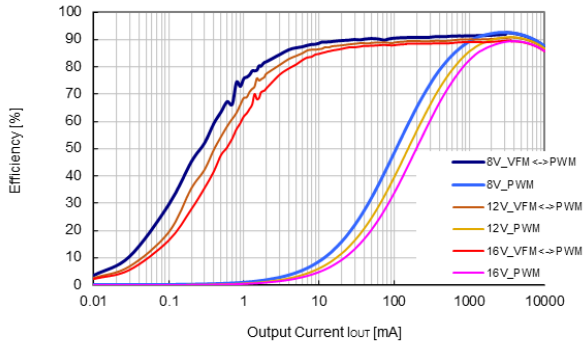


CE "L" input voltage

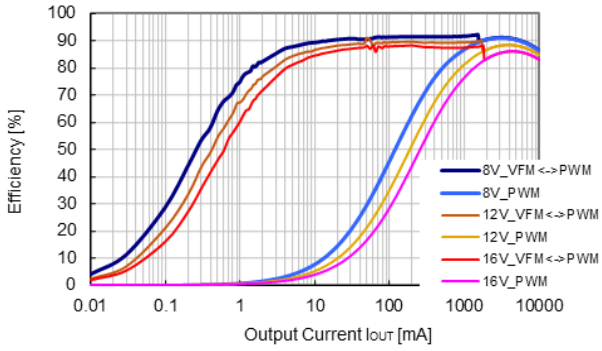


9) Output current vs. Efficiency

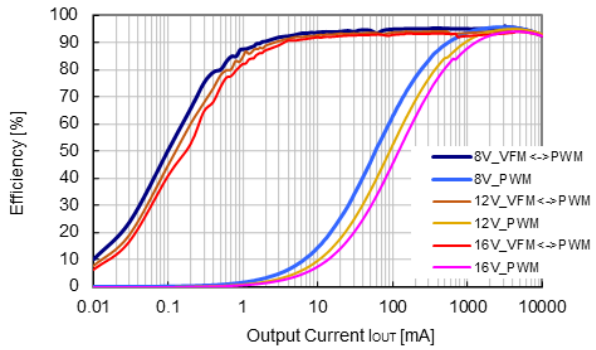
V_{OUT} = 1.5 V
f_{OSC} = 250 kHz / V_{IN} = 8 V / 12 V / 16 V



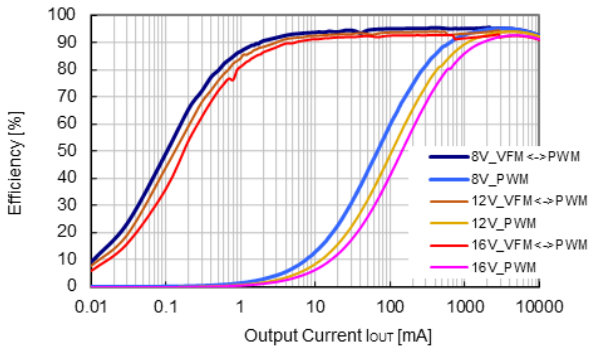
V_{OUT} = 1.5 V
f_{OSC} = 500 kHz / V_{IN} = 8 V / 12 V / 16 V



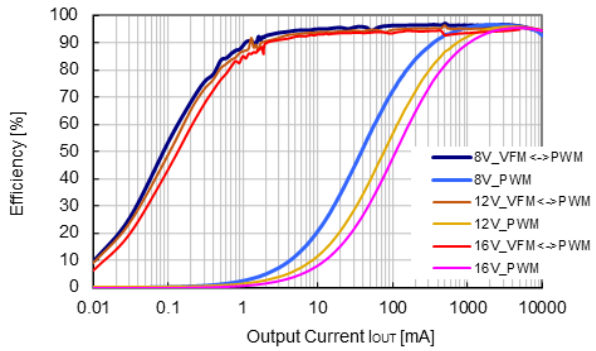
V_{OUT} = 3.3 V
f_{OSC} = 250 kHz, V_{IN} = 8 V / 12 V / 16 V



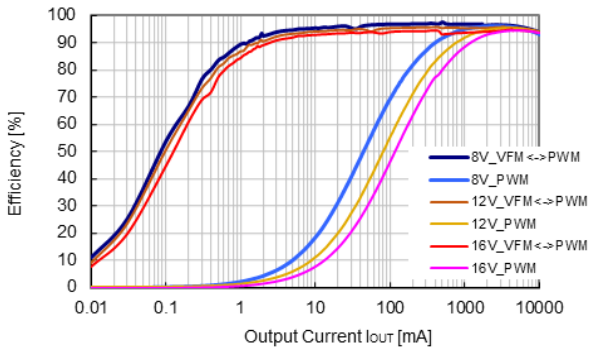
V_{OUT} = 3.3 V
f_{OSC} = 500 kHz, V_{IN} = 8 V / 12 V / 16 V



V_{OUT} = 5.0 V
f_{OSC} = 250 kHz / V_{IN} = 8 V / 12 V / 16 V

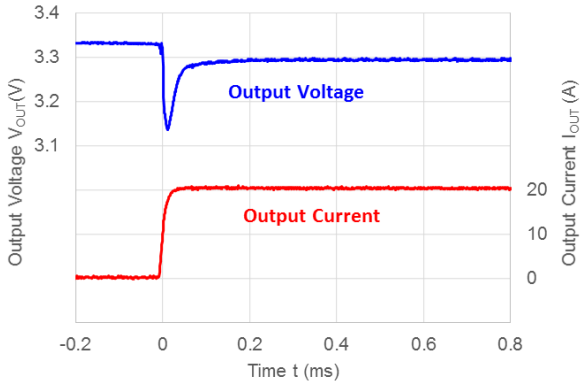


V_{OUT} = 5.0 V
f_{OSC} = 500 kHz / V_{IN} = 8 V / 12 V / 16 V

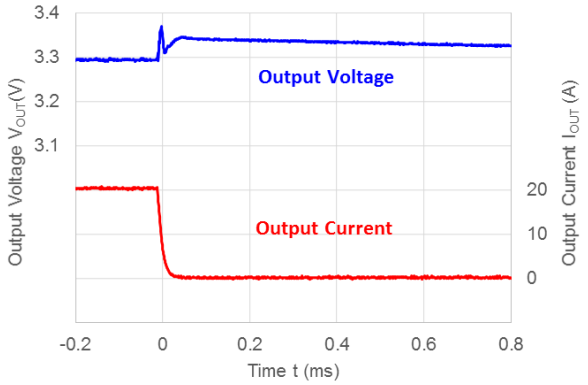


10) Load transient response

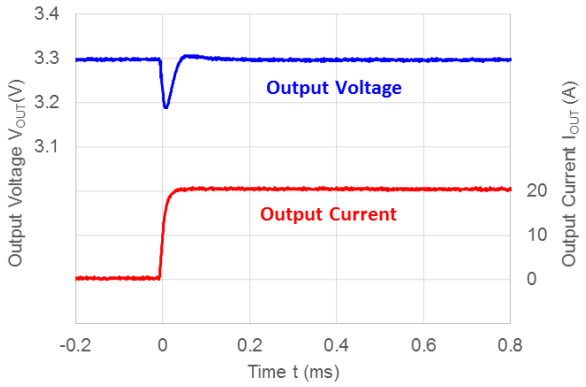
V_{IN} = 12 V, V_{OUT} = 3.3 V
f_{OSC}=500kHz, MODE=L VFM/PWM auto-switching



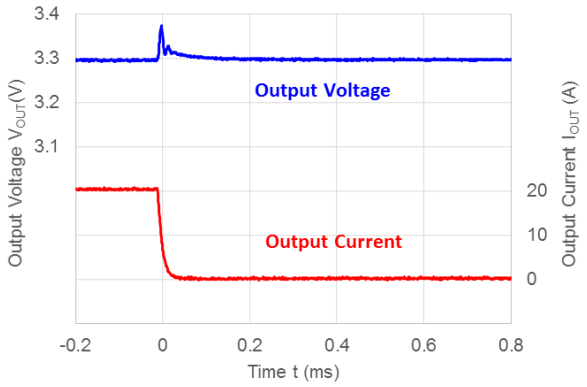
V_{IN} = 12 V, V_{OUT} = 3.3 V
f_{OSC}=500 kHz, MODE=L VFM/PWM auto-switching



V_{IN} = 12 V, V_{OUT} = 3.3 V
f_{OSC} = 500 kHz, MODE = H Forced PWM

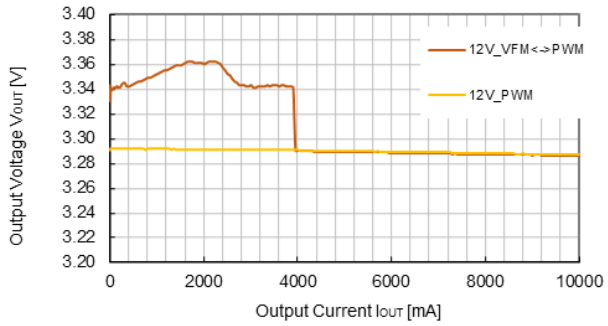


Vin = 12V, V_{OUT} = 3.3V
f_{OSC} = 500 kHz, MODE = H Forced PWM

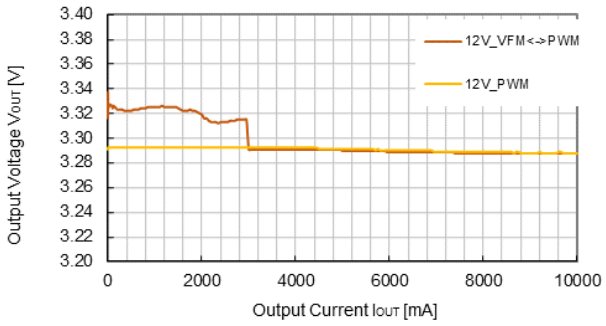


11) Output voltage vs. Output current

V_{OUT} = 3.3V
f_{OSC} = 250 kHz, V_{IN} = 12 V

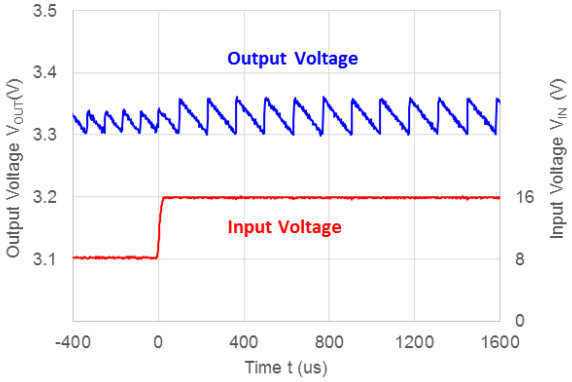


V_{OUT} = 3.3 V
f_{OSC} = 500 kHz, V_{IN} = 12 V

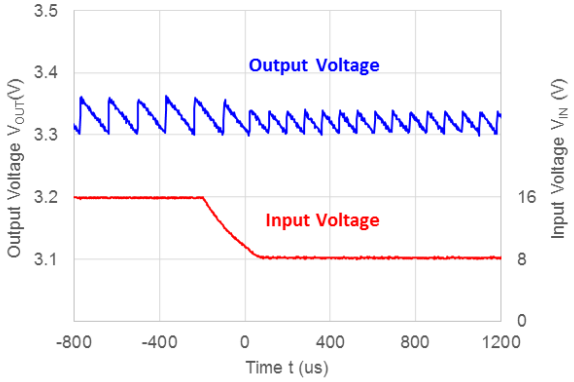


12) Input transient response

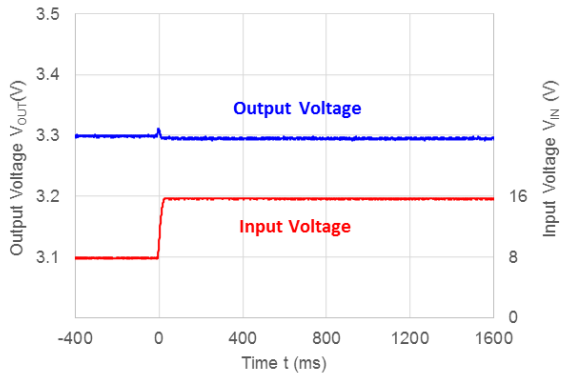
V_{OUT} = 3.3 V
f_{OSC}=500kHz, MODE=L VFM/PWM auto-switching
I_{OUT} = 0.1 A VFM mode



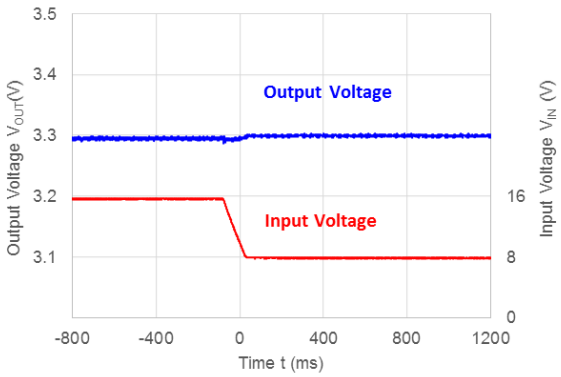
V_{OUT} = 3.3 V
f_{OSC}=500kHz, MODE=L VFM/PWM auto-switching
I_{OUT} = 0.1 A VFM mode



V_{OUT} = 3.3 V
f_{OSC}=500kHz, MODE=H VFM/PWM auto-switching
I_{OUT} = 5 A PWM mode

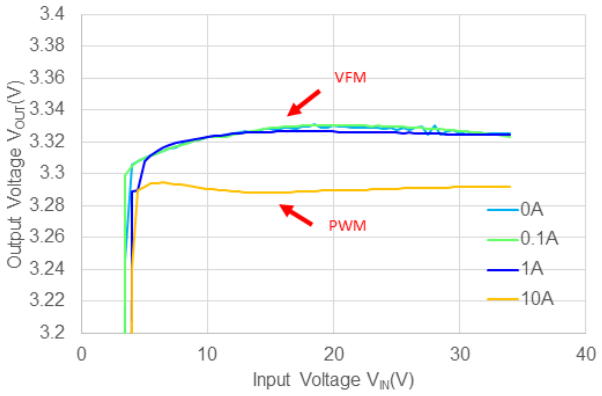


V_{OUT} = 3.3 V
f_{OSC}=500kHz, MODE=H VFM/PWM auto-switching
I_{OUT} = 5 A PWM mode

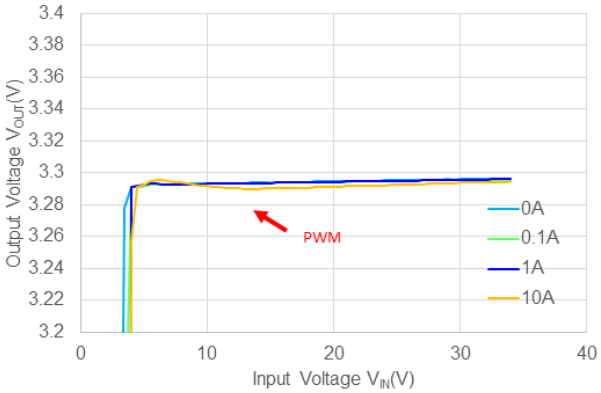


13) Input voltage vs. Output voltage

V_{OUT} = 3.3 V
f_{OSC}=500kHz, MODE= L VFM/PWM auto-switching

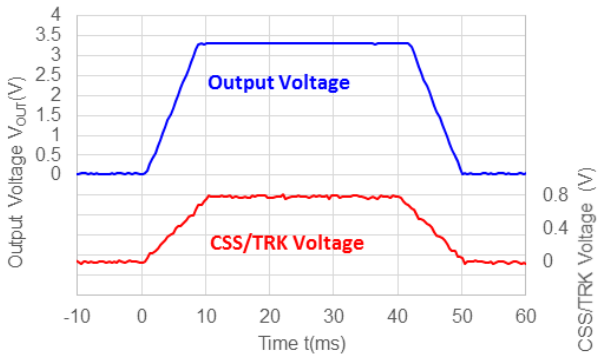


V_{OUT} = 3.3 V
f_{OSC}=500kHz, MODE=H Forced PWM



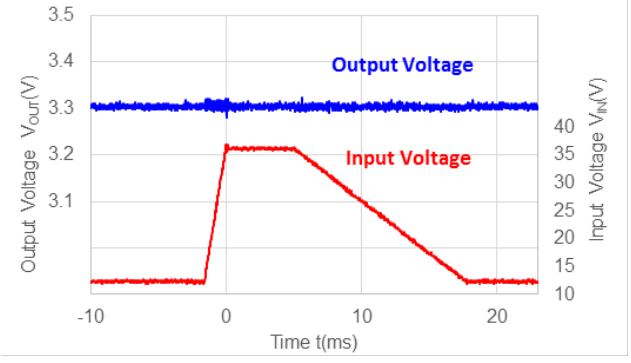
14) Up-down tracking

V_{IN} = 12 V、V_{OUT} = 3.3 V
f_{OSC} = 500 kHz, MODE = H Forced PWM



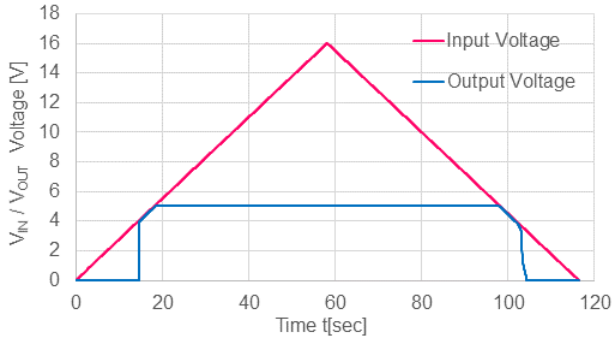
15) Load dump

V_{OUT} = 3.3 V
f_{OSC} = 500 kHz, MODE = H Forced PWM



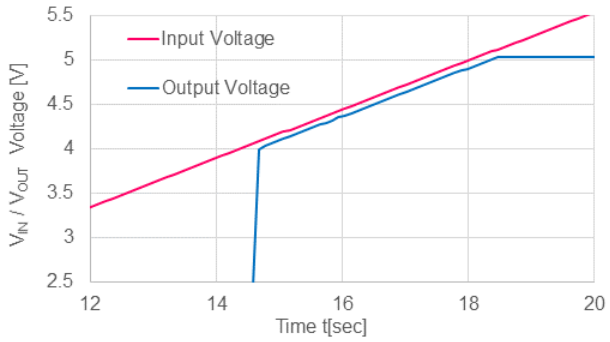
16) Line regulation

V_{OUT} = 5.0 V
f_{OSC} = 500 kHz, MODE = H Forced PWM



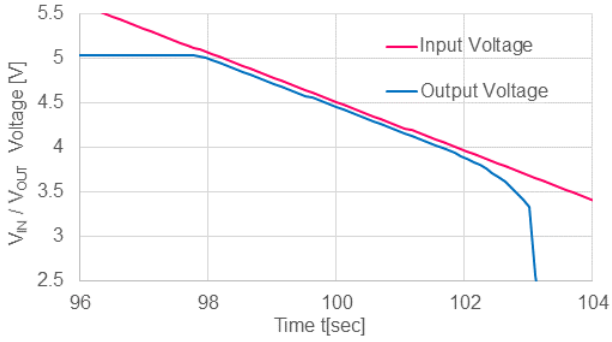
Line regulation UVLO release expanding

V_{OUT} = 5.0 V
f_{OSC} = 500 kHz, MODE = H Forced PWM



Line regulation UVLO detection expanding

V_{OUT} = 5.0 V
f_{OSC} = 500 kHz, MODE = H Forced PWM



Ver. C

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

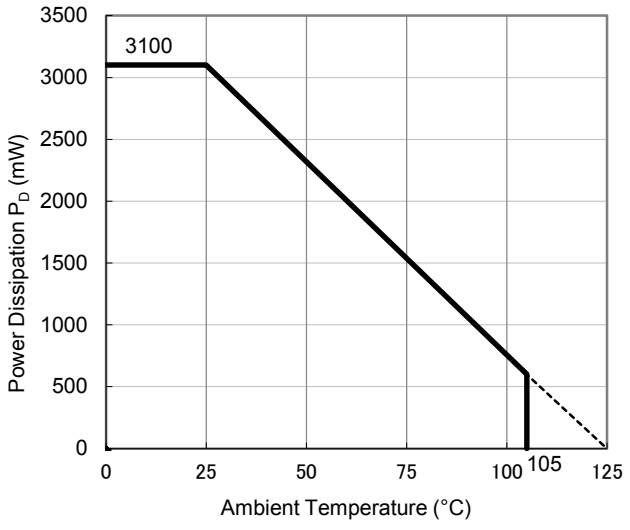
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

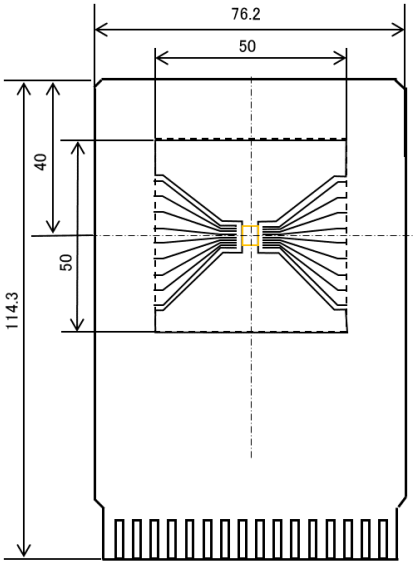
Item	Measurement Result
Power Dissipation	3100 mW
Thermal Resistance (θja)	θja = 32°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 8°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



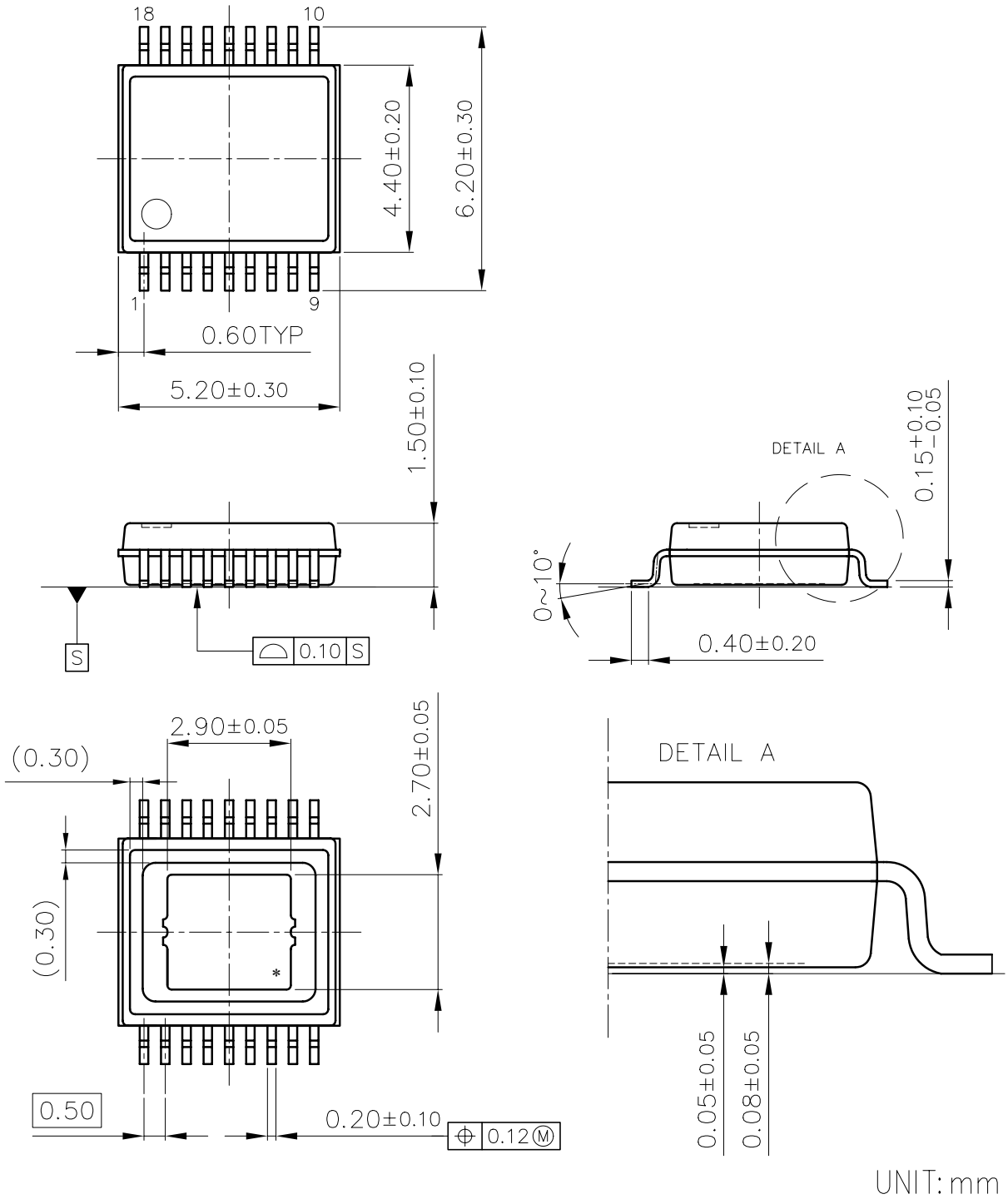
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH

DM-HSOP-18-JE-B



HSOP-18 Package Dimensions

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