SECO-NCD57000-GEVB

NCD57000 mini Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Purpose

This document describes the use and applications for the NCD57000 gate driver mini board. The board is designed on a two layer PCB and includes the NCD57000 driver and all the necessary drive circuitry. The board also includes ability to solder any MOSFET or SiC MOSFET in a TO−247 high voltage package and compatibility with SECO−GDBB−GEVB baseboard for out−of−the−box evaluation. The board does not include a power stage and is generic from the point of view that it is not optimized to any particular topology. It can be used in any low−side or high−side power switching application. For bridge configurations two or more of these boards can be configured in a totem pole type drive configuration. The boards can be considered as an isolator+driver+TO−247 discrete module.

NCD57000 Description

NCD57000 is a high−current single channel IGBT driver with internal galvanic isolation, designed for high system efficiency and reliability in high power applications. Its features include complementary inputs, open drain FAULT and Ready outputs, active Miller clamp, accurate UVLOs, DESAT protection, soft turn−off at DESAT, and separate high and low (OUTH and OUTL) driver outputs for system design convenience. NCD57000 accommodates both 5 V and 3.3 V signals on the input side and wide bias voltage range on the driver side including negative voltage capability. NCD57000 provides > 5 kVrms (UL1577 rating) galvanic isolation and > 1200 Viorm (working voltage) capabilities. NCD57000 is available in the wide−body SOIC−16 package with guaranteed 8 mm creepage distance between input and output to fulfill reinforced safety insulation requirements.

Collaterals

- SECO−NCD57000−GEVB
- SECO−GDBB−GEVB
- NCD57000

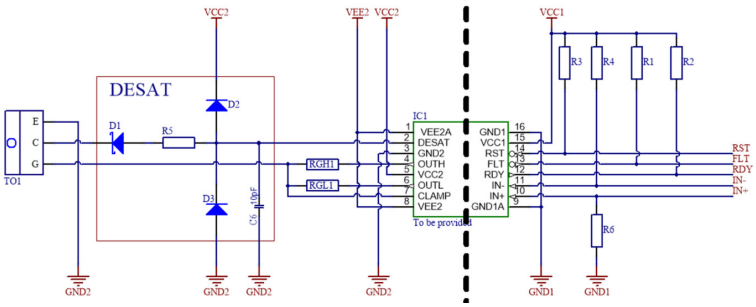


Figure 3. Schematic

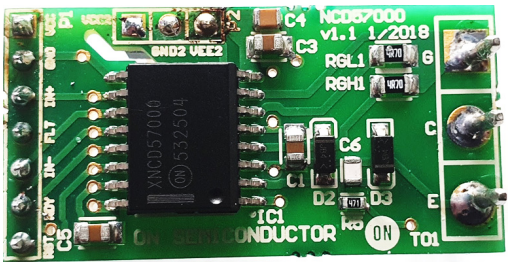


Figure 1. SECO−NCD57000−GEVB



Figure 2. Board Plugged into SECO−GDBB−EVB

Features

- Galvanic Isolated Gate Driver Circuit 5 kV
- Demonstrates NCD57000 Isolated Driver with Advanced Features
- Replaceable Load Capacitor and Gate Resistor for different Load Simulation
- Plug−and−Play Testing with SECO−GDBB−GEVB
- Minimized Form−factor for Embedding and Testing in Application Boards or New Designs
- Custom Voltage Levels with External Power Supply

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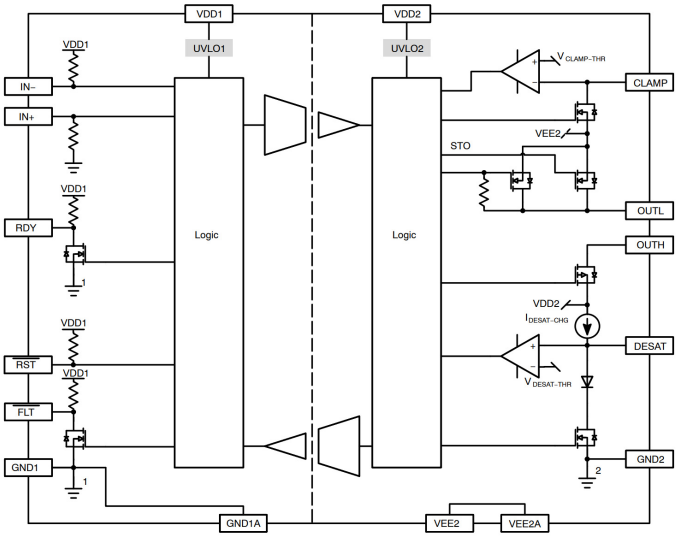


Figure 4. Simplified NCD57000 Block Diagram

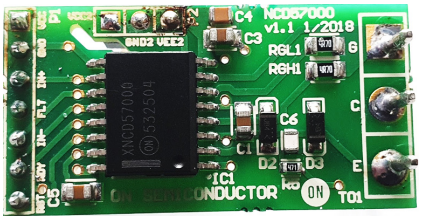


Figure 5. NCD57000 mini Board − Top View

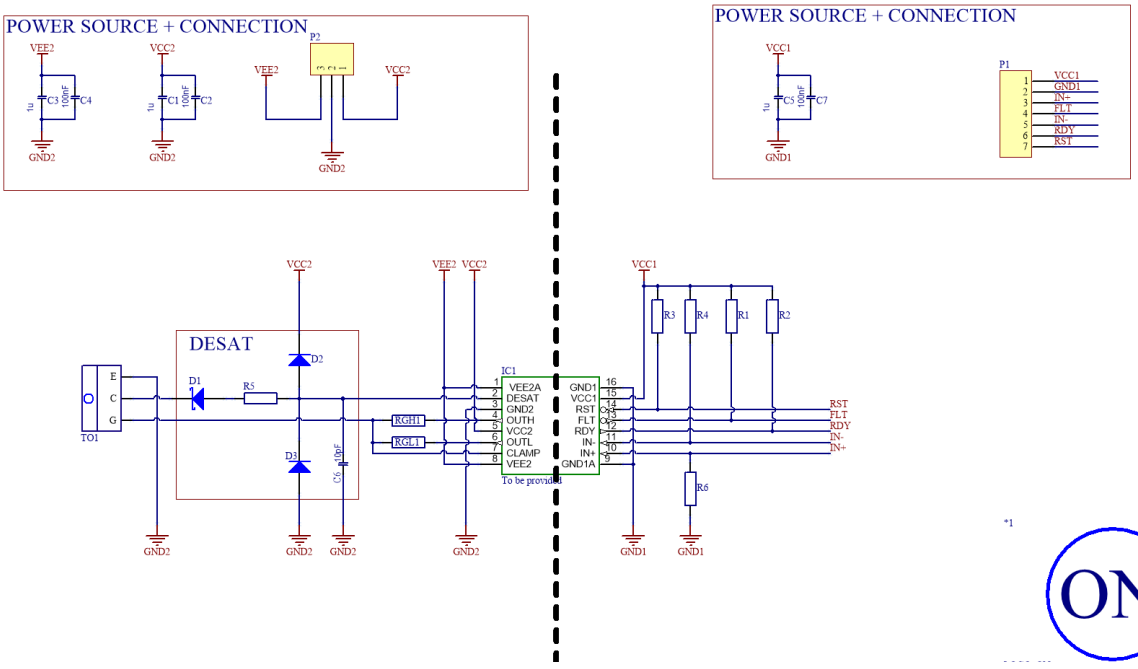


Figure 6. NCD57000 mini Board Schematic

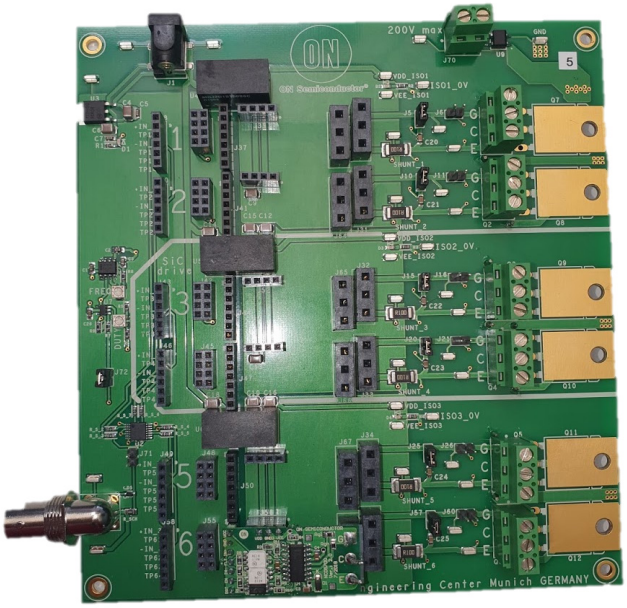


Figure 7. SECO−GDBB−GEVB

Table 1. NCD57000 mini BOARD BOM

Description	Designa-tor	Quantity	Value	Comment	Footprint	Manufacturer
Capacitor 0805 1 μF 50 V	C1, C3, C5	3	1 μF		CAP0805	TDK
Capacitor 0805 100 nF 50 V	C2, C4, C7	3	100 nF		CAP0603	Kyocera AVX
Capacitor 0805 10 pF 50 V	C6	1	10 pF		CAP0603	KEMET
BYG23T−M3/TR	D1	1			SMB	Vishay Semiconductor
Schottky Diode	D2, D3	2	MBR0540		SOD−123	ON Semiconductor
NCD57000	IC1	1			DSO−16_N	ON Semiconductor
Header, 7−Pin	P1	1		Don’t assembly	HDR1X7	Molex
Header, 3−Pin	P2	1		Don’t assembly	HDR1X3	Molex
RES SMD 10 kΩ 1% 1/10W 0603	R1, R2, R3, R4, R5	5	10k		RES0603	Yageo
RES SMD 1 kΩ 1% 1/10W 0603	R5	1	1k		RES0603	Bourns
RES SMD 4.7 Ω 1% 1/10W 0805	RGH1, RGL1	2	4.7R		RES0805	Yageo

PCB Assembly and Layers

Figure 8 and Figure 9 shows the top and bottom layouts of the PCB. The PCB is 35 mm x 18 mm x 1 mm (length x width x height) where the width of the PCB is approximately the width of a TO − 247 body.

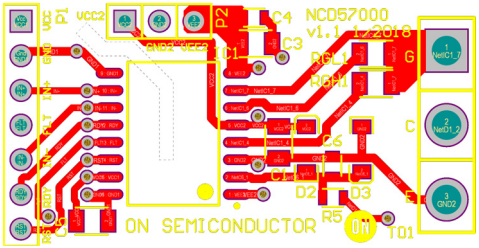


Figure 8. NCD57000 mini Board TOP Assembly Drawing

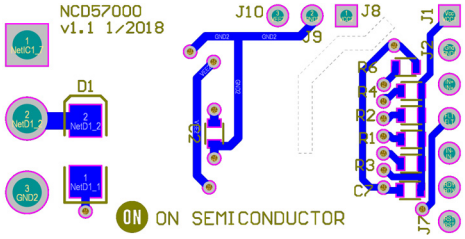


Figure 9. NCD57000 mini Board BOTTOM Assembly Drawing

I/O Connectors

There are 3 I/O connectors including 13 pins described in Table 2 below. The signals on low voltage side are noted as “primary” ground referenced. There is no true “primary” and “secondary” ground but there is 1.2 kV galvanic isolation across the isolation boundary. It is especially important to maintain isolation in high−side, high−voltage, switching applications where the “secondary” Vcc (P3.2 and P3.3) floats Vcc volts above the power supply input voltage:

Table 2. I/O CONNECTOR DESCRIPTIONS

Ref Des	Name	I/O	GND Ref	Description	Value [V]
P1.1	Vcc1	Power	Primary	Positive primary power supply	5
P1.2	Gnd1	Power	Primary	Ground	0
P1.3	IN+	Input	Primary	Non−inverting PWM input	0 − 3.3 (5)
P1.4	FLT	Output	Primary	Fault flag	0 − 5 (3.3)
P1.5	IN−	Input	Primary	Inverting PWM input	0 − 5 (3.3)
P1.6	RDY	Output	Primary	Ground	0 − 5 (3.3)
P1.7	RST	Input	Primary	Reset FLT pin	0 − 5 (3.3)
P2.1	Vcc2	Power	Secondary	Positive branch power supply	< 20
P2.2	Gnd2	Power	Secondary	Ground of the power supply	0
P2.3	Vee2	Power	Secondary	Negative branch of power supply	> −10
G (G)	Gate	Output	Secondary	Gate pin of a power switch	< 20
C (D)	Collector	Output	Secondary	Collector (drain) pin of a power switch	≤ 1200
E (S)	Emitter	Output	Secondary	Emitter (source) pin of a power switch	0

Mounting into Existing PCB

The board can be mounted into an existing power board, shown as “Main PCB” in Figure 6. If there are no components or low profile surface mount components only, the mini SMD EVB can be mounted parallel to the main PCB as shown in Figure 6. The TO−247, power device leads would pass through the mini EVB plated thru−holes and into the main PCB. Or, if necessary, the gate lead of the TO−247, power device can be soldered to the plated thru−hole on the EVB and cut so that it does not contact the main PCB. For mechanical strength, it is preferred that the TO−247 gate lead pass through both PCB’s. This configuration is helpful for already existing application with horizontal TO−247 positions.

Recommended procedure for Option 1 Mounting into an existing PCB:

1. On the main PCB, isolate the gate drive to the TO−247. If the existing design includes a gate drive resistor, removing it should serve the purpose of isolating the gate drive to the TO−247. If there is no series component between the PWM signal source and the TO−247 gate lead, the gate drive PCB track will need to be cut.
2. Measure the resistance between the PWM source and the TO−247 gate lead (or PWM source to gate drive transformer/isolator if applicable). Verify reading is high impedance (open).
3. If a TO−247 discrete is installed in the main PCB, remove it now.
4. Place Kapton or non−conductive tape over the main PCB area directly beneath the EVB. This is to avoid the possibility of having any components on the bottom of the mini SMD EVB touch components or conductive surfaces on the main PCB.
5. Solder a flying lead of bus wire to the main PCB, PWM signal and so on. Make sure there is enough length of the PWM input (flying lead) to reach through the EVB.
6. Solder the TO−247 through just the EVB first
7. With the TO−247 installed into the EVB, install and solder the TO−247 leads into the main PCB.
8. Solder the other end of the PWM input (flying lead) to IN+ for non−inverting PWM applications or IN− for inverting PWM applications.
9. Using the same size bus wire, solder the remaining connections between the EVB to the appropriate locations on the main PCB.
10. Solder flying leads for bias voltage. Note that P2 are across the isolation boundary from.

Mounting into Existing PCB − Option 2

If components mounted on the main PCB interfere with mounting the EVB as described by Option 1 (Figure 10), the TO−247 leads can be formed (lead length may need to be added) with the EVB mounted perpendicular to the main PCB as shown in Figure 11. If required, both mounting options allow the application of a heat sink to the TO−247 package. If high dv/dt is present on the drain of the TO−247, the EVB should be angled, away from being parallel to the TO−247, as much as possible.

1. On the main PCB, isolate the gate drive to the TO−247 power device. If the existing design includes a gate drive resistor, removing it should serve the purpose of isolating the gate drive to the TO−247. If there is no series component between the PWM signal source and the TO−247 gate lead, the gate drive PCB track will need to be cut.
2. Measure the resistance between the PWM source and the TO−247 gate lead (or PWM source to gate drive transformer/isolator if applicable). Verify reading is high impedance (open).
3. If a TO−247 discrete is installed in the main PCB, remove it now.
4. Solder a flying lead of bus wire to the main PCB, PWM signal. Make sure there is enough length of the PWM input (flying lead) to reach through the mini EVB plated thru−hole.
5. After the TO−247 leads have been formed, check for fit through the EVB and down into the main PCB
6. Solder the TO−247 through just the EVB first
7. With the TO−247 installed into the EVB, install and solder the TO−247 leads into the main PCB
8. Solder the other end of the PWM input (flying lead) to IN+ for non−inverting PWM applications or IN− for inverting PWM applications.
9. Using the same size bus wire, solder the remaining connections between EVB to the appropriate locations on the main PCB.
10. Solder flying leads from bias voltage to the EVB. Note that power supply connector is across the isolation boundary.

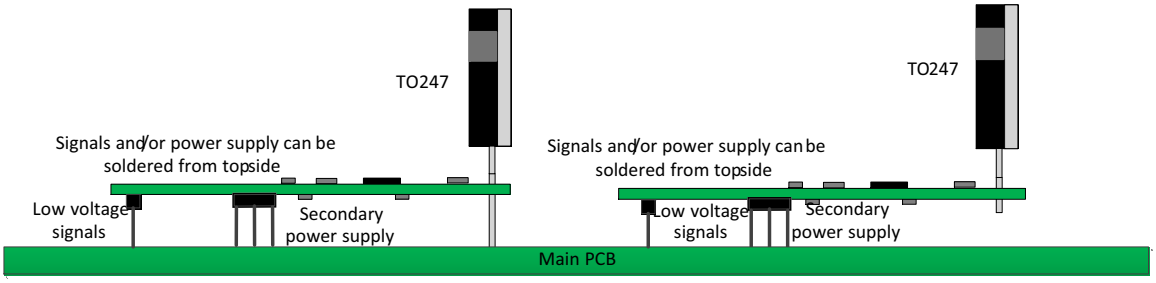


Figure 10. Mounting into Existing PCB

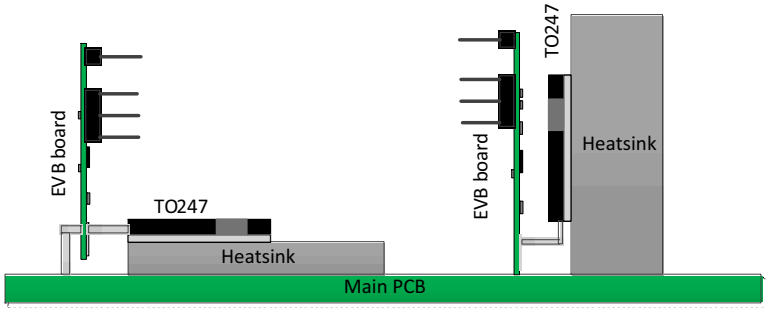


Figure 11. EVB Board Installations

Mounting into New PCB Design

The EVB can also be used as an isolator+driver+TO−247 “driver module” that can be integrated into a new PCB design. The gate lead of the TO−247 between the EVB and the main PCB is for mechanical strength only. For main PCB layout, the gate lead extends down through the main PCB and can be soldered to an isolated plated thru−hole. As shown in Figure 12, shoulder pins with appropriate flange are one option that can be used as mounting pins between mini EVB and the main PCB. In the case new design Figure 13 all needed for footprint design.

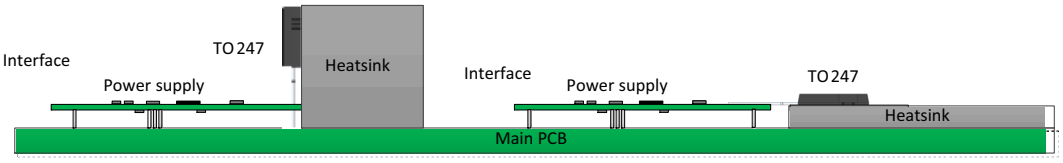


Figure 12. NCD57000 SMD mini Board New Design Installations

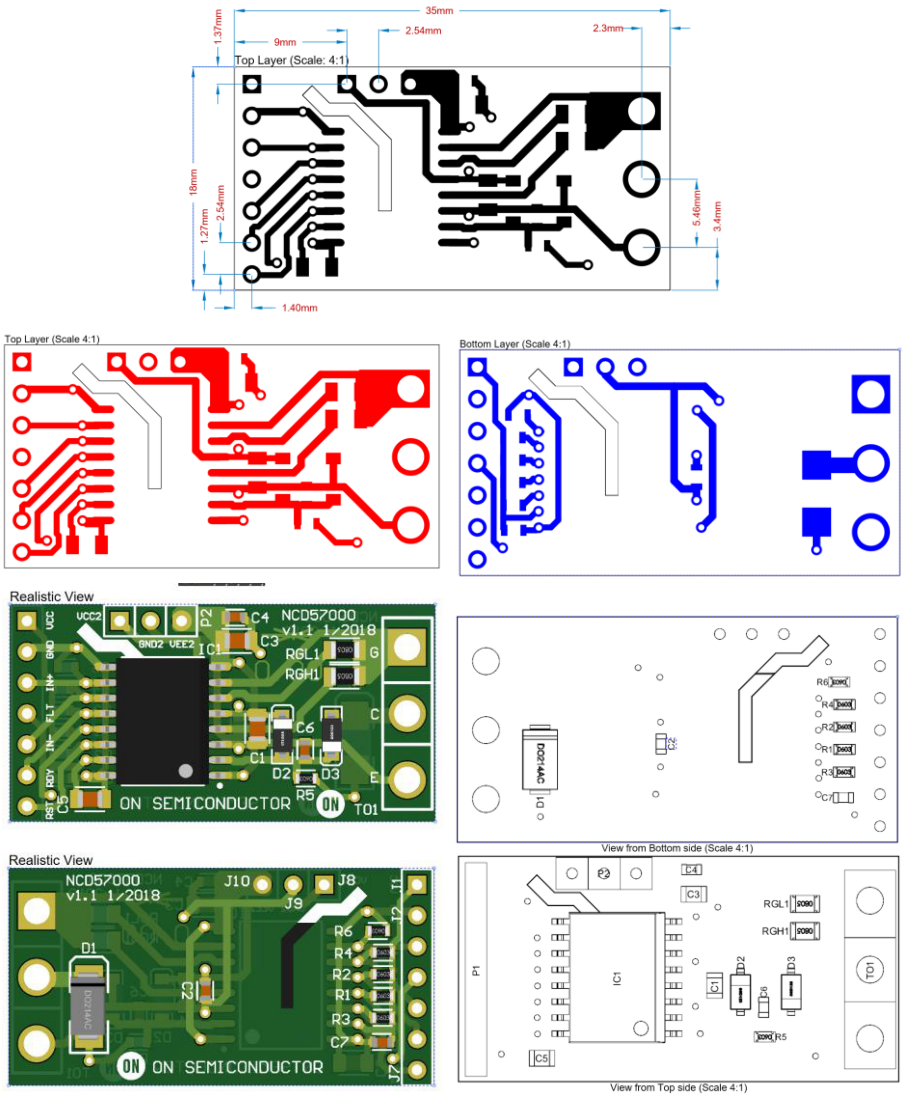


Figure 13. EVB's PCB Mechanical Data

Testing without Installing into a PCB

The EVB can also be tested without installing into a main PCB. However, since this EVB was designed for small form factor there are no test points included for connecting voltage probes. The EVB should be hand probed carefully since the components are very fine pitch or flying leads connected to desired probe points can be attached. The 20 Vdc bias (Vcc2 and Gnd2) is on the secondary side of the isolated gate driver IC and therefore has a separate/isolated return ground from the 5 Vdc bias (Vcc1 and Gnd2). The recommended series load of below 4.7 nF and 4.7 Ω is close to what might be representative of a power switch gate drive input impedance. Leaded passive components can be soldered into the TO−247 holes as shown in Figure 14. Alternatively, a TO−247 power switch can also be soldered in place and used as a load for the gate driver board. Note that testing without installing into a power stage, leaves the DESAT pin open since there is no active drain signal. The effect of operating DESAT this way is explained in section 'DESAT'.

Testing with Gate Driver Base Board

Another very easy way how to test and evaluate more mini boards at same time is to use dedicated base board containing all necessary for easy use. Figure 15 shows typical example where we only need scope for detail waveform analyzing and precise measurement. The base board makes possible connect up to 200 V voltage for power device loading to see impact of non−linear miller capacity to driving performance.

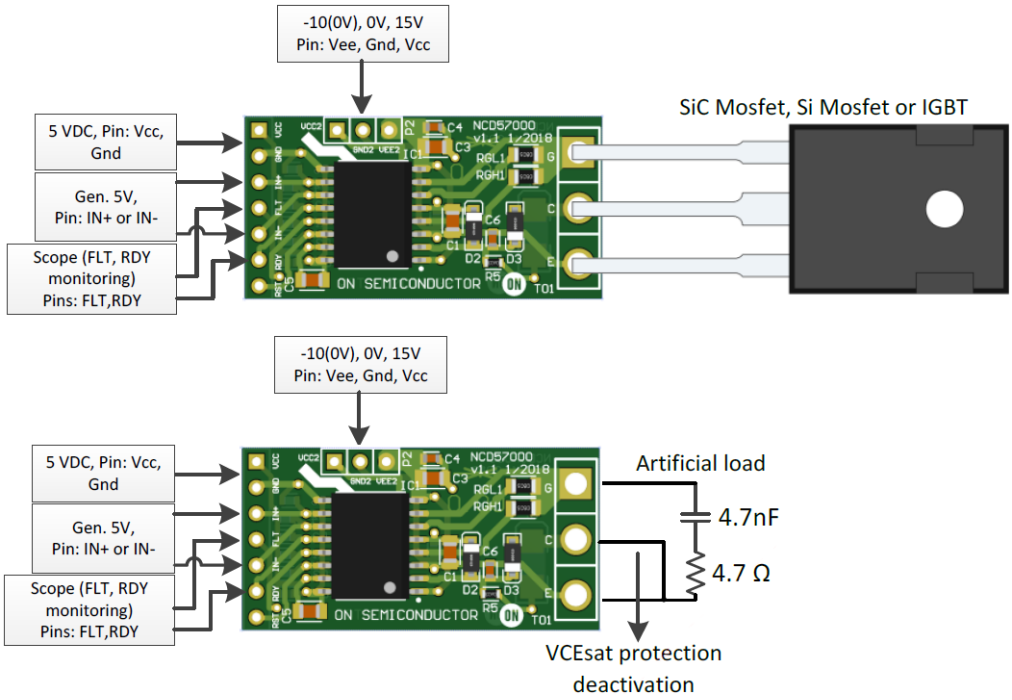


Figure 14. Test Configuration of EVB without Installing into Main or Base PCB

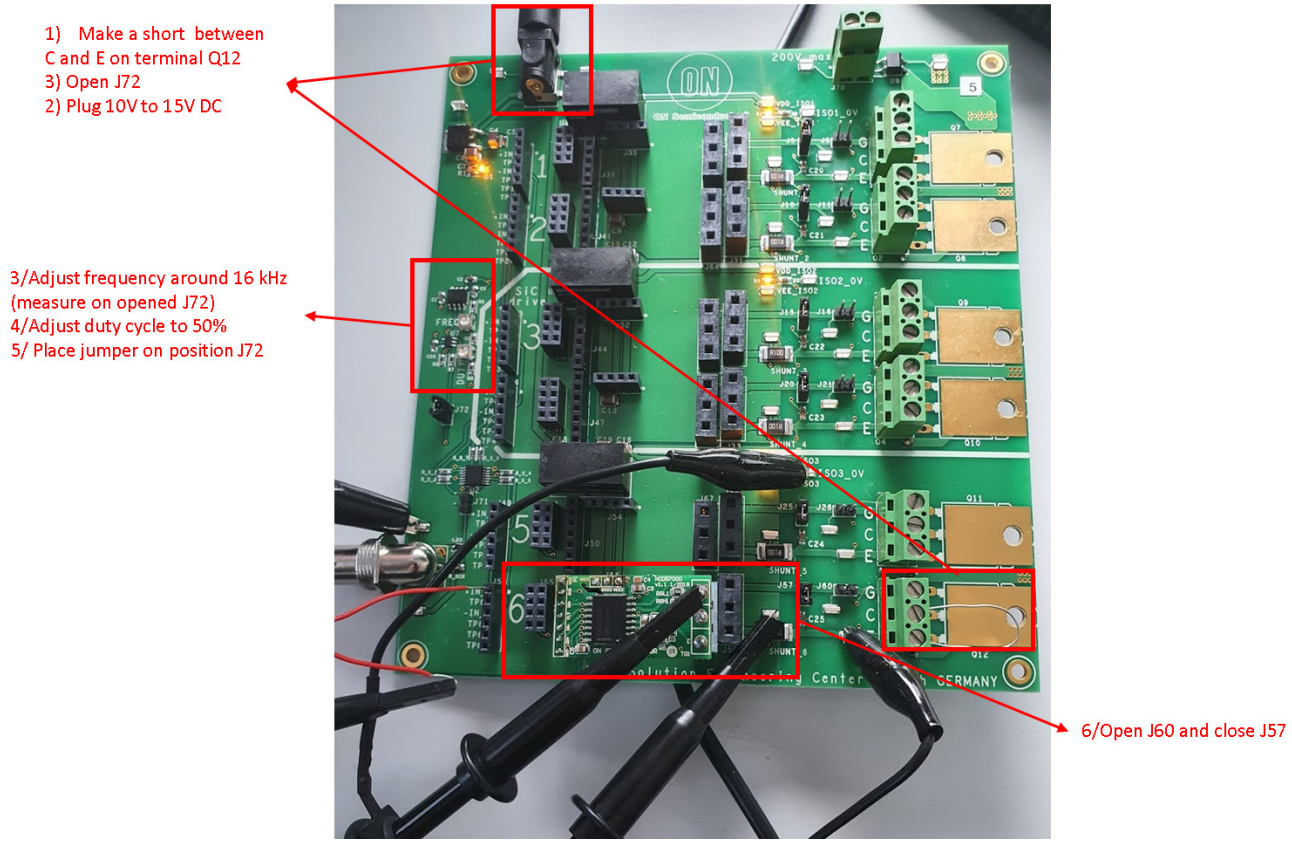


Figure 15. One of Examples How to Use Extended Mother Board (SECO−GDBB−EVB) for Gate Drive Mini Boards Testing and Evaluating

DESAT Setup

DESAT is a type of short circuit or/and over−current protection dedicated to monitoring the $I_D \cdot R_{DS}$ of the MOSFET or Vce_sat voltage for bipolar device like IGBTs. The EVB is preconfigured with R5 = 1 kΩ (DESAT resistor). The internal DESAT threshold is fixed at $V_{DESAT(TH)}$ = 9 V and the DESAT signal amplitude is adjustable by R5 and HV diode connected in series with R5. R5 = 1 kΩ may not be the correct resistor value for some applications. If V_{DESAT} > 9 V during normal operation, decrease R5 to lower the signal amplitude. If DESAT is active, the output is driven low. Further, the /FLT output is activated, please refer to datasheet for more details.

Basic Measurement

Figure 16 and Figure 17 show basic gate driver board connected to base board according the Figure 15. Very easily can be evaluated time delays, maximal gate current capability or maximal switch frequency before thermal runaway at given condition and similar. Typically we can measure time between fault event and FLT pin reaction. Typical task is to compare different part number at same time and/or same condition to see online all, for application, important behaviors.

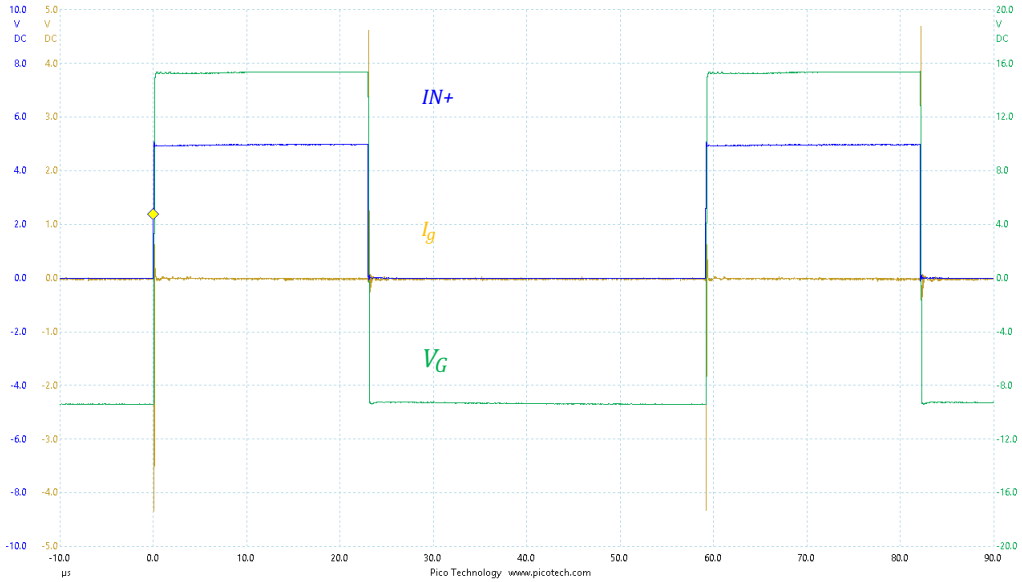


Figure 16. Normal Operation for Turn−on and Turn−off

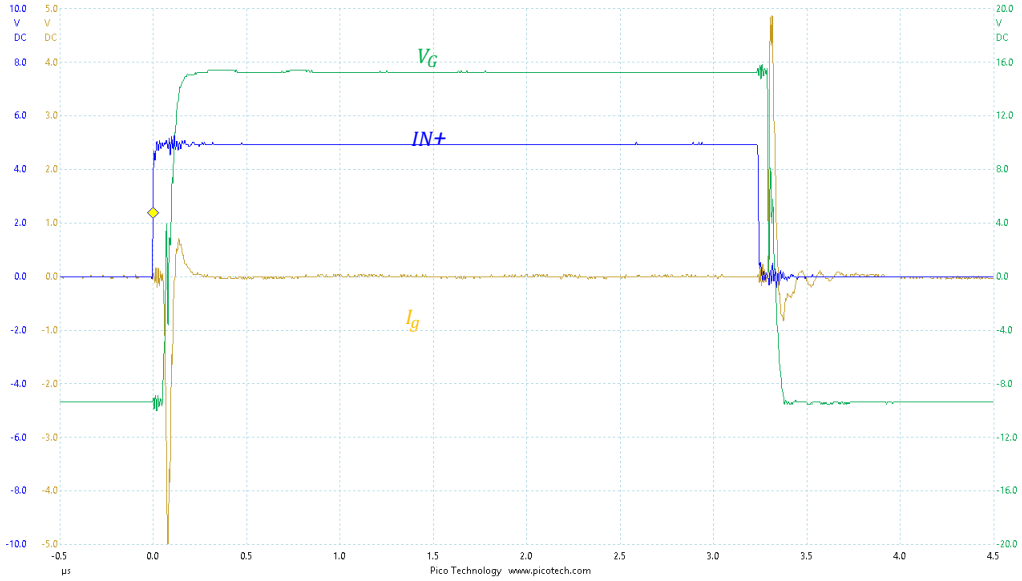


Figure 17. Zoom of Normal Operation for Turn−on and Turn−off

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