INA203-Q1 Automotive Grade, –16 V to +80 V, Low- or High-Side, High-Speed, Voltage Output Current Shunt Monitor With Dual Comparators and Reference

1 Features

- Qualified for Automotive Applications
- Current Sense Amplifier
  - Common-Mode Range: –16 V to +80 V
  - Accuracy: 3.5% (Maximum) Over Temperature
  - Bandwidth: 500 kHz
  - Gain: 20 V/V
- Integrated Dual Comparators:
  - Comparator 1 With Latch
  - Comparator 2 With Optional Delay
- Quiescent Current: 1.8 mA
- Latch-Up Performance Meets 100 mA Per AEC-Q100, Level I
- Packages: TSSOP-14

2 Applications

- Electric Power Steering (EPS) Systems
- Body Control Modules
- Brake Systems
- Electronic Stability Control (ESC) Systems

3 Description

The INA203-Q1 is a unidirectional current-shunt monitor (also called a current sense amplifier) with voltage output, dual comparators, and voltage reference. The INA203-Q1 can sense drops across shunts at common-mode voltages from –16 V to +80 V. The INA203-Q1 is available with 20-V/V gain with up to 500-kHz bandwidth.

The INA203-Q1 incorporates two open-drain comparators with internal 0.6-V references and also provides a 1.2-V reference output. The comparator references can be overridden by external inputs. Comparator 1 includes a latching capability, and Comparator 2 has a user-programmable delay.

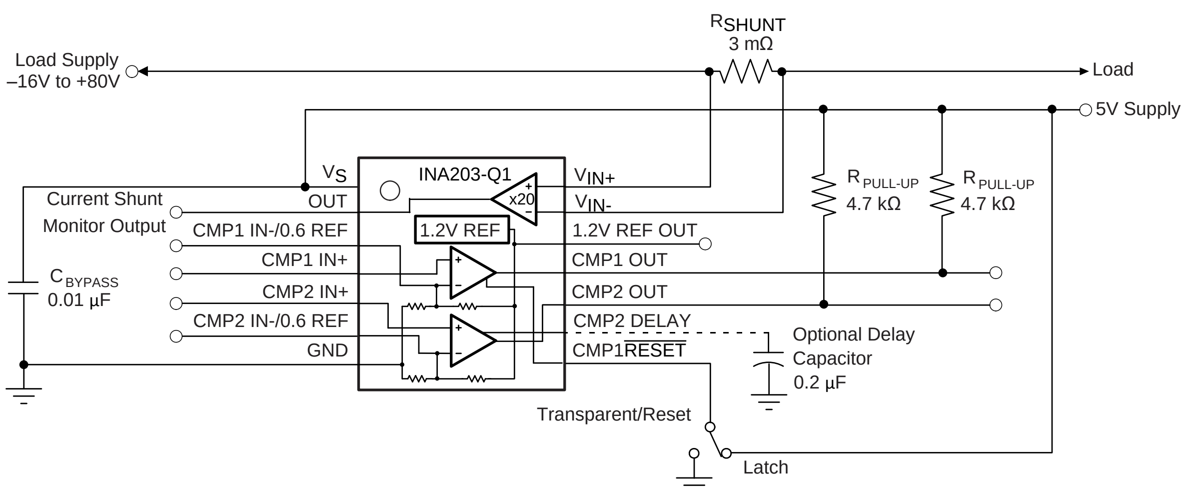
The INA203-Q1 operates from a single 2.7 V to 18 V supply. It is specified over the extended operating temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA203-Q1	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Basic Connections Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2010) to Revision A — **Page**

- Updated data sheet title, *Features*, *Applications*, and *Description* 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, *Mechanical, Packaging, and Orderable Information* section, *Pin Configuration and Functions* section, *Recommended Operating Conditions* Table, and *Thermal Information* Table 1
- Added *Device Comparison Table* 3
- Changed V+ to V_S throughout 4
- Changed MAX value 18 to (V_S) + 0.3 for Comparator output pins 4
- Changed MAX value 10 to (V_S) up to 10 for 1.2-V REF and CMP2 DELAY pins 4
- Changed pin names in *Absolute Maximum Ratings* to show correct names 4
- Added Operating Temperature to *Absolute Maximum Ratings* table 4
- Changed CMP2 IN– to CMP2 IN+ in *Electrical Characteristics: Current-Shunt Monitor* condition statement 5
- Changed CMP2 IN– to CMP2 IN+ in *Electrical Characteristics: General* condition statement 7
- Updated *Overview* section 12
- Deleted 10-pin device image 12
- Changed text from "RFILT – 3%" to "RFILT + 3%" in 2nd paragraph of *Input Filtering* section 16
- Changed Figure 35 caption 16

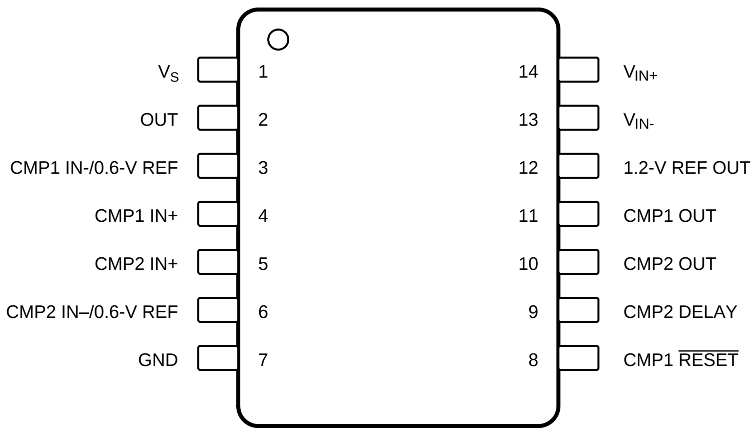
5 Device Comparison Table

Table 1. Related Products

PRODUCT	DESCRIPTION
INA200–Q1	Single comparator alternative to the INA203's dual comparators
INA193A–Q1	Same amplifier performance without the comparators integrated
INA282–Q1	High-accuracy, high common-mode capable current sense amplifier
INA300–Q1	36-V overcurrent protection comparator
INA301	High-accuracy, high slew-rate current sense amplifier with integrated high-speed comparator optimized for overcurrent protection.

6 Pin Configuration and Functions

PW Package
14-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_S	I	Power supply
2	OUT	O	Output voltage
3	CMP1 IN-/0.6-V REF	I	Comparator 1 negative input, can be used to override the internal 0.6-V reference
4	CMP1 IN+	I	Comparator 1 positive input
5	CMP2 IN+	I	Comparator 2 positive input
6	CMP2 IN–/0.6-V REF	I	Comparator 2 negative input, can be used to override the internal 0.6-V reference
7	GND	I	Ground
8	CMP1 $\overline{\text{RESET}}$	I	Comparator 1 ouput reset, active low
9	CMP2 DELAY	I	Connect an optional capacitor to adjust comparator 2 delay
10	CMP2 OUT	O	Comparator 2 output
11	CMP1 OUT	O	Comparator 1 output
12	1.2-V REF OUT	O	1.2-V reference output
13	$V_{IN–}$	I	Amplifier Negative Input. Connect to shunt low side
14	V_{IN+}	I	Amplifier Positive Input. Connect to shunt high side

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage	V_S		18	V
Current-shunt monitor analog inputs, V_{IN+} and V_{IN-}	Differential $(V_{IN+}) - (V_{IN-})$	–18	18	V
	Common-mode	–16	80	V
Comparator analog input	CMP1 IN+, CMP1 IN-/0.6-V REF, CMP2 IN+, CMP2 IN-/0.6-V REF	GND – 0.3	(V_S) + 0.3	V
Comparator reset	CMP1 $\overline{\text{RESET}}$	GND – 0.3	(V_S) + 0.3	
Analog output	OUT	GND – 0.3	(V_S) + 0.3	V
Comparator output	CMP1 OUT, CMP2 OUT	GND – 0.3	(V_S) + 0.3	V
1.2-V REF and CMP2 DELAY pins		GND – 0.3	(V_S) up to 10	V
Input current into any pin			5	mA
Operating temperature		–55	150	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	–16	12	80	V
V_S	Operating supply voltage	2.7	12	18	V
T_A	Operating free-air temperature	–40	25	125	ºC

7.4 Thermal Information

THERMAL METRIC (1)		INA203-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	150	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: Current-Shunt Monitor

At T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, and CMP1 IN+ = 1 V and CMP2 IN+ = GND, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{SENSE}	Full-scale sense input voltage	$V_{SENSE} = V_{IN+} – V_{IN–}$			0.15	(V_S – 0.25)/Gain	V
V_{CM}	Common-mode input range	T_A = –40°C to +125°C		–16		80	V
CMRR	Common-mode rejection ratio	V_{CM} = –16 V to +80 V		80	100		dB
	Over temperature	V_{CM} = 12 V to 80 V	T_A = 25°C to 125°C	100	123		dB
		T_A = –40°C to +25°C		90	100		dB
V_{OS}	Offset voltage, RTI(1)				±0.5	±2.5	mV
		T_A = 25°C to 125°C				±3	mV
		T_A = –40°C to +25°C				±3.5	mV
dV_{OS}/dT	Versus temperature	T_{MIN} to T_{MAX}	T_A = –40°C to +125°C		5		μV/°C
PSR	Versus power supply	V_{OUT} = 2 V, V_{CM} = +18 V	T_A = –40°C to +125°C		2.5	100	μV/V
I_B	Input bias current, $V_{IN–}$ Pin	T_A = –40°C to +125°C			±9	±16	μA
OUTPUT (V_{SENSE} ≥ 20 mV)							
G	Gain				20		V/V
	Gain error	V_{SENSE} = 20 mV to 100 mV			±0.2%	±1%	
	Over temperature	V_{SENSE} = 20 mV to 100 mV	T_A = –40°C to +125°C			±2%	
	Total output error(2)	V_{SENSE} = 120 mV, V_S = +16 V			±0.75%	±2.2%	
	Over temperature	V_{SENSE} = 120 mV, V_S = +16 V	T_A = –40°C to +125°C			±3.5%	
	Nonlinearity error(3)	V_{SENSE} = 20 mV to 100 mV			±0.002%		
R_O	Output impedance, Pin 2				1.5		Ω
	Maximum capacitive load	No sustained oscillation			10		nF
OUTPUT (V_{SENSE} < 20 mV)(4)							
V_{OUT}	Output voltage	–16 V ≤ V_{CM} < 0 V			300		mV
		0 V ≤ V_{CM} ≤ V_S, V_S = 5 V				0.4	V
		V_S < V_{CM} ≤ 80 V			300		mV
VOLTAGE OUTPUT(5)							
	Output swing to the positive rail	$V_{IN–}$ = 11 V, V_{IN+} = 12 V	T_A = –40°C to +125°C		(V_S) – 0.15	(V_S) – 0.25	V
	Output Swing to GND(6)	$V_{IN–}$ = 0 V, V_{IN+} = –0.5 V	T_A = –40°C to +125°C		(V_{GND}) + 0.004	(V_{GND}) + 0.05	V
FREQUENCY RESPONSE							
BW	Bandwidth	C_{LOAD} = 5 pF			500		kHz
	Phase margin	C_{LOAD} < 10 nF			40		Degrees
SR	Slew rate				1		V/μs
	Settling time (1%)	V_{SENSE} = 10 mV_{PP} to 100 mV_{PP}, C_{LOAD} = 5 pF			2		μs
NOISE, RTI							
	Output Voltage Noise Density				40		nV/√Hz

(1) Offset is extrapolated from measurements of the output at 20 mV and 100 mV V_{SENSE}.
(2) Total output error includes effects of gain error and V_{OS}.
(3) Linearity is best fit to a straight line.
(4) For details on this region of operation, see the *Accuracy Variations* section.
(5) See *Typical Characteristics* curve *Positive Output Voltage Swing vs Output Current* (Figure 8).
(6) Specified by design; not production tested.

7.6 Electrical Characteristics: Comparator

At T_A = +25°C, V_S = +12 V, V_{CM} = +12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, and $R_{PULL-UP}$ = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
	Offset voltage	Comparator common-mode voltage = threshold voltage		2		mV
	Offset voltage drift, comparator 1	T_A = –40°C to +125°C		±2		µV/°C
	Offset voltage drift, comparator 2	T_A = –40°C to +125°C		5.4		µV/°C
	Threshold	Rising Edge on Non-Inverting input, T_A = +25°C	590	608	620	mV
	Over temperature	T_A = –40°C to +125°C	586		625	mV
	Hysteresis(1), CMP1	T_A = –40°C to +85°C		–8		mV
	Hysteresis(1), CMP2	T_A = –40°C to +85°C		8		mV
INPUT BIAS CURRENT(2)						
	CMP1 IN+, CMP2 IN+			0.005	10	nA
	Over temperature	T_A = –40°C to +125°C			15	nA
INPUT IMPEDANCE						
Pins 3 and 6				10		kΩ
INPUT RANGE						
	CMP1 IN+ and CMP2 IN+			0 V to V_S – 1.5 V		V
	Pins 3 and 6(3)			0 V to V_S – 1.5 V		V
OUTPUT						
	Large-signal differential voltage gain	CMP V_{OUT} 1 V to 4 V, R_L ≥ 15 kΩ connected to 5 V		200		V/mV
	High-level output current	V_{ID} = 0.4 V, V_{OH} = V_S		0.0001	1	µA
	Low-level output voltage	V_{ID} = –0.6 V, I_{OL} = 2.35 mA		220	300	mV
RESPONSE TIME(4)						
	Comparator 1	R_L to 5 V, C_L = 15 pF, 100 mV input step with 5 mV overdrive		1.3		µs
	Comparator 2	R_L to 5 V, C_L = 15 pF, 100 mV input step with 5 mV overdrive, C_{DELAY} pin open		1.3		µs
RESET						
	RESET threshold(5)			1.1		V
	Logic input impedance			2		MΩ
	Minimum RESET pulse width			1.5		µs
	RESET propagation delay			3		µs
	Comparator 2 delay equation(6)			C_{DELAY} = t_D/5		µF
t_D	Comparator 2 delay	C_{DELAY} = 0.1 µF		0.5		s

(1) Hysteresis refers to the threshold (the threshold specification applies to a rising edge of a noninverting input) of a falling edge on the noninverting input of the comparator; refer to Figure 1.
(2) Specified by design; not production tested.
(3) See the *Comparator Maximum Input Voltage Range* section.
(4) The comparator response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.
(5) The CMP1 RESET input has an internal 2 MΩ (typical) pull-down. Leaving the CMP1 RESET open results in a LOW state, with transparent comparator operation.
(6) The Comparator 2 delay applies to both rising and falling edges of the comparator output.

7.7 Electrical Characteristics: Reference

At T_A = +25°C, V_S = +12 V, V_{CM} = +12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, and $R_{PULL-UP}$ = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE VOLTAGE							
	1.2 V_{REFOUT} output voltage			1.188	1.2	1.212	V
dV_{OUT}/dT	Reference drift(1)	T_A = –40°C to +85°C			40	100	ppm/°C
0.6 V_{REF}	Output voltage (Pins 3 and 6)				0.6		V
dV_{OUT}/dT	Reference drift(1)	T_A = –40°C to +85°C			40	100	ppm/°C
LOAD REGULATION							
dV_{OUT}/dI_{LOAD}	Sourcing	0 mA < I_{SINK} < 0.5 mA	V_{REFOUT} – 1.2 V		0.4	2	mV/mA
	Sinking		0 mA < I_{SOURCE} < 0.5 mA		0.4		mV/mA
LOAD CURRENT							
I_{LOAD}					1		mA
LINE REGULATION							
dV_{OUT}/dV_S		2.7 V < V_S < 18 V			30		μV/V
CAPACITIVE LOAD							
	Reference output maximum capacitive load	No sustained oscillations			10		nF
OUTPUT IMPEDANCE							
	Pins 3 and 6				10		kΩ

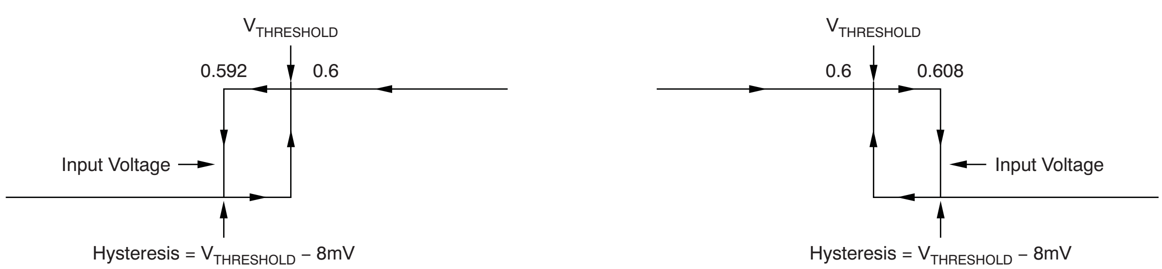
(1) Specified by design; not production tested.

7.8 Electrical Characteristics: General

All specifications at T_A = +25°C, V_S = +12 V, V_{CM} = +12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, and CMP1 IN+ = 1 V and CMP2 IN+ = GND, unless otherwise noted.

GENERAL PARAMETERS		CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_S	Operating Power Supply	T_A = –40°C to +125°C		2.7		18	V
I_Q	Quiescent current	V_{OUT} = 2 V			1.8	2.2	mA
	Over temperature	V_{SENSE} = 0 mV	T_A = –40°C to +125°C			2.8	mA
	Comparator power-on reset threshold(1)				1.5		V

(1) The INA203-Q1 is designed to power-up with the comparator in a defined reset state as long as CMP1 $\overline{RESET}$ is open or grounded. The comparator will be in reset as long as the power supply is below the voltage shown here. The comparator assumes a state based on the comparator input above this supply voltage. If CMP1 $\overline{RESET}$ is high at power-up, the comparator output comes up high and requires a reset to assume a low state, if appropriate.



a) CMP1 **b)** CMP2

Figure 1. Comparator Hysteresis

7.9 Typical Characteristics

All specifications at T_A = +25°C, V_S = +12 V, V_{CM} = +12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

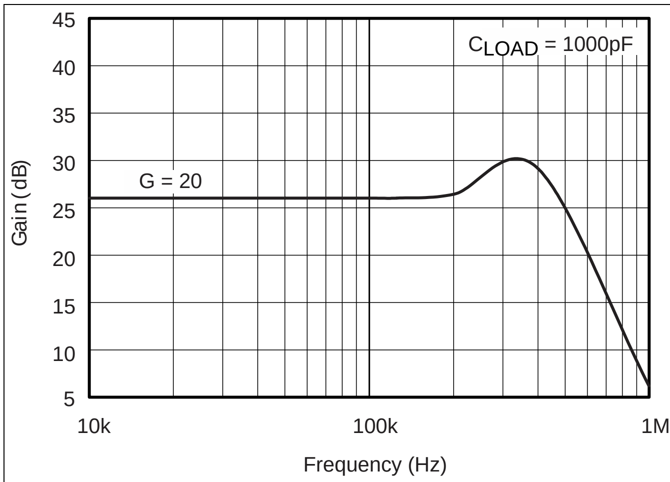


Figure 2. Gain vs Frequency

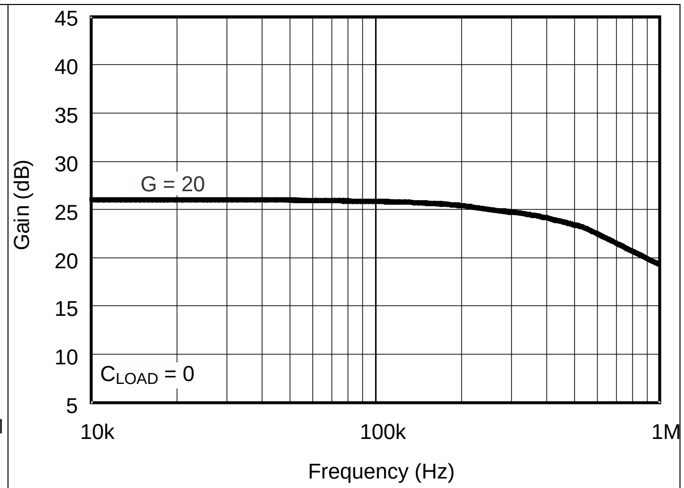


Figure 3. Gain vs Frequency

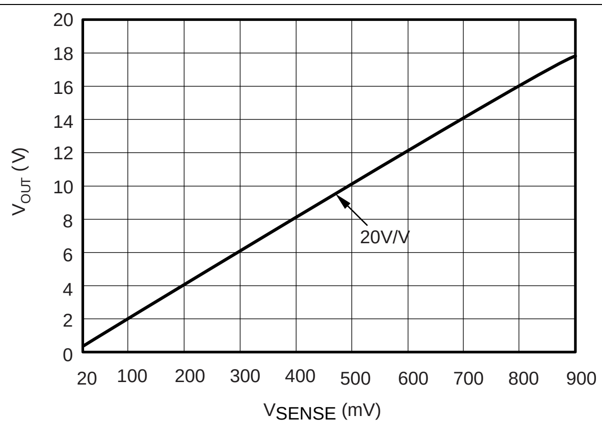


Figure 4. Gain Plot

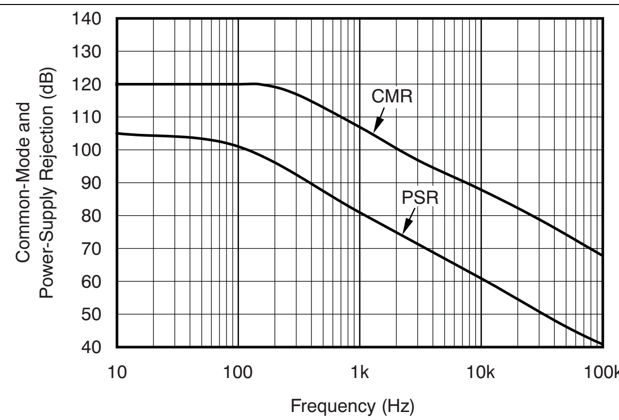


Figure 5. Common-Mode and Power-Supply Rejection vs Frequency

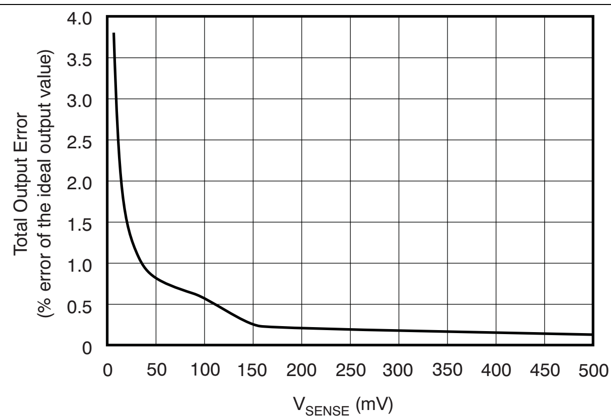


Figure 6. Total Output Error vs V_{SENSE}

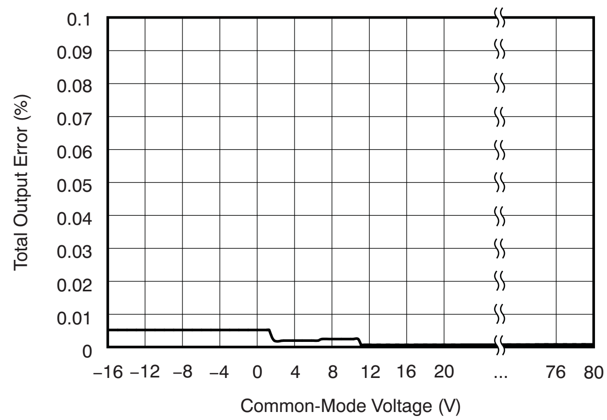


Figure 7. Total Output Error vs Common-Mode Voltage

Typical Characteristics (continued)

All specifications at T_A = +25°C, V_S = +12 V, V_{CM} = +12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

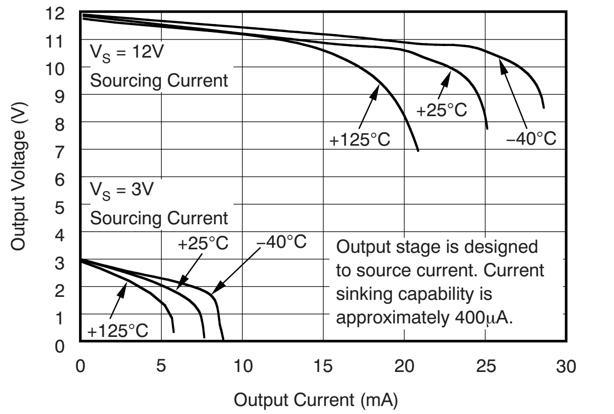


Figure 8. Positive Output Voltage Swing vs Output Current

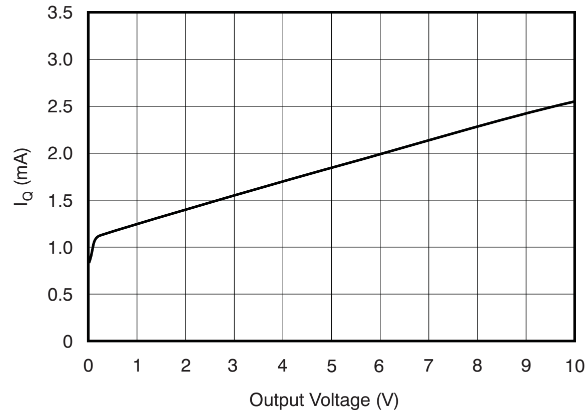


Figure 9. Quiescent Current vs Output Voltage

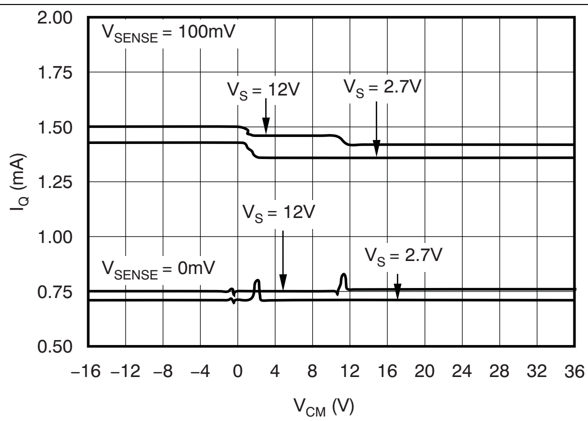


Figure 10. Quiescent Current vs Common-Mode Voltage

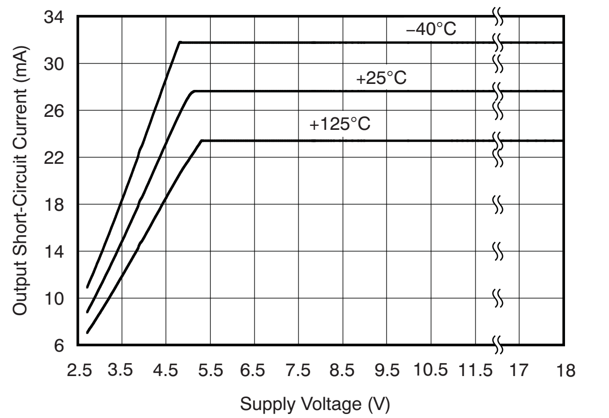


Figure 11. Output Short-Circuit Current vs Supply Voltage

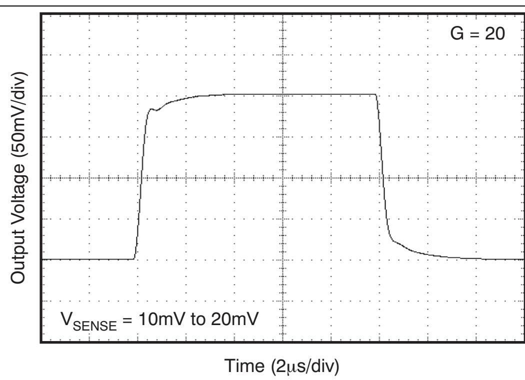


Figure 12. Step Response

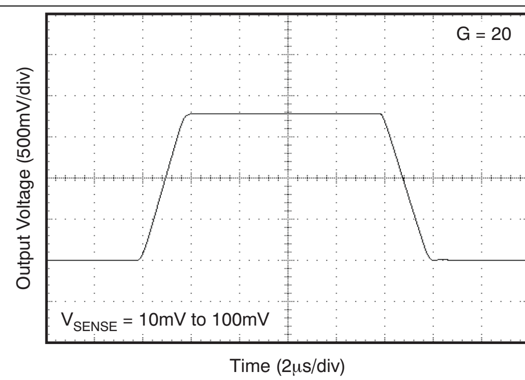


Figure 13. Step Response

Typical Characteristics (continued)

All specifications at T_A = +25°C, V_S = +12 V, V_{CM} = +12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

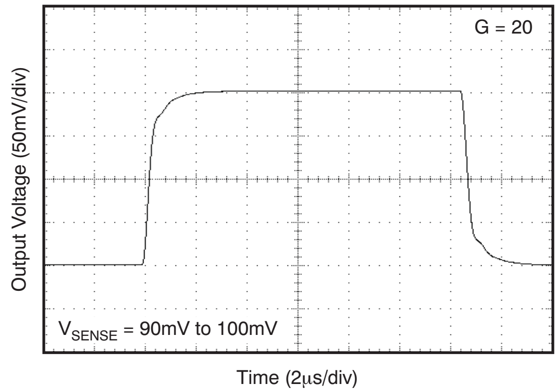


Figure 14. Step Response

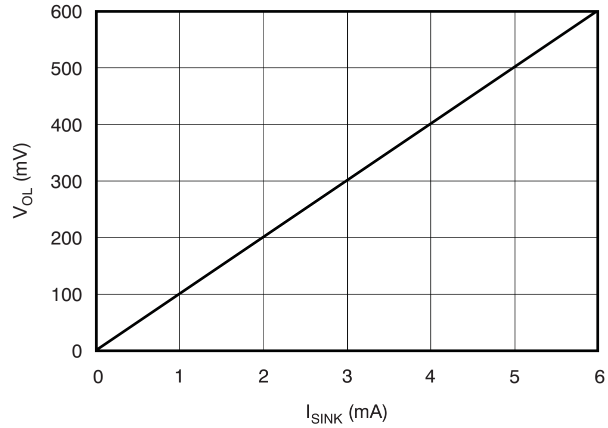


Figure 15. Comparator V_{OL} vs I_{SINK}

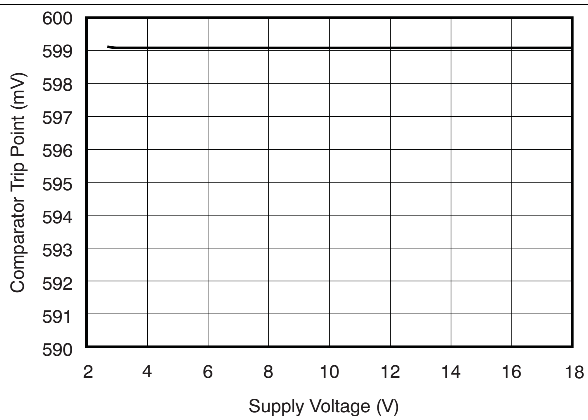


Figure 16. Comparator Trip Point vs Supply Voltage

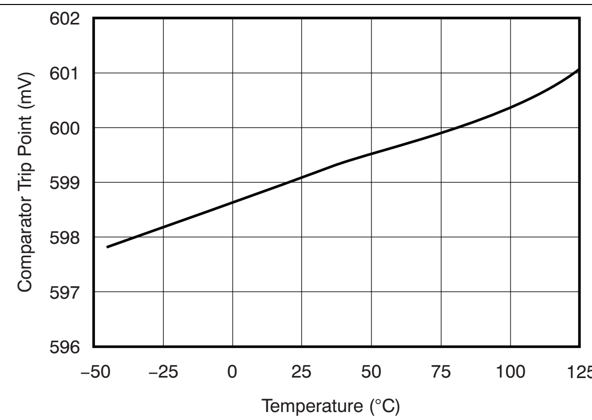


Figure 17. Comparator Trip Point vs Temperature

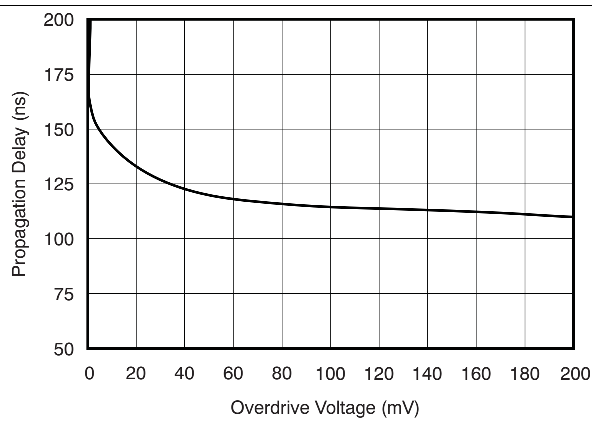


Figure 18. Comparator 1 Propagation Delay vs Overdrive Voltage

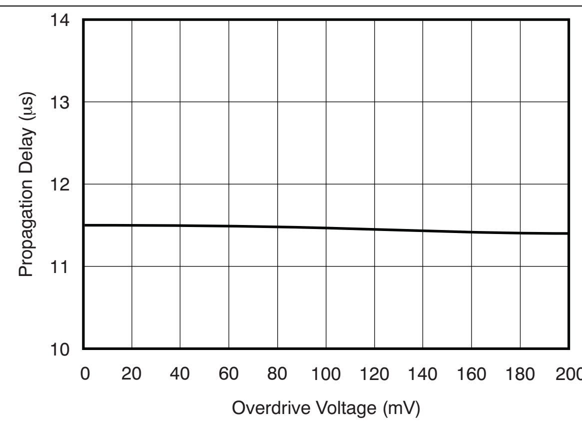


Figure 19. Comparator 2 Propagation Delay vs Overdrive Voltage

Typical Characteristics (continued)

All specifications at T_A = +25°C, V_S = +12 V, V_{CM} = +12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

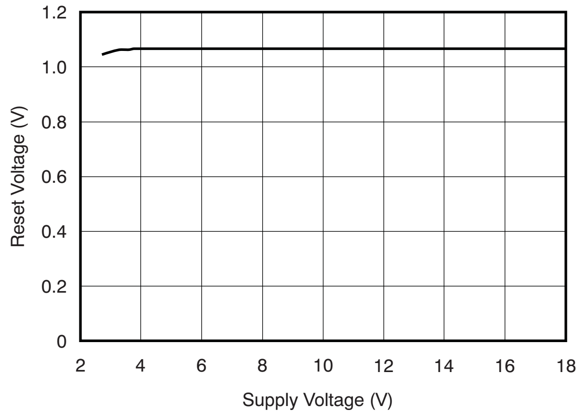


Figure 20. Comparator Reset Voltage vs supply Voltage

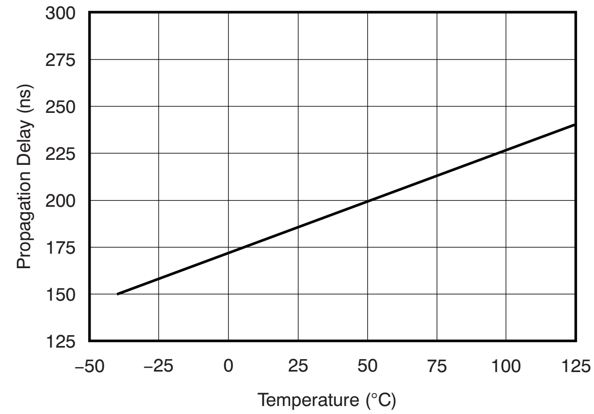


Figure 21. Comparator 1 Propagation Delay vs Temperature

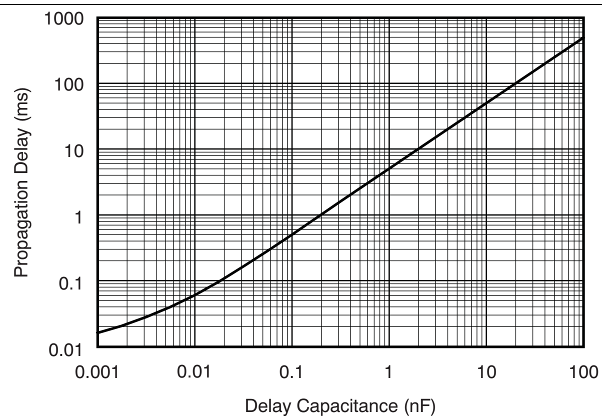


Figure 22. Comparator 2 Propagation Delay vs Capacitance

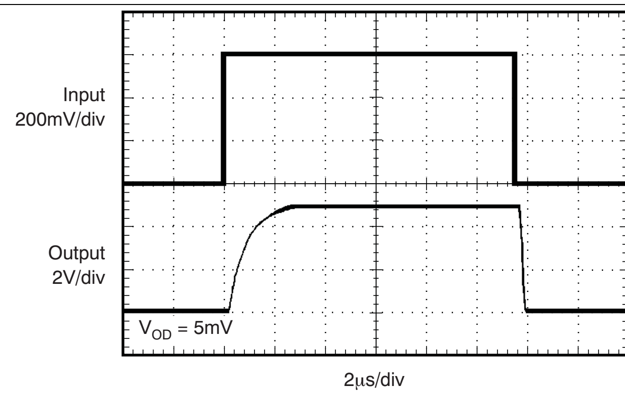


Figure 23. Comparator 1 Propagation Delay

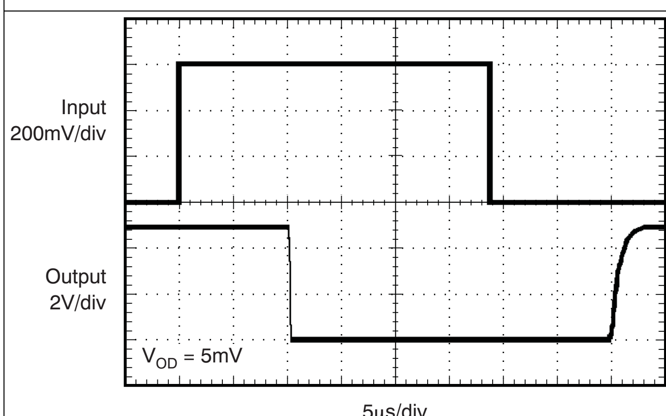


Figure 24. Comparator 2 Propagation Delay

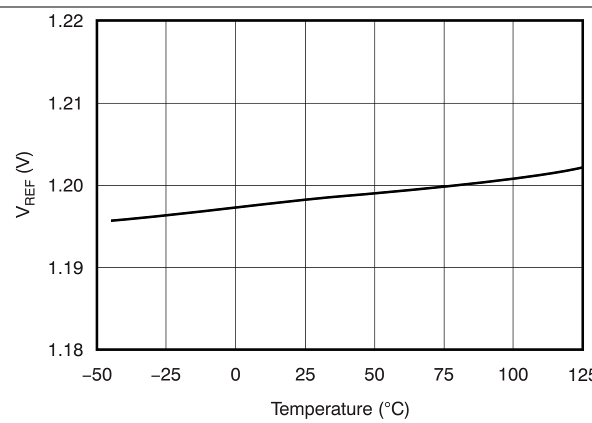


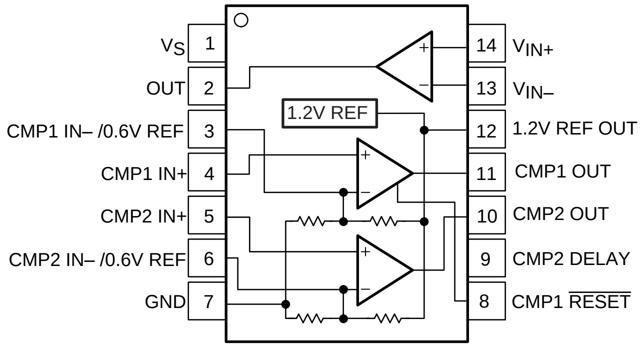
Figure 25. Reference Voltage vs Temperature

8 Detailed Description

8.1 Overview

The INA203-Q1 device is a unidirectional voltage output current-sense amplifier with dual comparators and voltage reference. The INA203-Q1 operates over a wide range of common-mode voltage (–16 V to +80 V) and incorporates two open-drain comparators with internal 0.6-V references. Comparator 1 includes a latching capability, and Comparator 2 has a user-programmable delay. The device also incorporates a 1.2-V reference output.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Comparator

The INA203-Q1 incorporates two open-drain comparators. These comparators typically have 2 mV of offset and a 1.3-µs (typical) response time. The output of Comparator 1 latches and is reset through the CMP1 $\overline{\text{RESET}}$ pin, as shown in Figure 26.

The INA203-Q1 device includes additional features for comparator functions. The comparator reference voltage of both Comparator 1 and Comparator 2 can be overridden by external inputs for increased design flexibility. Comparator 2 has a programmable delay.

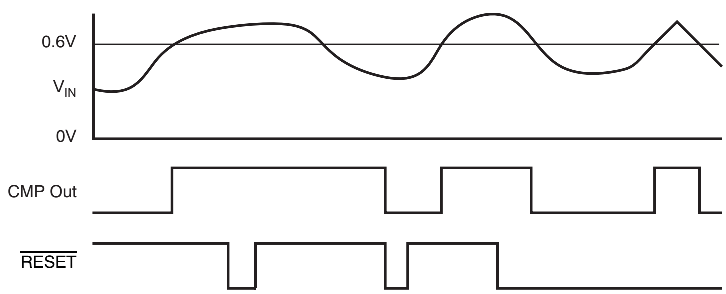


Figure 26. Comparator Latching Capability

8.3.2 Comparator Delay

The Comparator 2 programmable delay is controlled by a capacitor connected to the CMP2 Delay Pin; see Figure 30. The capacitor value (in µF) is selected by using Equation 1:

$$C_{DELAY} \text{ (in } \mu\text{F)} = \frac{t_D}{5} \quad (1)$$

A simplified version of the delay circuit for Comparator 2 is shown in Figure 27. The delay comparator consists of two comparator stages with the delay between them.

Feature Description (continued)

NOTE

I1 and I2 cannot be turned on simultaneously; I1 corresponds to a U1 low output and I2 corresponds to a U1 high output.

Using an initial assumption that the U1 output is low, I1 is on, then U2 +IN is zero. If U1 goes high, I2 supplies 120 nA to C_{DELAY}. The voltage at U2 +IN begins to ramp toward a 0.6-V threshold. When the voltage crosses this threshold, the U2 output goes high while the voltage at U2 +IN continues to ramp up to a maximum of 1.2 V when given sufficient time (twice the value of the delay specified for C_{DELAY}). This entire sequence is reversed when the comparator outputs go low, so that returning to low exhibits the same delay.

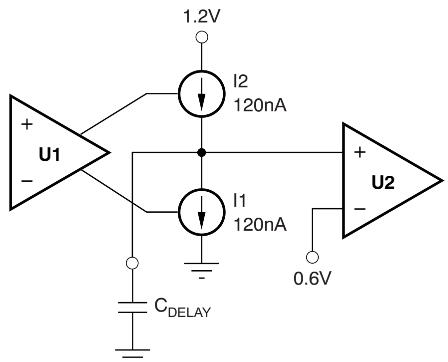


Figure 27. Simplified Model of The Comparator 2 Delay Circuit

It is important to note the behavior of the Comparator 2 when the events at the inputs occur more rapidly than the set delay timeout. For example, when the U1 output goes high (turning on I2), but returns low (turning I1 back on) prior to reaching the 0.6 V transition for U2. The voltage at U2 +IN ramps back down at a rate determined by the value of C_{DELAY}, and only returns to zero if given sufficient time.

In essence, when analyzing Comparator 2 for behavior with events more rapid than its delay setting, use the model shown in Figure 27.

8.3.3 Comparator Maximum Input Voltage Range

The maximum voltage at the comparator input for normal operation is up to (V_S) – 1.5 V. There are special considerations when overdriving the reference inputs (pins 3 and 6). Driving either or both inputs high enough to drive 1 mA back into the reference introduces errors into the reference. Figure 28 shows the basic input structure. A general guideline is to limit the voltage on both inputs to a total of 20 V. The exact limit depends on the available voltage and whether either or both inputs are subject to the large voltage. When making this determination, consider the 20 kΩ from each input back to the comparator. Figure 29 shows the maximum input voltage that avoids creating a reference error when driving both inputs (an equivalent resistance back into the reference of 10 kΩ).

Feature Description (continued)

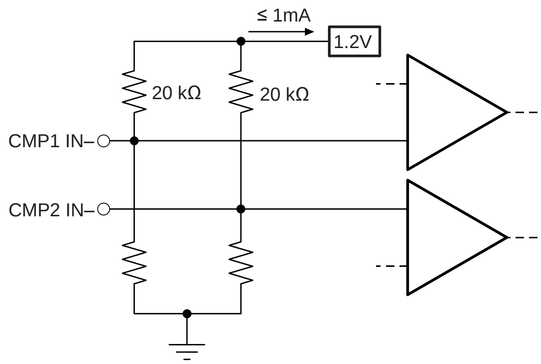


Figure 28. Limit Current Into Reference ≤ 1 mA

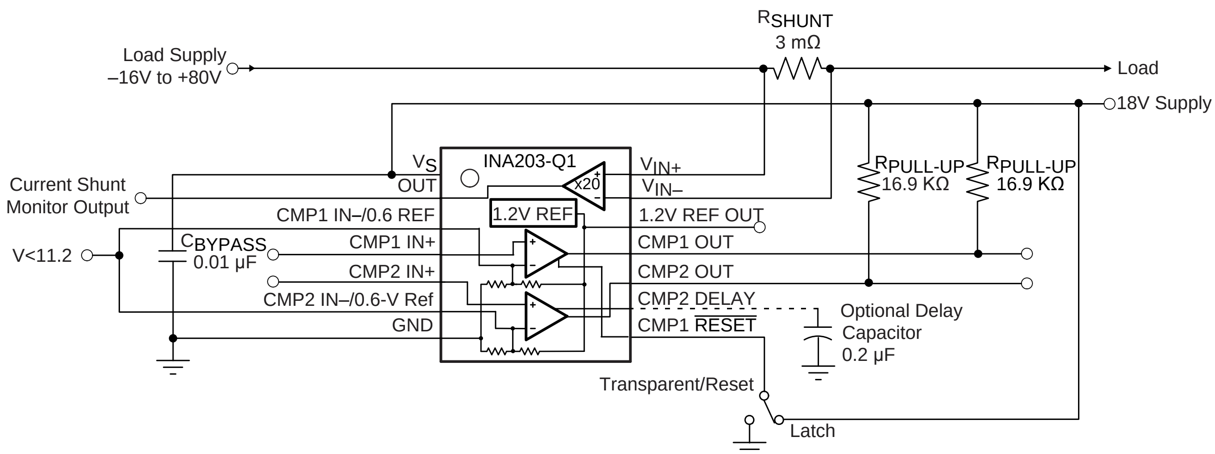


Figure 29. Overdriving Comparator Inputs Without Generating a Reference Error

8.3.4 Reference

The INA203-Q1 include an internal voltage reference that has a load regulation of 0.4 mV/mA (typical), and not more than 100 ppm/°C of drift. The device allows external access to reference voltages, where voltages of 1.2 V and 0.6 V are both available. Output current versus output voltage is illustrated in the *Typical Characteristics* section.

8.3.5 Output Voltage Range

The output of the INA203-Q1 is accurate within the output voltage swing range set by the power-supply pin, V_S. Given the device gain of 20, where a 250 mV full-scale input from the shunt resistor requires an output voltage swing of +5 V, and a power-supply voltage sufficient to achieve +5 V on the output.

8.4 Device Functional Modes

The INA203-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V. The common-mode voltage must be between –16 V and +80 V. The maximum power supply voltage for the INA203-Q1 is 18 V.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The INA203-Q1 device is designed to enable easy configuration for detecting overcurrent conditions and current monitoring in an application. This device is also incorporate two open-drain comparators with internal 0.6-V references. The comparator references can be overridden by external inputs. Comparator 1 includes a latching capability, and Comparator 2 has a user-programmable delay. The INA203-Q1 also provides a 1.2-V reference output. This device can also be paired with minimum additional devices to create more sophisticated monitoring functional blocks.

9.1.1 Basic Connections

Figure 30 shows the basic connections of the INA203-Q1. Connect the input pins, V_{IN+} and V_{IN-}, as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

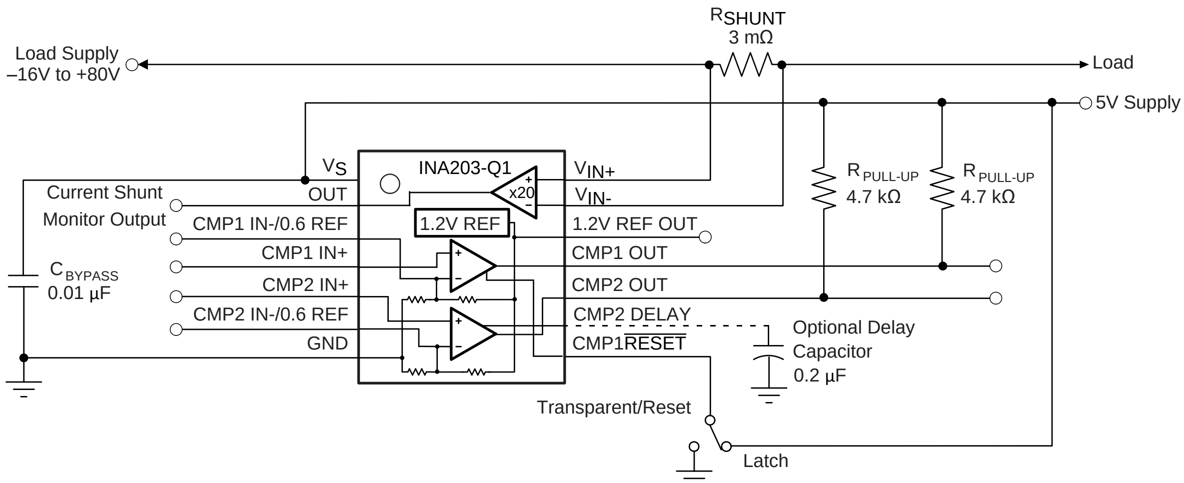


Figure 30. INA203-Q1 Basic Connection

9.1.2 Selecting R_{SHUNT}

The value chosen for the shunt resistor, R_{SHUNT}, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_{SHUNT} provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_{SHUNT} minimize voltage loss in the supply line. For most applications, best performance is attained with an R_{SHUNT} value that provides a full-scale shunt voltage range of 50 mV to 100 mV. Maximum input voltage for accurate measurements is (V_{SHUNT} – 0.25)/Gain.

Application Information (continued)

9.1.3 Input Filtering

An obvious and straightforward location for filtering is at the output of the INA203-Q1 series; however, this location negates the advantage of the low output impedance of the internal buffer. The only other option for filtering is at the input pins of the INA203-Q1, which is complicated by the internal 5 kΩ + 30% input impedance; this configuration is illustrated in Figure 31. Using the lowest possible resistor values minimizes both the initial shift in gain and effects of tolerance. Equation 2 gives the effect on initial gain:

$$\text{Gain Error \%} = 100 - \left(100 \times \frac{5k\Omega}{5k\Omega + R_{FILT}}\right) \quad (2)$$

To calculate the total effect on gain error, replace the 5-kΩ term with 5 kΩ – 30%, (or 3.5 kΩ) or 5 kΩ + 30% (or 6.5 kΩ). The tolerance extremes of R_{FILT} can also be inserted into the equation. If a pair of 100-Ω 1% resistors are used on the inputs, then the initial gain error will be 1.96%. Worst-case tolerance conditions will always occur at the lower excursion of the internal 5-kΩ resistor (3.5 kΩ), and the higher excursion of R_{FILT} + 3% in this case.

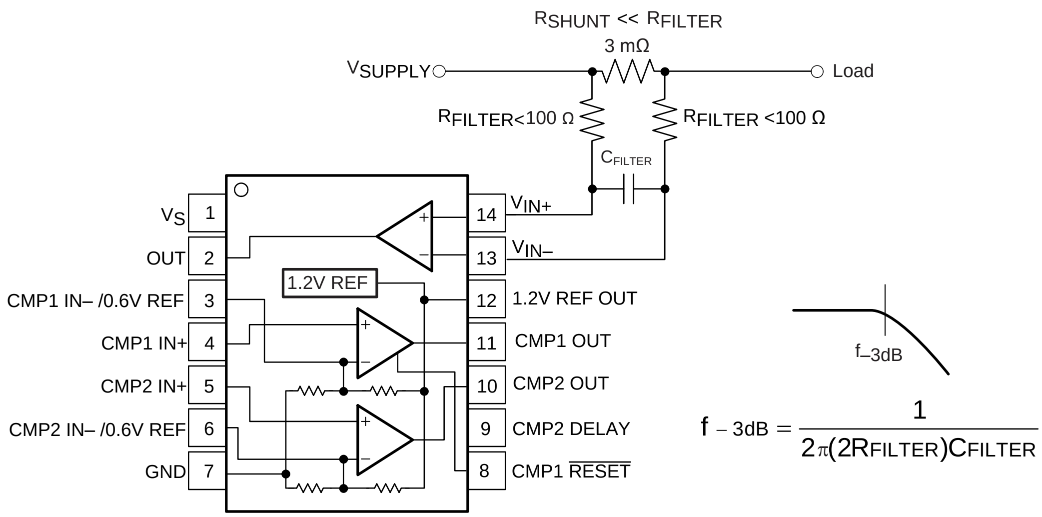


Figure 31. Input Filter

NOTE

The specified accuracy of the INA203-Q1 must then be combined in addition to these tolerances. While this discussion treated accuracy worst-case conditions by combining the extremes of the resistor values, it is appropriate to use geometric-mean or root-sum-square calculations to total the effects of accuracy variations.

9.1.4 Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage

The accuracy of the INA203-Q1 current-shunt monitors is a function of two main variables: V_{SENSE} ($V_{IN+} - V_{IN-}$) and common-mode voltage, V_{CM}, relative to the supply voltage, V_S. V_{CM} is expressed as ($V_{IN+} + V_{IN-}$)/2; however, in practice, V_{CM} is seen as the voltage at V_{IN+} because the voltage drop across V_{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

- Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$
- Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$
- Low V_{SENSE} Case 1: $V_{SENSE} < 20$ mV, $-16\ V \leq V_{CM} < 0$
- Low V_{SENSE} Case 2: $V_{SENSE} < 20$ mV, $0\ V \leq V_{CM} \leq V_S$
- Low V_{SENSE} Case 3: $V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

Application Information (continued)

9.1.4.1 Normal Case 1: V_{SENSE} ≥ 20 mV, V_{CM} ≥ V_S

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by Equation 3.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100mV - 20mV}$$

where

- V_{OUT1} = output voltage with V_{SENSE} = 100 mV
- V_{OUT2} = output voltage with V_{SENSE} = 20 mV (3)

Then the offset voltage is measured at V_{SENSE} = 100 mV and referred to the input (RTI) of the current shunt monitor, as shown in Equation 4.

$$V_{OS}\text{RTI (Referred-To-Input)} = \left(\frac{V_{OUT1}}{G}\right) - 100mV \quad (4)$$

In the *Typical Characteristics* section, the *Output Error vs Common-Mode Voltage* curve (Figure 7) shows the highest accuracy for this region of operation. In this plot, V_S = 12 V; for V_{CM} ≥ 12 V, the output error is at its minimum. This case is also used to create the V_{SENSE} ≥ 20 mV output specifications in the *Electrical Characteristics* table.

9.1.4.2 Normal Case 2: V_{SENSE} ≥ 20 mV, V_{CM} < V_S

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the part functions, as seen in the *Output Error vs Common-Mode Voltage* curve (Figure 7). As noted, for this graph V_S = 12 V; for V_{CM} < 12 V, the output error increases as V_{CM} becomes less than 12 V, with a typical maximum error of 0.005% at the most negative V_{CM} = –16 V.

9.1.4.3 Low V_{SENSE} Case 1:

V_{SENSE} < 20 mV, –16 V ≤ V_{CM} < 0; and

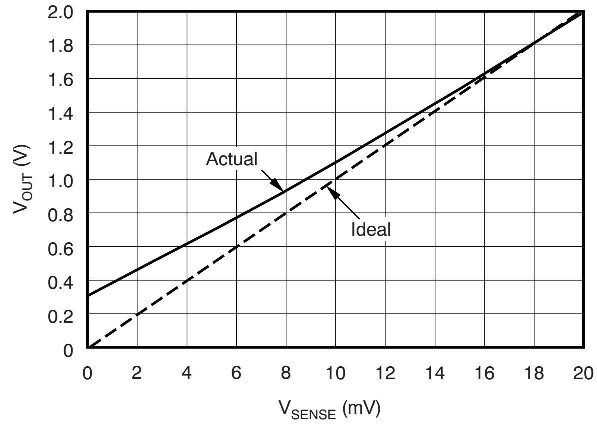
Low V_{SENSE} Case 3:

V_{SENSE} < 20 mV, V_S < V_{CM} ≤ 80 V

Although the INA203-Q1 is not designed for accurate operation in either of these regions, some applications are exposed to these conditions; for example, when monitoring power supplies that are switched on and off while V_S is still applied to the INA203-Q1. It is important to know what the behavior of the devices will be in these regions.

As V_{SENSE} approaches 0 mV, in these V_{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of V_{OUT} = 300 mV for V_{SENSE} = 0 mV. As V_{SENSE} approaches 20 mV, V_{OUT} returns to the expected output value with accuracy as specified in the *Electrical Characteristics*. Figure 32 illustrates this effect (Gain = 100).

Application Information (continued)

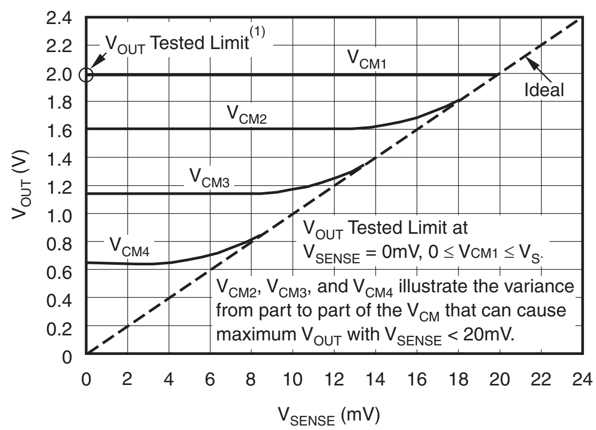


Data taken from INA205, a device of INA20x family with Gain = 100

Figure 32. Example for Low V_{SENSE} Cases 1 and 3 (Gain = 100)

9.1.4.4 Low V_{SENSE} Case 2: V_{SENSE} < 20 mV, 0 V ≤ V_{CM} ≤ V_S

This region of operation is the least accurate for the INA203-Q1. To achieve the wide input common-mode voltage range, this device uses two operational amplifiers (Opamp) front ends in parallel. One Opamp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominate and overall loop gain is very low. Within this region, V_{OUT} approaches voltages close to linear operation levels for Normal Case 2. This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0 V. Within this region, as V_{SENSE} approaches 20 mV, device operation is closer to that described by Normal Case 2. Figure 33 illustrates this behavior. The V_{OUT} maximum peak for this case is tested by maintaining a constant V_S, setting V_{SENSE} = 0 mV, and sweeping V_{CM} from 0 V to V_S. The exact V_{CM} at which V_{OUT} peaks during this test varies from part to part, but the V_{OUT} maximum peak is tested to be less than the specified V_{OUT} Tested Limit.



NOTE: (1) INA203-Q1 V_{OUT} Tested Limit = 0.4V.

Data taken from INA205, a device of INA20x family with Gain = 100

Figure 33. Example for Low V_{SENSE} Case 2 (Gain = 100)

Application Information (continued)

9.1.5 Transient Protection

The –16 V to +80 V common-mode range of the INA203-Q1 is ideal for withstanding automotive fault conditions ranging from 12-V battery reversal up to 80-V transients, since no additional protective components are needed up to those levels. In the event that the INA203-Q1 is exposed to transients on the inputs in excess of their ratings, then external transient absorption with semiconductor transient absorbers (zeners or *Transzorbs*) are necessary. Use of metal oxide varistors (MOVs) or video disk recorders (VDRs) is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it will never allow the INA203-Q1 to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage because of transient absorber dynamic impedance). Despite the use of internal zener-type ESD protection, the INA203-Q1 does not lend itself to using external resistors in series with the inputs because the internal gain resistors can vary up to ±30% but are closely matched. (If gain accuracy is not important, then resistors can be added in series with the INA203-Q1 inputs with two equal resistors on each input.)

9.2 Typical Applications

9.2.1 Polyswitch Warning and Fault Detection Circuit

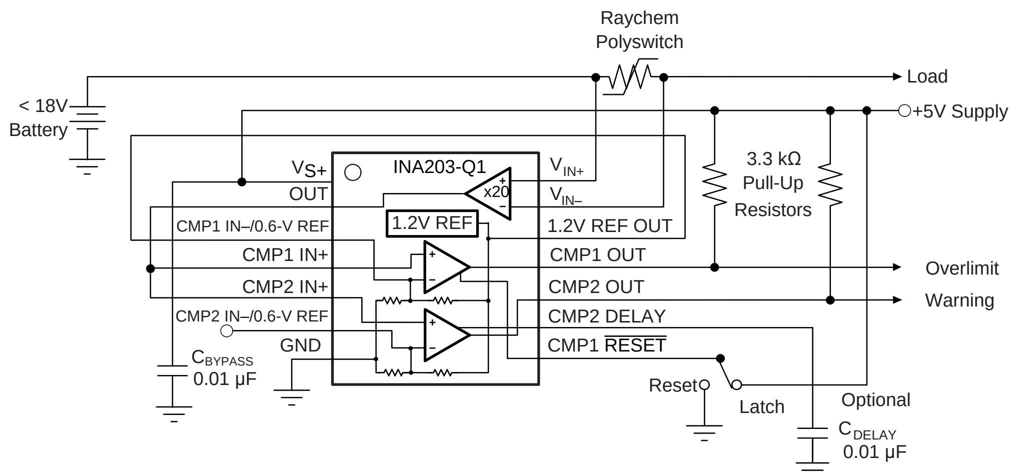


Figure 34. Polyswitch Warning and Fault Detection Circuit Schematic

9.2.1.1 Design Requirements

The device measures current through a resistive shunt with current flowing in one direction, thus enabling detection of an overlimit or warning event only when the differential input voltage exceeds the corresponding threshold limits. When the current reaches the warning limit of 0.6 V, the output of CMP2 will transition high indicating a warning condition. When the current further increases to or past the overlimit limit of 1.2 V, the output of CMP1 will transition high indicating an overlimit condition. Optional C_{DELAY} can be sized to add delay to CMP2.

9.2.1.2 Detailed Design Procedure

Figure 34 shows the basic connections of the device. The input terminals, V_{IN+} and $V_{IN–}$, should be connected as close as possible to the current-sensing resistor or polymeric switch to minimize any resistance in series with the shunt resistance. Additional resistance between the current-sensing resistor and input terminals can result in errors in the measurement. When input current flows through this external input resistance, the voltage developed across the shunt resistor can differ from the voltage reaching the input terminals.

Typical Applications (continued)

9.2.1.3 Application Curves

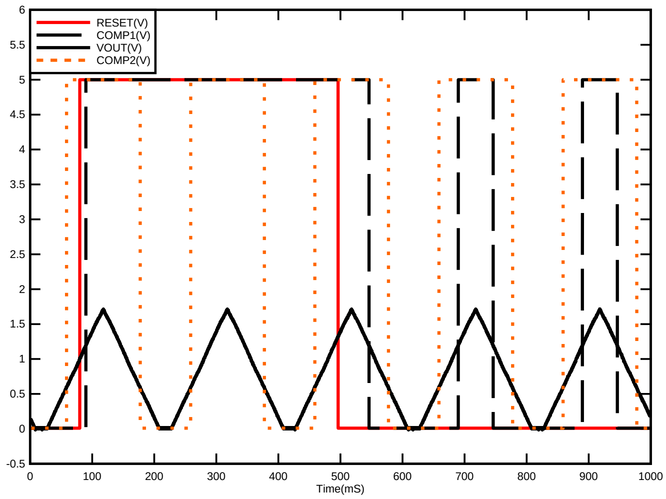


Figure 35. Polyswitch Warning and Fault Detection Circuit Response

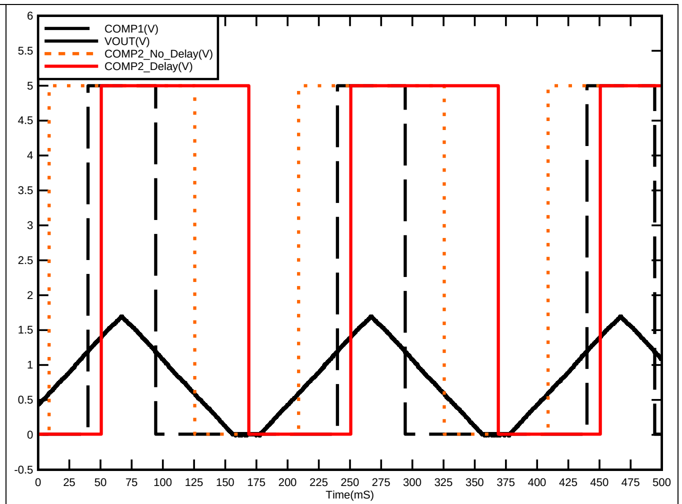


Figure 36. Polyswitch Warning and Fault Detection Circuit With Delay Response

9.2.2 Lead-Acid Battery Protection Circuit

See Figure 37 for a protection scheme using INA203-Q1 for a lead-acid battery application.

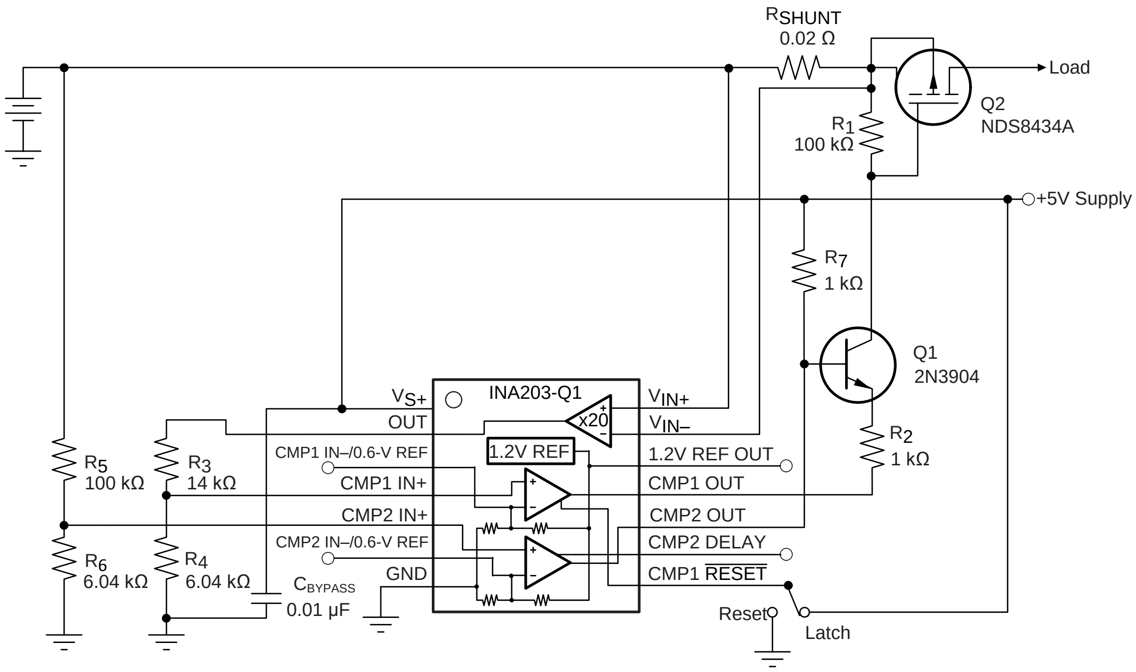


Figure 37. Lead-Acid Battery Protection Circuit Schematic

10 Power Supply Recommendations

The input circuitry of the INA203-Q1 can accurately measure beyond the power-supply voltage, V_S. For example, the V_S power supply can be 5 V, whereas the load power-supply voltage is up to 80 V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

11 Layout

11.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- The power-supply bypass capacitor should be placed as closely as possible to the supply and ground pins. TI recommends the value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

11.2 Layout Example

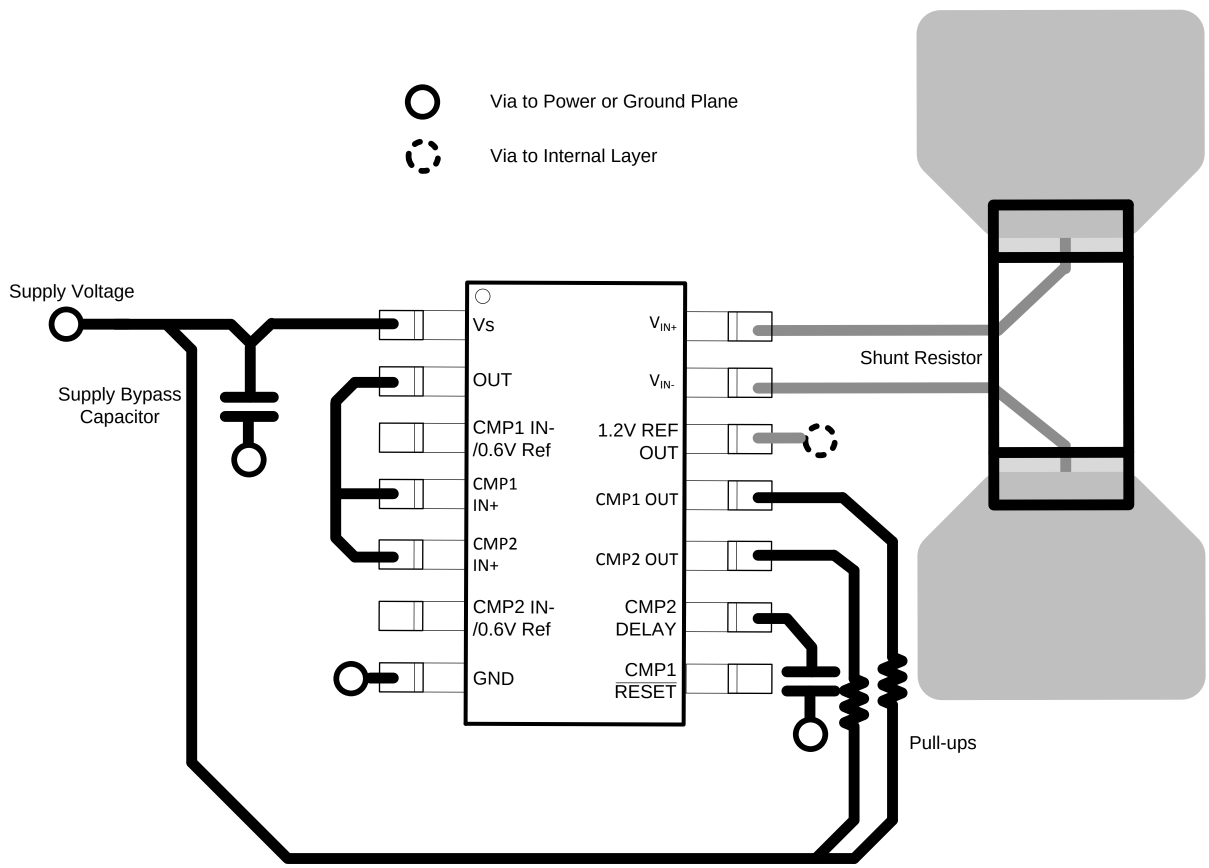


Figure 38. Layout Recommendation

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA203AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I203AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA203-Q1 :

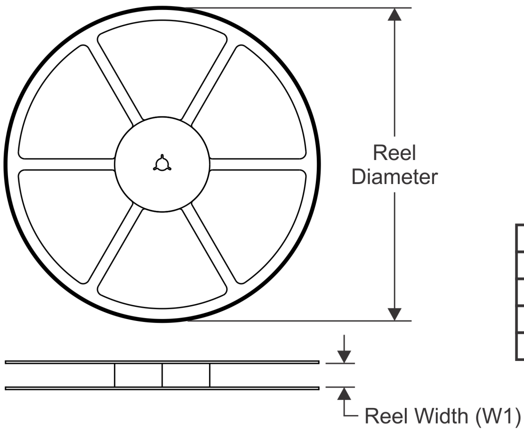
- Catalog: INA203

NOTE: Qualified Version Definitions:

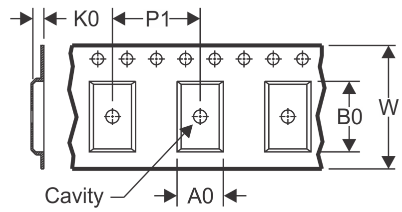
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

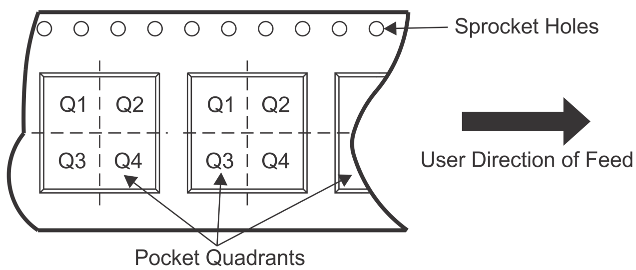


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

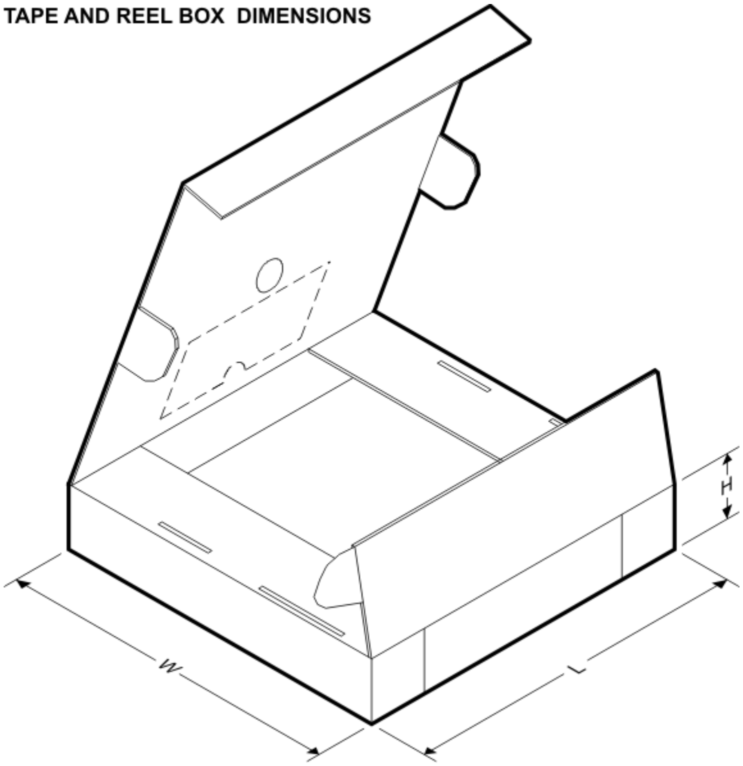
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA203AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

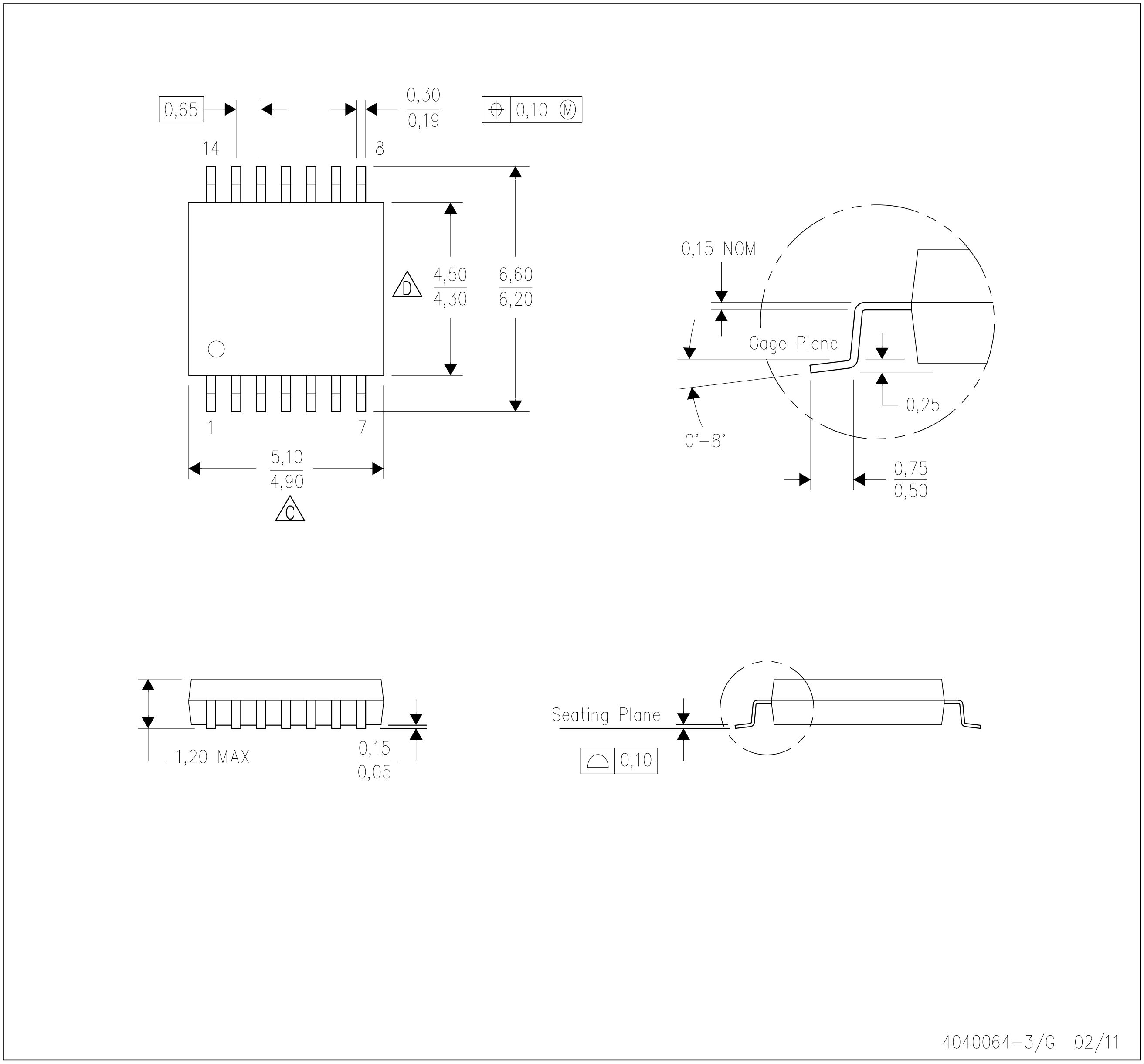
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

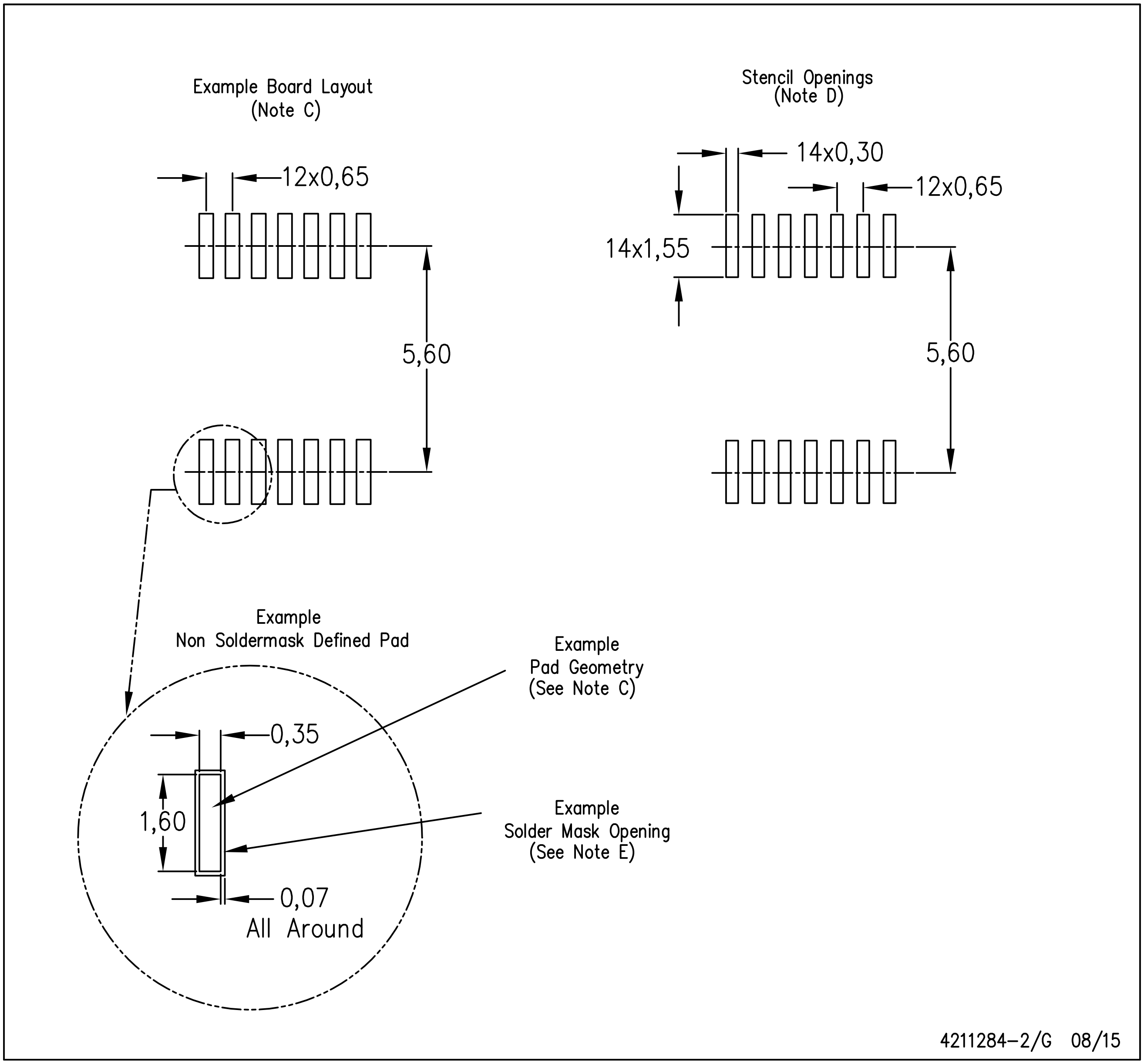
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA203AQPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

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