TPS254900-Q1 Automotive USB Host Charger With Short-to-V_{BATT} Protection

1 Features

- AEC-Q100 Qualified With the Following Results:
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C5
- 4.5-V to 6.5-V Input Operating Range
- Integrated 45-mΩ (typ.) High-Side MOSFET
- 3-A Maximum Continuous Output Current
- V_{BUS} ±5% Cable Compensation Accuracy at Connector
- Supports USB BC 1.2 CDP and SDP Modes
- Short-to-Battery Protection on OUT, DP_IN, and DM_IN Pins
- DP_IN and DM_IN IEC 61000-4-2 Rated
  - ±8-kV Contact and ±15-kV Air Discharge
- 20-Pin QFN (3-mm × 4-mm) Package

2 Applications

- Automotive USB Charging Ports (Host and Hubs)
- Automotive USB Protection

3 Description

The TPS254900-Q1 device is a USB charging-port controller and power switch with short-to-battery protection. This feature provides protection on OUT, DM_IN and DP_IN. These three pins withstand voltage up to 18 V. The internal MOSFET turns off quickly when the short-to-battery condition occurs. Rapid turnoff is very important to protect the upstream dc-dc converter, processor, or hub data lines.

The TPS254900-Q1 45-mΩ power switch has two selectable, adjustable current limits that support port power management by changing to a lower current limit when adjacent ports are experiencing heavy loads. This is important in systems with multiple ports and upstream power supplies with limited capacity.

The TPS254900-Q1 has a current-sense output that is able to control an upstream supply, which allows it to maintain 5 V at the USB port even with heavy charging currents. This feature is important in systems with long USB cables where significant voltage drops can occur with fast-charging portable devices.

A current monitor allows a system to monitor the load current in real time by monitoring the IMON voltage. The current monitor is very useful and can be used for dynamic port-power management.

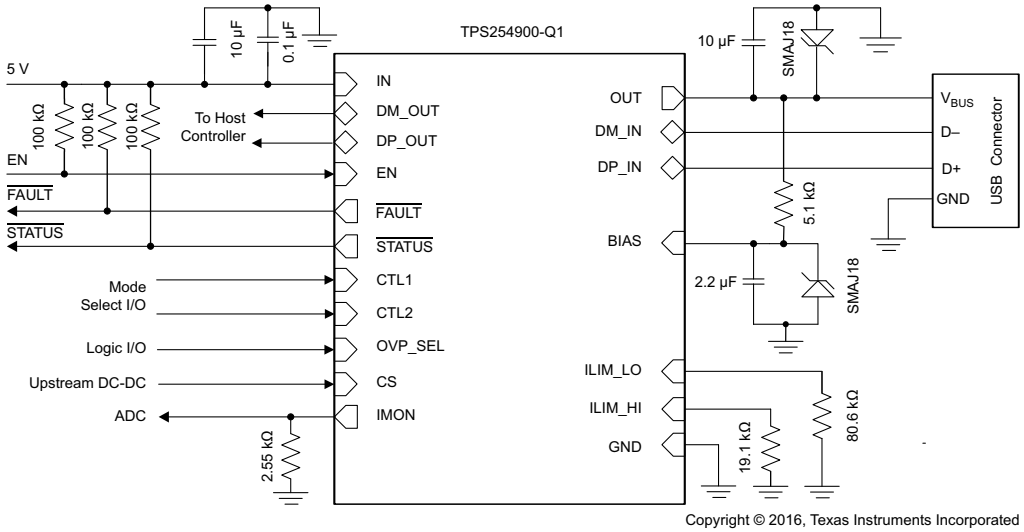
The TPS254900-Q1 device also provides ESD protection capability per IEC 61000-4-2, level 4 on DP_IN and DM_IN.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS254900-Q1	WQFN (20)	3.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Schematic



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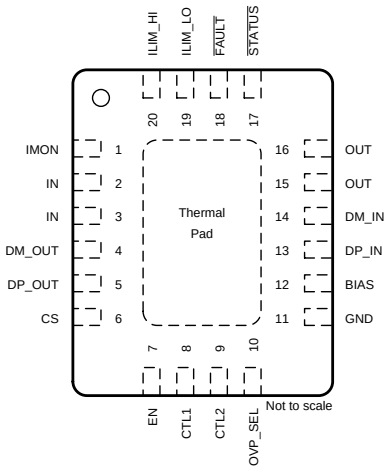
• Changed data sheet from PRODUCT PREVIEW to PRODUCTION DATA	1

5 Pin Configuration and Functions

RVC Package
20-Pin WQFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BIAS	12	PWR	Used for IEC protection. Typically, connect a 2.2-µF capacitor and a transient-voltage suppressor (TVS) to ground and 5.1 kΩ to OUT.
CS	6	O	Linear cable compensation current. Connect to divider resistor of front-end dc-dc converter.
CTL1	8	I	Logic-level control input for controlling the charging mode and the signal switches; see the Device Truth Table (TT).
CTL2	9	I	Logic-level control input for controlling the charging mode and the signal switches; see the Device Truth Table (TT).
DM_IN	14	I/O	D– data line to downstream connector
DM_OUT	4	I/O	D– data line to upstream USB host controller
DP_IN	13	I/O	D+ data line to downstream connector
DP_OUT	5	I/O	D+ data line to upstream USB host controller
EN	7	I	Logic-level control input for turning the power and signal switches on or off. When EN is low, the device is disabled, and the signal and power switches are OFF.
$\overline{\text{FAULT}}$	18	O	Active-low, open-drain output, asserted during overtemperature, overcurrent, and overvoltage conditions.
GND	11	—	Ground connection; should be connected externally to the thermal pad.
ILIM_HI	20	I	External resistor used to set the high current-limit threshold.
ILIM_LO	19	I	External resistor used to set the low current-limit threshold and the load-detection current threshold.
IMON	1	O	This pin sources a scaled-down ratio of current through the internal FET. A resistor from this pin to GND converts current to proportional voltage; used as an analog current monitor.
IN	2,3	PWR	Input supply voltage; connect a 0.1-µF or greater ceramic capacitor from IN to GND as close to the IC as possible.
OUT	15,16	PWR	Power-switch output
OVP_SEL	10	I	Logic-level control input for choosing the OUT overvoltage threshold. When OVP_SEL is low, $V_{(OV\_OUT\_LOW)}$ is active. When OVP_SEL is high, $V_{(OV\_OUT\_HIGH)}$ is active.
$\overline{\text{STATUS}}$	17	O	Active-low open-drain output, asserted in load-detect conditions
Thermal pad	—	—	Thermal pad on the bottom of the package

(1) I = Input, O = Output, I/O = Input and output, PWR = Power

6 Specifications

6.1 Absolute Maximum Ratings

Voltages are with respect to GND unless otherwise noted(1)

			MIN	MAX	UNIT
	Voltage range	CS, CTL1, CTL2, EN, $\overline{\text{FAULT}}$, ILIM_HI, ILIM_LO, IN, IMON, OVP_SEL, $\overline{\text{STATUS}}$	–0.3	7	V
		DM_OUT, DP_OUT	–0.3	5.7	
		BIAS, DM_IN, DP_IN, OUT	–0.3	18	
	Continuous current	DM_IN to DM_OUT or DP_IN to DP_OUT	–100	100	mA
		OUT	Internally limited		
I_{SRC}	Continuous output source current	ILIM_HI, ILIM_LO, IMON	Internally limited		A
I_{SNK}	Continuous output sink current	$\overline{\text{FAULT}}$, $\overline{\text{STATUS}}$		25	mA
		CS	Internally limited		A
T_J	Operating junction temperature		–40	Internally limited	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2 000(2)	V
		Charged-device model (CDM), per AEC Q100-011	±750(3)	
		IEC 61000-4-2 contact discharge, DP_IN and DM_IN(4)	±8 000	
		IEC 61000-4-2 air discharge, DP_IN and DM_IN(4)	±15 000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The passing level per AEC-Q100 Classification H2.
(3) The passing level per AEC-Q100 Classification C5
(4) Surges per IEC 61000-4-2, level 4, 1999 applied from DP_IN and DM_IN to output ground of the TPS254900Q1EVM-817 (SLUUBI0) evaluation module.

6.3 Recommended Operating Conditions

Voltages are with respect to GND unless otherwise noted.

			MIN	NOM	MAX	UNIT
$V_{(IN)}$	Supply voltage	IN	4.5		6.5	V
	Input voltage	CTL1, CTL2, EN, OVP_SEL	0		6.5	V
		DM_IN, DM_OUT, DP_IN, DP_OUT	0		3.6	V
$I_{(OUT)}$	Output continuous current	OUT (–40°C ≤ T_A ≤ 85°C)			3	A
		DM_IN to DM_OUT or DP_IN to DP_OUT	–30		30	mA
	Continuous output sink current	$\overline{\text{FAULT}}$, $\overline{\text{STATUS}}$			10	mA
$R_{(ILIM\_xx)}$	Current-limit-set resistors		14.3		1000	kΩ
T_J	Operating junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS254900-Q1 RVC (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted, –40°C ≤ T_J ≤ 125°C and 4.5 V ≤ $V_{(IN)}$ ≤ 6.5 V, $V_{(EN)}$ = $V_{(CTL1)}$ = $V_{(CTL2)}$ = $V_{(IN)}$, $R_{(FAULT)}$ = $R_{(STATUS)}$ = 10 kΩ, $R_{(IMON)}$ = 2.55 kΩ, $R_{(ILIM\_HI)}$ = 19.1 kΩ, $R_{(ILIM\_LO)}$ = 80.6 kΩ. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT – POWER SWITCH						
$r_{DS(on)}$	On-resistance[1]	T_J = 25°C		45	55	mΩ
		–40°C ≤ T_J ≤ 85°C		45	69	
		–40°C ≤T_J ≤ 125°C		45	77	
I_{lkg}	Reverse leakage current	V_{OUT} = 6.5 V, V_{IN} = V_{EN} = 0 V, –40°C ≤ T_J ≤ 85°C, measure $I_{(IN)}$		0.01	2	µA
OUT – DISCHARGE						
$R_{(DCHG)}$	Discharge resistance (mode change)		400	500	630	Ω
CTL1, CTL2, EN, OVP_SEL INPUTS						
	Input pin rising logic threshold voltage		1	1.35	2	V
	Input pin falling logic threshold voltage		0.85	1.15	1.65	V
	Hysteresis[2]			200		mV
	Input current	Pin voltage = 0 V or 6.5 V	–1		1	µA
CURRENT LIMIT						
I_{OS}	OUT short-circuit current limit	$R_{(ILIM\_LO)}$ = 210 kΩ	190	240	290	mA
		$R_{(ILIM\_LO)}$ = 80.6 kΩ	555	620	680	
		$R_{(ILIM\_LO)}$ = 21.5 kΩ	2145	2300	2460	
		$R_{(ILIM\_LO)}$ = 19.1 kΩ	2420	2590	2760	
		$R_{(ILIM\_HI)}$ = 18.2 kΩ	2545	2720	2895	
		$R_{(ILIM\_HI)}$ = 14.3 kΩ	3240	3455	3670	
		$R_{(ILIM\_HI)}$ shorted to GND	5000	6500	8000	
SUPPLY CURRENT						
$I_{(IN\_OFF)}$	Disabled IN supply current	$V_{(EN)}$ = 0 V, $V_{(OUT)}$ = 0 V, –40°C ≤ T_J ≤ 85°C, no 5.1-kΩ resistor (open) between BIAS and OUT		0.1	5	µA
$I_{(IN\_ON)}$	Enabled IN supply current	SDP mode (CTL1, CTL2 = 0, 1)		170	250	µA
		CDP mode (CTL1, CTL2 = 1, 1)		200	280	
		Client mode (CTL1, CTL2 = 0, 0)		120	210	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.
(2) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

Electrical Characteristics (continued)

Unless otherwise noted, –40°C ≤ T_J ≤ 125°C and 4.5 V ≤ $V_{(IN)}$ ≤ 6.5 V, $V_{(EN)}$ = $V_{(CTL1)}$ = $V_{(CTL2)}$ = $V_{(IN)}$, $R_{(FAULT)}$ = $R_{(STATUS)}$ = 10 kΩ, $R_{(IMON)}$ = 2.55 kΩ, $R_{(ILIM\_HI)}$ = 19.1 kΩ, $R_{(ILIM\_LO)}$ = 80.6 kΩ. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDERVOLTAGE LOCKOUT, IN						
$V_{(UVLO)}$	UVLO threshold voltage	IN rising	3.9	4.15	4.3	V
	Hysteresis(3)	T_J = 25°C		100		mV
$\overline{FAULT}$						
	Output low voltage	$I_{(FAULT)}$ = 1 mA			100	mV
	Off-state leakage	$V_{(FAULT)}$ = 6.5 V			2	µA
$\overline{STATUS}$						
	Output low voltage	$I_{(STATUS)}$ = 1 mA			100	mV
	Off-state leakage	$V_{(STATUS)}$ = 6.5 V			2	µA
THERMAL SHUTDOWN						
$T_{(OTSD2)}$	Thermal shutdown threshold		155			°C
$T_{(OTSD1)}$	Thermal shutdown threshold in current-limit		135			°C
	Hysteresis(3)			20		°C
LOAD DETECT (V_{CTL1} = V_{CTL2} = V_{IN})						
$I_{(LD)}$	I_{OUT} load detection threshold	$R_{(ILIM\_LO)}$ = 80.6 kΩ, rising load current	585	650	715	mA
	Hysteresis(3)			50		mA
DM_IN AND DP_IN OVERVOLTAGE PROTECTION						
$V_{(OV\_Data)}$	Protection trip threshold	DP_IN and DM_IN rising	3.7	3.9	4.15	V
	Hysteresis(3)			100		mV
$R_{(DCHG\_Data)}$	Discharge resistor after OVP(2)	DP_IN = DM_IN = 18 V, IN = 5 V or 0 V		200		kΩ
		DP_IN = DM_IN = 5 V, IN = 5 V		370		
		DP_IN = DM_IN = 5 V, IN = 0		390		
OUT OVERVOLTAGE PROTECTION						
$V_{(OV\_OUT\_LOW)}$	Protection trip threshold	OUT rising	5.65	6	6.35	V
	Hysteresis(3)			90		mV
$V_{(OV\_OUT\_HIGH)}$	Protection trip threshold	OUT rising	6.6	6.95	7.3	V
	Hysteresis(3)			130		mV
$R_{(DCHG\_OUT)}$	Discharge resistor	OUT = 18 V, IN = 5 V		55	85	kΩ
		OUT = 18 V, IN = 0		80	120	
CABLE COMPENSATION						
$I_{(CS)}$	Sink current	Load = 3 A, 2.5 V ≤ $V_{(CS)}$ ≤ 6.5 V	234	246	258	µA
		Load = 2.4 A, 2.5 V ≤ $V_{(CS)}$ ≤ 6.5 V	187	197	207	
		Load = 2.1 A, 2.5 V ≤ $V_{(CS)}$ ≤ 6.5 V	163	172	181	
		Load = 1 A, 2.5 V ≤ $V_{(CS)}$ ≤ 6.5 V	77	82	87	
CURRENT MONITOR OUTPUT (IMON)						
$I_{(IMON)}$	Source current	Load = 3 A, 0 ≤ $V_{(IMON)}$ ≤ 2.5 V	287	312	337	µA
		Load = 2.4 A, 0 ≤ $V_{(IMON)}$ ≤ 2.5 V	230	250	270	
		Load = 2.1 A, 0 ≤ $V_{(IMON)}$ ≤ 2.5 V	201	218	235	
		Load = 1 A, 0 ≤ $V_{(IMON)}$ ≤ 2.5 V	94	104	114	
		Load = 0.5 A, 0 ≤ $V_{(IMON)}$ ≤ 2.5 V	44	52	60	

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Electrical Characteristics (continued)

Unless otherwise noted, –40°C ≤ T_J ≤ 125°C and 4.5 V ≤ $V_{(IN)}$ ≤ 6.5 V, $V_{(EN)}$ = $V_{(CTL1)}$ = $V_{(CTL2)}$ = $V_{(IN)}$, $R_{(FAULT)}$ = $R_{(STATUS)}$ = 10 kΩ, $R_{(IMON)}$ = 2.55 kΩ, $R_{(ILIM\_HI)}$ = 19.1 kΩ, $R_{(ILIM\_LO)}$ = 80.6 kΩ. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-BANDWIDTH ANALOG SWITCH						
$R_{(HS\_ON)}$	DP and DM switch on-resistance	$V_{(DP\_OUT)}$ = $V_{(DM\_OUT)}$ = 0 V, $I_{(DP\_IN)}$ = $I_{(DM\_IN)}$ = 30 mA		3.2	6.5	Ω
		$V_{(DP\_OUT)}$ = $V_{(DM\_OUT)}$ = 2.4 V, $I_{(DP\_IN)}$ = $I_{(DM\_IN)}$ = –15 mA		3.8	7.6	
$\lvert\Delta R_{(HS\_ON)}\rvert$	Switch resistance mismatch between DP and DM channels	$V_{(DP\_OUT)}$ = $V_{(DM\_OUT)}$ = 0 V, $I_{(DP\_IN)}$ = $I_{(DM\_IN)}$ = 30 mA		0.05	0.15	Ω
		$V_{(DP\_OUT)}$ = $V_{(DM\_OUT)}$ = 2.4 V, $I_{(DP\_IN)}$ = $I_{(DM\_IN)}$ = –15 mA		0.05	0.15	
$C_{(IO\_OFF)}$	DP and DM switch off-state capacitance(4)	V_{EN} = 0 V, $V_{(DP\_IN)}$ = $V_{(DM\_IN)}$ = 0.3 V, Vac = 0.03 V_{PP} , f = 1 MHz		8.8		pF
$C_{(IO\_ON)}$	DP and DM switch on-state capacitance(4)	$V_{(DP\_IN)}$ = $V_{(DM\_IN)}$ = 0.3 V, Vac = 0.03 V_{PP}, f = 1 MHz		10.9		pF
	Off-state isolation(3)	$V_{(EN)}$ = 0 V, f = 250 MHz		8		dB
	On-state cross-channel isolation(4)	f = 250 MHz		30		dB
$I_{lkg(OFF)}$	Off-state leakage current	V_{EN} = 0 V, $V_{(DP\_IN)}$ = $V_{(DM\_IN)}$ = 3.6 V, $V_{(DP\_OUT)}$ = $V_{(DM\_OUT)}$ = 0 V, measure $I_{(DP\_OUT)}$ and $I_{(DM\_OUT)}$		0.1	1.5	µA
BW	Bandwidth (–3 dB)(4)	$R_{(L)}$ = 50 Ω		940		MHz
CHARGING DOWNSTREAM PORT DETECT						
$V_{(DM\_SRC)}$	DM_IN CDP output voltage	$V_{(DP\_IN)}$ = 0.6 V, –250 µA < $I_{(DM\_IN)}$ < 0 µA	0.5	0.6	0.7	V
$V_{(DAT\_REF)}$	DP_IN rising lower window threshold for $V_{(DM\_SRC)}$ activation		0.36		0.4	V
	Hysteresis(4)			50		mV
$V_{(LGC\_SRC)}$	DP_IN rising upper window threshold for VDM_SRC de-activation		0.8		0.88	V
$V_{(LGC\_SRC\_HYS)}$	Hysteresis(4)			100		mV
$I_{(DP\_SINK)}$	DP_IN sink current	$V_{(DP\_IN)}$ = 0.6 V	40	75	100	µA

(4) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

6.6 Switching Characteristics

Unless otherwise noted –40°C ≤ T_J ≤ 125°C and 4.5 V ≤ $V_{(IN)}$ ≤ 6.5 V, $V_{(EN)}$ = $V_{(IN)}$, $V_{(CTL1)}$ = $V_{(CTL2)}$ = $V_{(IN)}$. $R_{(FAULT)}$ = $R_{(STATUS)}$ = 10 kΩ, $R_{(IMON)}$ = 2.55 KΩ, $R_{(ILIM\_HI)}$ = 19.1 kΩ, $R_{(ILIM\_LO)}$ = 80.6 kΩ. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	OUT voltage rise time	$V_{(IN)}$ = 5 V, $C_{(L)}$ = 1 µF, $R_{(L)}$ = 100 Ω	1.05	1.75	3.1	ms
t_f	OUT voltage fall time		0.27	0.47	0.82	ms
t_{on}	OUT voltage turnon time	$V_{(IN)}$ = 5 V, $C_{(L)}$ = 1 µF, $R_{(L)}$ = 100 Ω		7.5	11	ms
t_{off}	OUT voltage turnoff time			2.7	5	ms
$t_{(DCHG\_S)}$	Discharge hold time (mode change)	Time $V_{(OUT)}$ < 0.7 V	1.1	2	2.9	s
$t_{(IOS)}$	OUT short-circuit response time (1)	$V_{(IN)}$ = 5 V, $R_{(SHORT)}$ = 50 mΩ		2		µs
$t_{(OC\_OUT\_FAULT)}$	OUT $\overline{FAULT}$ deglitch time	Bidirectional deglitch applicable to current-limit condition only (no deglitch assertion for OTSD)	5.5	8.5	11.5	ms
t_{pd}	Analog switch propagation delay (1)	$V_{(IN)}$ = 5 V		0.14		ns
$t_{(SK)}$	Analog switch skew between opposite transitions of the same port (t_{PHL} – t_{PLH}) (1)	$V_{(IN)}$ = 5 V		0.02		ns
$t_{(LD\_SET)}$	Load-detect set time	$V_{(IN)}$ = 5 V	120	210	280	ms
$t_{(LD\_RESET)}$	Load-detect reset time	$V_{(IN)}$ = 5 V	1.8	3	4.2	s
$t_{(OV\_Data)}$	DP_IN and DM_IN overvoltage protection response time			5		µs
$t_{(OV\_OUT)}$	OUT overvoltage protection response time			0.3		µs
$t_{(OV\_D\_FAULT)}$	DP_IN and DM_IN $\overline{FAULT}$-asserted degltich time		11	16	23	ms
	OUT $\overline{FAULT}$-asserted degltich time		11	16	23	ms

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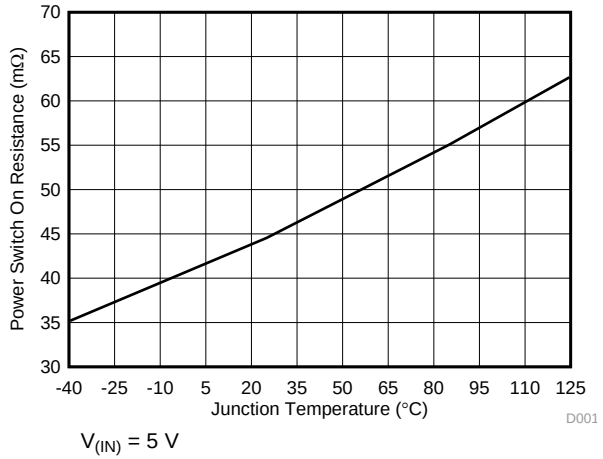
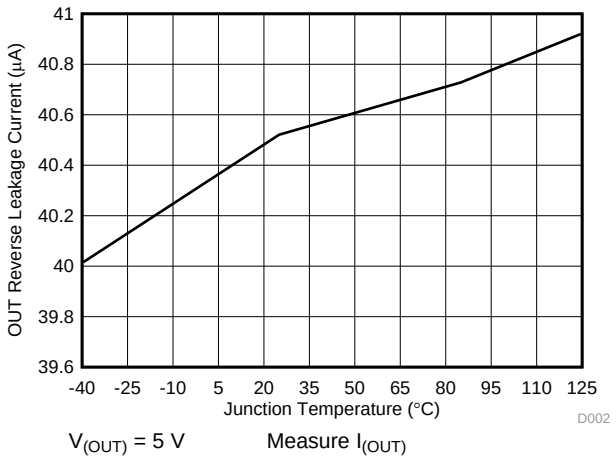
6.7 Typical Characteristics

T_A = 25°C, $V_{(IN)}$ = 5 V, $V_{(EN)}$ = 5 V, $V_{(CTL1)}$ = $V_{(CTL2)}$ = 5 V, $\overline{FAULT}$ and $\overline{STATUS}$ connect to $V_{(IN)}$ via a 10-kΩ pullup resistor (unless stated otherwise)



$V_{(IN)}$ = 5 V

Figure 1. Power Switch On-Resistance vs Temperature



$V_{(OUT)}$ = 5 V Measure $I_{(OUT)}$

Figure 2. Reverse Leakage Current vs Temperature

Typical Characteristics (continued)

T_A = 25°C, $V_{(IN)}$ = 5 V, $V_{(EN)}$ = 5 V, $V_{(CTL1)}$ = $V_{(CTL2)}$ = 5 V, $\overline{FAULT}$ and $\overline{STATUS}$ connect to $V_{(IN)}$ via a 10-kΩ pullup resistor (unless stated otherwise)

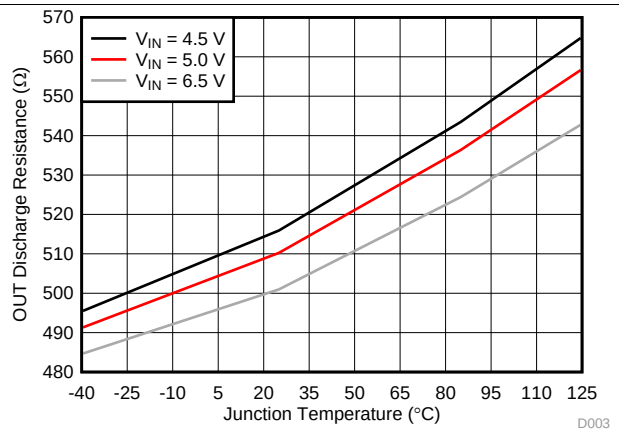


Figure 3. OUT Discharge Resistance (Mode Change) vs Temperature

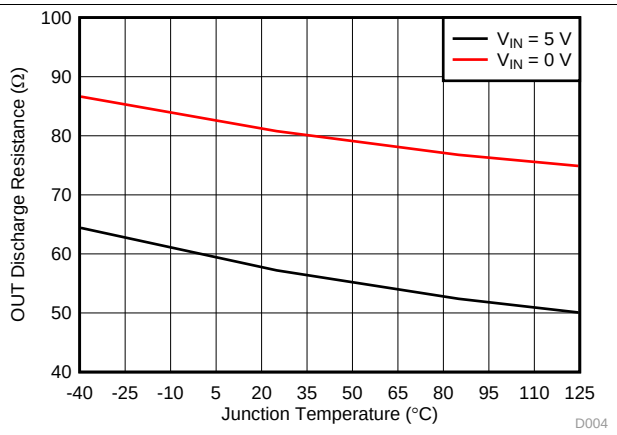


Figure 4. OUT Discharge Resistance (OVP) vs Temperature

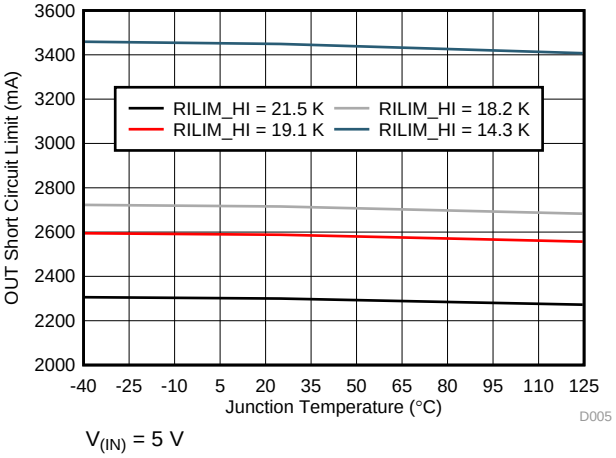


Figure 5. OUT Short-Circuit Current Limit vs Temperature I

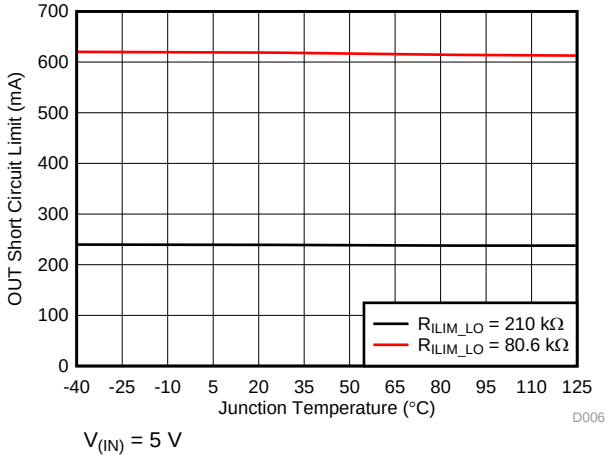


Figure 6. OUT Short-Circuit Current Limit vs Temperature II

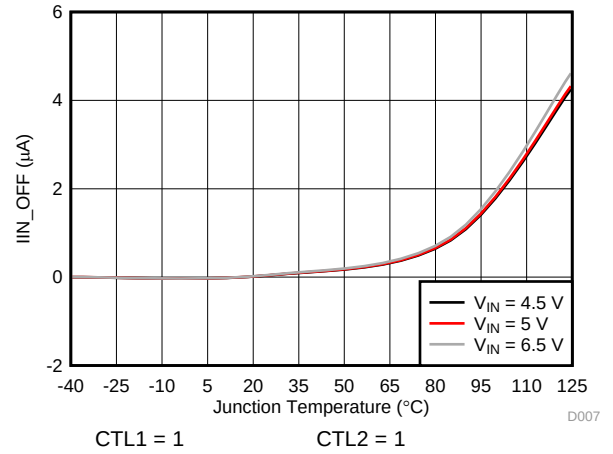


Figure 7. Disabled IN Supply Current vs Temperature

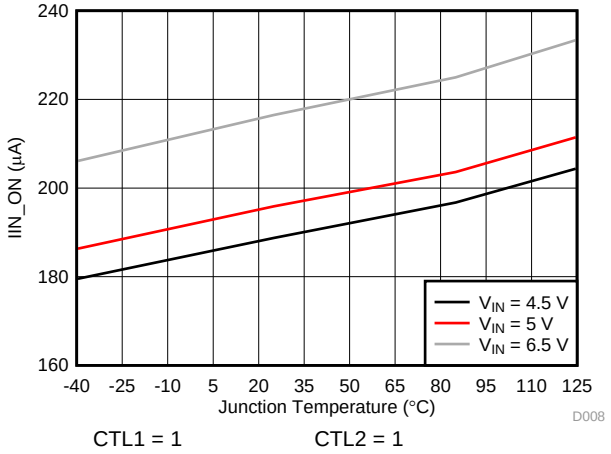


Figure 8. Enabled IN Supply Current – CDP (11) vs Temperature

Typical Characteristics (continued)

T_A = 25°C, $V_{(IN)}$ = 5 V, $V_{(EN)}$ = 5 V, $V_{(CTL1)}$ = $V_{(CTL2)}$ = 5 V, $\overline{FAULT}$ and $\overline{STATUS}$ connect to $V_{(IN)}$ via a 10-kΩ pullup resistor (unless stated otherwise)

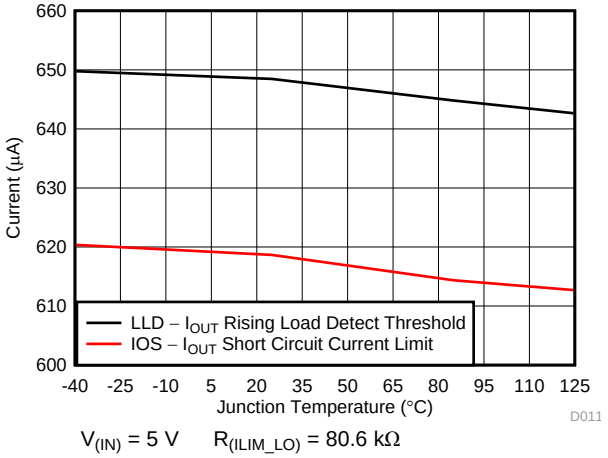


Figure 9. $I_{(OUT)}$ Rising Load-Detect Threshold and OUT Short-Circuit Limit vs Temperature

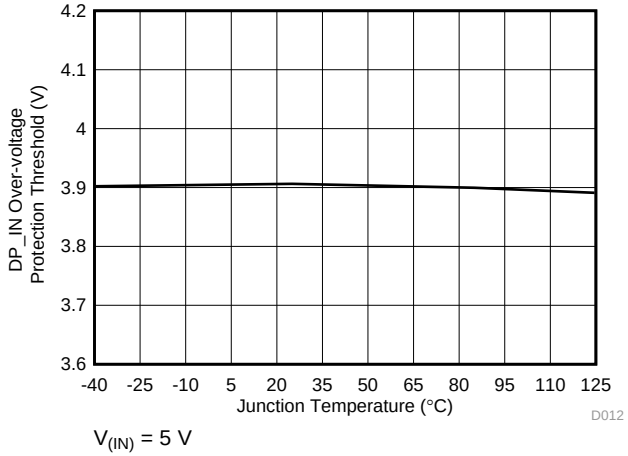


Figure 10. DP_IN Overvoltage Protection Threshold vs Temperature

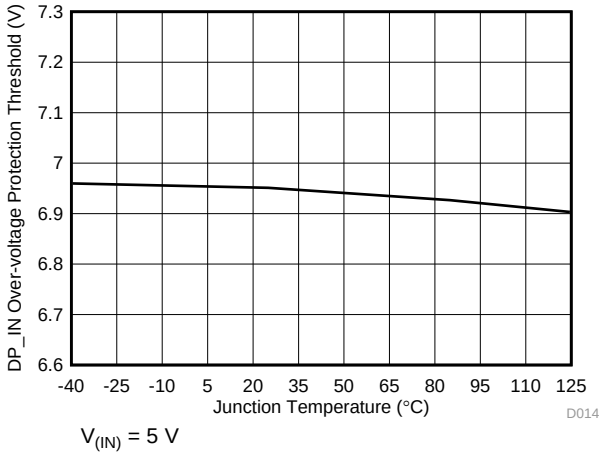


Figure 11. OUT Overvoltage Protection Threshold vs Temperature

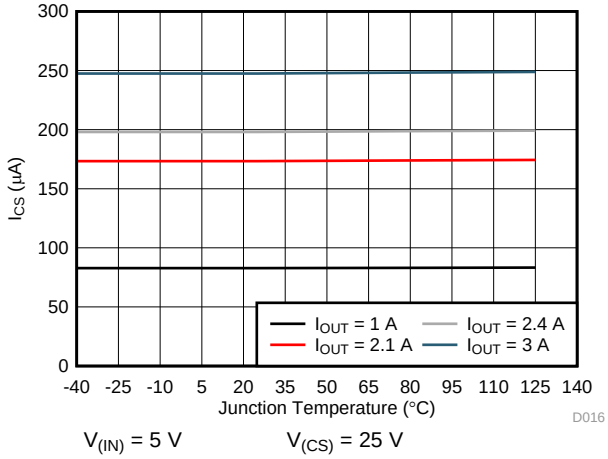


Figure 12. $I_{(CS)}$ vs Temperature

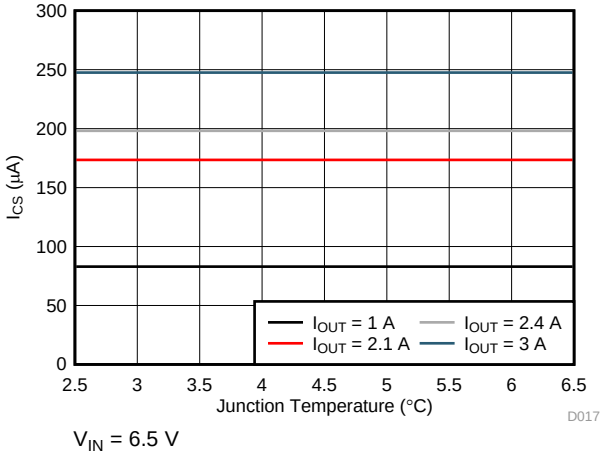


Figure 13. $I_{(CS)}$ vs $V_{(CS)}$ Voltage

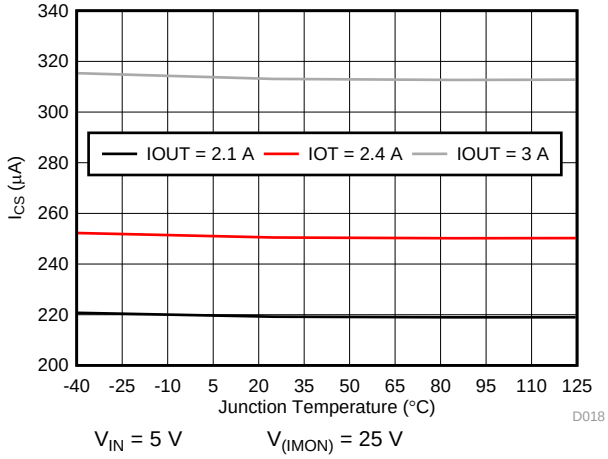
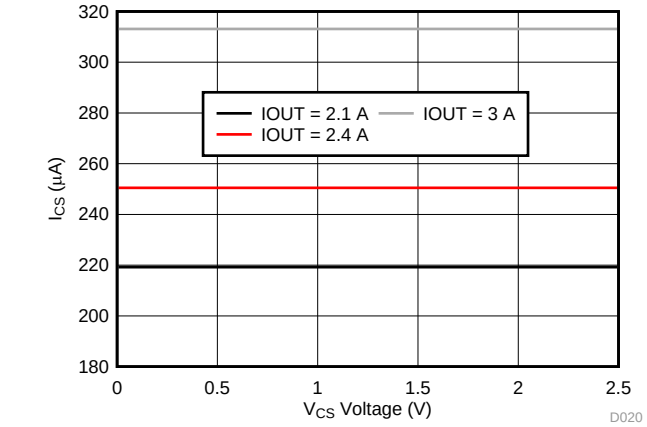


Figure 14. $I_{(IMON)}$ vs Temperature

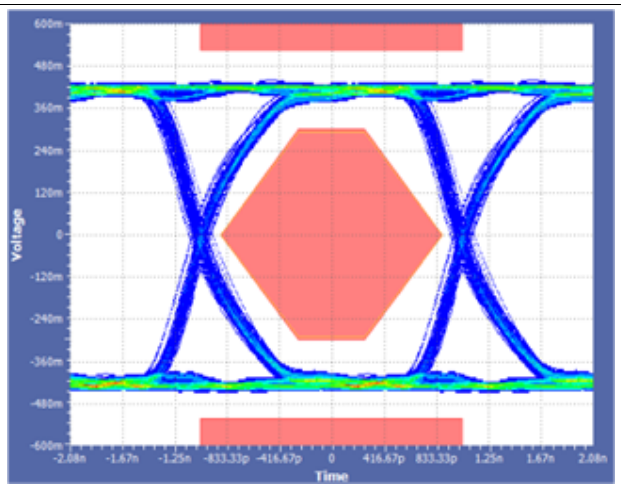
Typical Characteristics (continued)

T_A = 25°C, $V_{(IN)}$ = 5 V, $V_{(EN)}$ = 5 V, $V_{(CTL1)}$ = $V_{(CTL2)}$ = 5 V, $\overline{FAULT}$ and $\overline{STATUS}$ connect to $V_{(IN)}$ via a 10-kΩ pullup resistor (unless stated otherwise)



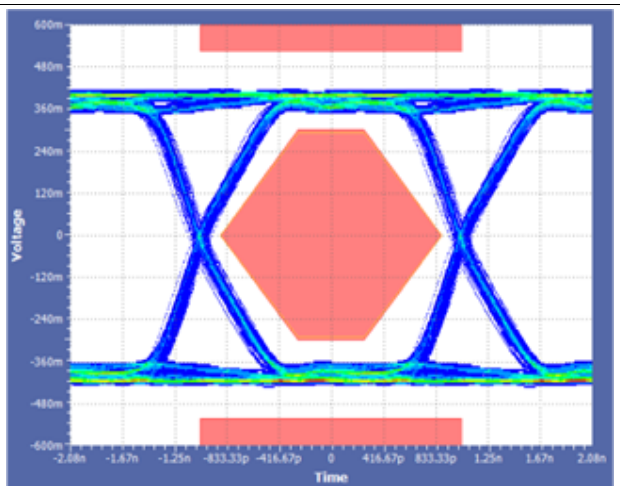
V_{IN} = 4.5 V

Figure 15. $I_{(IMON)}$ vs $V_{(CS)}$ Voltage



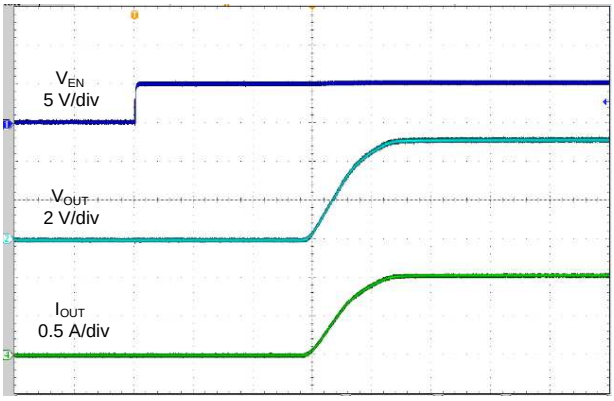
Measured on EVM with 10-cm cable

Figure 16. Bypassing the TPS254900-Q1 Data Switch



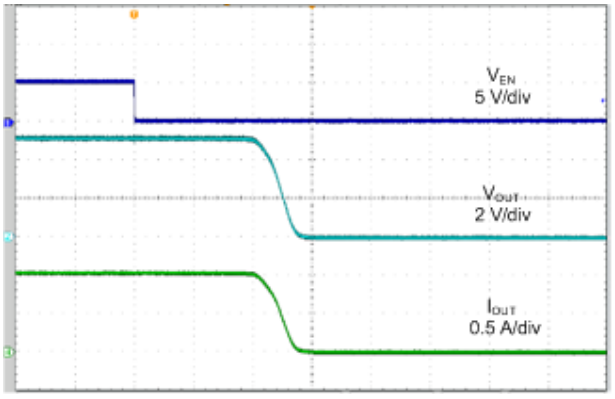
Measured on EVM with 10-cm cable

Figure 17. Through the TPS254900-Q1 Data Switch



$R_{(LOAD)}$ = 5 Ω $C_{(LOAD)}$ = 10 µF t = 2 ms/div

Figure 18. Turnon Response

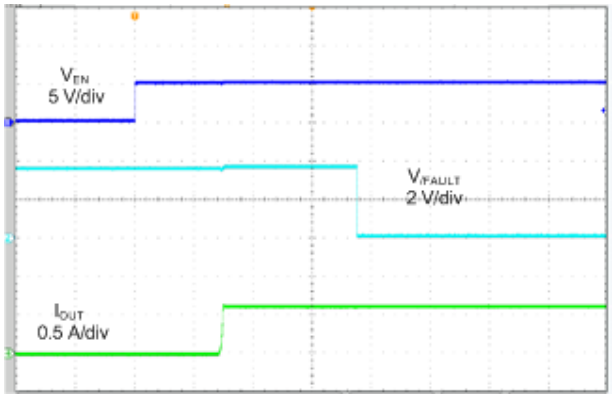


$R_{(LOAD)}$ = 5 Ω $C_{(LOAD)}$ = 10 µF t = 1 ms/div

Figure 19. Turnoff Response

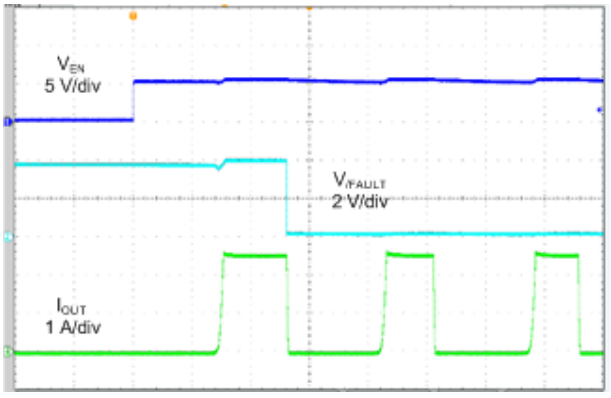
Typical Characteristics (continued)

T_A = 25°C, $V_{(IN)}$ = 5 V, $V_{(EN)}$ = 5 V, $V_{(CTL1)}$ = $V_{(CTL2)}$ = 5 V, $\overline{FAULT}$ and $\overline{STATUS}$ connect to $V_{(IN)}$ via a 10-kΩ pullup resistor (unless stated otherwise)



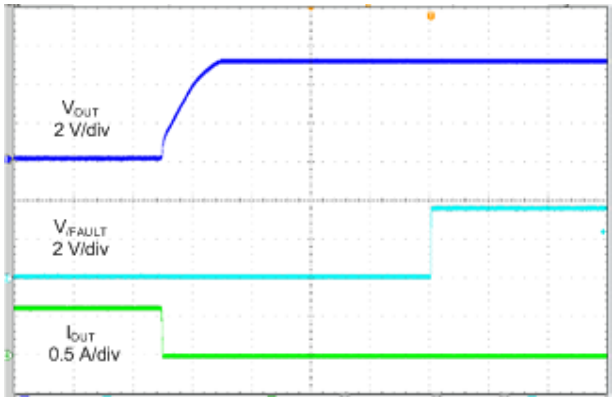
$R_{(ILIM\_LO)}$ = 80.6 kΩ t = 4 ms/div

Figure 20. Enable Into Short (SDP)



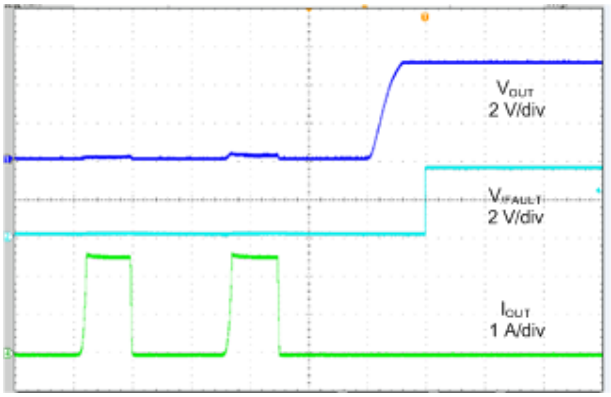
$R_{(ILIM\_HI)}$ = 19.1 kΩ t = 4 ms/div

Figure 21. Enable Into Short (CDP) – Thermal Cycling



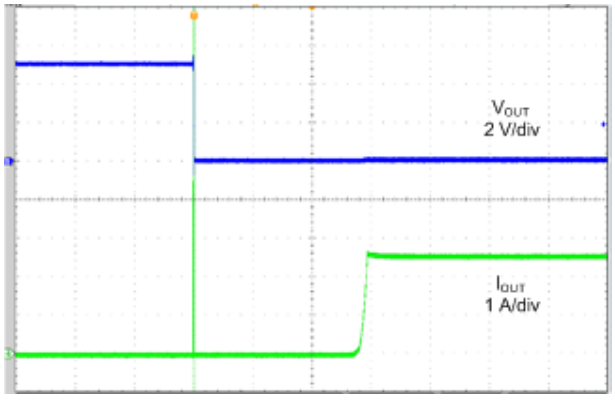
$R_{(ILIM\_LO)}$ = 80.6 kΩ t = 2 ms/div

Figure 22. Short Circuit to No Load (SDP)



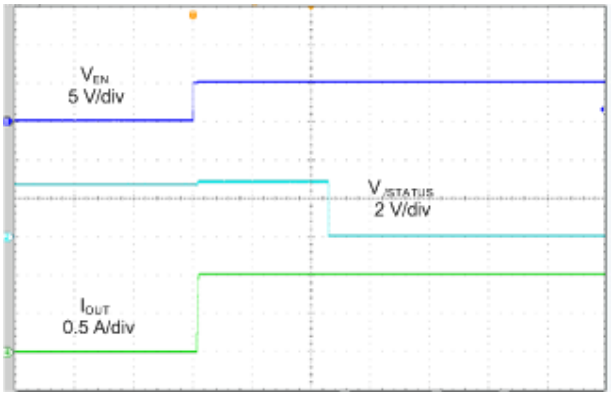
$R_{(ILIM\_HI)}$ = 19.1 kΩ t = 4 ms/div

Figure 23. Short Circuit to No Load (CDP)



$R_{(ILIM\_HI)}$ = 19.1 kΩ R(short) = 50 mΩ t = 2 ms/div

Figure 24. Hot Short

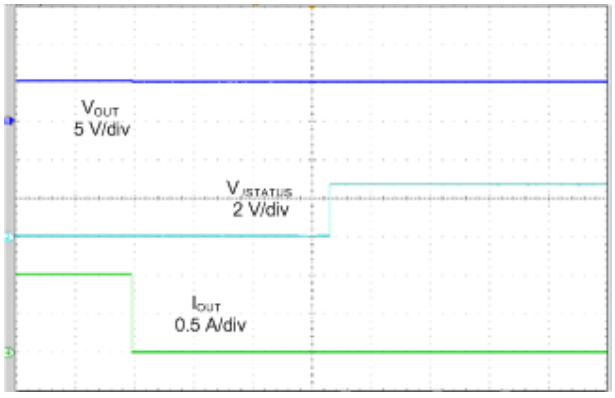


$R_{(ILIM\_LO)}$ = 80.6 kΩ t = 100 ms/div

Figure 25. Load-Detection Set Time

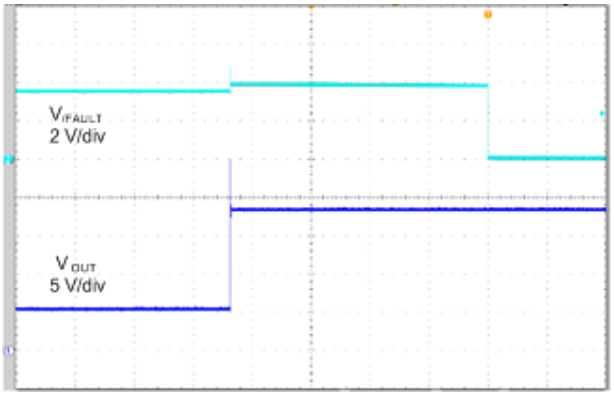
Typical Characteristics (continued)

T_A = 25°C, $V_{(IN)}$ = 5 V, $V_{(EN)}$ = 5 V, $V_{(CTL1)}$ = $V_{(CTL2)}$ = 5 V, $\overline{\text{FAULT}}$ and $\overline{\text{STATUS}}$ connect to $V_{(IN)}$ via a 10-kΩ pullup resistor (unless stated otherwise)



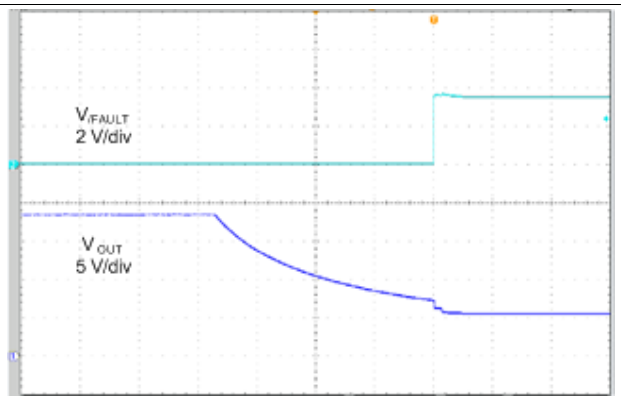
$R_{(ILIM\_LO)}$ = 80.6 kΩ t = 1 s/div

Figure 26. Load-Detection Reset Time



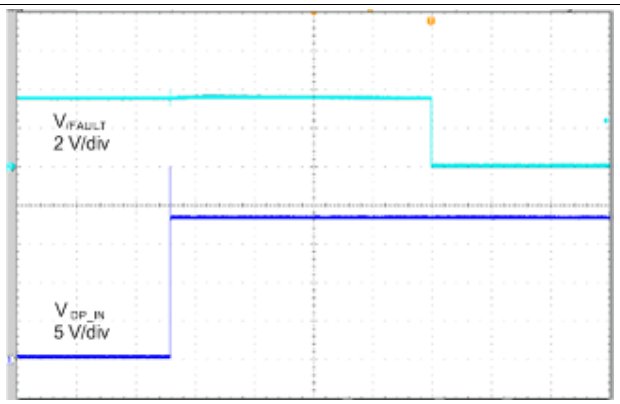
t = 4 ms/div

Figure 27. OUT Short to Battery



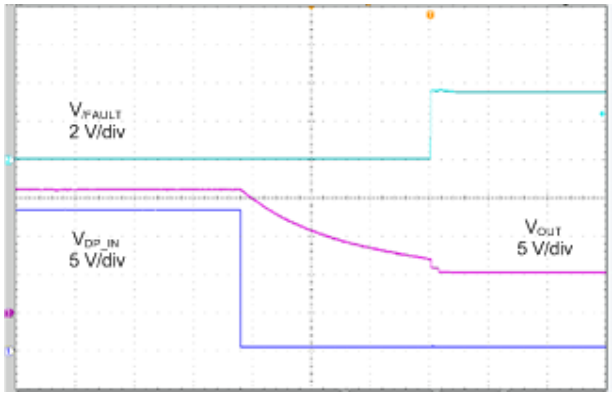
t = 100 ms/div

Figure 28. OUT Short-to-Battery Recovery



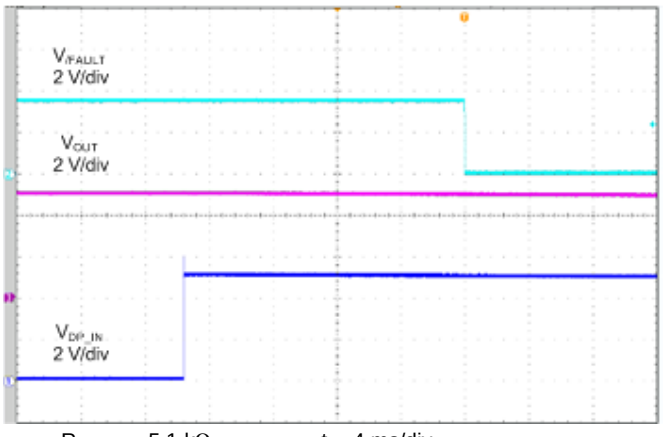
t = 4 ms/div

Figure 29. DP_IN Short to Battery



$R_{(BIAS)}$ = 5.1 kΩ t = 100 ms/div

Figure 30. DP_IN Short-to-Battery Recovery



$R_{(BIAS)}$ = 5.1 kΩ t = 4 ms/div

Figure 31. DP_IN Short to V_{BUS}

Typical Characteristics (continued)

T_A = 25°C, $V_{(IN)}$ = 5 V, $V_{(EN)}$ = 5 V, $V_{(CTL1)}$ = $V_{(CTL2)}$ = 5 V, $\overline{FAULT}$ and $\overline{STATUS}$ connect to $V_{(IN)}$ via a 10-kΩ pullup resistor (unless stated otherwise)

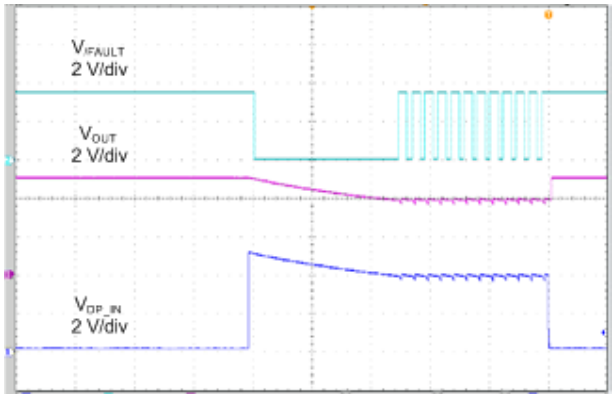


Figure 32. DP_IN Short-to-V_{BUS} and Recovery

Figure 33. Data Transmission Characteristics vs Frequency

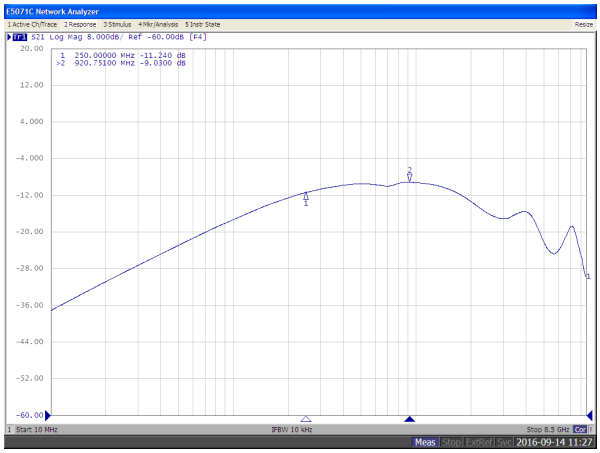


Figure 34. Off-State Data-Switch Isolation vs Frequency

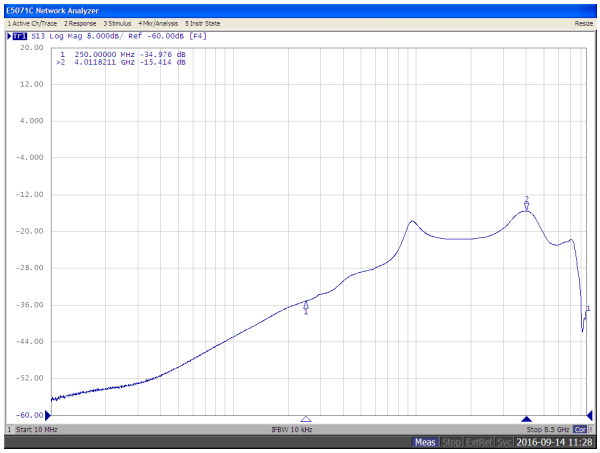


Figure 35. On-State Cross-Channel Isolation vs Frequency

7 Parameter Measurement Information

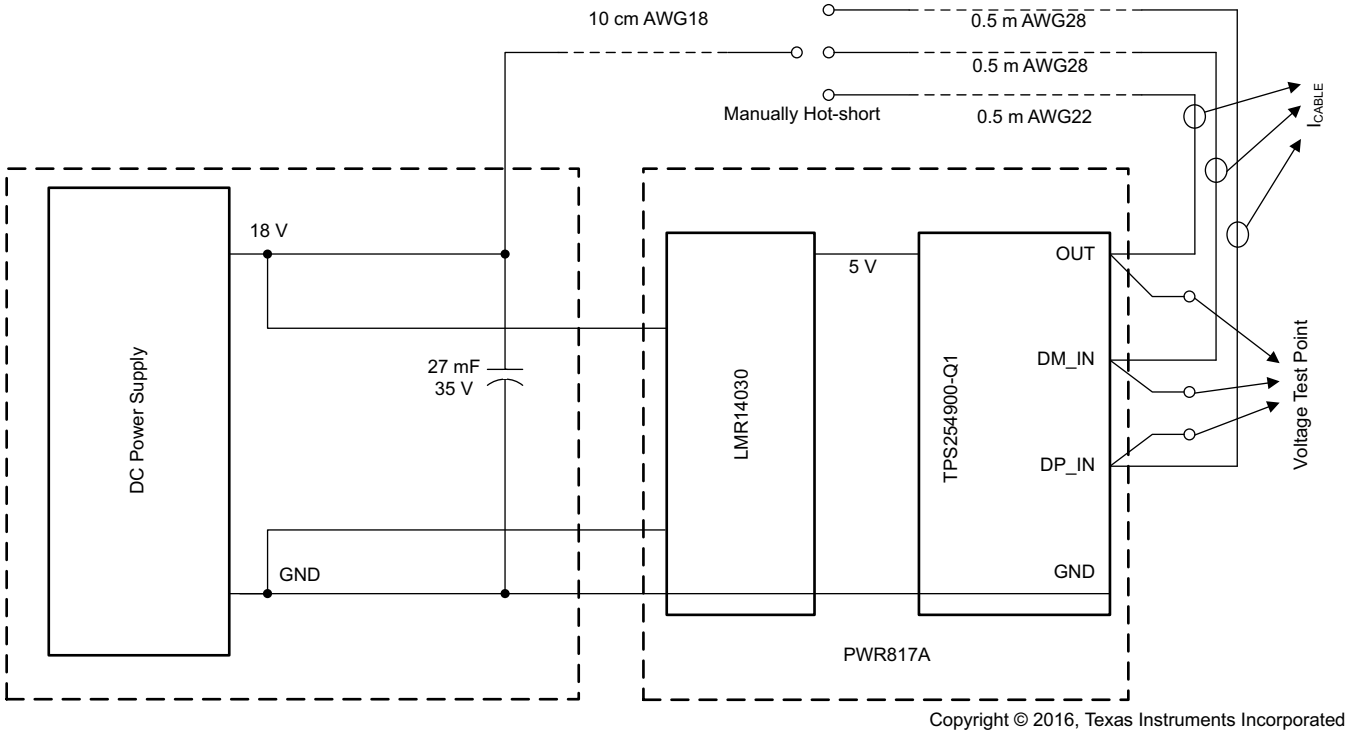


Figure 36. Short-to-Battery System Test Setup

8 Detailed Description

8.1 Overview

The TPS254900-Q1 device is a USB charging controller and power switch which integrates D+ and D– short-to-battery protection, cable compensation, current monitor (IMON), and IEC ESD protection suitable for automotive USB charging and USB port protection applications.

The integrated power distribution switch uses N-channel MOSFETs suitable for applications where short circuits or heavy capacitive loads will be encountered. The device allows the user to adjust the current-limit thresholds using external resistors. The device enters constant-current mode when the load exceeds the current-limit threshold.

The TPS254900-Q1 device provides V_{BUS}, D+, and D– short-to-battery protection. This protects the upstream voltage regulator, automotive processor, and hub when these pins are exposed to fault conditions.

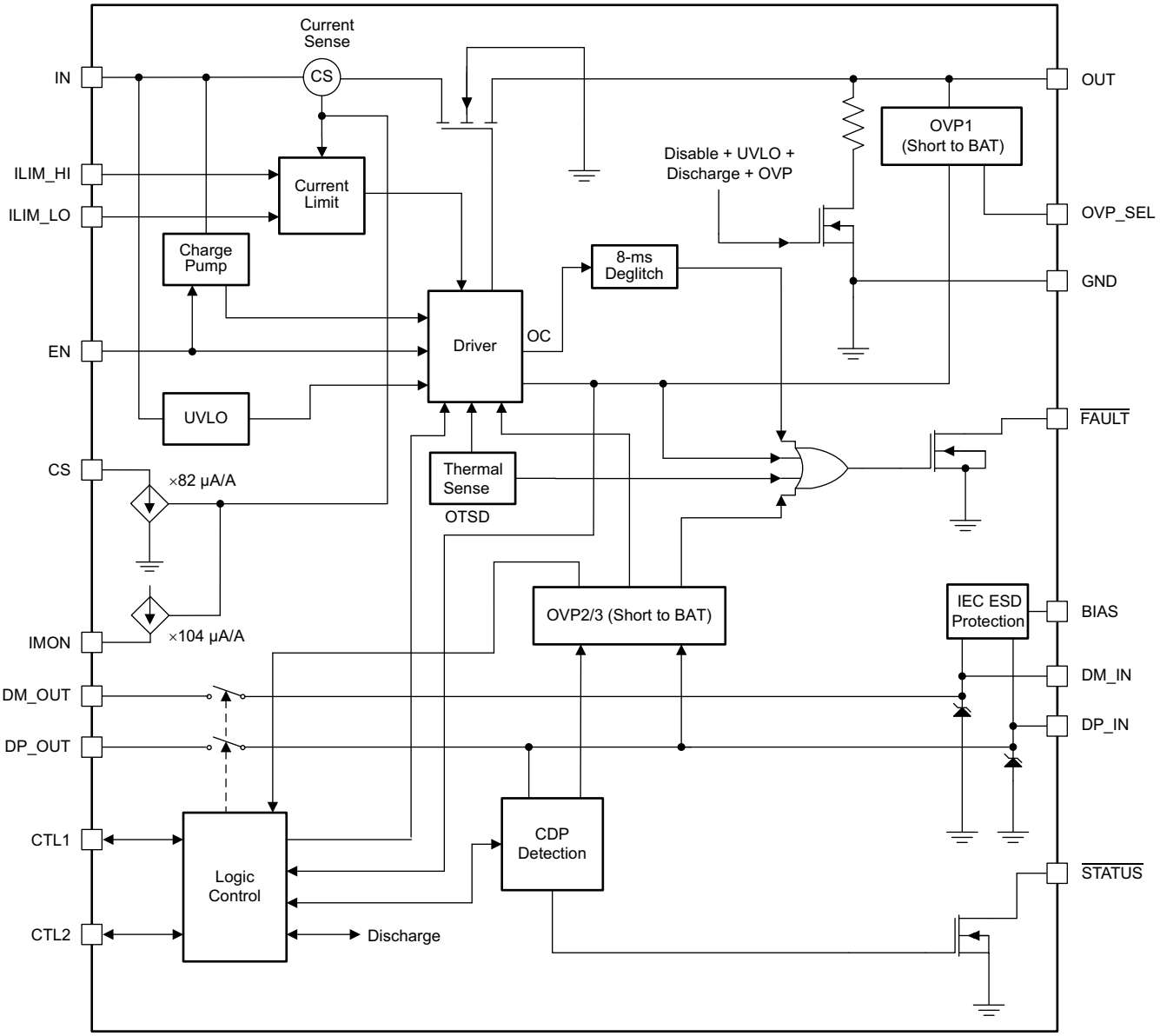
The device also integrates CDP mode, defined in the BC1.2 specification, to enable up to 1.5-A fast charging of most portable devices during data communication.

The TPS254900-Q1 device integrates a cable compensation (CS) feature to compensate for long-cable voltage drop. This keeps the remote USB port output voltage constant to enhance the user experience under high-current charging conditions.

The TPS254900-Q1 device provides a current-monitor function (IMON) by connecting a resistor from the IMON pin to GND to provide a positive voltage linearly with load current. This can be used for system power or dynamic power management.

Additionally, the device provides ESD protection up to ±8 kV (contact discharge) and ±15 kV (air discharge) per IEC 61000-4-2 on DP_IN and DM_IN.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 $\overline{\text{FAULT}}$ Response

The device features an active-low, open-drain fault output. $\overline{\text{FAULT}}$ goes low when there is a fault condition. Fault detection includes overtemperature, overcurrent, or overvoltage on V_{BUS}, DP_IN and DM_IN. Connect a 10-kΩ pullup resistor from $\overline{\text{FAULT}}$ to IN.

Table 1 summarizes the conditions that generate a fault and actions taken by the device.

Feature Description (continued)

Table 1. Fault Conditions

EVENT	CONDITION	ACTION
Overvoltage on the data lines	$V_{(DP\_IN)}$ or $V_{(DM\_IN)}$ > 3.9 V	The device immediately shuts off the USB data switches and the internal power switch. The fault indicator asserts with a 16-ms deglitch, and deasserts without deglitch.
Overvoltage on $V_{(OUT)}$	$V_{(OUT)}$ > 6 V or 6.95 V	The device immediately shuts off the internal power switch and the USB data switches. The fault indicator asserts with a 16-ms deglitch and deasserts without deglitch.
Overcurrent on $V_{(OUT)}$	$I_{(OUT)} > I_{(OS)}$	The device regulates switch current at $I_{(OS)}$ until thermal cycling occurs. The fault indicator asserts and deasserts with an 8-ms deglitch (the device does not assert $\overline{FAULT}$ on overcurrent in SDP1 mode).
Overtemperature	T_J > OTSD2 in non-current-limited or T_J > OTSD1 in current-limited mode.	The device immediately shuts off the internal power switch and the USB data switches. The fault indicator asserts immediately when the junction temperature exceeds OTSD2 or OTSD1 while in a current-limiting condition. The device has a thermal hysteresis of 20°C.

8.3.2 Cable Compensation

When a load draws current through a long or thin wire, there is an IR drop that reduces the voltage delivered to the load. In the vehicle from the voltage regulator 5-V output to the V_{PD_IN} (input voltage of portable device), the total resistance of power switch $r_{DS(on)}$ and cable resistance causes an IR drop at the PD input. So the charging current of most portable devices is less than their expected maximum charging current.

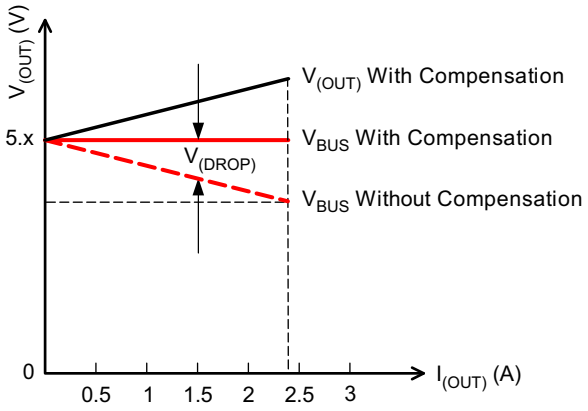


Figure 37. Voltage Drop

TPS254900-Q1 device detects the load current and applies a proportional sink current that can be used to adjust the output voltage of the upstream regulator to compensate for the IR drop in the charging path. The gain $G_{(CS)}$ of the sink current proportional to load current is 82 µA/A.

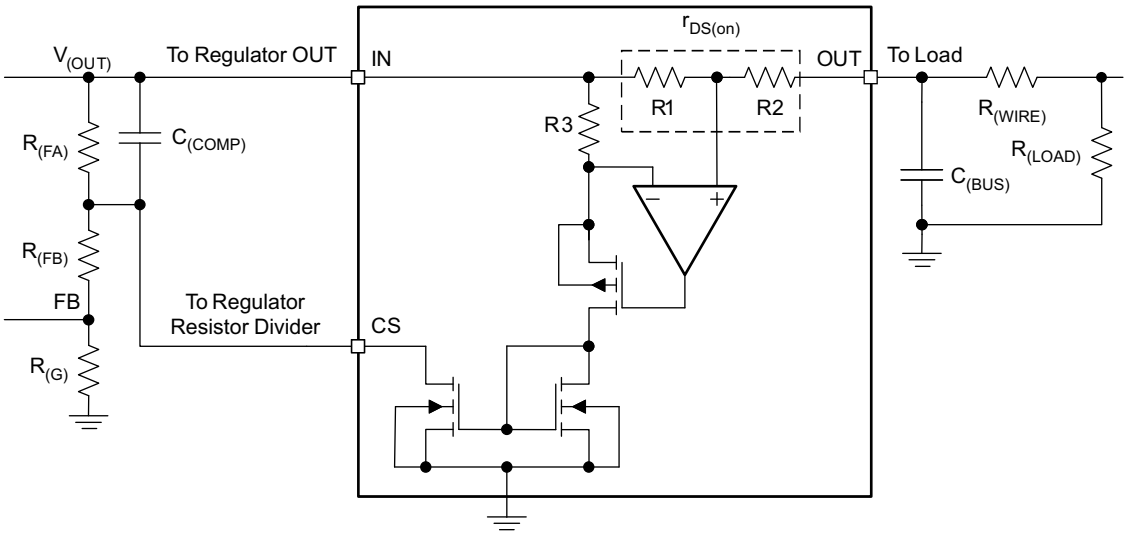


Figure 38. Cable Compensation Equivalent Circuit

8.3.2.1 Design Procedure

To start the procedure, the total resistance, including the power switch $r_{DS(on)}$ and wire resistance $R_{(WIRE)}$, must be known.

1. Choose $R_{(G)}$ following the voltage-regulator feedback resistor-divider design guideline.
2. Calculate $R_{(FA)}$ according to Equation 1.

$$R_{FA} = (r_{DS(on)} + R_{(WIRE)}) / G_{(CS)} \quad (1)$$

3. Calculate $R_{(FB)}$ according to Equation 2.

$$R_{(FB)} = \frac{V_{(OUT)}}{V_{(FB)} / R_{(G)}} - R_{(G)} - R_{(FA)} \quad (2)$$

4. $C_{(COMP)}$ in parallel with $R_{(FA)}$ is required to stablilize $V_{(OUT)}$ when $C_{(BUS)}$ is large. Start with $C_{(COMP)} \geq 3 \times G_{(CS)} \times C_{(OUT)}$, then adjust $C_{(COMP)}$ to optimize the load transient of the voltage regulator output. $V_{(OUT)}$ stability should always be verified in the end application circuit.

8.3.3 D+ and D– Protection

D+ and D– protection consists of ESD and OVP (overvoltage protection). The DP_IN and DM_IN pins provide ESD protection up to ±15 kV (air discharge) and ±8 kV (contact discharge) per IEC 61000-4-2 (see the *ESD Ratings* section for test conditions).

The ESD stress seen at DP_IN and DM_IN is impacted by many external factors, like the parasitic resistance and inductance between ESD test points and the DP_IN and DM_IN pins. For air discharge, the temperature and humidity of the environment can cause some difference, so the IEC performance should always be verified in the end-application circuit.

The IEC ESD performance of the TPS254900-Q1 device depends on the capacitance connected from BIAS to GND. A 2.2-µF capacitor placed close to the BIAS pin is recommended. Connect the BIAS pin to OUT using a 5.1-kΩ resistor as a discharge path for the ESD stress.

OVP protection is provided for short-to-V_{BUS} or short-to-battery conditions in the vehicle harness, preventing damage to the upstream USB transceiver or hub. When the voltage on DP_IN or DM_IN exceeds 3.9 V (typical), the TPS254900-Q1 device quickly responds to block the high-voltage reverse connection to DP_OUT and DM_OUT. Overcurrent short-to-GND protection for D+ and D– is provided by the upstream USB transceiver.

8.3.4 V_{BUS} OVP Protection

The TPS254900-Q1 OUT pin can withstand up to 18 V. The internal MOSFET turns off quickly when a short-to-battery condition occurs.

The TPS254900-Q1 device has two OVP thresholds; one is 6 V (typical) and the other is 6.95 V (typical). Set the OVP threshold using the external OVP_SEL pin.

8.3.5 Output and D+ or D– Discharge

To allow a charging port to renegotiate current with a portable device, the TPS254900-Q1 device uses the OUT discharge function. During mode change, the TPS254900-Q1 device turns off the power switch while discharging OUT with a 500-Ω resistance, then turning back on the power switches to reassert the OUT voltage.

When an OVP condition occurs on DP_IN or DM_IN, the TPS254900-Q1 device enables an internal 200-kΩ discharge resistance from DP_IN to ground and from DM_IN to ground. The analog switches are also turned off. The TPS254900-Q1 device automatically disables the discharge paths and turns on the analog switches once the OVP condition is removed.

When an OVP condition occurs on OUT, the TPS254900-Q1 device turns on an internal discharge path (see Table 2 for the discharge resistance). The TPS254900-Q1 device automatically turns off the discharge path and turns on the power switch once the OVP condition is removed.

Table 2. OUT Discharge Resistance

VIN(1)	EN(1)	OVP(1)	OUT Discharge Resistance(2)
0	0	0	—
0	0	1	80 kΩ
0	1	0	—
0	1	1	80 kΩ
1	0	0	500 Ω
1	0	1	500 Ω or 55 kΩ
1	1	0	—
1	1	1	55 kΩ

(1) 0 = inactive, 1 = active
(2) — = no discharge resistance

8.3.6 Port Power Management (PPM)

PPM is the intelligent and dynamic allocation of power. PPM is for systems that have multiple charging ports but cannot power them all simultaneously.

8.3.6.1 Benefits of PPM

The benefits of PPM include the following:

- Delivers better user experience
- Prevents overloading of system power supply
- Allows for dynamic power limits based on system state
- Allows every port potentially to be a high-power charging port
- Allows for smaller power-supply capacity because loading is controlled

8.3.6.2 PPM Details

All ports are allowed to broadcast high-current charging. The current limit is based on ILIM_HI. The system monitors the $\overline{\text{STATUS}}$ pin to see when high-current loads are present. Once the allowed number of ports asserts $\overline{\text{STATUS}}$, the remaining ports are toggled to a non-charging port. The current limit of the non-charging port is based on the ILIM_LO setting. The non-charging ports are automatically toggled back to charging ports when a charging port deasserts $\overline{\text{STATUS}}$.

$\overline{\text{STATUS}}$ asserts in a charging port when the load current is above ILIM_LO + 30 mA for 210 ms (typical). $\overline{\text{STATUS}}$ deasserts in a charging port when the load current is below ILIM_LO – 20 mA for 3 seconds (typical).

8.3.6.3 Implementing PPM in a System With Two Charging Ports (CDP and SDP1)

Figure 39 shows the implementation of the two charging ports with data communication, each with a TPS254900-Q1 device and configured in CDP mode. In this example, the 5-V power supply for the two charging ports is rated at less than 3.5 A. Both TPS254900-Q1 devices have $R_{(ILIM)}$ chosen to correspond to the low (1-A) and high (2.4-A) current-limit setting for the port. In this implementation, the system can support only one of the two ports at 2.4-A charging current, whereas the other port is set to the SDP1 mode and I_{OS} corresponds to 1 A.

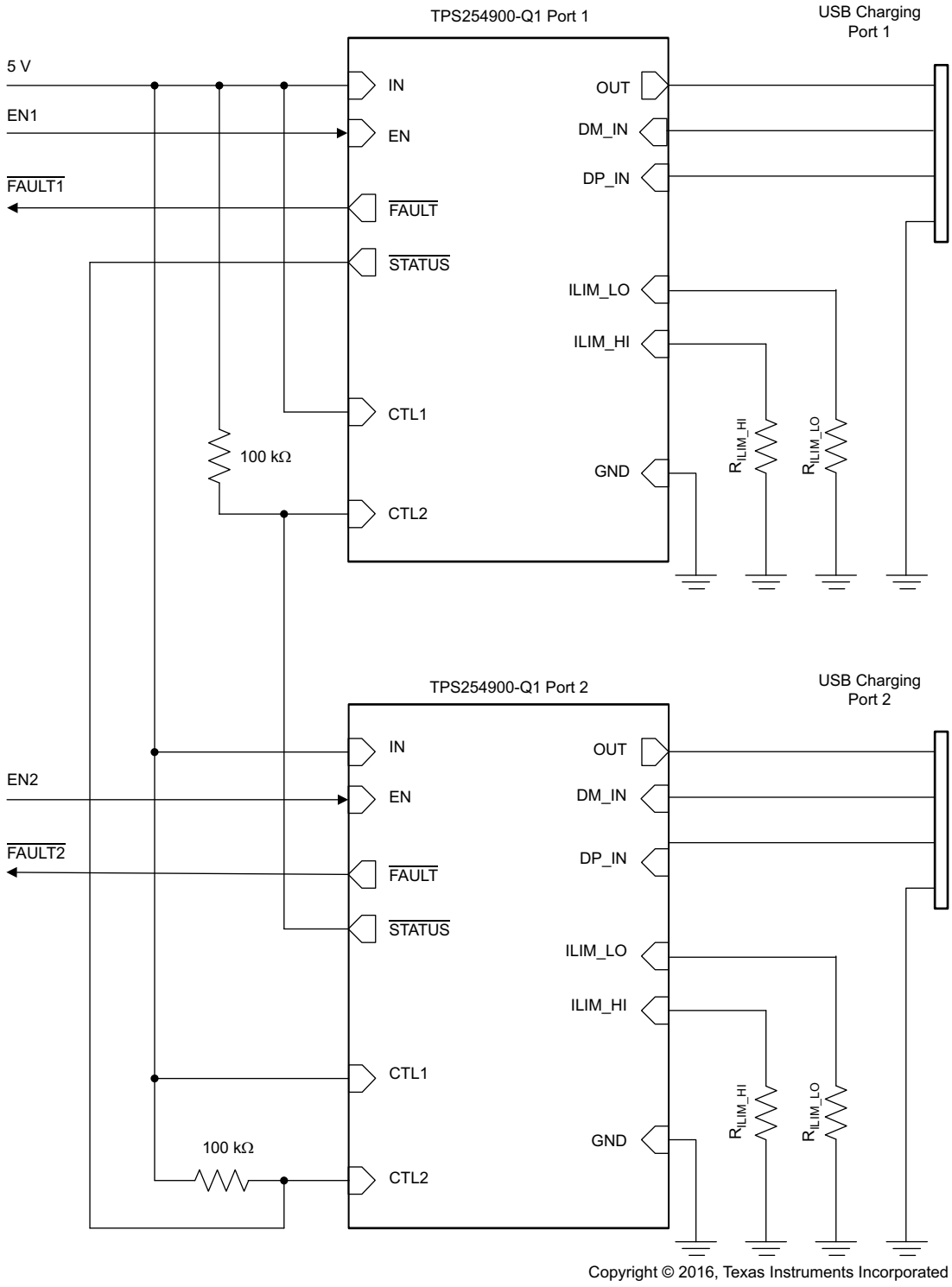


Figure 39. PPM Between CDP and SDP1

8.3.7 Overcurrent Protection

When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur. In the first condition, the output is shorted before the device is enabled or before the application of $V_{(IN)}$. The TPS254900-Q1 device senses the short and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents flow for 1 to 2 μs (typical) before the current-limit circuit reacts. The device operates in constant-current mode after the current-limit circuit has responded. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting. The device remains off until the junction temperature cools approximately 20°C and then restarts. The device continues to cycle on and off until the overcurrent condition is removed.

8.3.8 Undervoltage Lockout

The undervoltage-lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted oscillations on the output due to input voltage drop from large current surges.

8.3.9 Thermal Sensing

Two independent thermal-sensing circuits protect the TPS254900-Q1 device if the temperature exceeds recommended operating conditions. These circuits monitor the operating temperature of the power-distribution switch and disable operation. The power dissipation in the package is proportional to the voltage drop across the power switch, so the junction temperature rises during an overcurrent condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135ºC and the device is in current limit. The second thermal sensor turns off the power switch when the die temperature exceeds 155ºC regardless of whether the power switch is in current limit. Hysteresis is built into both thermal sensors, and the switch turns on after the device has cooled by approximately 20°C. The switch continues to cycle off and then on until the fault is removed. The open-drain false-reporting output, $\overline{FAULT}$, is asserted (low) during an overtemperature shutdown condition.

8.3.10 Current-Limit Setting

The TPS254900-Q1 has two independent current-limit settings that are each adjusted externally with a resistor. The ILIM_HI setting is adjusted with $R_{(ILIM\_HI)}$ connected between ILIM_HI and GND. The ILIM_LO setting is adjusted with $R_{(ILIM\_LO)}$ connected between ILIM_LO and GND. Consult the device truth table (Table 3) to see when each current limit is used. Both settings have the same relation between the current limit and the adjusting resistor.

The following equation calculates the value of resistor for adjusting the typical current limit:

$$I_{OS(nom)}\ (mA) = \frac{48687\ V}{R_{(ILIM\_xx)}^{0.9945}\ k\Omega} \tag{3}$$

Many applications require that the current limit meet specific tolerance limits. When designing to these tolerance limits, both the tolerance of the TPS254900-Q1 current limit and the tolerance of the external adjusting resistor must be taken into account. The following equations approximate the TPS254900-Q1 minimum and maximum current limits to within a few milliamperes and are appropriate for design purposes. The equations do not constitute part of TI's published device specifications for purposes of TI's product warranty. These equations assume an ideal—no variation—external adjusting resistor. To take resistor tolerance into account, first determine the minimum and maximum resistor values based on its tolerance specifications and use these values in the equations. Because of the inverse relation between the current limit and the adjusting resistor, use the maximum resistor value in the $I_{OS(min)}$ equation and the minimum resistor value in the $I_{OS(max)}$ equation.

$$I_{OS(min)}\ (mA) = \frac{46464\ V}{R_{(ILIM\_xx)}^{0.9974}\ k\Omega} - 32 \tag{4}$$

$$I_{OS(max)}\ (mA) = \frac{51820\ V}{R_{(ILIM\_xx)}^{0.9987}\ k\Omega} + 38 \tag{5}$$

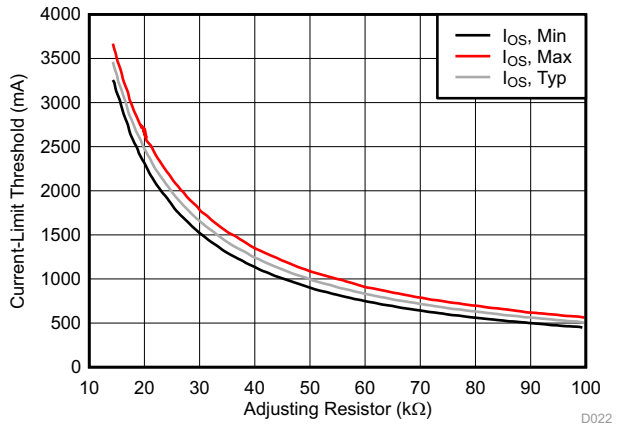


Figure 40. Current-Limit Setting vs Adjusting Resistor I

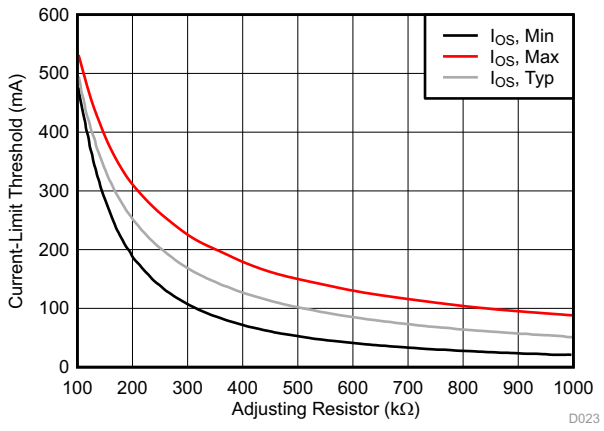


Figure 41. Current-Limit Setting vs Adjusting Resistor II

The routing of the traces to the $R_{(ILIM\_xx)}$ resistors should have a sufficiently low resistance so as not to affect the current-limit accuracy. The ground connection for the $R_{(ILIM\_xx)}$ resistors is also very important. The resistors must reference back to the TPS254900-Q1 GND pin. Follow normal board layout practices to ensure that current flow from other parts of the board does not impact the ground potential between the resistors and the TPS254900-Q1 GND pin.

8.4 Device Functional Modes

8.4.1 Device Truth Table (TT)

The device truth table (Table 3) lists all valid combinations for both control pins (CTL1 and CTL2), and the corresponding charging mode. The TPS254900-Q1 device monitors the CTL inputs and transitions to the charging mode to which it is commanded.

Table 3. Truth Table

CTL1	CTL2	CURRENT LIMIT SELECTED	MODE	$\overline{\text{STATUS}}$ for Load Detect	$\overline{\text{CS}}$ FOR CABLE COMPENSATION	IMON FOR CURRENT MONITOR	$\overline{\text{FAULT}}$ REPORT	NOTES
0	0	N/A	Client mode (1)	OFF	OFF	OFF	OFF	Power switch is disabled, only analog switch is on.
0	1	ILIM_LO	SDP	OFF	ON	ON	ON	Standard SDP
1	0	ILIM_LO	SDP1 (2)	OFF	ON	ON	ON (3)	No OUT discharge between CDP and SDP1 for PPM
1	1	ILIM_HI	CDP (2)	ON	ON	ON	ON	

(1) No 5.1-kΩ resistor from BIAS to OUT (open between the pins), or OUT still has 5-V voltage from an external downstream port; client mode is still active.
(2) No OUT discharge when changing from 10 to 11 or from 11 to 10.
(3) A fault only trips OTSD, OUT, DP_IN, DM_IN, and OVP.

8.4.2 USB BC1.2 Specification Overview

The BC1.2 specification includes three different port types:

- Standard downstream port (SDP)
- Charging downstream port (CDP)
- Dedicated charging port (DCP)

BC1.2 defines a charging port as a downstream-facing USB port that provides power for charging portable equipment. Under this definition, CDP and DCP are defined as charging ports.

Table 4 lists the difference between these port types.

Table 4. Operating Modes Table

PORT TYPE	SUPPORTS USB2.0 COMMUNICATION	MAXIMUM ALLOWABLE CURRENT DRAWN BY PORTABLE EQUIPMENT (A)
SDP (USB 2.0)	YES	0.5
SDP (USB 3.0)	YES	0.9
CDP	YES	1.5
DCP	NO	1.5

8.4.3 Standard Downstream Port (SDP) Mode — USB 2.0 and USB 3.0

An SDP is a traditional USB port that follows the USB 2.0 or USB 3.0 protocol. An SDP supplies a minimum of 500 mA per port for USB 2.0 and 900 mA per port for USB 3.0. USB 2.0 and USB 3.0 communication is supported, and the host controller must be active to allow charging.

8.4.4 Charging Downstream Port (CDP) Mode

A CDP is a USB port that follows the USB BC1.2 specification and supplies a minimum of 1.5 A per port. A CDP provides power and meets the USB 2.0 requirements for device enumeration. USB 2.0 communication is supported, and the host controller must be active to allow charging. The difference between CDP and SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device and allows for additional current draw by the client device.

The CDP handshaking process occurs in two steps. During the first step, the portable equipment outputs a nominal 0.6-V output on the D+ line and reads the voltage input on the D– line. The portable device detects the connection to an SDP if the voltage is less than the nominal data-detect voltage of 0.3 V. The portable device detects the connection to a CDP if the D– voltage is greater than the nominal data-detect voltage of 0.3 V and optionally less than 0.8 V.

The second step is necessary for portable equipment to determine whether the equipment is connected to a CDP or a DCP. The portable device outputs a nominal 0.6-V output on the D– line and reads the voltage input on the D+ line. The portable device concludes the equipment is connected to a CDP if the data line being read remains less than the nominal data detects voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data-detect voltage of 0.3 V.

The TPS254900-Q1 integrates CDP detection protocol, used at a downstream port as the CDP controller to support CDP portable-device fast charge up to 1.5 A.

8.4.5 Client Mode

The TPS254900-Q1 device integrates client mode as shown in Figure 42. The internal power switch is OFF to block current flow from OUT to IN, and the signal switches are ON. This mode can be used for software upgrades from the USB port.

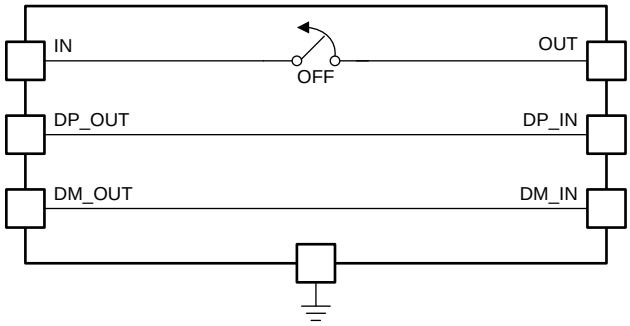


Figure 42. Client-Mode Equivalent Circuit

Passing the IEC 61000-4-2 test for DP_IN and DM_IN requires connecting a discharge resistor to OUT during USB 2.0 high-speed enumeration. In client mode, because the power switch is OFF, OUT must be 5 V so that the device can work normally (usually powered by an external downstream USB port). If the OUT voltage is low, the communication may not work properly.

8.4.6 High-Bandwidth Data-Line Switch

The D+ and D– data lines pass through the device to enable monitoring and handshaking while supporting the charging operation. A wide-bandwidth signal switch allows data to pass through the device without corrupting signal integrity. The data-line switches are turned on in any of the CDP, SDP or client operating modes. The EN input must be at logic high for the data-line switches to be enabled.

NOTE

- While in CDP mode, the data switches are ON, even during CDP handshaking.
- The data switches are only for the USB-2.0 differential pair. In the case of a USB-3.0 host, the super-speed differential pairs must be routed directly to the USB connector without passing through the TPS254900-Q1 device.
- Data switches are OFF during OUT (V_{BUS}) discharge.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS254900-Q1 device is a USB charging-port controller and power switch with cable compensation and short-to-battery protection for V_{BUS}, D+, and D–. The device is typically used for automotive USB port protection and as a USB charging controller. The following design procedure can be used to select components for the TPS254900-Q1. This section presents a simplified discussion of how to choose external components for V_{BUS}, D+, and D– short-to-battery protection. For cable-compensation design information, see the data sheet (SLUSCE3) for the TPS2549-Q1 device, which has features and design considerations very similar to those of the TPS254900-Q1 device.

9.2 Typical Application

For an automotive USB charging port, the V_{BUS}, D+, and D– pins are exposed and require a protection device. The protection required includes V_{BUS} overcurrent, D+ and D– ESD protection, and short-to-battery protection. This charging-port device protects the upstream dc-dc converter (bus line) and automotive SOC or hub chips (D+ and D– data lines). An application schematic of this circuit with short-to-battery protection is shown in Figure 43.

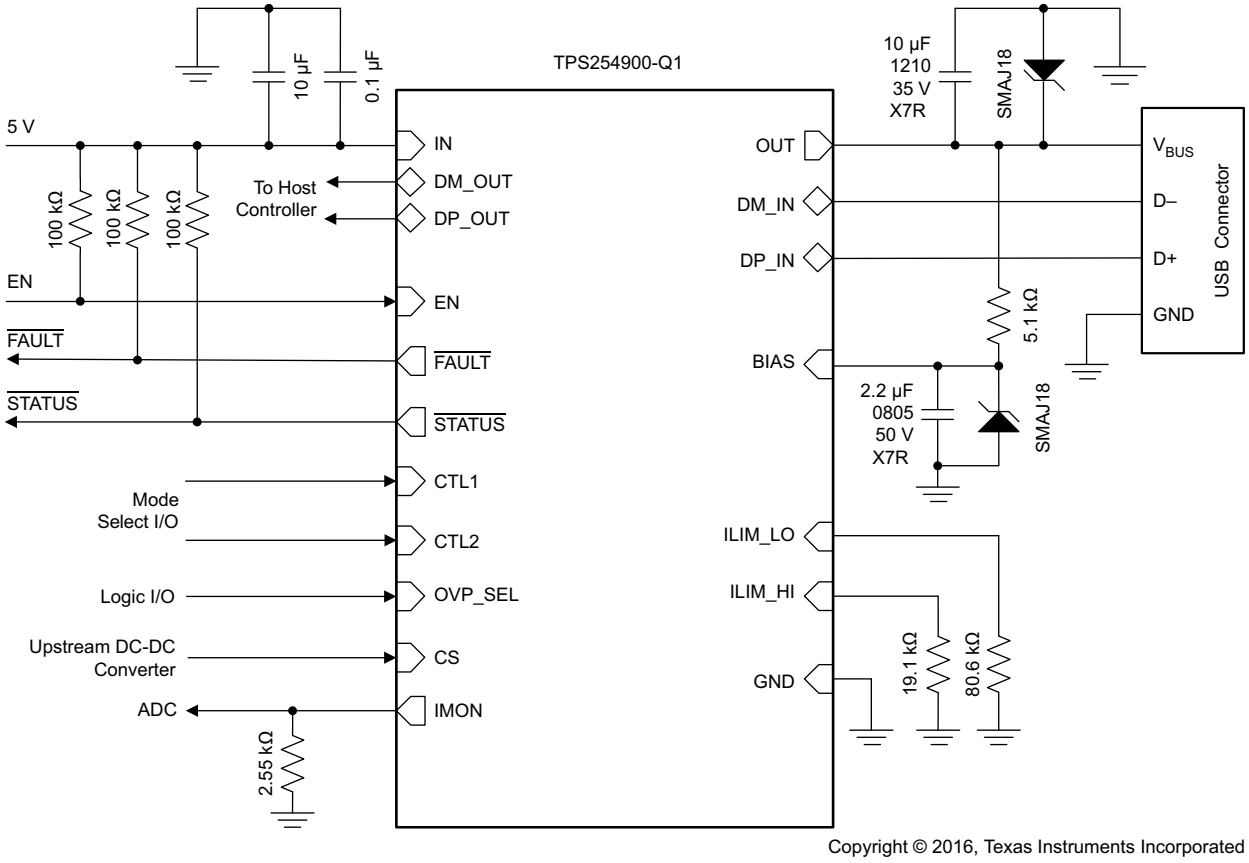


Figure 43. Typical Application Schematic: USB Port Charging With Cable Compensation

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the following as the input parameters.

DESIGN PARAMETER	EXAMPLE VALUE
Battery voltage, $V_{(BAT)}$	18 V
Short-circuit cable	0.5 m

9.2.2 Detailed Design Procedure

To begin the design process, the designer must know the following:

- The battery voltage
- The short-circuit cable length
- The maximum continuous output current for the charging port. The minimum current-limit setting of TPS254900-Q1 device must be higher than this current.
- The maximum output current of the upstream dc-dc converter. The maximum current-limit setting of TPS254900-Q1 device must be lower than this current.
- For cable compensation, the total resistance including power switch $r_{DS(on)}$, cable resistance, and connector contact resistance must be specified.

9.2.2.1 Input Capacitance

Consider the following application situations when choosing the input capacitors.

For all applications, TI recommends a 0.1-µF or greater ceramic bypass capacitor between IN and GND, placed as close as possible to the device for local noise decoupling.

During output short or hot plug-in of a capacitive load, high current flows through the TPS254900-Q1 device back to the upstream dc-dc converter until the TPS254900-Q1 device responds (after $t_{(IOS)}$). During this response time, the TPS254900-Q1 input capacitance and the dc-dc converter output capacitance source current to keep V_{IN} above the UVLO of the TPS254900-Q1 device and any shared circuits. Size the input capacitance for the expected transient conditions and keep the path between the TPS254900-Q1 device and the dc-dc converter short to help minimize voltage drops.

Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power-bus inductance and input capacitance when the IN pin is in the high-impedance state (before turnon). Theoretically, the peak voltage is 2 times the applied voltage. The second cause is due to the abrupt reduction of output short-circuit current when the TPS254900-Q1 device turns off and energy stored in the input inductance drives the input voltage high. Applications with large input inductance (for example, a connection between the evaluation board and the bench power supply through long cables) may require large input capacitance to prevent the voltage overshoot from exceeding the absolute-maximum voltage of the device.

During the short-to-battery (EN = HIGH) condition, the input voltage follows the output voltage until OVP protection is triggered ($t_{(OV\_OUT)}$). After the TPS254900-Q1 device responds and turns off the power switch, the stored energy in the input inductance can cause ringing.

Based on the three situations described, 10-µF and 0.1-µF low-ESR ceramic capacitors, placed close to the input, are recommended.

9.2.2.2 Output Capacitance

Consider the following application situations when choosing the output capacitors.

After an output short occurs, the TPS254900-Q1 device abruptly reduces the OUT current, and the energy stored in the output power-bus inductance causes voltage undershoot and potentially reverse voltage as it discharges.

Applications with large output inductance (such as from a cable) benefit from the use of a high-value output capacitor to control the voltage undershoot.

For USB port applications, because the V_{BUS} pin is exposed to IEC61000-4-2 level-4 ESD, use a low-ESR capacitance to protect OUT.

The TPS254900-Q1 device is capable of handling up to 18-V battery voltage. When V_{BUS} is shorted to the battery, the LCR tank circuit formed can induce ringing. The peak voltage seen on the OUT pin depends on the short-circuit cable length. The parasitic inductance and resistance varies with length, causing the damping factor and peak voltage to differ. Longer cables with larger resistance reduce the peak current and peak voltage. Consider high-voltage derating for the ceramic capacitor, because the peak voltage can be higher than twice the battery voltage.

Based on the three situations described, a 10-µF, 35-V, X7R, 1210 low-ESR ceramic capacitor placed close to OUT is recommended. If the battery voltage is 16 V and a 16-V transient voltage suppressor (TVS) is used, then the capacitor voltage can be reduced to 25 V. Considering temperature variation, placing an additional 35-V aluminum electrolytic capacitor can lower the peak voltage and make the system more robust.

9.2.2.3 BIAS Capacitance

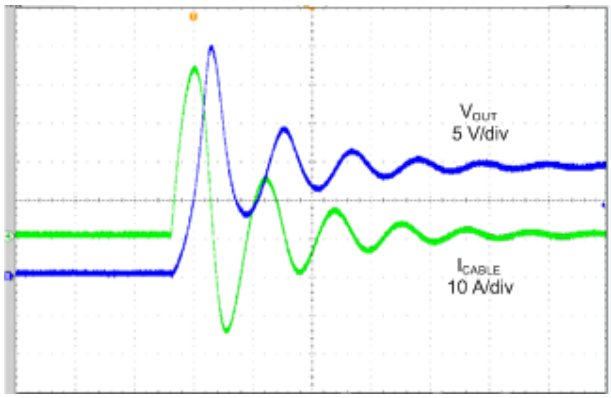
The capacitance on the BIAS pin helps the IEC ESD performance on the DM_IN and DP_IN pins.

When a short to battery on DP_IN, DM_IN and/or OUT occurs, high voltage can be seen on the BIAS pin. Place a 2.2-µF, 50-V, X7R, 0805, low-ESR ceramic capacitor close to the BIAS pin. The whole current path from BIAS to GND should be as short as possible. Additionally, use a 5.1-kΩ discharge resistor from BIAS to OUT.

9.2.2.4 Output and BIAS TVS

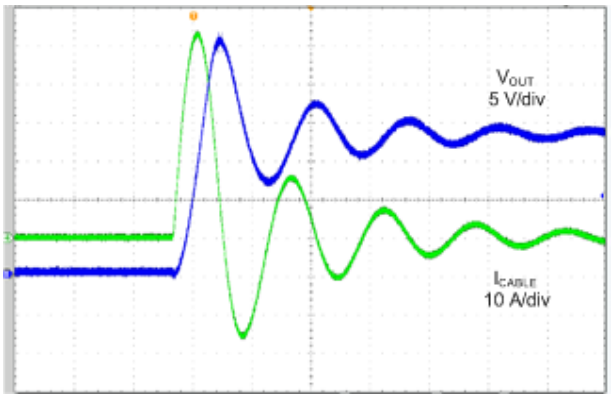
The TPS254900-Q1 device can withstand high transient voltages due to LCR tank ringing, but in order to make OUT, DP_IN, and DM_IN robust, place one TVS close to the OUT pin, and another TVS close to the BIAS pin. When choosing the TVS, the reverse standoff voltage V_R depends on the battery voltage (16 V or 18 V). Considering the peak pulse power capability, a 400-W device is recommended such as an SMAJ16 for a 16-V battery or an SMAJ18 for an 18-V battery.

9.2.3 Application Curves



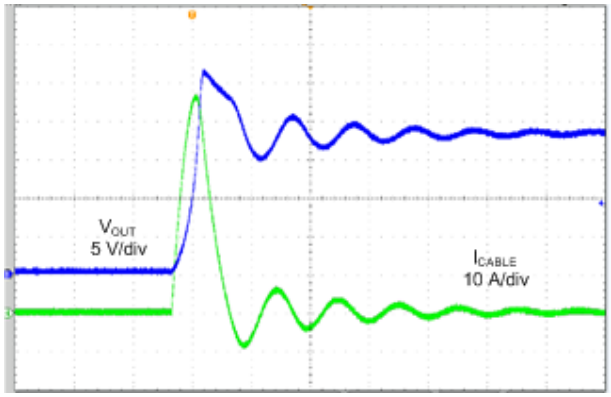
V_{BAT} = 14 V t = 10 µs/div

Figure 44. Disabled, 25-V, 1206, X7R C_{OUT} Capacitor Without SMAJ18



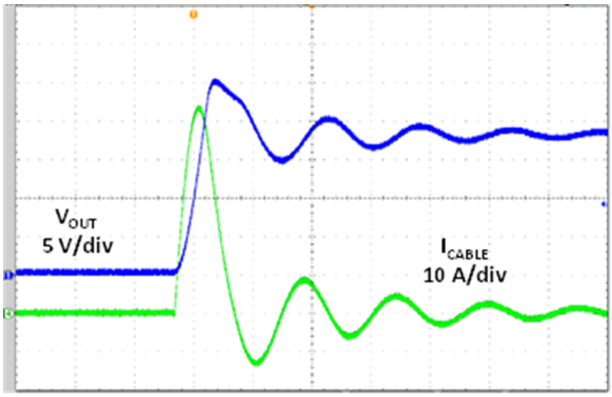
V_{BAT} = 18 V t = 10 µs/div

Figure 45. Disabled, 35-V, 1210, X7R C_{OUT} Capacitor Without SMAJ18



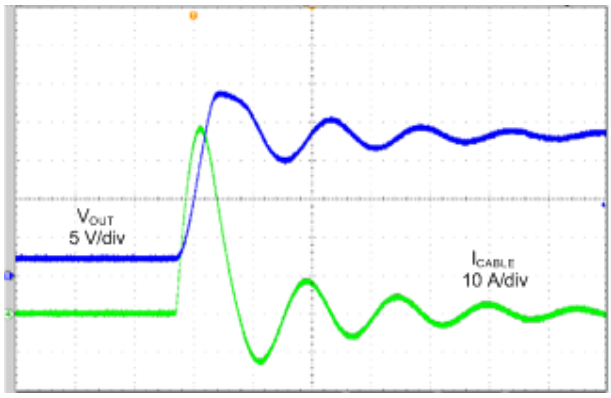
t = 10 µs/div

Figure 46. Disabled, 25-V, 1206, X7R C_{OUT} Capacitor With SMAJ18, OUT Shorted to Battery



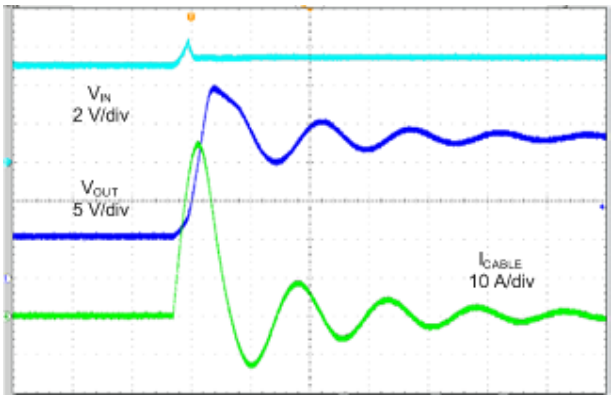
t = 10 µs/div

Figure 47. Disabled, 35-V, 1210, X7R C_{OUT} Capacitor With SMAJ18, OUT Shorted to Battery



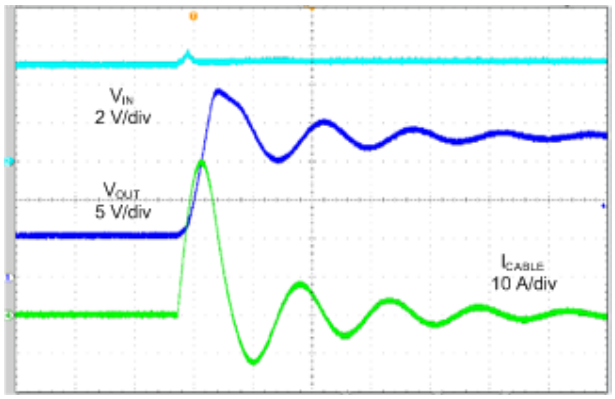
t = 10 µs/div

Figure 48. DC-DC Input Is Floating, OUT Shorted to Battery



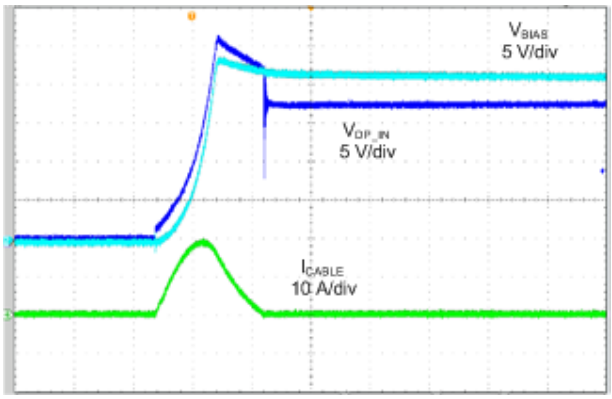
t = 10 µs/div

Figure 49. Enabled With OVP_SEL = High, OUT Shorted to Battery



t = 10 µs/div

Figure 50. Enabled With OVP_SEL = Low, OUT Shorted to Battery



R_{BIAS} = 5.1 kΩ t = 2 µs/div

Figure 51. Disabled, DP_IN Shorted to Battery

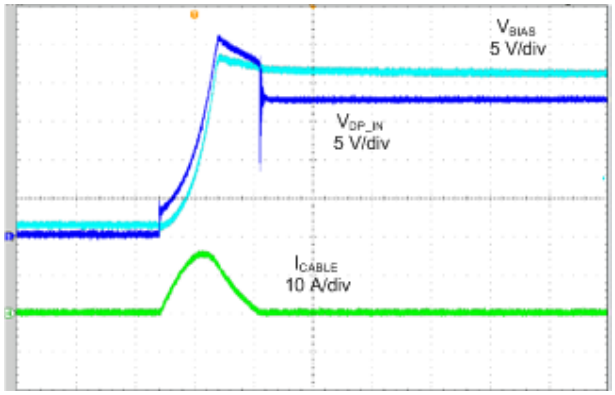


Figure 52. DC-DC Input Is Floating, DP_IN Shorted to Battery

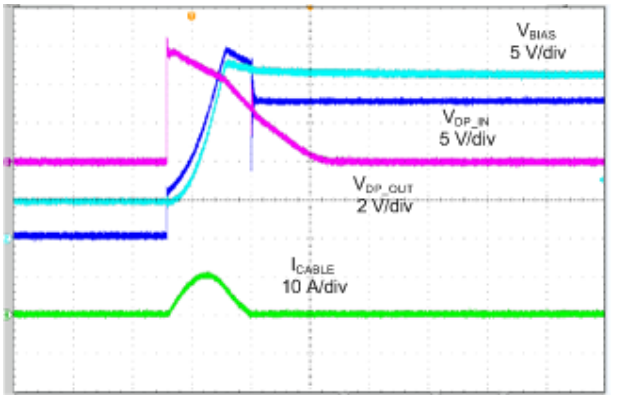


Figure 53. Enabled, DP_IN Shorted to Battery

10 Power Supply Recommendations

The TPS254900-Q1 device is designed for a supply voltage range of 4.5 V ≤ V_{IN} ≤ 6.5 V, with its power switch used for protecting the upstream power supply when a fault such as overcurrent or short to ground occurs on the USB port. Therefore, the power supply should be rated higher than the current-limit setting to avoid voltage drops during overcurrent or short-circuit conditions.

11 Layout

11.1 Layout Guidelines

Layout best practices for the TPS254900-Q1 are listed as follows.

- Considerations for input and output power traces
  - Make the power traces as short as possible.
  - Make the power traces as wide as possible.
- Considerations for input-capacitor traces
  - For all applications, 10-µF and 0.1-µF low-ESR ceramic capacitors are recommended, placed close to the IN pin.
- The resistors attached to the ILIM_HI and ILIM_LO pins of the device have several requirements.
  - It is recommended to use 1% low-temperature-coefficient resistors.
  - The trace routing between these two pins and GND should be as short as possible to reduce parasitic effects on current limit. These traces should not have any coupling to switching signals on the board.
- Locate all TPS254900-Q1 pullup resistors for open-drain outputs close to their connection pin. Pullup resistors should be 100 kΩ.
  - If a particular open-drain output is not used or needed in the system, tie it to GND.
- ESD considerations
  - The TPS254900-Q1 device has built-in ESD protection for DP_IN and DM_IN. Keep trace lengths minimal from the USB connector to the DP_IN and DM_IN pins on the TPS254900-Q1 device, and use minimal vias along the traces.
  - The capacitor on BIAS helps to improve the IEC ESD performance. A 2.2-µF capacitor should be placed close to BIAS, and the current path from BIAS to GND across this capacitor should be as short as possible. Do not use vias along the connection traces.
  - A 10-µF output capacitor should be placed close to the OUT pin and TVS.
  - See the *ESD Protection Layout Guide* (SLVA680) for additional information.
- TVS Considerations
  - For OUT, a TVS like SMAJ18 should be placed near the OUT pin.
  - For BIAS, a TVS like SMAJ18 should be placed close to the BIAS pin, but behind the 2.2-µF capacitor.

Layout Guidelines (continued)

  - The whole path from OUT to GND or BIAS to GND across the TVS should be as short as possible.
- DP_IN, DM_IN, DP_OUT, and DM_OUT routing considerations
  - Route these traces as microstrips with nominal differential impedance of 90 Ω.
  - Minimize the use of vias on the high-speed data lines.
  - Keep the reference GND plane devoid from cuts or splits above the differential pairs to prevent impedance discontinuities.
  - For more USB 2.0 high-speed D+ and D– differential routing information, see the *High Speed USB Platform Design Guideline* from Intel.
- Thermal Considerations
  - When properly mounted, the thermal-pad package provides significantly greater cooling ability than an ordinary package. To operate at rated power, the thermal pad must be soldered to the board GND plane directly under the device. The thermal pad is at GND potential and can be connected using multiple vias to inner-layer GND. Other planes, such as the bottom side of the circuit board, can be used to increase heat sinking in higher-current applications. See the *PowerPad™ Thermally Enhanced Package* application report (SLMA002) and *PowerPAD™ Made Easy* application brief (SLMA004) for more information on using this thermal pad package.

11.2 Layout Example

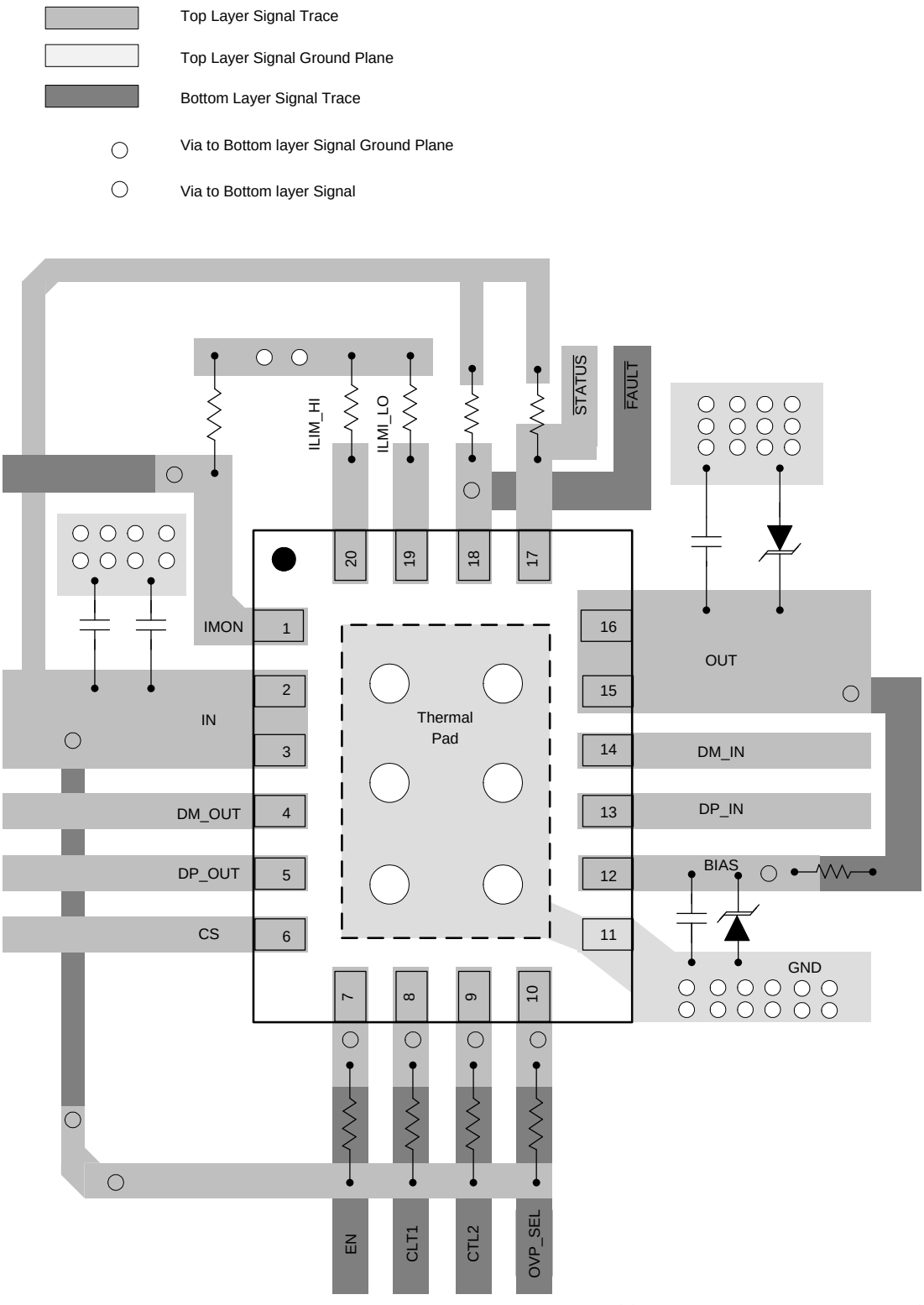


Figure 54. TPS254900-Q1 Layout Diagram

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

High Speed USB Platform Design Guidelines, Intel

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS254900IRVCRQ1	ACTIVE	WQFN	RVC	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	254900Q	Samples
TPS254900IRVCTQ1	ACTIVE	WQFN	RVC	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	254900Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

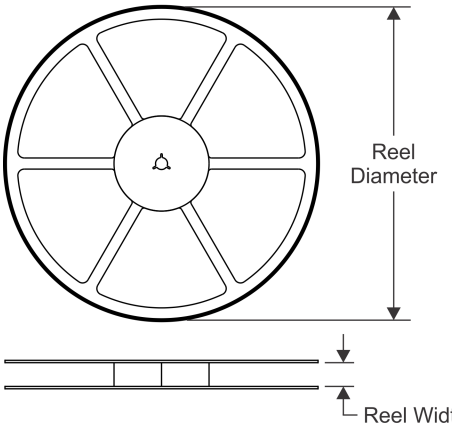
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

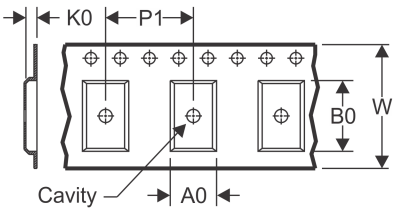
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

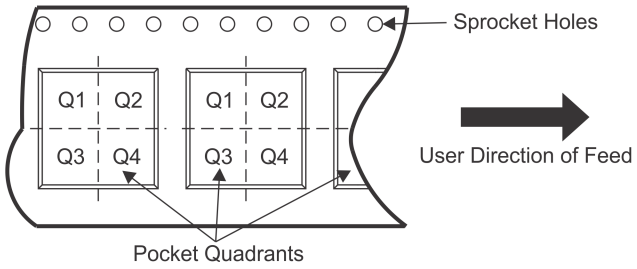


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

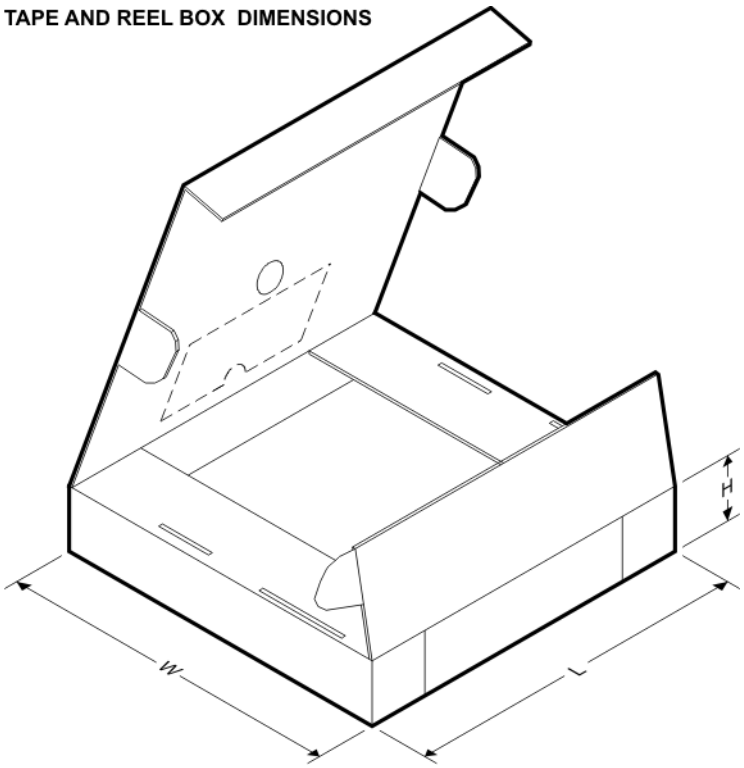
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS254900IRVCRQ1	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS254900IRVCTQ1	WQFN	RVC	20	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1

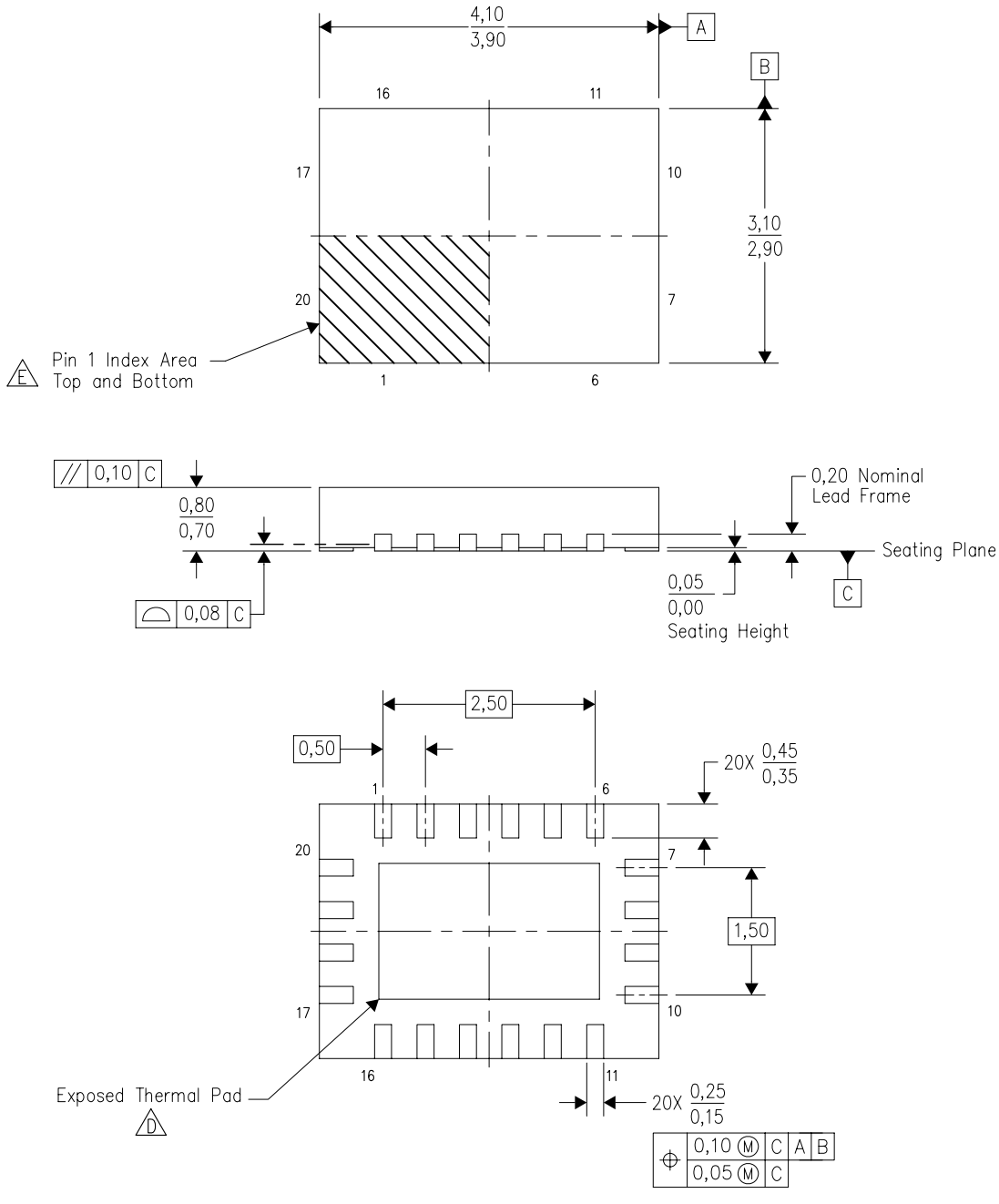
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS254900IRVCRQ1	WQFN	RVC	20	3000	367.0	367.0	35.0
TPS254900IRVCTQ1	WQFN	RVC	20	250	210.0	185.0	35.0

RVC (R–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



4209819/A 10/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

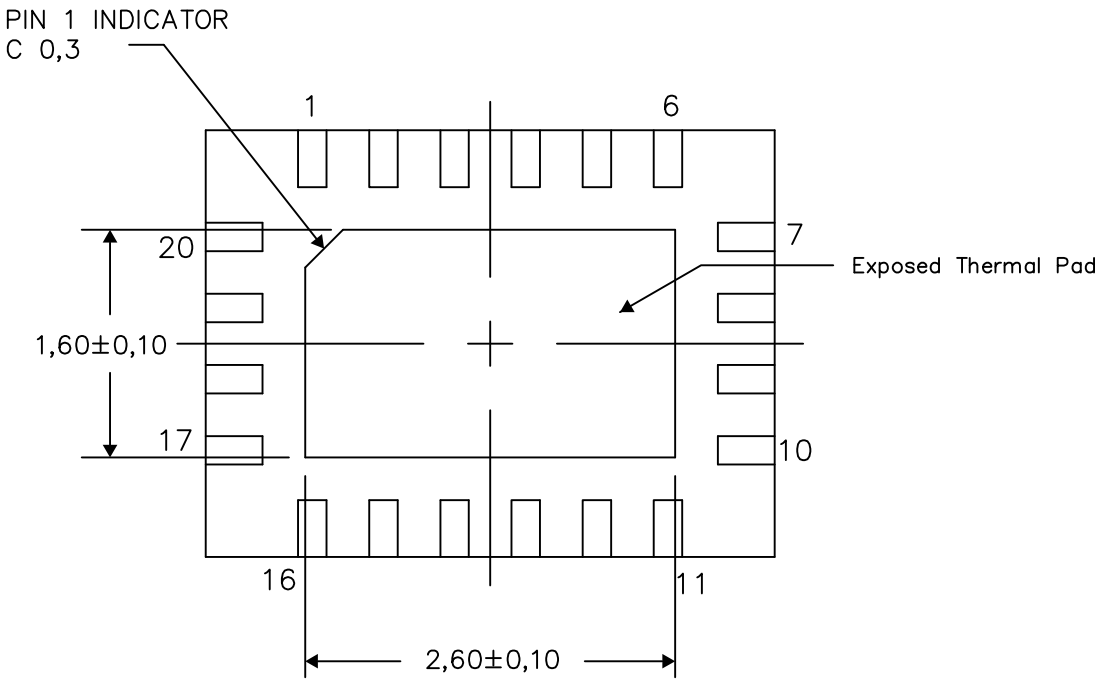
RVC (R–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4209820–2/F 03/15

NOTE: All linear dimensions are in millimeters

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