Freescale Semiconductor
Data Sheet: Technical Data

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PXD10



416 TEPBGA
27 mm x 27 mm



208 LQFP
28 mm x 28 mm



176 LQFP
24 mm x 24 mm

PXD10 Microcontroller Data Sheet

The PXD10 family represents a new generation of 32-bit microcontrollers based on the Power Architecture®. These devices provide a cost-effective, single chip display solution for the industrial market. An integrated TFT driver with digital video input ability from an external video source, significant on-chip memory, and low power design methodologies provide flexibility and reliability in meeting display demands in rugged environments. The advanced processor core offers high performance processing optimized for low power consumption, operating at speeds as high as 64 MHz. The family itself is fully scalable from 512 KB to 1 MB internal flash memory. The memory capacity can be further expanded via the on-chip QuadSPI serial flash controller module.

The PXD10 family platform has a single level of memory hierarchy supporting on-chip SRAM and flash memories. The 1 MB flash version features 160 KB of on-chip graphics SRAM to buffer cost effective color TFT displays driven via the on-chip Display Control Unit (DCU). See Table 1 for specific memory size and feature sets of the product family members.

The PXD10 family benefits from the extensive development infrastructure for Power Architecture devices, which is already well established. This includes full support from available software drivers, operating systems, and configuration code to assist with users' implementations. See Section 3, Developer support, for more information.

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1 Overview

1.1 Document overview

This document describes the device features and highlights important electrical and physical characteristics. For functional characteristics, see the *PXD10 Microcontroller Reference Manual*.

1.2 Description

The PXD10 family of chips is designed to enable the development of industrial HMI applications by providing a single-chip solution capable of hosting real-time applications and driving a TFT display directly using an on-chip color TFT display controller.

PXD10 chips incorporate a cost-efficient host processor core compliant with the Power Architecture® embedded category. The processor is 100% user-mode compatible with the Power Architecture and capitalizes on the available development infrastructure of current Power Architecture devices with full support from available software drivers, operating systems and configuration code to assist with users' implementations.

Offering high performance processing at speeds up to 64 MHz, the PXD10 family is optimized for low power consumption and supports a range of on-chip SRAM and internal flash memory sizes. The version with 1 MB of flash memory (PXD1010) features 160 KB of on-chip graphics SRAM.

See Table 1 for specific memory and feature sets of the product family members.

1.3 Device comparison

Table 1. PXD10 family feature set

Feature	PXD1005	PXD1010
CPU	e200z0h	
Execution speed	Static – 64 MHz	
Flash (ECC)	512 KB	1 MB
EEPROM Emulation Block (ECC)	4 × 16 KB	
RAM (ECC)	48 KB	
Graphics RAM	No	160 KB
MPU	12 entry	
eDMA	16 channels	
Display Control Unit (DCU)	No	Yes
Parallel Data Interface	No	Yes
Stepper Motor Controller (SMC)	6 motors	
Stepper Stall Detect (SSD)	Yes	
Sound Generation Logic (SGL)	Yes	

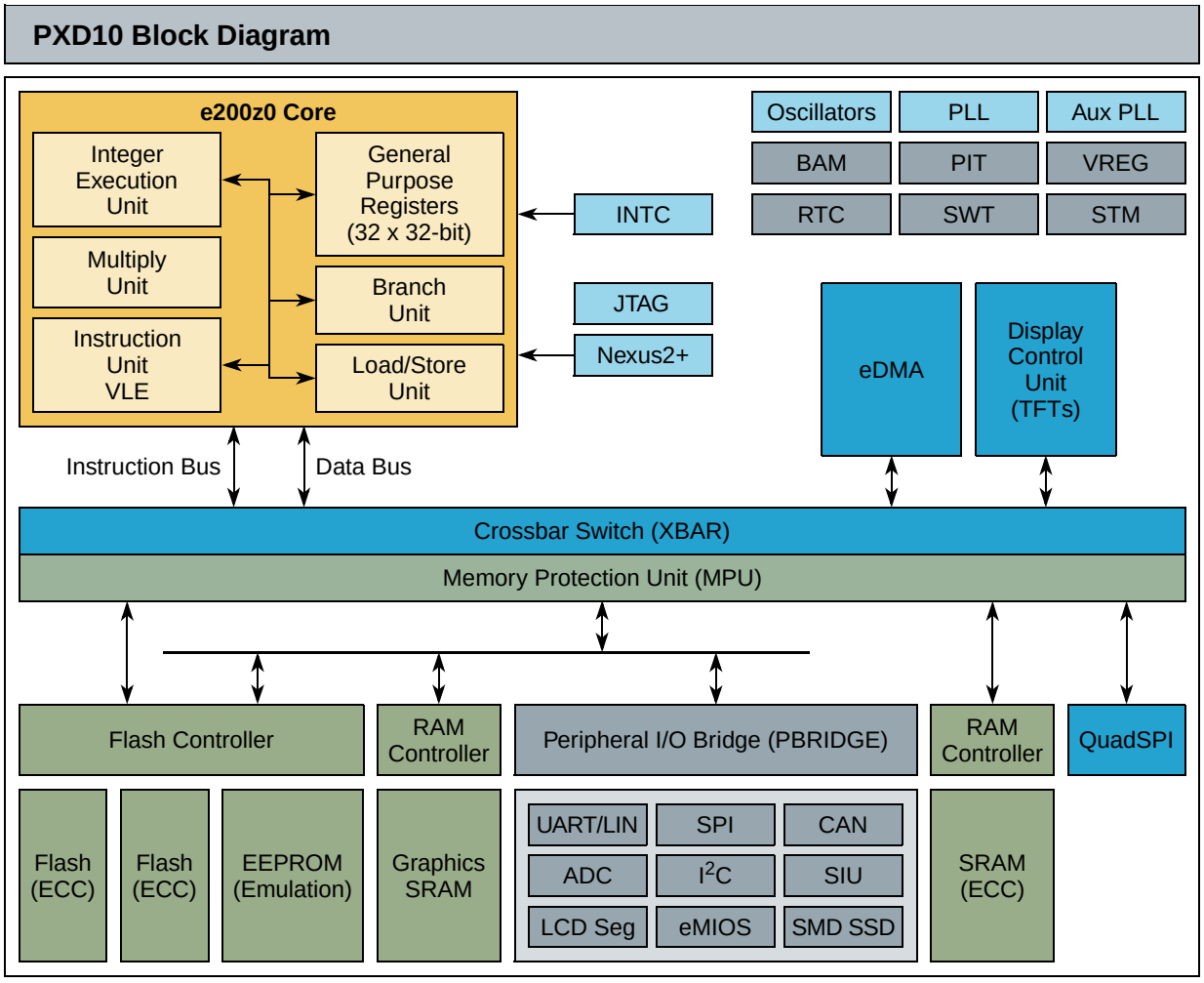
Table 1. PXD10 family feature set (continued)

Feature	PXD1005	PXD1010
LCD driver	64 × 6	40 × 4, 38 × 6
32 kHz slow external crystal oscillator	Yes	
Real-Time Counter and Autonomous Periodic Interrupt	Yes	
Periodic Interrupt Timer (PIT)	4 ch, 32-bit	
Software Watchdog Timer (SWT)	Yes	
System Timer Module (STM)	4 ch, 32-bit	
Timed I/O (eMIOS)	8 ch, 16-bit IC/OC	
	16 ch, 16-bit PWM/IC/OC	
ADC	16 channels, 10-bit	
CAN (64 Mailboxes)	2 × CAN	
CAN Sampler	Yes	
SCI	2 × UART	
SPI	2 × SPI	3 × SPI
QuadSPI Serial Flash Interface	No	Yes
I^2C	2	4
GPIO	105	105 (144-pin package) 133 (176-pin package)
Debug	Nexus 1	Nexus 2+
Package	144 LQFP	144 LQFP 176 LQFP

1.4 PXD10 series blocks

1.4.1 Block diagram

Figure 1 shows a high-level block diagram of the PXD10 series.



ADC – Analog-to-digital converter
BAM – Boot assist module
CAN – Controller area network controller
ECC – Error correction code
eDMA – Enhanced direct memory access controller
eMIOS – Timed input/output
I²C – Inter-integrated circuit controller
INTC – Interrupt controller
JTAG – Joint Test Action Group interface
LCD – Liquid crystal display
PIT – Periodic interrupt timer
PLL – Phase-locked loop
RTC – Real time clock
SIU – System integration unit
SMD SSD – Stepper motor driver/stepper stall detect
SPI – Serial peripheral interface controller
SRAM – Static random-access memory
STM – System timer module
SWT – Software watchdog timer
UART/LIN – Universal asynchronous receiver/transmitter/ local interconnect network
VLE – Variable-length execution set
VREG – Voltage regulator

Figure 1. PXD10 series block diagram

1.5 PXD10 features

1.5.1 Summary

- Single issue, 32-bit Power Architecture technology compliant CPU core complex (e200z0h)
  - — Compatible with Power Architecture instruction set
  - — Includes variable length encoding (VLE) instruction set for smaller code size footprint; with the encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction over conventional Book E compliant code
- On-chip ECC flash memory with flash controller
  - — As much as 1 MB primary flash—two 512 KB modules with prefetch buffer and 128-bit data access port
  - — 64 KB data flash—separate 4×16 KB flash block for EEPROM emulation with prefetch buffer and 128-bit data access port
- As much as 48 KB on-chip ECC SRAM with SRAM controller
- As much as 160 KB on-chip non-ECC graphics SRAM with SRAM controller
- Memory Protection Unit (MPU) with as many as 12 region descriptors and 32-byte region granularity to provide basic memory access permission
- Interrupt Controller (INTC) with as many as 127 peripheral interrupt sources and eight software interrupts
- Two Frequency-Modulated Phase-Locked Loops (FMPLLs)
  - — Primary FMPLL provides a 64 MHz system clock
  - — Auxiliary FMPLL is available for use as an alternate, modulated or non-modulated clock source to eMIOS modules and as alternate clock to the DCU for pixel clock generation
- Crossbar switch architecture enables concurrent access of peripherals, flash memory or RAM from multiple bus masters (AMBA 2.0 v6 AHB)
- 16-channel Enhanced Direct Memory Access controller (eDMA) with multiple transfer request sources using a DMA channel multiplexer
- Boot Assist Module (BAM) supports internal flash programming via a serial link (FlexCAN or LINFlex)
- Display Control Unit to drive TFT LCD displays
  - — Includes processing of as many as four planes that can be blended together
  - — Offers a direct unbuffered hardware bit-blitter of as many as 16 software-configurable dynamic layers in order to drastically minimize graphic memory requirements and provide fast animations
  - — Programmable display resolutions are available up to WVGA
- Parallel Data Interface (PDI) for digital video input
- LCD segment driver module with two software programmable configurations:
  - — As many as 40 frontplane drivers and four backplane drivers

  - As many as 38 frontplane drivers and six backplane drivers
- Stepper Motor Controller (SMC) module with high-current drivers for as many as six stepper motors driven in full dual H-Bridge configuration including full diagnostics for short circuit detection
- Stepper motor return-to-zero and stall detection module
- Sound generation and playback utilizing PWM channels and eDMA; supports monotonic and polyphonic sound
- 24 eMIOS channels providing as many as 16 PWM and 24 input capture / output compare channels
- 10-bit Analog-to-Digital Converter (ADC)
  - Maximum conversion time of 1 µs
  - As many as 16 internal channels, expandable to 23 via external multiplexing
- As many as two Serial Peripheral Interface (DSPI) modules for full-duplex, synchronous, communications with external devices (extendable to include up to 8 multiplexed external channels)
- QuadSPI serial flash memory controller supporting single, dual and quad modes of operation to interface to external serial flash memory. QuadSPI can be configured to function as another DSPI module.
- Two Local Interconnect Network Flexible (LINFlex) controller modules capable of autonomous message handling (master), autonomous header handling (slave mode), and UART support. Compliant with LIN protocol rev 2.1
- Two full CAN 2.0B controllers with 64 configurable buffers each; bit rate programmable as fast as 1 Mbit/s
- As many as four inter-integrated circuit (I^2C) internal bus controllers with master/slave bus interface
- As many as 133 configurable general purpose pins supporting input and output operations
- Real Time Counter (RTC) with multiple clock sources:
  - 128 kHz slow internal RC oscillator or 16 MHz fast internal RC oscillator supporting autonomous wakeup with 1 ms resolution with maximum timeout of 2 seconds
  - 32 KHz slow external crystal oscillator, supporting wakeup with 1 s resolution and maximum timeout of one hour
  - 4–16 MHz fast external crystal oscillator
- System timers:
  - Four-channel 32-bit System Timer Module (STM)—included in processor platform
  - Four-channel 32-bit Periodic Interrupt Timer (PIT) module
  - Software Watchdog Timer (SWT)
- System Integration Unit (SIU) module to manage resets, external interrupts, GPIO and pad control
- System Status and Configuration Module (SSCM) to provide information for identification of the device, last boot mode, or debug status and provides an entry point for the censorship password mechanism

- Clock Generation Module (MC_CGM) to generate system clock sources and provide a unified register interface, enabling access to all clock sources
- Clock Monitor Unit (CMU) to monitor the integrity of the main crystal oscillator and the PLL and act as a frequency meter, measuring the frequency of one clock source and comparing it to a reference clock
- Mode Entry Module (MC_ME) to control the device power mode, i.e., RUN, HALT, STOP, or STANDBY, control mode transition sequences, and manage the power control, voltage regulator, clock generation and clock management modules
- Reset Generation Module (MC_RGM) to manage reset assertion and release to the device at initial power-up
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus standard
- Device/board boundary-scan testing supported per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator controller for regulating the 3.3 or 5 V supply voltage down to 1.2 V for core logic (requires external ballast transistor)
- The PXD10 microcontrollers are offered in the following packages:[1]
  - 144 LQFP, 0.5 mm pitch, 20 mm × 20 mm outline
  - 176 LQFP, 0.5 mm pitch, 24 mm × 24 mm outline

1.6 Details

1.6.1 Low-power operation

PXD10 devices are designed for optimized low-power operation and dynamic power management of the core processor and peripherals. Power management features include software-controlled clock gating of peripherals and multiple power domains to minimize leakage in low-power modes.

There are two static low-power modes, STANDBY and STOP, and two dynamic power modes—RUN and HALT. Both low power modes use clock gating to halt the clock for all or part of the device. The STANDBY mode also uses power gating to automatically turn off the power supply to parts of the device to minimize leakage.

STANDBY mode turns off the power to the majority of the chip to offer the lowest power consumption mode. The contents of the cores, on-chip peripheral registers and potentially some of the volatile memory are lost. STANDBY mode is configurable to make certain features available with the disadvantage that these consume additional current:

- It is possible to retain the contents of the full RAM or only 8 KB.
- It is possible to enable the internal 16 MHz or 128 kHz RC oscillator, the external 4–16 MHz oscillator, or the external 32 KHz oscillator.
- It is possible to keep the LCD module active.

1. See the device comparison table or orderable parts summary for package offerings for each device in the family.

The device can be awakened from STANDBY mode via from any of as many as 19 I/O pins, a reset or from a periodic wake-up using a low power oscillator.

STOP mode maintains power to the entire device allowing the retention of all on-chip registers and memory, and providing a faster recovery low power mode than the lowest STANDBY mode. There is no need to reconfigure the device before executing code. The clocks to the core and peripherals are halted and can be optionally stopped to the oscillator or PLL at the expense of a slower start-up time.

STOP is entered from RUN mode only. Wake-up from STOP mode is triggered by an external event or by the internal periodic wake-up, if enabled.

RUN modes are the main operating mode where the entire device can be powered and clocked and from which most processing activity is done. Four dynamic RUN modes are supported—RUN0 - RUN3. The ability to configure and select different RUN modes enables different clocks and power configurations to be supported with respect to each other and to allow switching between different operating conditions. The necessary peripherals, clock sources, clock speed and system clock prescalers can be independently configured for each of the four RUN modes of the device.

HALT mode is a reduced activity, low power mode intended for moderate periods of lower processing activity. In this mode the core system clocks are stopped but user-selected peripheral tasks can continue to run. It can be configured to provide more efficient power management features (switch-off PLL, flash memory, main regulator, etc.) at the cost of longer wake up latency. The system returns to RUN mode as soon as an event or interrupt is pending.

Table 1 summarizes the operating modes of PXD10 devices.

Table 1. Operating mode summary[1]

Operating modes	SOC features					Clock sources						Periodic Wake-up	Wake-up input	VREG mode	Wake-up time[2]						
	Core	Peripherals	Flash	RAM	Graphics RAM	Main PLL	Auxiliary PLL	16 MHz IRC	X OSC	128 kHz IRC	32 KHz X OSC				VREG start-up	IRC Wake-up	Flash Recovery	OSC Stabilization	PLL Lock	S/W Reconfig	Mode switch over
RUN	On	OP	OP	On	On	OP	OP	On	OP	On	OP	—	—	FP	—	—	—	—	—	—	—
HALT	CG	OP	OP	On	On	OP	OP	On	OP	On	OP	OP	OP	FP	—	—	—	—	—	—	TBD
STOP	CG	CG	CG	On	On	CG	CG	OP	OP	On	OP	OP	OP	LP	50 µs	4 µs	20 µs	1ms	200 µs	—	24 µs
STANDBY	Off	Off[3]	Off	CG[4]	Off	Off	Off	OP	OP	On	OP	OP	OP	LP	50 µs	8 µs	100 µs	1ms	200 µs	Var	28 µs
	Off	Off	Off	8K[5]	Off	Off	Off	OP	OP	On	OP	OP	OP	LP	50 µs	8 µs	100 µs	1ms	200 µs	Var	28 µs
POR															500 µs	8 µs	100 µs	1ms	200 µs		BAM

NOTES:

1 Table Key:

On—Powered and clocked

OP—Optionally configurable to be enabled or disabled (clock gated)

CG—Clock Gated, Powered but clock stopped

Off—Powered off and clock gated

FP—VREG Full Performance mode

LP—VREG Low Power mode, reduced output capability of VREG but lower power consumption

Var—Variable duration, based on the required reconfiguration and execution clock speed

BAM—Boot Assist Module Software and Hardware used for device start-up and configuration

2 A high level summary of some key durations that need to be considered when recovering from low power modes. This does not account for all durations at wake up. Other delays will be necessary to consider including, but not limited to the external supply start-up time.
IRC Wake-up time must not be added to the overall wake-up time as it starts in parallel with the VREG.
All other wake-up times must be added to determine the total start-up time

3 The LCD can optionally be kept running while the device is in STANDBY mode.

4 All of the RAM contents is retained, but not accessible in STANDBY mode.

5 8 KB of the RAM contents is retained, but not accessible in STANDBY mode.

Additional notes on low power operation:

- Fast wake-up using the on-chip 16 MHz internal RC oscillator allows rapid execution from RAM on exit from low power modes
- The 16 MHz internal RC oscillator supports low speed code execution and clocking of peripherals when it is selected as the system clock and can also be used as the PLL input clock source to provide fast start-up without the external oscillator delay
- PXD10 devices include an internal voltage regulator that includes the following features:
  - Regulates input to generate all internal supplies
  - Manages power gating
  - Low power regulators support operation when in STOP and STANDBY modes to minimize power consumption
  - Startup on-chip regulators in <50 µs for rapid exit of STOP and STANDBY modes
  - Low voltage detection on main supply and 1.2 V regulated supplies

1.6.2 e200z0h core processor

The e200z0h processor is similar to other processors in the e200zx series but supports only the VLE instruction set and does not include the signal processing extension for DSP applications or a floating point unit.

The e200z0h has all the features of the e200z0 plus:

- Branch acceleration using Branch Target Buffer (BTB)
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and Flash memory via independent Instruction and Data BIUs

The e200z0h processor uses a four stage in-order pipeline for instruction execution. The Instruction Fetch (stage 1), Instruction Decode/Register file Read/Effective Address Calculation (stage 2), Execute/Memory Access (stage 3), and Register Writeback (stage 4) stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

The integer execution unit consists of a 32-bit Arithmetic Unit (AU), a Logic Unit (LU), a 32-bit Barrel shifter (Shifter), a Mask-Insertion Unit (MIU), a Condition Register manipulation Unit (CRU), a Count-Leading-Zeros unit (CLZ), an 8 × 32 Hardware Multiplier array, result feed-forward hardware, and a hardware divider.

Most arithmetic and logical operations are executed in a single cycle with the exception of the divide and multiply instructions. A Count-Leading-Zeros unit operates in a single clock cycle. The Instruction Unit contains a PC incrementer and a dedicated Branch Address adder to minimize delays during change of flow operations. Branch target prefetching from the BTB is performed to accelerate certain taken branches. Sequential prefetching is performed to ensure a supply of instructions into the execution pipeline. Branch target prefetching is performed to accelerate taken branches. Prefetched instructions are placed into an instruction buffer capable of holding four instructions.

Conditional branches not taken execute in a single clock. Branches with successful target prefetching have an effective execution time of one clock on e200z0h. All other taken branches have an execution time of two clocks.

Memory load and store operations are provided for byte, halfword, and word (32-bit) data with automatic zero or sign extension of byte and halfword load data as well as optional byte reversal of data. These instructions can be pipelined to allow effective single cycle throughput. Load and store multiple word instructions allow low overhead context save and restore operations. The load/store unit contains a dedicated effective address adder to allow effective address generation to be optimized. Also, a load-to-use dependency does not incur any pipeline bubbles for most cases.

The Condition Register unit supports the condition register (CR) and condition register operations defined by the Power Architecture. The condition register consists of eight 4-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching.

Vectored and autovectored interrupts are supported. Hardware vectored interrupt support is provided to allow multiple interrupt sources to have unique interrupt handlers invoked with no software overhead.

The CPU includes support for Variable Length Encoding (VLE) instruction enhancements. This allows the classic PowerPC instruction set to be represented by a modified instruction set made up from a mixture of 16-bit and 32-bit instructions. This results in a significantly smaller code size footprint without affecting performance noticeably.

The CPU core is enhanced by an additional interrupt source—Non Maskable Interrupt. This interrupt source is routed directly from package pins, via edge detection logic in the SIU to the CPU, bypassing the Interrupt Controller completely. Once the edge detection logic is programmed, it can not be disabled, except by reset. The Non Maskable Interrupt is, as the name suggests, completely un-maskable and when asserted will always result in the immediate execution of the respective interrupt service routine. The Non maskable interrupt is not guaranteed to be recoverable.

The CPU core has an additional ‘Wait for Interrupt’ instruction that is used in conjunction with low power STOP mode. When Low Power Stop mode is selected, this instruction is executed to allow the system clock to be stopped. An external interrupt source or the system wake-up timer is used to restart the system clock and allow the CPU to service the interrupt.

Additional features include:

- Load/store unit
  - 1-cycle load latency
  - Misaligned access support
  - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Reservation instructions for implementing read-modify-write constructs
- Multi-cycle divide (divw) and load multiple (lmw) store multiple (smw) multiple class instructions, can be interrupted to prevent increases in interrupt latency
- Extensive system development support through Nexus debug port

1.6.3 Display Control Unit (DCU)

The DCU is a display controller designed to drive TFT LCD displays capable of driving up to WQVGA resolution screens with 16 layers and 4 planes with real time alpha-blending.

The DCU generates all the necessary signals required to drive the display: up to 24-bit RGB data bus, Pixel Clock, Data Enable, Horizontal-Sync and Vertical-Sync.

Internal memory resource of the PXD10 allows to easily handle complex graphics contents (pictures, icons, languages, fonts) on a color TFT panel in up to Wide Quarter Video Graphics Array (WQVGA) sizes. All the data fetches from internal and/or external memory are performed by the internal four-channel DMA of the DCU providing a high speed/low latency access to the system backbone.

Control Descriptors (CDs) associated with each layer enable effective merging of different resolutions into one plane to optimize use of internal memory buffers. A layer may be constructed from graphic content of various resolutions including 1bpp, 2bpp, 4bpp, 8bpp, 16bpp, 24bpp and 24bpp+alpha. The ability of the DCU to handle input data in resolutions as low as 1bpp, 2bpp and 4bpp enables a highly efficient use of internal memory resources of the PXD10. A special tiled mode can be enabled on any of the 16 layers to repeat a pattern optimizing graphic memory usage.

A hardware cursor can be managed independently of the layers at blending level increasing the efficient use of the internal DCU resources.

To secure the content of all critical information to be displayed, a safety mode can be activated to check the integrity of critical data along the whole system data path from the memory to the TFT pads.

The DCU features the following:

- Display color depth: up to 24 bpp
- Generation of all RGB and control signals for TFT
- Four-plane blending
- Maximum number of Input Layers: 16 (fixed priority)
- Dynamic look-up table (color and gamma look-up)
- α–blending range: as many as 256 levels
- Transparency Mode
- Gamma Correction
- Tiled mode on all the layers
- Hardware cursor
- Critical display content integrity monitoring for functional safety support
- Internal Direct Memory Access (DMA) module to transfer data from internal and/or external memory.

1.6.4 Parallel Data Interface (PDI)

The PDI is a digital interface used to receive external digital video or graphic content into the DCU.

The PDI input is directly injected into the DCU background plane FIFO. When the PDI is activated, all the DCU synchronization is extracted from the external video stream to guarantee the synchronization of the two video sources.

The PDI can be used to:

- Connect a video camera output directly to the PDI
- Connect a secondary display driver as slave with a minimum of extra cost
- Connect a device gathering various Video sources
- Provide flexibility to allow the DCU to be used in slave mode (external synchronization)

The PDI features the following:

- Supported color modes:
  - 8-bit mono
  - 8-bit color multiplexed
  - RGB565
  - 16-bit/18-bit RAW color
- Supported synchronization modes:
  - Embedded ITU-R BT.656-4 (RGB565 mode 2)
  - HSYNC, VSYNC
  - Data Enable
- Direct interface with DCU background plane FIFO
- Synchronization generation for the DCU

1.6.5 Liquid Crystal Display (LCD) driver

The LCD driver module has two configurations allowing a maximum of 160 or 228 LCD segments:

- As many as 40 frontplane drivers and four backplane drivers
- As many as 38 frontplane drivers and six backplane drivers

Each segment is controlled and can be masked by a corresponding bit in the LCD RAM.

Four to six multiplex modes (1/1, 1/2, 1/3, 1/4, 1/5, 1/6 duty), and three bias (1/1, 1/2, 1/3) methods are available. All frontplane and backplane pins can be multiplexed with other port functions.

The LCD driver module features the following:

- Programmable frame clock generator from different clock sources:
  - System clock
  - Internal RC oscillator
- Programmable bias voltage level selector
- On-chip generation of all output voltage levels

  - LCD voltage reference taken from main 5V supply
- LCD RAM
  - Contains the data to be displayed on the LCD
  - Data can be read from or written to the display RAM at any time
- End of Frame interrupt
  - Optimizes the refresh of the data without visual artefact
  - Provides selectable number of frames between each interrupt
- Contrast adjustment using programmable internal voltage reference
- Remapping capability of four or six backplanes with frontplanes
  - Increase pin selection flexibility
- In low power modes, the LCD operation can be suspended under software control. The LCD can also operate in low power modes, clocked by the internal 128 kHz IRC or external 32 KHz crystal oscillator
- Selectable output current boost during transitions

1.6.6 Stepper Motor Controller (SMC)

The SMC module is a PWM motor controller suitable to drive loads requiring a PWM signal. The motor controller has twelve PWM channels associated with two pins each (24 pins in total).

The SMC module includes the following features:

- 10/11-bit PWM counter
- 11-bit resolution with selectable PWM dithering function
- Left, right, or center aligned PWM
- Output slew rate control
- Output Short Circuit Detection

This module is suited for, but not limited to, driving small stepper and air core motors used in instrumentation applications. This module can be used for other motor control or PWM applications that match the frequency, resolution, and output drive capabilities of the module.

1.6.7 Stepper Stall Detector (SSD)

The stepper stall detector (SSD) module provides a circuit to measure and integrate the induced voltage on the non-driven coil of a stepper motor using full steps when the gauge pointer is returning to zero (RTZ).

The SSD module features the following:

- Programmable full step state
- Programmable integration polarity
- Blanking (recirculation) state
- 16-bit integration accumulator register
- 16-bit modulus down counter with interrupt

1.6.8 Flash memory

The PXD10 microcontroller has the following flash memory features:

- As much as 1 MB of burst flash memory
  - — Typical flash memory access time: 0 wait-state for buffer hits, 2 wait-states for page buffer miss at 64 MHz
  - — Two 4 × 128-bit page buffers with programmable prefetch control
    - – One set of page buffers can be allocated for code-only, fixed partitions of code and data, all available for any access
    - – One set of page buffers allocated to Display Controller Unit and the eDMA
  - — 64-bit ECC with single-bit correction, double-bit detection for data integrity
  - — 64 KB data flash memory — separate 4 × 16 KB flash block for EEPROM emulation with prefetch buffer and 128-bit data access port
- Small block flash memory arrangement to support features such as boot block, operating system block
- Hardware managed flash memory writes, erase and verify sequence
- Censorship protection scheme to prevent flash memory content visibility
- Separate dedicated 64 KB data flash memory for EEPROM emulation
  - — Four erase sectors each containing 16 KB of memory
  - — Offers Read-While-Write functionality from main program space
  - — Same data retention and program erase specification as main program flash memory array

1.6.9 Static random-access memory (SRAM)

The PXD10 microcontrollers have as much as 48 KB general-purpose on-chip SRAM with the following features:

- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait-state for 8- and 16-bit writes if back to back with a read to same memory block
- 32-bit ECC with single-bit correction, double bit detection for data integrity
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- User transparent ECC encoding and decoding for byte, half word, and word accesses
- Separate internal power domain applied to full SRAM block, 8 KB SRAM block during STANDBY modes to retain contents during low power mode.

1.6.10 On-chip graphics SRAM

The PXD10 microcontroller has 160 KB on-chip graphics SRAM with the following features:

- Usable as general purpose SRAM
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory

1.6.11 QuadSPI serial flash controller

The QuadSPI module enables use of external serial flash memories supporting single, dual and quad modes of operation. It features the following:

- Memory mapping of external serial flash
- Automatic serial flash read command generation by CPU, DMA or DCU read access on AHB bus
- Supports single, dual and quad serial flash read commands
- Flexible buffering scheme to maximize read bandwidth of serial flash
- 'Legacy' mode allowing QuadSPI to be used as a standard SPI (no DSI or CSI mode)

1.6.12 Analog-to-digital converter (ADC)

The ADC features the following:

- 10-bit A/D resolution
- 0 to 5 V common mode conversion range
- Supports conversions speeds of as fast as 1 µs
- 16 internal and 8 external channels support
- As many as 16 single-ended inputs channels
  - All channels configured to have alternate function as general purpose input/output pins
    - 10-bit ±3 counts accuracy (TUE)
- External multiplexer support to increase as many as 23 channels
  - Automatic 1 × 8 multiplexer control
  - External multiplexer connected to a dedicated input channel
  - Shared register between the 8 external channels
- Result register available for every non-multiplexed channel
- Configurable left- or right-aligned result format
- Supports for one-shot, scan and injection conversion modes
- Injection mode status bit implemented on adjacent 16-bit register for each result
  - Supports access to result and injection status with single 32-bit read
- Independently enabling of function for channels:
  - Pre-sampling
  - Offset error cancellation
  - Offset refresh
- Conversion Triggering support
  - Internal conversion triggering from periodic interrupt timer (PIT)
- Four configurable analog comparator channels offering range comparison with triggered alarm
  - Greater than
  - Less than
  - Out of range

- All unused analog inputs can be used as general purpose input and output pins
- Power down mode
- Optional support for DMA transfer of results

1.6.13 Sound generation logic (SGL) module

The SGL module has two modes of operation:

- Amplitude modulated PWM mode for low cost buzzers using any two eMIOS channels
  - — Monophonic signal with amplitude control
  - — 8-bit amplitude resolution
  - — Ability to mix any two eMIOS channels.
  - — Requires simple external RC lowpass filter
- Digital sample mode for higher quality sound using one eMIOS channel and eDMA
  - — Up to 10-bit audio amplitude resolution
  - — Polyphonic sound synthesis
  - — Playback of sample based waveforms
  - — Text-to-speech possibility
  - — Requires external lowpass filter

1.6.14 Serial communication interface module (UART)

The PXD10 devices include as many as two UART modules and support UART Master mode, UART Slave mode and UART mode. The modules are UART state machine compliant to the UART 1.3 and 2.0 and 2.1 Specifications and handle UART frame transmission and reception without CPU intervention.

The serial communication interface module offers the following:

- UART features:
  - — Full-duplex operation
  - — Standard non return-to-zero (NRZ) mark/space format
  - — Data buffers with 4-byte receive, 4-byte transmit
  - — Configurable word length (8-bit or 9-bit words)
  - — Error detection and flagging
    - – Parity, noise and framing errors
  - — Interrupt driven operation with four interrupts sources
  - — Separate transmitter and receiver CPU interrupt sources
  - — 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - — Two receiver wake-up methods
- LIN features:
  - — Autonomous LIN frame handling
  - — Message buffer to store identifier and as many as 8 data bytes

- — Supports message length of as long as 64 bytes
- — Detection and flagging of LIN errors
- — Sync field; Delimiter; ID parity; Bit, Framing; Checksum and Timeout errors
- — Classic or extended checksum calculation
- — Configurable Break duration of up to 36-bit times
- — Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
- — Diagnostic features
  - – Loop back
  - – Self Test
  - – LIN bus stuck dominant detection
- — Interrupt driven operation with 16 interrupt sources
- — LIN slave mode features
  - – Autonomous LIN header handling
  - – Autonomous LIN response handling
  - – Discarding of irrelevant LIN responses using as many as 16 ID filters

1.6.15 Serial Peripheral Interface (SPI) module

The SPI modules provide a synchronous serial interface for communication between the PXD10 MCU and external devices.

The SPI features the following:

- As many as two SPI modules
- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from four to 16 bits
- As many as six chip select lines available, depending on package and pin multiplexing, enable 64 external devices to be selected using external muxing from a single SPI
- Eight clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering as many as four transfers on the transmit and receive side
- General purpose I/O functionality on pins when not used for SPI
- Queueing operation possible through use of eDMA

1.6.16 Controller Area Network (CAN) module

The PXD10 contains two CAN modules that offer the following features:

- Compliant with CAN protocol specification, Version 2.0B active
- 64 mailboxes, each configurable as transmit or receive
  - Mailboxes configurable while module remains synchronized to CAN bus
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid PLL jitter
- Listen only mode capabilities
- CAN Sampler
  - Can catch the first message sent on the CAN network while the PXD10 is stopped. This guarantees a clean startup of the system without missing messages on the CAN network.
  - The CAN sampler is connected to one of the CAN RX pins.

1.6.17 Inter-IC Communications (I^2C) module

The I^2C module features the following:

- As many as four I^2C modules supported
- Two-wire bi-directional serial bus for on-board communications
- Compatibility with I^2C bus standard
- Multimaster operation
- Software-programmable for one of 256 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

1.6.18 Real Time Counter (RTC)

The Real Timer Counter supports wake-up from Low Power modes or Real Time Clock generation

- Configurable resolution for different timeout periods
  - 1 s resolution for >1 hour period
  - 1 ms resolution for 2 second period
- Selectable clock sources from external 32 KHz crystal, external 4–16 MHz crystal, internal 128 kHz RC oscillator or divided internal 16 MHz RC oscillator

1.6.19 Enhanced Modular Input/Output System (Timers, PWM)

PXD10 microcontrollers have two eMIOS modules—one with 16 channels and one with 8—with input/output channels supporting a range of 16-bit input capture, output compare, and Pulse Width Modulation functions.

The modules are configurable and can implement 8-channel, 16-bit input capture/output compare or 16-channel, 16-bit output pulse width modulation/input compare/output compare. As many as five additional channels are configurable as modulus counters.

eMIOS features include:

- Selectable clock source from main FMPLL, auxiliary FMPLL, external 4–16 MHz oscillator or 16 MHz Internal RC oscillator
- Timed I/O channels with 16-bit counter resolution
- Buffered updates
- Support for shifted PWM outputs to minimize occurrence of concurrent edges
- Edge aligned output pulse width modulation
  - Programmable pulse period and duty cycle
  - Supports 0% and 100% duty cycle
  - Shared or independent time bases
- Programmable phase shift between channels
- Selectable combination of pairs of eMIOS outputs to support sound generation
- DMA transfer support
- Selectable clock source from the primary FMPLL, auxiliary FMPLL, external 4–16 MHz oscillator or the 16 MHz internal RC oscillator.

The channel configuration options for the 16-channel eMIOS module are summarized in Table 2.

Table 2. 16-channel eMIOS module channel configuration

Channel mode	Channel number				
	8 IC/OC Counter	9–15 IC/OC	16 PWM Counter	17–22 PWM	23 PWM Counter
General Purpose Input/Output	X	X	X	X	X
Single Action Input Capture	X	X	X	X	X
Single Action Output Compare	X	X	X	X	X
Modulus Counter Buffered[1]	X		X		X
Output Pulse Width and Frequency Modulation Buffered			X	X	X
Output Pulse Width Modulation Buffered			X	X	X

NOTES:
1 Modulus up and down counters to support driving local and global counter busses

The channel configuration options for the 8-channel eMIOS module are summarized in Table 3.

Table 3. 8-Channel eMIOS module channel configuration

Channel mode	Channel number		
	16 PWM Counter	17–22 PWM	23 PWM Counter
General Purpose Input/Output	X	X	X
Single Action Input Capture	X	X	X
Single Action Output Compare	X	X	X
Modulus Counter Buffered[1]	X		X
Output Pulse Width and Frequency Modulation Buffered	X	X	X
Output Pulse Width Modulation Buffered	X	X	X

NOTES:
1 Modulus up and down counters to support driving local and global counter busses

1.6.20 Periodic interrupt timer (PIT) module

The PIT features the following:

- Four general purpose interrupt timers
- As many as two dedicated interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency
- 32-bit counter for Real Time Interrupt, clocked from main external oscillator

1.6.21 System Timer Module (STM)

The STM is a 32-bit timer that supports commonly required system and application software timing functions. The STM includes a 32-bit up counter and four 32-bit compare channels with a separate interrupt source for each channel. The counter is driven by the system clock divided by an 8-bit prescale value (1 to 256).

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.6.22 Software Watchdog Timer (SWT)

The SWT features the following:

- Watchdog supporting software activation or enabled out of reset
- Supports normal or windowed mode
- Watchdog timer value writable once after reset
- Watchdog supports optional halting during low power modes
- Configurable response on timeout: reset, interrupt, or interrupt followed by reset
- Selectable clock source for main system clock or internal 16 MHz RC oscillator clock

1.6.23 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

Multiple processors can assert interrupt requests to each other through software settable interrupt requests. These same software settable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software settable interrupt request to finish the servicing in a lower priority ISR. Therefore these software settable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS. The INTC provides the following features:

- Unique 9-bit vector for each of the possible 128 separate interrupt sources
- Eight software-triggerable interrupt sources

- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority.
  - — Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- External non-maskable interrupt directly accessing the main core critical interrupt mechanism
- 32 external interrupts

1.6.24 System Integration Unit (SIU)

The SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.

The GPIO features the following:

- As many as four levels of internal pin multiplexing, allowing exceptional flexibility in the allocation of device functions for each package
- Centralized general purpose input output (GPIO) control of as many as 132 input/output pins (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins can be alternatively configured as both general purpose input or output pins except ADC channels which support alternative configuration as general purpose inputs
- Direct readback of the pin value supported on all digital output pins through the SIU
- Configurable digital input filter that can be applied to as many as 14 general purpose input pins for noise elimination on external interrupts
- Register configuration protected against change with soft lock for temporary guard or hard lock to prevent modification until next reset.

1.6.25 System Clocks and Clock Generation Modules

The system clock on the PXD10 can be derived from an external oscillator, an on-chip FMPLL, or the internal 16 MHz oscillator.

- The source system clock frequency can be changed via an on-chip programmable clock divider (÷1 to ÷32).
- Additional programmable peripheral bus clock divider ratio (÷1 to ÷16)
- The PXD10 has two on-chip FMPLLs—the primary module and an auxiliary module.
  - — Each features the following:
    - – Input clock frequency from 4 MHz to 16 MHz
    - – Lock detect circuitry continuously monitors lock status
    - – Loss Of Clock (LOC) detection for reference and feedback clocks
    - – On-chip loop filter (for improved electromagnetic interference performance and reduction of number of external components required)

  - Support for frequency ramping from PLL
  - The primary FMPLL module is for use as a system clock source. The auxiliary FMPLL is available for use as an alternate, modulated or non-modulated clock source to eMIOS modules and as alternate clock to the DCU for pixel clock generation.
- The main oscillator provides the following features:
  - Input frequency range 4–16 MHz
  - Square-wave input mode
  - Oscillator input mode 3.3 V (5.0 V)
  - Automatic level control
  - PLL reference
- PXD10 includes a 32 KHz low power external oscillator for slow execution, low power, and Real Time Clock
- Dedicated internal 128 kHz RC oscillator for low power mode operation and self wake-up
  - ±10% accuracy across voltage and temperature (after factory trimming)
  - Trimming registers to support improved accuracy with in-application calibration
- Dedicated 16 MHz internal RC oscillator
  - Used as default clock source out of reset
  - Provides a clock for rapid start-up from low power modes
  - Provides a back-up clock in the event of PLL or External Oscillator clock failure
  - Offers an independent clock source for the Watchdog timer
  - ±5% accuracy across voltage and temperature (after factory trimming)
  - Trimming registers to support frequency adjustment with in-application calibration

1.6.26 Crossbar Switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows four concurrent transactions to occur from any master port to any slave port but one of those transfers must be an instruction fetch from internal flash. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters having equal priority are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- Four master ports
  - e200z0h core instruction port
  - e200z0h core complex load/store data port
  - eDMA controller
  - Display control unit

- Four slave ports
  - — One flash port dedicated to the CPU
  - — Platform SRAM
  - — QuadSPI serial flash controller
  - — One slave port combining:
    - – Flash port dedicated to the Display Control Unit and eDMA module
    - – Graphics SRAM
    - – Peripheral bridge
- 32-bit internal address bus, 32-bit internal data bus

1.6.27 Enhanced Direct Memory Access (eDMA)

The eDMA module is a controller capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size. The eDMA module provides the following features:

- 16 channels support independent 8-, 16- or 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, periodic timer interrupt or eDMA channel request
- Each DMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, QuadSPI, SPIs, I^2C, ADC, eMIOS and General Purpose I/Os (GPIOs)
- Programmable DMA Channel Mux allows assignment of any DMA source to any available DMA channel with a total of as many as 64 potential request sources.

1.6.28 Memory Protection Unit (MPU)

The MPU features the following:

- 12 region descriptors for per-master protection
- Start and end address defined with 32-byte granularity
- Overlapping regions supported
- Protection attributes can optionally include process ID
- Protection offered for 3 concurrent read ports
- Read and write attributes for all masters
- Execute and supervisor/user mode attributes for processor masters

1.6.29 Boot Assist Module (BAM)

The BAM is a block of read-only memory that is programmed once by Freescale. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (A program is downloaded into RAM via CAN or UART and then executed)
- Booting from external memory

Additionally, the BAM:

- Enables and manages the transition of the MCU from reset to user code execution
- Configures device for serial bootload
- Enables multiple bootcode starting locations out of reset through implementation of search for valid Reset Configuration Halfword
- Enables or disables software watchdog timer out of reset through BAM read of the Reset Configuration Halfword option bit

1.6.30 IEEE 1149.1 JTAG Controller (JTAGC)

JTAGC features the following:

- Backward compatible to standard JTAG IEEE 1149.1-2001 test access port (TAP) interface
- Support for boundary scan testing

1.6.31 Nexus Development Interface (NDI)

Nexus features the following:

- Per IEEE-ISTO 5001-2003
- Nexus 2 Plus features supported
  - — Static debug
  - — Watchpoint messaging
  - — Ownership trace messaging
  - — Program trace messaging
  - — Real time read/write of any internally memory mapped resources through JTAG pins
  - — Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information
  - — Watchpoint triggering, watchpoint triggers program tracing
- Configured via the IEEE 1149.1 (JTAG) port
- Nexus Auxiliary port supported on the 176 LQFP package FOR DEVELOPMENT ONLY
  - — Narrow Auxiliary Nexus port supporting support trace, with two MDO pins
  - — Wide Auxiliary Nexus port supporting higher bandwidth trace, with four MDO pins

2 Pinout and signal descriptions

2.1 144 LQFP package pinouts

This section shows the pinouts for the 144-pin LQFP packages.

CAUTION

Any pins labeled “NC” must not be connected to any external circuit.

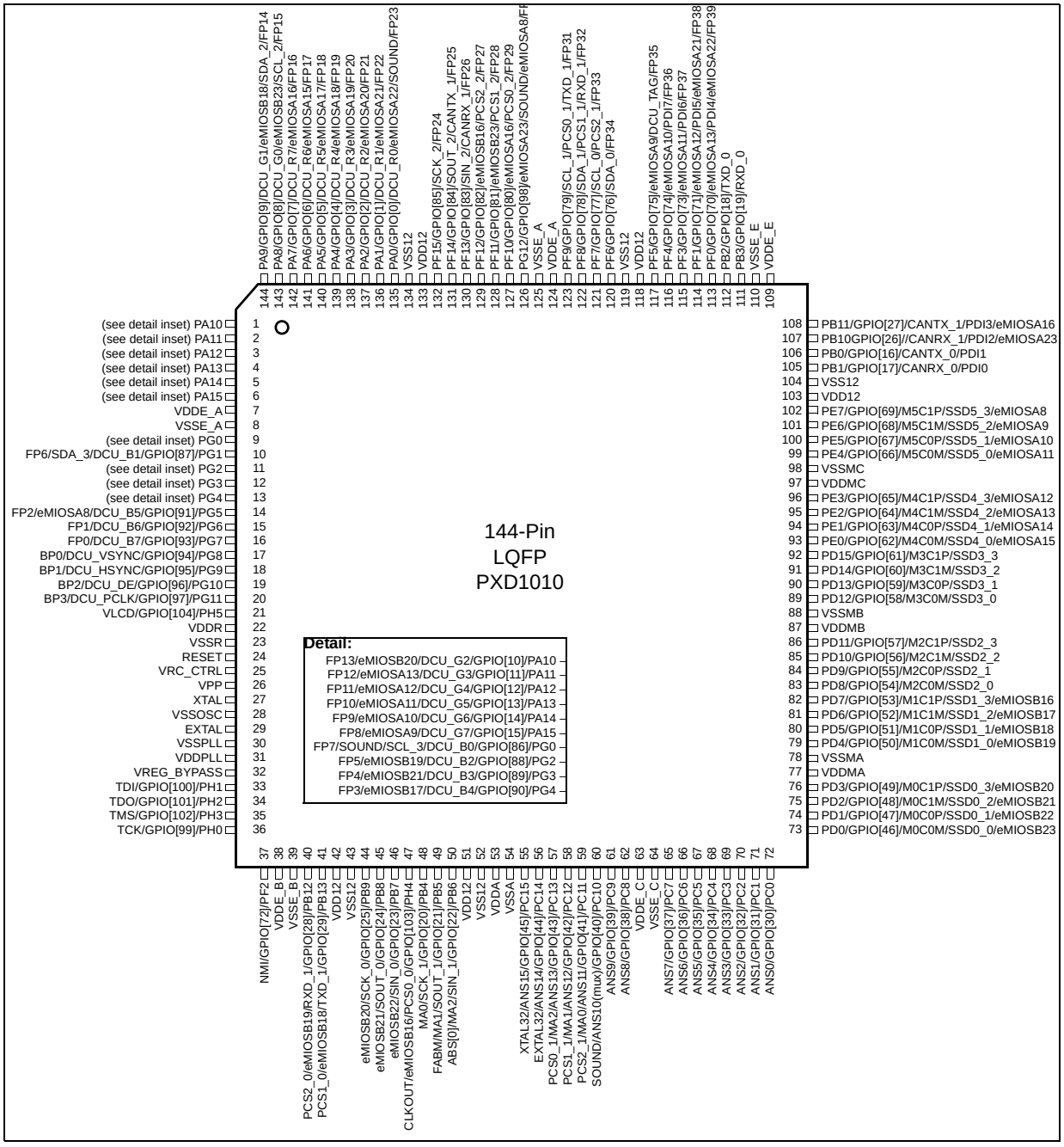


Figure 2. 144-pin LQFP pinout for PXD1010

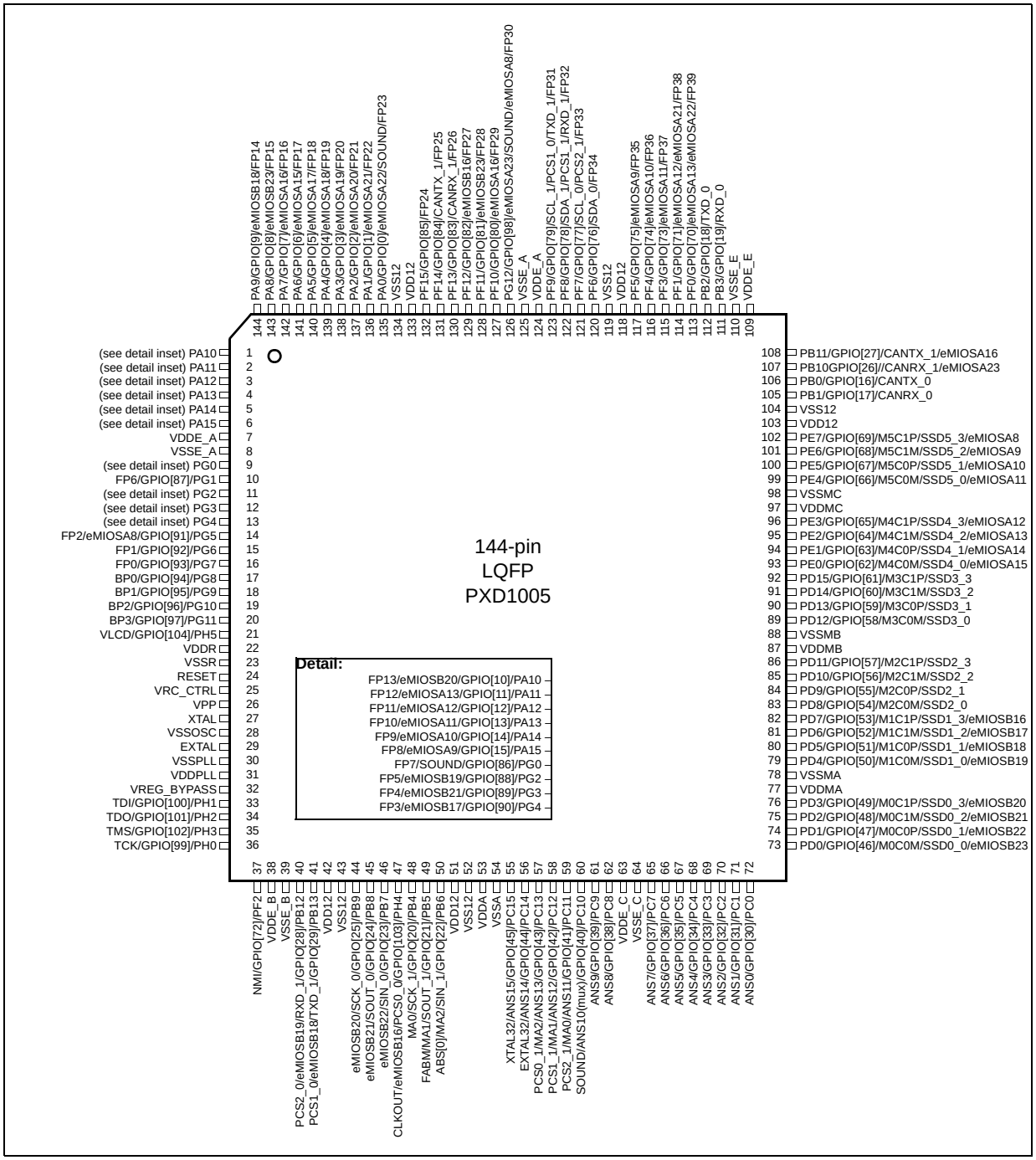


Figure 3. 144-pin LQFP pinout for PXD1005

2.2 176 LQFP package pinout

Figure 4 shows the pinout for the 176-pin LQFP package.

CAUTION

Any pins labeled “NC” must not be connected to any external circuit.

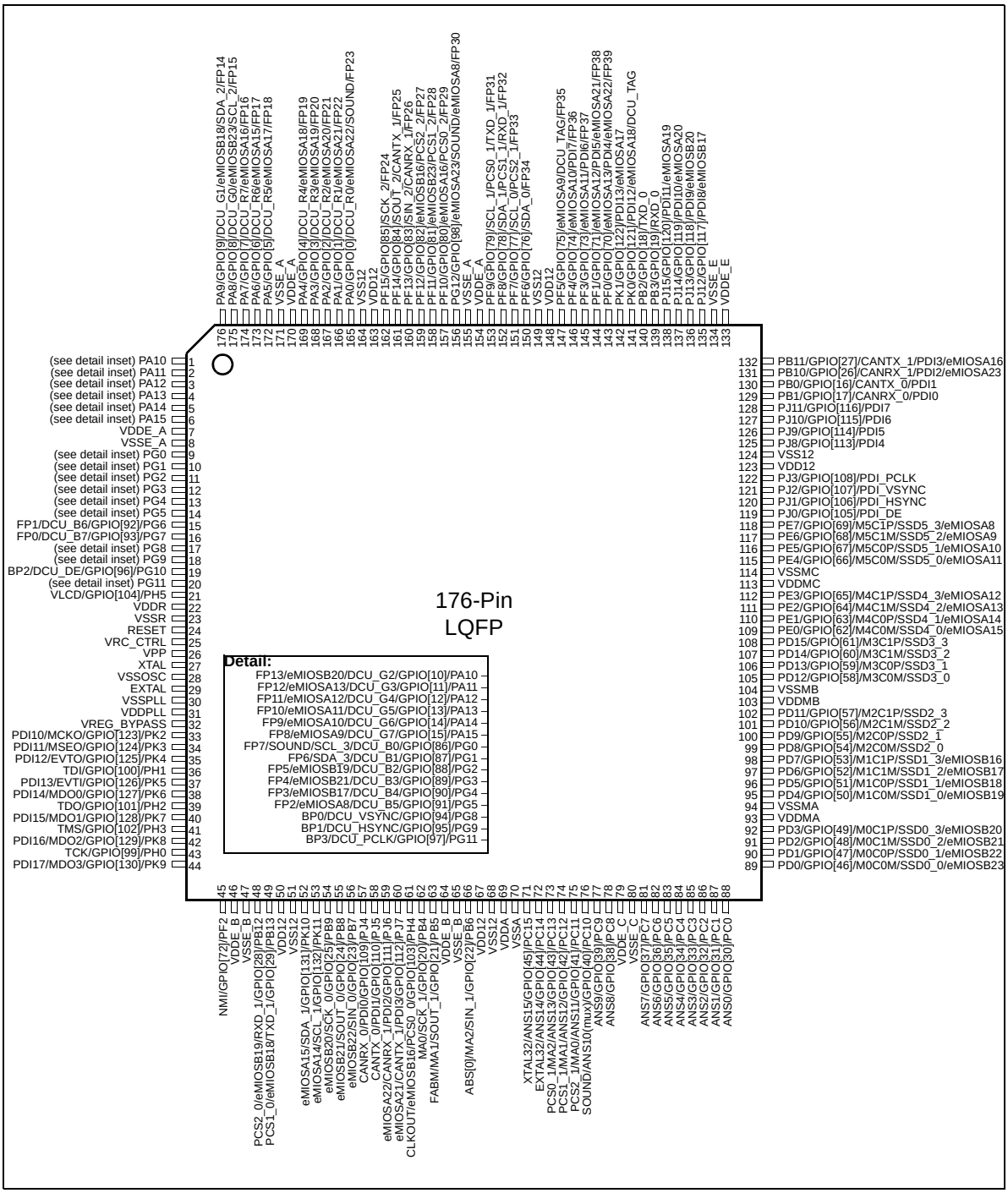


Figure 4. 176-pin LQFP pinout

2.3 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are floating with the following exceptions:

- PB[5] (FAB) is pull-down. Without external strong pullup the device starts fetching from flash.
- RESET pad is driven low. This is released only after PHASE2 reset completion.
- Main oscillator pads (EXTAL, XTAL) are tristate.
- Nexus output pads (MDO[n], MCKO, EVTO, MSEO) are forced to output.
- The following pads are pullup:
  - PB[6]
  - PH[0]
  - PH[1]
  - PH[3]
  - EVTI

2.4 Voltage supply pins

Voltage supply pins are used to provide power to the device. Two dedicated pins are used for 1.2 V regulator stabilization.

There is a preferred power-up sequence for devices in the PXD10 family. That sequence is described in the following paragraphs.

Broadly, the supply voltages can be grouped as follows:

- VREG HV supply (V_{DDR})
- Generic I/O supply
  - V_{DDA}
  - V_{DDE_A}
  - V_{DDE_B}
  - V_{DDE_C}
  - V_{DDE_E}
  - V_{DDMA}
  - V_{DDMB}
  - V_{DDMC}
  - V_{DDPLL}
- LV supply (V_{DD12})

The preferred order of ramp up is as follows:

1. Generic I/O supply

2. VREG HV supply (V_{DDR} - Should be the last HV supply to ramp up. It is also OK if all HV and generic I/O supplies including V_{DDR} ramp up together)
3. LV supply

The reason for following this sequence is to ensure that when VREG releases its LVDs, the I/O and other HV segments are powered properly. This is important because the PXD10 does not monitor LVDs on I/O HV supplies.

Table 2. Voltage supply pin descriptions

Supply Pin	Function	Pin number	
		144 LQFP	176 LQFP
VDD12[1]	1.2 V core supply	42, 51, 103, 118, 133	50, 67, 123, 148, 163
VDDA	3.3 V/5 V ADC supply source	53	69
VDDE_A	3.3 V/5 V I/O supply	7, 124	7, 154, 170
VDDE_B	3.3 V/5 V I/O supply	38	46, 64
VDDE_C	3.3 V/5 V I/O supply	63	79
VDDE_E	3.3 V/5 V I/O supply	109	133
VDDMA[2]	Motor pads 5 V supply	77	93
VDDMB[2]	Motor pads 5 V supply	87	103
VDDMC[2]	Motor pads 5 V supply	97	113
VDDPLL	1.2 V PLL supply	31	31
VDDR	VREG reg supply	22	22
VPP[3]	9 V - 12 V flash test analog write signal	26	26
VSS	Digital ground	8, 23, 39, 43, 52, 64, 104, 110, 119, 125, 134	8, 23, 47, 51, 68, 80, 124, 134, 149, 155, 164, 65, 171
VSSA	ADC ground	54	70
VSSMA	Stepper motor ground	78	94
VSSMB	Stepper motor ground	88	104
VSSMC	Stepper motor ground	98	114
VSSOSC	MHz oscillator ground	28	28
VSSPLL	PLL ground	30	30

NOTES:
1 Decoupling capacitors must be connected between these pins and the nearest V_{SS12} pin.
2 All stepper motor supplies need to be at same level (3.3 V or 5 V).
3 This signal needs to be connected to ground during normal operation.

2.5 Pad types

The pads available for system pins and functional port pins are described in:

- The port pin summary table
- The pad type descriptions

- The description of the pad configuration registers in Chapter 37, System Integration Unit Lite (SIUL)
- The device data sheet

2.6 System pins

The system pins are listed in Table 3.

Table 3. System pin descriptions

System pin	Function	I/O direction	Pad type	RESET config	Pin No.		
					144 LQFP	176 LQFP	208 MAPBGA
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull up	24	24	J1
EXTAL	Analog output of the oscillator amplifier circuit. Input for the clock generator in bypass mode.		X	—	29	29	M1
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	X	—	27	27	K1
VRC_CTRL	VREG ballast control gain	—	—	—	25	25	P1
VREG_BYPASS[1]	Pin used for factory testing	I	X	—	32	32	M4

NOTES:
1 VREG_BYPASS should be pulled down externally.

2.7 Debug pins

The debug pins are listed in Table 4 and Table 5.

Table 4. Debug pin descriptions

Debug pin	Function	Pad type	I/O direction	Reset Configuration	Pin number		
					144 LQFP	176 LQFP [1]	208 MAPBGA
EVTI	Nexus event input	M	I/O	None	—	37	A11
EVTO	Nexus event output	M	I/O	None	—	35	D12
MCKO	Nexus message clock output	F	I/O	None	—	33	B12
MDO0	Nexus message clock output	M	I/O	None	—	38	B11

Table 4. Debug pin descriptions (continued)

Debug pin	Function	Pad type	I/O direction	Reset Configuration	Pin number		
					144 LQFP	176 LQFP [1]	208 MAPBGA
MDO1	Nexus message clock output	M	I/O	None	—	40	C11
MDO2	Nexus message clock output	M	I/O	None	—	42	D11
MDO3	Nexus message clock output	M	I/O	None	—	44	A10
MSEO	Nexus message clock output	M	I/O	None	—	34	C12

NOTES:
1 On the 176 LQFP package options the Nexus pins are multiplexed with other GPIO. On the 208 TEPBGA package, there are additional dedicated Nexus pins.

Table 5. Debug pin descriptions

Debug pin	Function	Pad type	I/O direction	Reset Configuration	Pin number		
					144 LQFP	176 LQFP	TEPBGA208 [1]
EVTI	Nexus event input	M	I/O	Input, Pull Up	—	—	T3
EVTO	Nexus event output	M	I/O	Input, Pull Up	—	—	R3
MCKO	Nexus message clock output	F	I/O	Input, Pull Up	—	—	T1
MDO0	Nexus message clock output	M	I/O	Input, Pull Up	—	—	T5
MDO1	Nexus message clock output	M	I/O	Input, Pull Up	—	—	P5
MDO2	Nexus message clock output	M	I/O	Input, Pull Up	—	—	P4
MDO3	Nexus message clock output	M	I/O	Input, Pull Up	—	—	L4
MSEO	Nexus message clock output	M	I/O	Input, Pull Up	—	—	T2

NOTES:
1 The dedicated (208 pin package only) Nexus output pins (Message Data outputs 0:3 [MDO] and Message Start/End outputs 0:1 [MSEO]) may drive an unknown value (high or low) immediately after power up but before-the 1st clock edge propagates through the device (instead of being weakly pulled low). This may cause high currents if the pins are tied directly to a supply/ground or any low resistance-driver (when used as a general purpose input [GPI] in the application).

2.8 Port pin summary

The functional port pins are listed in Table 6.

Table 6. Port pin summary

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PA[0]	PCR[0]	Option 0 Option 1 Option 2 Option 3	GPIO[0] DCU_R0 eMIOSA[22] SOUND	FP23	SIUL DCU PWM/Timer Sound	I/O	M1	None, None	135	165
PA[1]	PCR[1]	Option 0 Option 1 Option 2 Option 3	GPIO[1] DCU_R1 eMIOSA[21] —	FP22	SIUL DCU PWM/Timer —	I/O	M1	None, None	136	166
PA[2]	PCR[2]	Option 0 Option 1 Option 2 Option 3	GPIO[2] DCU_R2 eMIOSA[20] —	FP21	SIUL DCU PWM/Timer —	I/O	M1	None, None	137	167
PA[3]	PCR[3]	Option 0 Option 1 Option 2 Option 3	GPIO[3] DCU_R3 eMIOSA[19] —	FP20	SIUL DCU PWM/Timer —	I/O	M1	None, None	138	168
PA[4]	PCR[4]	Option 0 Option 1 Option 2 Option 3	GPIO[4] DCU_R4 eMIOSA[18] —	FP19	SIUL DCU PWM/Timer —	I/O	M1	None, None	139	169
PA[5]	PCR[5]	Option 0 Option 1 Option 2 Option 3	GPIO[5] DCU_R5 eMIOSA[17] —	FP18	SIUL DCU PWM/Timer —	I/O	M1	None, None	140	172
PA[6]	PCR[6]	Option 0 Option 1 Option 2 Option 3	GPIO[6] DCU_R6 eMIOSA[15] —	FP17	SIUL DCU PWM/Timer —	I/O	M1	None, None	141	173
PA[7]	PCR[7]	Option 0 Option 1 Option 2 Option 3	GPIO[7] DCU_R7 eMIOSA[16] —	FP16	SIUL DCU PWM/Timer —	I/O	M1	None, None	142	174

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PA[8]	PCR[8]	Option 0 Option 1 Option 2 Option 3	GPIO[8] DCU_G0 eMIOSB[23] SCL_2	FP15	SIUL DCU PWM/Timer I^2C_2	I/O	M1	None, None	143	175
PA[9]	PCR[9]	Option 0 Option 1 Option 2 Option 3	GPIO[9] DCU_G1 eMIOSB[18] SDA_2	FP14	SIUL DCU PWM/Timer I^2C_2	I/O	M1	None, None	144	176
PA[10]	PCR[10]	Option 0 Option 1 Option 2 Option 3	GPIO[10] DCU_G2 eMIOSB[20] —	FP13	SIUL DCU PWM/Timer —	I/O	M1	None, None	1	1
PA[11]	PCR[11]	Option 0 Option 1 Option 2 Option 3	GPIO[11] DCU_G3 eMIOSA[13] —	FP12	SIUL DCU PWM/Timer —	I/O	M1	None, None	2	2
PA[12]	PCR[12]	Option 0 Option 1 Option 2 Option 3	GPIO[12] DCU_G4 eMIOSA[12] —	FP11	SIUL DCU PWM/Timer —	I/O	M1	None, None	3	3
PA[13]	PCR[13]	Option 0 Option 1 Option 2 Option 3	GPIO[13] DCU_G5 eMIOSA[11] —	FP10	SIUL DCU PWM/Timer —	I/O	M1	None, None	4	4
PA[14]	PCR[14]	Option 0 Option 1 Option 2 Option 3	GPIO[14] DCU_G6 eMIOSA[10] —	FP9	SIUL DCU PWM/Timer —	I/O	M2	None, None	5	5
PA[15]	PCR[15]	Option 0 Option 1 Option 2 Option 3	GPIO[15] DCU_G7 eMIOSA[9] —	FP8	SIUL DCU PWM/Timer —	I/O	M1	None, None	6	6

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PB[0]	PCR[16]	Option 0 Option 1 Option 2 Option 3	GPIO[16] CANTX_0 PDI1 —	—	SIUL FlexCAN_0 PDI —	I/O	M1	None, None	106	130
PB[1]	PCR[17]	Option 0 Option 1 Option 2 Option3	GPIO[17] CANRX_0 PDI0 —	—	SIUL FlexCAN_0 PDI —	I/O	S	None, None	105	129
PB[2]	PCR[18]	Option 0 Option 1 Option 2 Option3	GPIO[18] TXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, None	112	140
PB[3]	PCR[19]	Option 0 Option 1 Option 2 Option3	GPIO[19] RXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, None	111	139
PB[4]	PCR[20]	Option 0 Option 1 Option 2 Option 3	GPIO[20] SCK_1 MA0 —	—	SIUL DSPI_1 ADC —	I/O	M1	None, None	48	62
PB[5]	PCR[21]	Option 0 Option 1 Option 2 Option 3	GPIO[21] SOUT_1 MA1 FABM	—	SIUL DSPI_1 ADC Control	I/O	M1	Input, Pulldown	49	63
PB[6]	PCR[22]	Option 0 Option 1 Option 2 Option 3	GPIO[22] SIN_1 MA2 ABS[0]	—	SIUL DSPI_1 ADC Control	I/O	S	Input, Pullup	50	66
PB[7]	PCR[23]	Option 0 Option 1 Option 2 Option 3	GPIO[23] SIN_0 eMIOSB[22] —	—	SIUL DSPI_0 PWM/Timer —	I/O	S	None, None	46	56

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PB[8]	PCR[24]	Option 0 Option 1 Option 2 Option 3	GPIO[24] SOUT_0 eMIOSB[21] —	—	SIUL DSPI_0 PWM/Timer —	I/O	M1	None, None	45	55
PB[9]	PCR[25]	Option 0 Option 1 Option 2 Option 3	GPIO[25] SCK_0 eMIOSB[20] —	—	SIUL DSPI_0 PWM/Timer —	I/O	M1	None, None	44	54
PB[10]	PCR[26]	Option 0 Option 1 Option 2 Option 3	GPIO[26] CANRX_1 PDI2 eMIOSA[23]	—	SIUL FlexCAN_1 PDI PWM/Timer	I/O	S	None, None	107	131
PB[11]	PCR[27]	Option 0 Option 1 Option 2 Option 3	GPIO[27] CANTX_1 PDI3 eMIOSA[16]	—	SIUL FlexCAN_1 PDI PWM/Timer	I/O	M1	None, None	108	132
PB[12]	PCR[28]	Option 0 Option 1 Option 2 Option 3	GPIO[28] RXD_1 eMIOSB[19] PCS2_0	—	SIUL LINFlex_1 PWM/Timer DSPI_0	I/O	S	None, None	40	48
PB[13]	PCR[29]	Option 0 Option 1 Option 2 Option 3	GPIO[29] TXD_1 eMIOSB[18] PCS1_0	—	SIUL LINFlex_1 PWM/Timer DSPI_0	I/O	S	None, None	41	49
PB[14]	—	—	Reserved	—	—	—	—	—	—	—
PB[15]	—	—	Reserved	—	—	—	—	—	—	—
PC[0]	PCR[30]	Option 0 Option 1 Option 2 Option 3	GPIO[30] — — —	ANS[0]	SIUL — — —	I/O	J	None, None	72	88
PC[1]	PCR[31]	Option 0 Option 1 Option 2 Option 3	GPIO[31] — — —	ANS[1]	SIUL — — —	I/O	J	None, None	71	87

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PC[2]	PCR[32]	Option 0 Option 1 Option 2 Option 3	GPIO[32] — — —	ANS[2]	SIUL — — —	I/O	J	None, None	70	86
PC[3]	PCR[33]	Option 0 Option 1 Option 2 Option 3	GPIO[33] — — —	ANS[3]	SIUL — — —	I/O	J	None, None	69	85
PC[4]	PCR[34]	Option 0 Option 1 Option 2 Option 3	GPIO[34] — — —	ANS[4]	SIUL — — —	I/O	J	None, None	68	84
PC[5]	PCR[35]	Option 0 Option 1 Option 2 Option 3	GPIO[35] — — —	ANS[5]	SIUL — — —	I/O	J	None, None	67	83
PC[6]	PCR[36]	Option 0 Option 1 Option 2 Option 3	GPIO[36] — — —	ANS[6]	SIUL — — —	I/O	J	None, None	66	82
PC[7]	PCR[37]	Option 0 Option 1 Option 2 Option 3	GPIO[37] — — —	ANS[7]	SIUL — — —	I/O	J	None, None	65	81
PC[8]	PCR[38]	Option 0 Option 1 Option 2 Option 3	GPIO[38] — — —	ANS[8]	SIUL — — —	I/O	J	None, None	62	78
PC[9]	PCR[39]	Option 0 Option 1 Option 2 Option 3	GPIO[39] — — —	ANS[9]	SIUL — — —	I/O	J	None, None	61	77

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PC[10]	PCR[40]	Option 0 Option 1 Option 2 Option 3	GPIO[40] — SOUND —	ANS[10]	SIUL — SGL —	I/O	J	None, None	60	76
PC[11]	PCR[41]	Option 0 Option 1 Option 2 Option 3	GPIO[41] — MA0 PCS2_1	ANS[11]	SIUL — ADC DSPI_1	I/O	J	None, None	59	75
PC[12]	PCR[42]	Option 0 Option 1 Option 2 Option 3	GPIO[42] — MA1 PCS1_1	ANS[12]	SIUL — ADC DSPI_1	I/O	J	None, None	58	74
PC[13]	PCR[43]	Option 0 Option 1 Option 2 Option 3	GPIO[43] — MA2 PCS0_1	ANS[13]	SIUL — ADC DSPI_1	I/O	J	None, None	57	73
PC[14]	PCR[44]	Option 0 Option 1 Option 2 Option 3	GPIO[44] — — —	ANS[14] EXTAL32	SIUL — — —	I/O	J	None, None	56	72
PC[15]	PCR[45]	Option 0 Option 1 Option 2 Option 3	GPIO[45] — — —	ANS[15] XTAL32	SIUL — — —	I/O	J	None, None	55	71
PD[0]	PCR[46]	Option 0 Option 1 Option 2 Option 3	GPIO[46] M0C0M SSD0_0 eMIOSB[23]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	73	89
PD[1]	PCR[47]	Option 0 Option 1 Option 2 Option 3	GPIO[47] M0C0P SSD0_1 eMIOSB[22]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	74	90

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PD[2]	PCR[48]	Option 0 Option 1 Option 2 Option 3	GPIO[48] M0C1M SSD0_2 eMIOSB[21]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	75	91
PD[3]	PCR[49]	Option 0 Option 1 Option 2 Option 3	GPIO[49] M0C1P SSD0_3 eMIOSB[20]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	76	92
PD[4]	PCR[50]	Option 0 Option 1 Option 2 Option 3	GPIO[50] M1C0M SSD1_0 eMIOSB[19]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	79	95
PD[5]	PCR[51]	Option 0 Option 1 Option 2 Option 3	GPIO[51] M1C0P SSD1_1 eMIOSB[18]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	80	96
PD[6]	PCR[52]	Option 0 Option 1 Option 2 Option 3	GPIO[52] M1C1M SSD1_2 eMIOSB[17]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	81	97
PD[7]	PCR[53]	Option 0 Option 1 Option 2 Option 3	GPIO[53] M1C1P SSD1_3 eMIOSB[16]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	82	98
PD[8]	PCR[54]	Option 0 Option 1 Option 2 Option 3	GPIO[54] M2C0M SSD2_0 —	—	SIUL SMC SSD —	I/O	SMD	None, None	83	99
PD[9]	PCR[55]	Option 0 Option 1 Option 2 Option 3	GPIO[55] M2C0P SSD2_1 —	—	SIUL SMC SSD —	I/O	SMD	None, None	84	100

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PD[10]	PCR[56]	Option 0 Option 1 Option 2 Option 3	GPIO[56] M2C1M SSD2_2 —	—	SIUL SMC SSD —	I/O	SMD	None, None	85	101
PD[11]	PCR[57]	Option 0 Option 1 Option 2 Option 3	GPIO[57] M2C1P SSD2_3 —	—	SIUL SMC SSD —	I/O	SMD	None, None	86	102
PD[12]	PCR[58]	Option 0 Option 1 Option 2 Option 3	GPIO[58] M3C0M SSD3_0 —	—	SIUL SMC SSD —	I/O	SMD	None, None	89	105
PD[13]	PCR[59]	Option 0 Option 1 Option 2 Option 3	GPIO[59] M3C0P SSD3_1 —	—	SIUL SMC SSD —	I/O	SMD	None, None	90	106
PD[14]	PCR[60]	Option 0 Option 1 Option 2 Option 3	GPIO[60] M3C1M SSD3_2 —	—	SIUL SMC SSD —	I/O	SMD	None, None	91	107
PD[15]	PCR[61]	Option 0 Option 1 Option 2 Option 3	GPIO[61] M3C1P SSD3_3 —	—	SIUL SMC SSD —	I/O	SMD	None, None	92	108
PE[0]	PCR[62]	Option 0 Option 1 Option 2 Option 3	GPIO[62] M4C0M SSD4_0 eMIOSA[15]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	93	109
PE[1]	PCR[63]	Option 0 Option 1 Option 2 Option 3	GPIO[63] M4C0P SSD4_1 eMIOSA[14]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	94	110

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PE[2]	PCR[64]	Option 0 Option 1 Option 2 Option 3	GPIO[64] M4C1M SSD4_2 eMIOSA[13]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	95	111
PE[3]	PCR[65]	Option 0 Option 1 Option 2 Option 3	GPIO[65] M4C1P SSD4_3 eMIOSA[12]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	96	112
PE[4]	PCR[66]	Option 0 Option 1 Option 2 Option 3	GPIO[66] M5C0M SSD5_0 eMIOSA[11]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	99	115
PE[5]	PCR[67]	Option 0 Option 1 Option 2 Option 3	GPIO[67] M5C0P SSD5_1 eMIOSA[10]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	100	116
PE[6]	PCR[68]	Option 0 Option 1 Option 2 Option 3	GPIO[68] M5C1M SSD5_2 eMIOSA[9]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	101	117
PE[7]	PCR[69]	Option 0 Option 1 Option 2 Option 3	GPIO[69] M5C1P SSD5_3 eMIOSA[8]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	102	118
PE[8]	—	—	Reserved	—	—	—	—	—	—	—
PE[9]	—	—	Reserved	—	—	—	—	—	—	—
PE[10]	—	—	Reserved	—	—	—	—	—	—	—
PE[11]	—	—	Reserved	—	—	—	—	—	—	—
PE[12]	—	—	Reserved	—	—	—	—	—	—	—
PE[13]	—	—	Reserved	—	—	—	—	—	—	—
PE[14]	—	—	Reserved	—	—	—	—	—	—	—
PE[15]	—	—	Reserved	—	—	—	—	—	—	—

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PF[0]	PCR[70]	Option 0 Option 1 Option 2 Option 3	GPIO[70] eMIOSA[13] PDI4 eMIOSA[22]	FP39	SIUL PWM/Timer PDI PWM/Timer	I/O	S	None, None	113	143
PF[1]	PCR[71]	Option 0 Option 1 Option 2 Option 3	GPIO[71] eMIOSA[12] PDI5 eMIOSA[21]	FP38	SIUL PWM/Timer PDI PWM/Timer	I/O	S	None, None	114	144
PF[2]	PCR[72]	Option 0 Option 1 Option 2 Option 3	GPIO[72] NMI — —	—	SIUL NMI — —	I/O	S	None, None	37	45
PF[3]	PCR[73]	Option 0 Option 1 Option 2 Option 3	GPIO[73] eMIOSA[11] PDI6 —	FP37	SIUL PWM/Timer PDI —	I/O	M1	None, None	115	145
PF[4]	PCR[74]	Option 0 Option 1 Option 2 Option 3	GPIO[74] eMIOSA[10] PDI7 —	FP36	SIUL PWM/Timer PDI —	I/O	M1	None, None	116	146
PF[5]	PCR[75]	Option 0 Option 1 Option 2 Option 3	GPIO[75] eMIOSA[9] DCU_TAG —	FP35	SIUL PWM/Timer DCU —	I/O	M1	None, None	117	147
PF[6]	PCR[76]	Option 0 Option 1 Option 2 Option 3	GPIO[76] SDA_0 — —	FP34	SIUL I^2C_0 — —	I/O	S	None, None	120	150
PF[7]	PCR[77]	Option 0 Option 1 Option 2 Option 3	GPIO[77] SCL_0 PCS2_1 —	FP33	SIUL I^2C_0 DSPI_1 —	I/O	S	None, None	121	151

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PF[8]	PCR[78]	Option 0 Option 1 Option 2 Option 3	GPIO[78] SDA_1 PCS1_1 RXD_1	FP32	SIUL I^2C_1 DSPI_1 LINFlex_1	I/O	S	None, None	122	152
PF[9]	PCR[79]	Option 0 Option 1 Option 2 Option 3	GPIO[79] SCL_1 PCS0_1 TXD_1	FP31	SIUL I^2C_1 DSPI_1 LINFlex_1	I/O	S	None, None	123	153
PF[10]	PCR[80]	Option 0 Option 1 Option 2 Option 3	GPIO[80] eMIOSA[16] PCS0_2 —	FP29	SIUL PWM/Timer QuadSPI —	I/O	M1	None, None	127	157
PF[11]	PCR[81]	Option 0 Option 1 Option 2 Option 3	GPIO[81] eMIOSB[23] IO2/PCS1_2[6] —	FP28	SIUL PWM/Timer QuadSPI —	I/O	M1	None, None	128	158
PF[12]	PCR[82]	Option 0 Option 1 Option 2 Option 3	GPIO[82] eMIOSB[16] IO3/PCS2_2[6] —	FP27	SIUL PWM/Timer QuadSPI —	I/O	M1	None, None	129	159
PF[13]	PCR[83]	Option 0 Option 1 Option 2 Option 3	GPIO[83] IO0/SIN_2[6] CANRX_1 —	FP26	SIUL QuadSPI FlexCAN_1 —	I/O	M1	None, None	130	160
PF[14]	PCR[84]	Option 0 Option 1 Option 2 Option 3	GPIO[84] IO1/SOUT_2[6] CANTX_1 —	FP25	SIUL QuadSPI FlexCAN_1 —	I/O	M1	None, None	131	161
PF[15]	PCR[85]	Option 0 Option 1 Option 2 Option 3	GPIO[85] SCK_2 — —	FP24	SIUL QuadSPI — —	I/O	F	None, None	132	162

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PG[0]	PCR[86]	Option 0 Option 1 Option 2 Option 3	GPIO[86] DCU_B0 SCL_3 SOUND	FP7	SIUL DCU I^2C_3 SGL	I/O	M2	None, None	9	9
PG[1]	PCR[87]	Option 0 Option 1 Option 2 Option 3	GPIO[87] DCU_B1 SDA_3 —	FP6	SIUL DCU I^2C_3 —	I/O	M1	None, None	10	10
PG[2]	PCR[88]	Option 0 Option 1 Option 2 Option 3	GPIO[88] DCU_B2 eMIOSB[19] —	FP5	SIUL DCU PWM/Timer —	I/O	M2	None, None	11	11
PG[3]	PCR[89]	Option 0 Option 1 Option 2 Option 3	GPIO[89] DCU_B3 eMIOSB[21] —	FP4	SIUL DCU PWM/Timer —	I/O	M1	None, None	12	12
PG[4]	PCR[90]	Option 0 Option 1 Option 2 Option 3	GPIO[90] DCU_B4 eMIOSB[17] —	FP3	SIUL DCU PWM/Timer —	I/O	M2	None, None	13	13
PG[5]	PCR[91]	Option 0 Option 1 Option 2 Option 3	GPIO[91] DCU_B5 eMIOSA[8] —	FP2	SIUL DCU PWM/Timer —	I/O	M1	None, None	14	14
PG[6]	PCR[92]	Option 0 Option 1 Option 2 Option 3	GPIO[92] DCU_B6 — —	FP1	SIUL DCU — —	I/O	M2	None, None	15	15
PG[7]	PCR[93]	Option 0 Option 1 Option 2 Option 3	GPIO[93] DCU_B7 — —	FP0	SIUL DCU — —	I/O	M1	None, None	16	16

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PG[8]	PCR[94]	Option 0 Option 1 Option 2 Option 3	GPIO[94] DCU_VSYNC — —	BP0	SIUL DCU — —	I/O	M2	Input, None	17	17
PG[9]	PCR[95]	Option 0 Option 1 Option 2 Option 3	GPIO[95] DCU_HSYNC — —	BP1	SIUL DCU — —	I/O	M1	Input, None	18	18
PG[10]	PCR[96]	Option 0 Option 1 Option 2 Option 3	GPIO[96] DCU_DE — —	BP2	SIUL DCU — —	I/O	M2	None, None	19	19
PG[11]	PCR[97]	Option 0 Option 1 Option 2 Option 3	GPIO[97] DCU_PCLK — —	BP3	SIUL DCU — —	I/O	M1	None, None	20	20
PG[12]	PCR[98]	Option 0 Option 1 Option 2 Option 3	GPIO[98] eMIOSA[23] SOUND eMIOSA[8]	FP30	SIUL PWM/Timer SGL PWM/Timer	I/O	S	None, None	126	156
PG[13]	—	—	Reserved	—	—	—	—	—	—	—
PG[14]	—	—	Reserved	—	—	—	—	—	—	—
PG[15]	—	—	Reserved	—	—	—	—	—	—	—
PH[0][7]	PCR[99]	Option 0 Option 1 Option 2 Option 3	GPIO[99] TCK — —	—	SIUL JTAG — —	I/O	S	Input, Pullup	36	43
PH[1][7]	PCR[100]	Option 0 Option 1 Option 2 Option 3	GPIO[100] TDI — —	—	SIUL JTAG — —	I/O	S	Input, Pullup	33	36

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PH[2][7]	PCR[101]	Option 0 Option 1 Option 2 Option 3	GPIO[101] TDO — —	—	SIUL JTAG — —	I/O	M1	Output, None	34	39
PH[3][7]	PCR[102]	Option 0 Option 1 Option 2 Option 3	GPIO[102] TMS — —	—	SIUL JTAG — —	I/O	S	Input, Pullup	35	41
PH[4]	PCR[103]	Option 0 Option 1 Option 2 Option 3	GPIO[103] PCS0_0 eMIOSB[16] CLKOUT	—	SIUL DSPI_0 PWM/Timer Control	I/O	F	None, None	47	61
PH[5]	PCR[104]	Option 0 Option 1 Option 2 Option 3	GPIO[104] VLCD[8] — —	—	SIUL LCD — —	I/O	S	None, None	21	21
PH[6]	—	—	Reserved	—	—	—	—	—	—	—
PH[7]	—	—	Reserved	—	—	—	—	—	—	—
PH[8]	—	—	Reserved	—	—	—	—	—	—	—
PH[9]	—	—	Reserved	—	—	—	—	—	—	—
PH[10]	—	—	Reserved	—	—	—	—	—	—	—
PH[11]	—	—	Reserved	—	—	—	—	—	—	—
PH[12]	—	—	Reserved	—	—	—	—	—	—	—
PH[13]	—	—	Reserved	—	—	—	—	—	—	—
PH[14]	—	—	Reserved	—	—	—	—	—	—	—
PH[15]	—	—	Reserved	—	—	—	—	—	—	—
PJ[0]	PCR[105]	Option 0 Option 1 Option 2 Option 3	GPIO[105] PDI_DE — —	—	SIUL PDI — —	I/O	S	None, None	—	119

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PJ[1]	PCR[106]	Option 0 Option 1 Option 2 Option 3	GPIO[106] PDI_HSYNC — —	—	SIUL PDI — —	I/O	S	None, None	—	120
PJ[2]	PCR[107]	Option 0 Option 1 Option 2 Option 3	GPIO[107] PDI_VSYNC — —	—	SIUL PDI — —	I/O	S	None, None	—	121
PJ[3]	PCR[108]	Option 0 Option 1 Option 2 Option 3	GPIO[108] PDI_PCLK — —	—	SIUL PDI — —	I/O	M1	None, None	—	122
PJ[4]	PCR[109]	Option 0 Option 1 Option 2 Option 3	GPIO[109] PDI[0] CANRX_0 —	—	SIUL PDI FlexCAN_0 —	I/O	S	None, None	—	57
PJ[5]	PCR[110]	Option 0 Option 1 Option 2 Option 3	GPIO[110] PDI[1] CANTX_0 —	—	SIUL PDI FlexCAN_0 —	I/O	M1	None, None	—	58
PJ[6]	PCR[111]	Option 0 Option 1 Option 2 Option 3	GPIO[111] PDI[2] CANRX_1 eMIOSA[22]	—	SIUL PDI FlexCAN_1 PWM/Timer	I/O	S	None, None	—	59
PJ[7]	PCR[112]	Option 0 Option 1 Option 2 Option 3	GPIO[112] PDI[3] CANTX_1 eMIOSA[21]	—	SIUL PDI FlexCAN_1 PWM/Timer	I/O	M1	None, None	—	60
PJ[8]	PCR[113]	Option 0 Option 1 Option 2 Option 3	GPIO[113] PDI[4] — —	—	SIUL PDI — —	I/O	S	None, None	—	125

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PJ[9]	PCR[114]	Option 0 Option 1 Option 2 Option 3	GPIO[114] PDI[5] — —	—	SIUL PDI — —	I/O	S	None, None	—	126
PJ[10]	PCR[115]	Option 0 Option 1 Option 2 Option 3	GPIO[115] PDI[6] — —	—	SIUL PDI — —	I/O	S	None, None	—	127
PJ[11]	PCR[116]	Option 0 Option 1 Option 2 Option 3	GPIO[116] PDI[7] — —	—	SIUL PDI — —	I/O	S	None, None	—	128
PJ[12]	PCR[117]	Option 0 Option 1 Option 2 Option 3	GPIO[117] PDI[8] eMIOSB[17] —	—	SIUL PDI PWM/Timer —	I/O	M1	None, None	—	135
PJ[13]	PCR[118]	Option 0 Option 1 Option 2 Option 3	GPIO[118] PDI[9] eMIOSB[20] —	—	SIUL PDI PWM/Timer —	I/O	M1	None, None	—	136
PJ[14]	PCR[119]	Option 0 Option 1 Option 2 Option 3	GPIO[119] PDI[10] eMIOSA[20] —	—	SIUL PDI PWM/Timer —	I/O	M1	None, None	—	137
PJ[15]	PCR[120]	Option 0 Option 1 Option 2 Option 3	GPIO[120] PDI[11] eMIOSA[19] —	—	SIUL PDI PWM/Timer —	I/O	M1	None, None	—	138
PK[0]	PCR[121]	Option 0 Option 1 Option 2 Option 3	GPIO[121] PDI[12] eMIOSA[18] DCU_TAG	—	SIUL PDI PWM/Timer DCU	I/O	M1	None, None	—	141

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PK[1]	PCR[122]	Option 0 Option 1 Option 2 Option 3	GPIO[122] PDI[13] eMIOSA[17] —	—	SIUL PDI PWM/Timer —	I/O	M1	None, None	—	142
PK[2]	PCR[123]	Option 0 Option 1 Option 2 Option 3	GPIO[123] MCKO PDI[10] —	—	SIUL Nexus PDI —	I/O	F	None, None	—	33
PK[3]	PCR[124]	Option 0 Option 1 Option 2 Option 3	GPIO[124] MSEO PDI[11] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	34
PK[4]	PCR[125]	Option 0 Option 1 Option 2 Option 3	GPIO[125] EVTO PDI[12] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	35
PK[5]	PCR[126]	Option 0 Option 1 Option 2 Option 3	GPIO[126] EVTI PDI[13] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	37
PK[6]	PCR[127]	Option 0 Option 1 Option 2 Option 3	GPIO[127] MDO0 PDI[14] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	38
PK[7]	PCR[128]	Option 0 Option 1 Option 2 Option 3	GPIO[128] MDO1 PDI[15] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	40
PK[8]	PCR[129]	Option 0 Option 1 Option 2 Option 3	GPIO[129] MDO2 PDI[16] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	42

Table 6. Port pin summary (continued)

Port pin	PCR register	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad type[4]	RESET config.[5]	Pin number	
									144 LQFP	176 LQFP
PK[9]	PCR[130]	Option 0 Option 1 Option 2 Option 3	GPIO[130] MDO3 PDI[17] —	—	SIUL Nexus PDI —	I/O	M1	None, None	—	44
PK[10]	PCR[131]	Option 0 Option 1 Option 2 Option 3	GPIO[131] SDA_1 eMIOSA[15] —	—	SIUL I^2C_1 PWM/Timer —	I/O	S	None, None	—	52
PK[11]	PCR[132]	Option 0 Option 1 Option 2 Option 3	GPIO[132] SCL_1 eMIOSA[14] —	—	SIUL I^2C_1 PWM/Timer —	I/O	S	None, None	—	53
PK[12]	—	—	Reserved	—	—	—	—	—	—	—
PK[13]	—	—	Reserved	—	—	—	—	—	—	—
PK[14]	—	—	Reserved	—	—	—	—	—	—	—
PK[15]	—	—	Reserved	—	—	—	—	—	—	—

NOTES:

1 Alternate functions are chosen by setting the values of the PCR[*n*].PA bitfields inside the SIUL module. PCR[*n*].PA = 00 → Option 0; PCR[n*n*.PA = 01 → Option 1; PCR[*n*].PA = 10 → Option 2; PCR[*n*].PA = 11→ Option 3. This is intended to select the output functions; to use one of the input functions, the PCR[*n*].IBE bit must be written to '1', regardless of the values selected in the PCR[*n*].PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

2 Special functions are enabled independently from the standard digital pin functions. Enabling standard I/O functions in the PCR registers may interfere with their functionality. ADC functions are enabled using the PCR[APC] bit; other functions are enabled by enabling the respective module.

3 Using the PSMI registers in the System Integration Unit Lite (SIUL), different pads can be multiplexed to the same peripheral input. Please see the SIUL chapter of the *PXD10 Microcontroller Reference Manual* for details.

4 See Table 7.

5 Reset configuration is given as I/O direction and pull, e.g., "Input, Pullup".

6 This option on this pin has alternate functions that depend on whether the QuadSPI is in SPI mode or in serial flash mode (SFM).

7 Out of reset pins PH[0:3] are available as JTAG pins (TCK, TDI, TDO and TMS respectively). It is up to the user to configure pins PH[0:3] when needed.

8 This pin can be used for LCD supply pin VLCD. Refer to the voltage supply pin descriptions in the PXD10 data sheet for details.

Table 7. Pad type descriptions

Abbreviation[1]	Description
F	Fast (with GPIO and digital alternate function)
J	Slow pads with analog muxing (built for ADC channels)
M1	Medium (with GPIO and digital alternate function)
M2	Programmable medium/slow pad (programmed via the slew rate control in the PCR): Slew rate disabled: Slow driver configuration (AC/DC parameters same as for a slow pad) Slew rate enabled: Medium driver configuration (AC/DC parameters same as for a medium pad)
S	Slow (with GPIO and digital alternate function)
SMD	Stepper motor driver (with slew rate control)
X	Oscillator

NOTES:
1 The pad descriptions refer to the different Pad Configuration Register (PCR) types. Refer to the SIUL chapter in the device reference manual for the features available for each pad type.

2.8.1 Signal details

Table 8. Signal details

Signal	Peripheral	Description
ABS[0]	BAM	Alternate Boot Select. Gives an option to boot by downloading code via CAN or LIN.
ANS[0:15]	ADC	Inputs used to bring into the device sensor-based signals for A/D conversion. ANS[0:15] connect to ATD channels [32:47].
MA[0:2]	ADC	These three control bits are output to enable the selection for an external Analog Mux for expansion channels. The available 8 multiplexed channels connect to ATD channels [64:71].
FABM		Force Alternate Boot mode. Forces the device to boot from the external bus (Can or LIN). If not asserted, the device boots up from the lowest flash sector containing a valid boot signature.
DCU_DE	DCU	Indicates that valid pixels are present.
DCU_HSYNC	DCU	Horizontal sync pulse for TFT-LCD display
DCU_PCLK	DCU	Output pixel clock for TFT-LCD display
DCU_R[0:7], DCU_G[0:7], DCU_B[0:7]	DCU	Red, green and blue color 8-bit Pixel values for TFT-LCD displays
DCU_TAG	DCU	Indicates when a tagged pixel is present in safety mode
DCU_VSYNC	DCU	Vertical sync pulse for TFT-LCD display
PCS[0..2]_0, PCS[0..2]_1	DSPI	Peripheral chip selects when device is in Master mode; not used in slave modes.
SCK_0, SCK_1	DSPI	SPI clock signal—bidirectional

Table 8. Signal details (continued)

Signal	Peripheral	Description
SIN_0, SIN_1	DSPI	SPI data input signal
SOUT_0, SOUT_1	DSPI	SPI data output signal
PCS0_2	QuadSPI	Peripheral chip select for serial flash mode or chip select 0 for SPI master mode
IO2/PCS1_2	QuadSPI	Chip select 1 for SPI master mode and bidirectional IO2 for serial flash mode
IO3/PCS2_2	QuadSPI	Chip select 2 for SPI master mode and bidirectional IO3 for serial flash mode
IO0/SIN_2	QuadSPI	Data input signal for SPI master and slave modes and bidirectional IO0 for serial flash mode
IO1/SOUT_2	QuadSPI	Data output signal for SPI master and slave modes and bidirectional IO1 for serial flash mode
SCK_2	QuadSPI	Clock output signal for SPI master and serial flash modes and clock input signal for SPI slave mode
eMIOSA[8:23], eMIOSB[16:23]	eMIOS	Enhanced Modular Input Output System. 16+8 channel eMIOS for timed input or output functions.
CANRX_0, CANRX_1	FlexCAN	Receive (RX) pins for the CAN bus transceiver
CANTX_0, CANTX_1	FlexCAN	Transmit (TX) pins for the CAN bus transceiver
SCL_0, SCL_1, SCL_2, SCL_3	I^2C	Bidirectional serial clock compatible with I^2C specifications
SDA_0, SDA_1, SDA_2, SDA_3	I^2C	Bidirectional serial data compatible with I^2C specifications
TCK	JTAG	Debug port serial clock as per JTAG specifications
TDI	JTAG	Debug port serial data input port as per JTAG standards specifications
TDO	JTAG	Debug port serial data output port as per JTAG standards specifications
TMS	JTAG	Debug port Test Mode Select signal for the JTAG TAP controller state machine and indicates various state transitions for the TAP controller in the device
BP[0:3]	LCD	Backplane signals from the LCD controlling the backplane reference voltage for the LCD display
FP[0:39]	LCD	Frontplane signals for LCD segments
$\overline{\text{EVTI}}$	Nexus	Nexus2+ event input trigger
$\overline{\text{EVTO}}$	Nexus	Nexus2+ event output trigger

Table 8. Signal details (continued)

Signal	Peripheral	Description
MCKO	Nexus	Output clock for the development tool
MDO[0:3]	Nexus	Message output port pins that send information bits to the development tools for messages such as Branch Trace Message (BTM), Ownership Trace Message (OTM), Data Trace Message (DTM). Only available in reduced port mode.
$\overline{\text{MSEO}}$	Nexus	Output pin—Indicates the start or end of the variable length message on the MDO pins
PDI[0:17]	DCU (PDI)	Video/graphic data in various RGB modes input to the DCU
PDI_DE	DCU (PDI)	Input signal indicates the validity of pixel data on the Input PDI data bus.
PDI_HSYNC	DCU (PDI)	Input indicates the timing reference for the start of each frame line for the PDI Input data.
PDI_PCLK	DCU (PDI)	Input pixel clock from PDI
PDI_VSYNC	DCU (PDI)	Input indicates the timing reference for the start of a frame for the PDI input data.
RXD_0	LINFlex	SCI/LIN Receive data signal—This port is used to download the code for the BAM boot sequence.
RXD_1	LINFlex	SCI/LIN Receive data signal. Input pad for the LIN SCI module. Connects to the internal LIN second port.
TXD_0	LINFlex	SCI/LIN Transmit data signal. This port is used to download the code for the BAM boot sequence.
TXD_1	LINFlex	SCI/LIN Transmit data signal—Transmit (output) port for the second LIN module in the chip
SOUND	SGL	Sound signal to the speaker/buzzer
SSD[0:5]_0 SSD[0:5]_1 SSD[0:5]_2 SSD[0:5]_3	SSD	Bidirectional control of stepper motors using stall detection module
M[0:5]C0M M[0:5]C0P M[0:5]C1M M[0:5]C1P	SMC	Controls stepper motors in various configuration
CLKOUT	MC_CGM	Output clock—It can be selected from several internal clocks of the device from the clock generation module.

3 Electrical characteristics

3.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by internal pull up and pull down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 9 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 9. Parameter Classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the Nonvolatile User Options (NVUSRO) register. For a detailed description of the NVUSRO register, please see the chip reference manual.

3.3.1 NVUSRO[PAD3V5V] field description

Table 10 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 10. PAD3V5V field description[1]

Value[2]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

NOTES:
1 See the device reference manual for more information on the NVUSRO register.
2 Default manufacturing value before Flash initialization is ‘1’ (3.3 V)

The DC electrical characteristics are dependent on the PAD3V5V bit value.

3.3.2 NVUSRO[OSCILLATOR_MARGIN] field description

Table 10 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 11. OSCILLATOR_MARGIN field description[1]

Value[2]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

NOTES:
1 See the device reference manual for more information on the NVUSRO register.
2 Default manufacturing value before Flash initialization is ‘1’

The 4–16 MHz fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value.

3.4 Absolute maximum ratings

Table 12. Absolute maximum ratings

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDA}	SR	C	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SSA})	—	–0.3	6.0	V
V_{SSA}	SR	C	Voltage on VSSA (ADC reference) pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DDPLL}	CC	C	Voltage on VDDPLL (1.2 V PLL supply) pin with respect to ground (V_{SSPLL})	—	-0.1	1.4	V
V_{SSPLL}	SR	C	Voltage on VSSPLL pin with respect to V_{SS12}	—	V_{SS12} – 0.1	V_{SS12} + 0.1	V
V_{DDR}	SR	C	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})	—	–0.3	6.0	V
V_{SSR}	SR	C	Voltage on VSSR (regulator ground) pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD12}	CC	C	Voltage on VDD12 pin with respect to ground (V_{SS12})	—	-0.1	1.4	V
V_{SS12}	CC	C	Voltage on VSS12 pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DDE_A}[1]	SR	C	Voltage on VDDE_A (I/O supply) pin with respect to ground (V_{SSE_A})	—	–0.3	6.0	V
V_{DDE_B}[1]	SR	C	Voltage on VDDE_B (I/O supply) pin with respect to ground (V_{SSE_B})	—	–0.3	6.0	V
V_{DDE_C}[1]	SR	C	Voltage on VDDE_C (I/O supply) pin with respect to ground (V_{SSE_C})	—	–0.3	6.0	V
V_{DDE_E}[1]	SR	C	Voltage on VDDE_E (I/O supply) pin with respect to ground (V_{SSE_E})	—	–0.3	6.0	V
V_{DDMA}[1]	SR	C	Voltage on VDDMA (stepper motor supply) pin with respect to ground (V_{SSMA})	—	–0.3	6.0	V
V_{DDMB}[1] V_{DDMC}[1]	SR	C	Voltage on VDDMB/C (stepper motor supply) pin with respect to ground (V_{SSMB})	—	–0.3	6.0	V
V_{SS}[2]	SR	C	I/O supply ground	—	0	0	V
V_{SSOSC}	SR	C	Voltage on VSSOSC (oscillator ground) pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{LCD}	SR	C	Voltage on VLCD (LCD supply) pin with respect to V_{SS}	—	0	V_{DDE_A} + 0.3	V
V_{IN}	SR	C	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
		C		Relative to V_{DD}	–0.3	V_{DD} + 0.3[3]	

Table 12. Absolute maximum ratings (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
I_{INJPAD}	SR	C	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	C	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{MAX}	CC	D	Absolute maximum current drive rating	—	—	45	
$T_{STORAGE}$	SR	C	Storage temperature	—	–55	150	°C

NOTES:
1 Throughout the remainder of this document V_{DD} refers collectively to I/O voltage supplies, i.e., V_{DDE_A}, V_{DDE_B}, V_{DDE_C}, V_{DDE_E}, V_{DDMA}, V_{DDMB} and V_{DDMC}, unless otherwise noted.
2 Throughout the remainder of this document V_{SS} refers collectively to I/O voltage supply grounds, i.e., V_{SSE_A}, V_{SSE_B}, V_{SSE_C}, V_{SSE_E}, V_{SSMA}, V_{SSMB} and V_{SSMC}, unless otherwise noted.
3 As long as the current injection specification is adhered to, then a higher potential is allowed.

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

3.4.1 Recommended operating conditions

NOTE

Maximum slew time for the supplies to ramp up should be 1 second, which is slowest ramp-up time.

CAUTION

V_{DDE_C} and V_{DDA} must be the same voltage.

V_{DDMB} and V_{DDMC} must be the same voltage.

Table 13. Recommended operating conditions (3.3 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDA}[1]	SR	C	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})	—	3.0	3.6	V
		C		Relative to V_{DDE_C}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SSA}	SR	C	Voltage on VSSA (ADC reference) pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{SSPLL}	SR	C	Voltage on VSSPLL pin with respect to V_{SS12}	—	0	0	V
V_{DDR}[2]	SR	C	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})	—	3.0	3.6	V
V_{SSR}	SR	C	Voltage on VSSR (regulator ground) pin with respect to V_{SS12}	—	0	0	V
V_{SS12}[4]	CC	C	Voltage on VSS12 pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD}[3,4,5]	SR	C	Voltage on VDD pins (VDDE_A, VDDE_B, VDDE_C, VDDE_E, VDDMA, VDDMB, VDDMC) with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS}[6]	SR	C	I/O supply ground	—	0	0	V
V_{DDE_A}	SR	C	Voltage on VDDE_A (I/O supply) pin with respect to ground (V_{SSE_A})	—	3.0	3.6	V
V_{DDE_B}	SR	C	Voltage on VDDE_B (I/O supply) pin with respect to ground (V_{SSE_B})	—	3.0	3.6	V
V_{DDE_C}	SR	C	Voltage on VDDE_C (I/O supply) pin with respect to ground (V_{SSE_C})	—	3.0	3.6	V
V_{DDE_E}	SR	C	Voltage on VDDE_E (I/O supply) pin with respect to ground (V_{SSE_E})	—	3.0	3.6	V
V_{DDMA}	SR	C	Voltage on VDDMA (stepper motor supply) pin with respect to ground (V_{SSMA})	—	3.0	3.6	V
V_{DDMB}	SR	C	Voltage on VDDMB (stepper motor supply) pin with respect to ground (V_{SSMB})	—	3.0	3.6	V
V_{DDMC}	SR	C	Voltage on VDDMC (stepper motor supply) pin with respect to ground (V_{SSMC})	—	3.0	3.6	V

Table 13. Recommended operating conditions (3.3 V) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SSOSC}	SR	C	Voltage on VSSOSC (oscillator ground) pin with respect to V_{SS}	—	0	0	V
V_{LCD}	SR	C	Voltage on VLCD (LCD supply) pin with respect to V_{SS}	—	0	V_{DDE_A} + 0.3	V
TV_{DD}	SR	C	V_{DD} slope to ensure correct power up	—	5×10^{-6}	0.25	V/µs
T_A	SR	C	Ambient temperature under bias	—	−40	105	°C
T_J	SR	C	Junction temperature under bias		−40	150	

NOTES:
1. 100 nF capacitance needs to be provided between V_{DDA}/V_{SSA} pair.
2. At least 10 µF capacitance must be connected between V_{DDR} and V_{SS}. This is required because of sharp surge due to external ballast.
3. V_{DD} refers collectively to I/O voltage supplies, i.e., V_{DDE_A}, V_{DDE_B}, V_{DDE_C}, V_{DDE_E}, V_{DDMA}, V_{DDMB} and V_{DDMC}.
4. 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair
5. Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/O's DC electrical specification may not be guaranteed.
   When voltage drops below V_{LVDHVL} device is reset.
6. V_{SS} refers collectively to I/O voltage supply grounds, i.e., V_{SSE_A}, V_{SSE_B}, V_{SSE_C}, V_{SSE_E}, V_{SSMA}, V_{SSMB} and V_{SSMC}) unless otherwise noted.

Table 14. Recommended operating conditions (5.0 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDA}[1]	SR	C	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
		C		Voltage drop[2]	3.0	5.5	
		C		Relative to V_{DDE_C}	V_{DD} − 0.1	V_{DD} + 0.1	
V_{SSA}	SR	C	Voltage on VSSA (ADC reference) pin with respect V_{SS}	—	V_{SS} − 0.1	V_{SS} + 0.1	V
V_{SSPLL}	SR	C	Voltage on VSSPLL pin with respect to V_{SS12}	—	0	0	V
V_{DDR}[3]	SR	C	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})	—	4.5	5.5	V
		C		Voltage drop[2]	3.0	5.5	
		C		Relative to V_{DD}	V_{DD} − 0.1	V_{DD} + 0.1	
V_{SSR}	SR	C	Voltage on VSSR (regulator ground) pin with respect to V_{SS12}	—	0	0	V
V_{SS12}	CC	C	Voltage on VSS12 pin with respect to V_{SS}	—	V_{SS} − 0.1	V_{SS} + 0.1	V
V_{DD}[4,5]	SR	C	Voltage on VDD pins (VDDE_A, VDDE_B, VDDE_C, VDDE_E, VDDMA, VDDMB, VDDMC) with respect to ground (V_{SS})	Voltage drop[2]	4.5	5.5	V

Table 14. Recommended operating conditions (5.0 V) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SS}[6]	SR	C	I/O supply ground	—	0	0	V
V_{DDE_A}	SR	C	Voltage on VDDE_A (I/O supply) pin with respect to ground (V_{SSE_A})	—	4.5	5.5	V
V_{DDE_B}	SR	C	Voltage on VDDE_B (I/O supply) pin with respect to ground (V_{SSE_B})	—	4.5	5.5	V
V_{DDE_C}[7]	SR	C	Voltage on VDDE_C (I/O supply) pin with respect to ground (V_{SSE_C})	—	4.5	5.5	V
V_{DDE_E}	SR	C	Voltage on VDDE_E (I/O supply) pin with respect to ground (V_{SSE_E})	—	4.5	5.5	V
V_{DDMA}	SR	C	Voltage on VDDMA (stepper motor supply) pin with respect to ground (V_{SSMA})	—	4.5	5.5	V
V_{DDMB}	SR	C	Voltage on VDDMB (stepper motor supply) pin with respect to ground (V_{SSMB})	—	4.5	5.5	V
V_{DDMC}	SR	C	Voltage on VDDMC (stepper motor supply) pin with respect to ground (V_{SSMC})	—	4.5	5.5	V
V_{SSOSC}	SR	C	Voltage on VSSOSC (oscillator ground) pin with respect to V_{SS}	—	0	0	V
V_{LCD}	SR	C	Voltage on VLCD (LCD supply) pin with respect to V_{SS}	—	0	V_{DDE_A} + 0.3	V
TV_{DD}	SR	C	V_{DD} slope to ensure correct power up	—	3×10^{-6}	0.25	V/µs
T_A	SR	C	Ambient temperature under bias	—	−40	105	°C
T_J	SR	C	Junction temperature under bias	—	−40	150	°C

NOTES:
1. 100 nF capacitance needs to be provided between V_{DDA}/V_{SSA} pair.
2. Full functionality cannot be guaranteed when voltage drops below 4.5 V. In particular, I/O DC and ADC electrical characteristics may not be guaranteed below 4.5 V during the voltage drop sequence.
3. 10 µF capacitance must be connected between V_{DDR} and V_{SS12}. This is required because of sharp surge due to external ballast.
4. V_{DD} refers collectively to I/O voltage supplies, i.e., V_{DDE_A}, V_{DDE_B}, V_{DDE_C}, V_{DDE_E}, V_{DDMA}, V_{DDMB} and V_{DDMC}.
5. 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair
6. V_{SS} refers collectively to I/O voltage supply grounds, i.e., V_{SSE_A}, V_{SSE_B}, V_{SSE_C}, V_{SSE_E}, V_{SSMA}, V_{SSMB} and V_{SSMC}) unless otherwise noted.
7. V_{DDE_C} should be the same as V_{DDA} with a 100 mV variation, i.e., $V_{DDE_C} = V_{DDA} \pm 100$ mV.

NOTE

RAM data retention is guaranteed with VDD12 not below 1.08 V.

3.4.2 Connecting power supply pins: What to do and what not to do

- Do:
  - Have all power/ground supplies connected on the board from a strong supply source rather than weak voltage divider sources unless there is “NO IO activity” in the section
  - Meet the supply specifications for max / typical operating conditions to guarantee correct operation
  - Place the decoupling near the supply/ground pin pair for EMI emissions reduction
  - Route high-noise supply/ground away from sensitive signals (for example, ADC channels must be away from SMD supply/motor pads)
  - Use star routing for the ballast supply from the VDDR supply to avoid ballast startup noise injected to VDDR supply of the device
  - Use LC inductive filtering for ADC, OSC, and PLL supplies if these are generated from common board regulators
- Do not:
  - Violate injection current limit per IO/All IO pins as per specifications
  - Connect sensitive supplies/ground on noisy supplies/ground (that is, ADC, PLL, and OSC)
  - Use SMD supply for generation of noise free supply as these are most noisy lines in the system
  - Connect different VDD pins (connected together inside the device) to different potentials.

3.5 Thermal characteristics

Table 15. LQFP thermal characteristics

Symbol		C	Parameter	Conditions	Value		Unit
					144-pin	176-pin	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[1]	Single layer board—1s	50	43	°C/W
	CC			Four layer board—2s2p	41	35	°C/W
$R_{\theta JMA}$	CC	D	Thermal resistance, junction-to-moving-air ambient[2]	@ 200 ft./min., single layer board—1s	41	35	°C/W
	CC			@ 200 ft./min., four layer board—2s2p	35	30	°C/W
$R_{\theta JB}$	CC	D	Thermal resistance, junction-to-board[2]	—	29	24	°C/W
$R_{\theta JCtop}$	CC	D	Thermal resistance, junction-to-case (top)[3]	—	10	9	°C/W
Ψ_{JT}	CC	D	Junction-to-package top thermal characterization parameter, natural convection[4]	—	2	2	°C/W

NOTES:
1 Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[3] Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[4] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.5.1 General notes for specifications at maximum junction temperature

An estimate of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using Equation 2:

$$T_J = T_B + (R_{\theta JB} \times P_D) \quad \textit{Eqn. 2}$$

where:

T_B = board temperature for the package perimeter (°C)
$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8S
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 3}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction to case thermal resistance (°C/W)
$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ s device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using Equation 4:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
805 East Middlefield Rd.
Mountain View, CA 94043 USA
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

3.6 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.6.1 EMC requirements on board

The following practices help minimize noise in applications.

- Place a 100 nF capacitor between each of the V_{DD12}/V_{SS12} supply pairs and also between the V_{DDPLL}/V_{SSPLL} pair. The voltage regulator also requires stability capacitors for these supply pairs.
- Place a 10 μF capacitor on VDDR.
- Isolate VDDR with ballast emitter to avoid voltage droop during STANDBY mode exit.
- Enable pad slew rate only as necessary to eliminate I/O noise:
  - — Enabling slew rate for SMD pads will reduce noise on motors.
  - — Disabling slew rate for non-SMD pads will reduce noise on non-SMD IOs.
- Enable PLL modulation (± 2%) for system clock.
- Place decoupling capacitors for all HV supplies close to the pins.

3.6.2 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:

— Corrupted program counter
— Unexpected reset
— Critical data corruption (control registers...)

- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

3.6.3 Electromagnetic interference (EMI)

Table 16. EMI testing specifications[1]

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	SR	T	Scan range	150 kHz – 30 MHz: RBW 9 kHz, step size 5 kHz 30 MHz – 1 GHz: RBW 120 kHz, step size 80 kHz	0.15	—	1000	MHz
—	SR	T	Operating frequency	Crystal frequency 8 MHz	—	64	—	MHz
—	SR	T	VDD12, VDDPLL operating voltages	—	—	1.28	—	V
—	SR	T	VDD, VDDA operating voltages	—	—	5	—	V
—	SR	T	Maximum amplitude	No PLL frequency modulation	—	33	—	dBµV
				±2% PLL frequency modulation	—	30	—	
—	SR	T	Operating temperature	—	—	25	—	°C

NOTES:
1 EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03.

3.6.4 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

3.6.4.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 17. ESD absolute maximum ratings[1] [2]

Symbol		C	Ratings	Conditions	Class	Max value	Unit
$V_{ESD(HBM)}$	CC	T	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	CC	T	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	CC	T	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
						750 (corners)	

NOTES:
1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.6.4.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 18. Latch-up results

Symbol		C	Parameter	Conditions	Class
LU	CC	T	Static latch-up class	T_A = 105 °C conforming to JESD 78	II level A

3.7 Power management electrical characteristics

3.7.1 Voltage regulator electrical characteristics

The internal high power or main regulator (HPREG) requires an external NPN ballast transistor (see Table 19 and Table 20) to be connected as shown in Figure 5 as well as an external capacitance (C_{REG}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 15 nH.

For the PXD10 microcontroller, 100 nF should be placed between each of the V_{DD12}/V_{SS12} supply pairs and also between the V_{DDPLL}/V_{SSPLL} pair. These decoupling capacitors are in addition to the required stability capacitance. Additionally, 10 µF should be placed between the V_{DDR} pin and the adjacent V_{SS} pin.

V_{DDR} = 3.0 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 to 105 °C, unless otherwise specified.

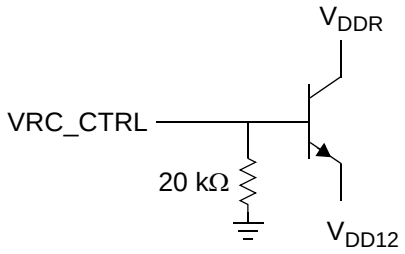


Figure 5. External NPN ballast connections

Table 19. Allowed ballast components

Part	Manufacturer	Recommended derivative
BCP68	ON, IFX, NXP, Fairchild, ST, etc.	BCP68
BCX68	IFX	BCX68-10 BCX68-16
BC817	ON, IFX, NXP, Fairchild, etc.	BC817Su BC817-25
BCP56	ON, IFX, NXP, Fairchild, ST, etc.	BCP68-10 BCP68-16

Table 20. Ballast component parameters

Parameter	Specification
Capacitance on VDDR	10 μF (minimum) Place close to NPN collector
Stability capacitance on VDD12	40 μF (minimum) Place close to NPN emitter
Decoupling capacitance on VDD12	100 nF × number of pins (minimum) Place on each VDD12/VSS12 pair and on the PLL supply/ground pair
Base resistor	20 kΩ

The capacitor values listed in Table 20 include a de-rating factor of 40%, covering tolerance, temperature, and aging effects. These factors are taken into account to assure proper operation under worst-case conditions. X7R type materials are recommended for all capacitors, based on ESR characteristics.

Large capacitors are for regulator stability and should be located near the external ballast transistor. The number of capacitors is not important — only the overall capacitance value and the overall ESR value are important.

Small capacitors are for power supply decoupling, although they do contribute to the overall capacitance values. They should be located close to the device pin.

Table 21. Voltage regulator electrical characteristics

Symbol		C	Parameter		Conditions	Value			Unit
						Min	Typ	Max	
T_J	SR	C	Junction temperature		—	–40	—	150	°C
I_{REG}	CC	C	Current consumption		Reference included, @ 55 °C No load @ Full load	—	—	 2 11	mA
I_L	CC	C	Output current capacity		DC load current	—	—	200	mA
V_{DD12}	CC	C	Output voltage		Pre-trimming sigma < 7 mV	—	1.330	—	V
		P			Post-trimming	1.145	1.28	1.32	V
	SR	C	External decoupling/stability capacitor		4 capacitances of 10 µF each	—	—	10 × 4	µF
		C			ESR of external cap	0.05	—	0.2	Ω
		C			1 bond wire R + 1 pad R	0.2		1	Ω
L_{BOND}	CC	D	Bonding Inductance for Bipolar Base Control pad		—	0	—	15	nH
	CC	D	Power supply rejection	@ DC @ no load	C_L = 10 µF × 4	—	—	–30	dB
		D		@ 200 kHz @ no load				–100	
		D		@ DC @ 200 mA				–30	
		D		@ 200 kHz @ 200 mA				–30	
	CC	D	Load current transient		C_L = 10 µF × 4	—	—	10% to 90% of I_L (max) in 100 ns	
t_{SU}	CC	C	Start-up time after input supply stabilizes[1]		C_L = 10 µF × 4	—	—	100	µs

NOTES:
1 Time after the input supply to the voltage regulator has ramped up (V_{DDR}).

Table 22. Low-power voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
T_J	SR	C	Junction temperature	—	–40		150	°C
I_{REG}	CC	C	Current consumption	Reference included, @ 55 °C No load @ Full load	—	—	 5 600	µA
I_L	CC	C	Output current capacity[1]	DC load current	—	—	15	mA
V_{DD12}	CC	C	Output voltage	Pre-trimming sigma < 7 mV	—	1.33		V
		P		Post-trimming	1.14	1.24	1.32	

Table 22. Low-power voltage regulator electrical characteristics (continued)

Symbol		C	Parameter		Conditions	Value			Unit
						Min	Typ	Max	
	SR	C	External decoupling/stability capacitor		4 capacitances of 10 µF each	10 × 4	—	10 × 4	µF
		C			ESR of external cap	0.1	—	0.6	ohm
		C			1 bond wire R + 1 pad R	0.2	—	1	ohm
L_{BOND}	CC	D	Bonding Inductance for Bipolar Base Control pad		—	0	—	15	nH
	CC	D	Power supply rejection	@ DC @ no load	C_L = 10 µF × 4	—	—	55	dB
		D		any frequency @ no load				32	
		D		@ DC @ max load				24	
		D		any frequency @ max load				12	
	CC	D	Load current transient		C_L = 10 µF × 4	—	—	10% to 90% of I_L in 10 µs	
t_{SU}	CC	C	Start-up time after input supply stabilizes[2]		C_L = 10 µF × 4	—	—	700	µs

NOTES:
1 On this device, the ultra-low-power regulator is always enabled when the low-power regulator is enabled. Therefore, the total low-power current capacity is the sum of I_L values for the two regulators.

2 Time after the input supply to the voltage regulator has ramped up (V_{DDR}) and the voltage regulator has asserted the Power OK signal.

Table 23. Ultra-low-power voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
T_J	SR	C	Junction temperature	—	−40	—	150	°C
I_{REG}	CC	C	Current consumption	Reference included, @ 55 °C No load @ Full load	—	—	2 100	µA
I_L	CC	C	Output current capacity	DC load current	—	—	5	mA
V_{DD12}	CC	C	Output voltage (value @ I_L = 0 @ 27 °C)	Pre-trimming sigma < 7 mV	—	1.33	—	V
				Post-trimming	1.14	1.24	1.32	

Table 23. Ultra-low-power voltage regulator electrical characteristics (continued)

Symbol		C	Parameter		Conditions	Value			Unit
						Min	Typ	Max	
	CC	D	Power supply rejection	@ DC @ no load	—	—		25	dB
		D		any frequency @ no load				7	
		D		@ DC @ max load				25	
		D		any frequency @ max load				8	
	CC	D	Load current transient		—	—		10 to 90 μA in 70 μs	

3.7.2 Voltage monitor electrical characteristics

The device implements a Power-on Reset (POR) module to ensure correct power-up initialization, as well as four low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD12} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

Table 24. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{PORH}	CC	P	Power-on reset threshold	—	1.5	—	2.6	V
$V_{LVDHV3H}$	CC	P	LVDHV3 low voltage detector high threshold	—	—	—	2.9	
$V_{LVDHV5H}$	CC	P	LVDHV5 low voltage detector high threshold	—	—	—	4.4	
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold	—	2.6	—	—	
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold	—	3.8	—	—	
$V_{LVDLVCORH}$	CC	P	LVDLVCOR low voltage detector high threshold	T_A = 25 °C, after trimming	—	—	1.14	
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold		1.08	—	—	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified

3.7.3 Low voltage domain power consumption

Table 25 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 25. DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	T_A	Value			Unit
						Min	Typ	Max	
I_{DDRUN}[2]	CC	P	RUN mode current	—		—	130	180	mA
I_{DDHALT}	CC	P	HALT mode current	—		—	4	25	mA
I_{DDSTOP}	CC	P	STOP mode current	16 MHz fast internal RC oscillator off, HPVREG off	25°C	—	250	1800	µA
					105°C	—	5	20	mA
				16 MHz fast internal RC oscillator off, HPVREG on	25°C	—	2.5	6.5	mA
					105°C	—	7	25	mA
$I_{DDSTDBY}$	CC	C	STANDBY mode current	See Table 26					
$I_{DDSTDBY1}$[3]	CC	P	STANDBY1 mode current		25°C	—	20	100	µA
					105°C	—	180	—	µA
				T_J = 150°C	—	—	350	1500	µA
$I_{DDSTDBY2}$[4]	CC	P	STANDBY2 mode current		25°C	—	30	100	µA
					105°C	—	350	—	µA
				T_J = 150°C	—	—	600	2500	µA

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C
2. Value is for maximum peripherals turned on. May vary significantly based on different configurations, active peripherals, operating frequency, etc.
3. ULPreg on, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.
4. ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.

Table 26. IDDSTDBY specification[1]

Temperature (T_A,°C)	FIRC off, 8 KB RAM on		FIRC on, 8 KB RAM on		32 kHz SXOSC on, 8 KB RAM on		32 kHz SXOSC on, all RAM on	
	3.3 V	5.5 V	3.3 V	5.5 V	3.3 V	5.5 V	3.3 V	5.5 V
–40	16 µA	25 µA	326 µA	340 µA	16 µA	26 µA	22 µA	32 µA
0	18 µA	29 µA	334 µA	347 µA	19 µA	29 µA	26 µA	37 µA
25	23 µA	33 µA	342 µA	355 µA	24 µA	34 µA	34 µA	45 µA
55	41 µA	51 µA	363 µA	377 µA	42 µA	53 µA	69 µA	80 µA
85	93 µA	104 µA	421 µA	435 µA	100 µA	110 µA	182 µA	195 µA
105	173 µA	185 µA	502 µA	517 µA	181 µA	194 µA	344 µA	358 µA
125[2]	320 µA	334 µA	648 µA	667 µA	321 µA	335 µA	620 µA	638 µA
150[2]	681 µA	698 µA	1005 µA	1028 µA	654 µA	677 µA	1270 µA	1300 µA

NOTES:
1. All current values are typical values.

[2] Values provided for reference only. The permitted temperature range of the chip is specified separately.

3.7.4 Recommended power-up and power-down order

Figure 6 shows the recommended order for powering up the power supplies on this device.

The 1.2 V regulator output starts after the device's internal POR (VDDREG HV) is deasserted at approximately 2.7 V on VDDREG.

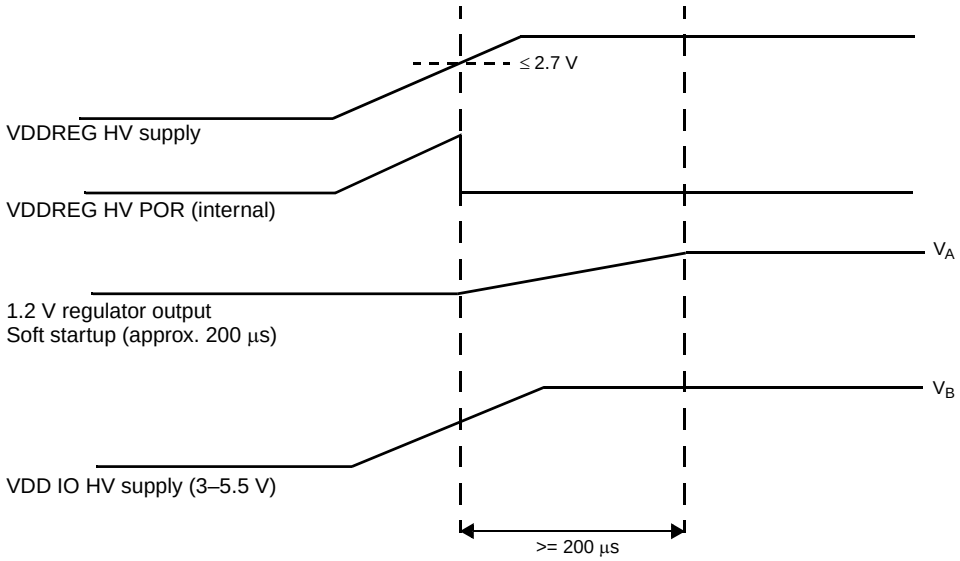


Figure 6. Recommended order for powering up the power supplies

CAUTION

The voltages V_A and V_B in Figure 6 must always obey the relation $V_B \geq V_A - 0.7$ V. Otherwise, currents from the 1.2 V supply to the 3.3 V supply may result.

Figure 7 shows the recommended order for powering down the power supplies on this device.

It is acceptable for the VDD IO HV supply to ramp down faster than the 1.2 V regulator output, even if the latter takes time to discharge the high 40 µF capacitance. (The capacitor will ultimately discharge.)

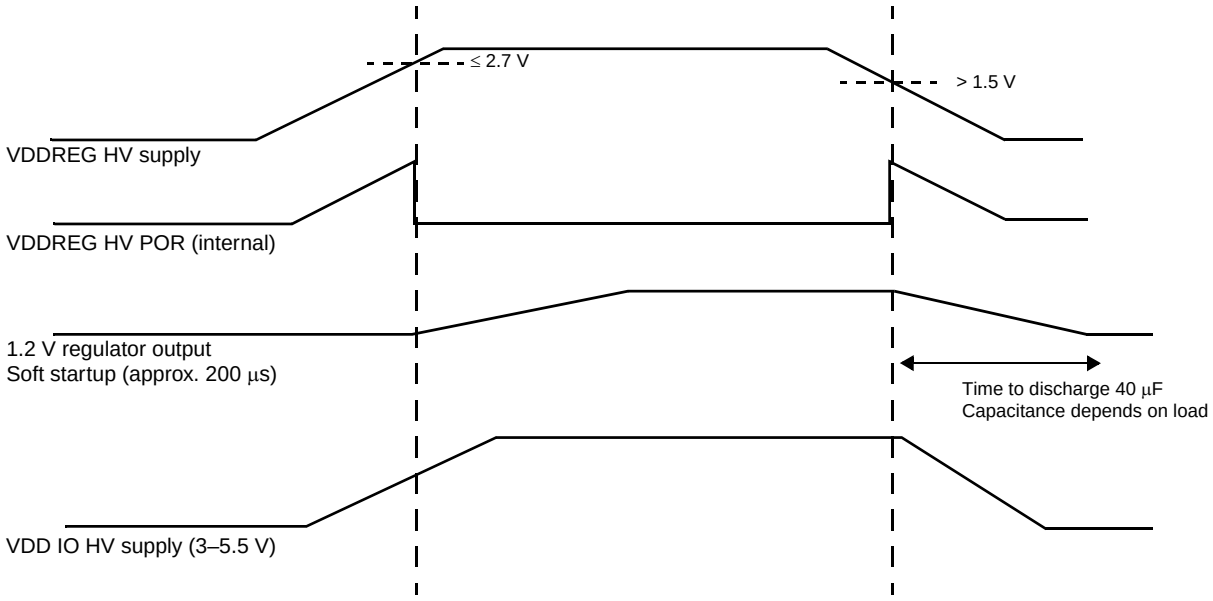


Figure 7. Recommended order for powering down the power supplies

CAUTION

The VDD IO HV supply must be disabled after the VDDREG HV supply voltage drops below 1.5 V. This is to ensure that the 1.2 V regulator shuts down before the 3.3 V regulator shuts down.

3.7.5 Power-up inrush current profile

Figure 8 shows the power up inrush current profile of the ballast transistor under the worst possible startup condition (fastest PVT and fastest power ramp time).

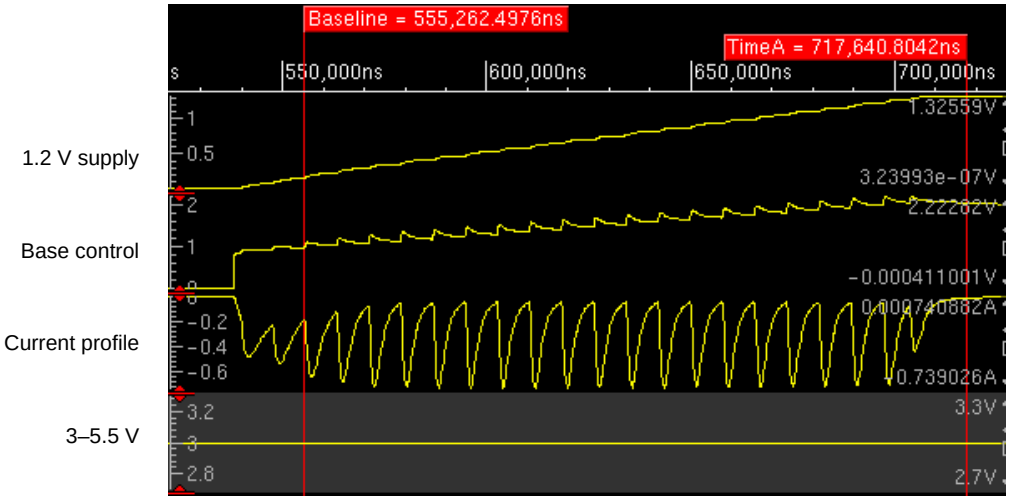


Figure 8. Power-up inrush current profile

The HPREG has a “soft startup” profile which increases the supply in steps of approximately 50 mV in a series of approximately 25 steps. Therefore, the peak current is within 750 mA of the maximum current during startup. This eliminates any noise on the VDDR supply during startup and charging of NPN emitter stability capacitance of 40 µF (minimum).

Soft startup also occurs when waking up from standby mode to limit noise on the VDDR supply.

In case VDDR is shared between the device and the ballast, it must be star routed on the board or isolated as much as possible to avoid any noise injected by the ballast. Soft startup will help to limit this noise but a VDDR capacitor close to the ballast pin is critical here. A minimum capacitance of 10 µF is needed.

Table 27 shows the typical and maximum startup currents.

Table 27. Startup current

Symbol		C	Parameter	Value		Unit
				Typ	Max	
I_{START}	CC	T	Startup current	300	800	mA

3.7.6 HPREG load regulation characteristics

The HPREG exhibits a very strong load-regulation behavior (the transition from low- to high-current state is regulated quickly). This is illustrated in Figure 10, which shows a 10–150 mA jump over 10 ns. Under any case of load transition, the HPREG responds within 100 ns and stabilizes within 5 µs. This helps improve the stability of the 1.2 V supply and settling time.

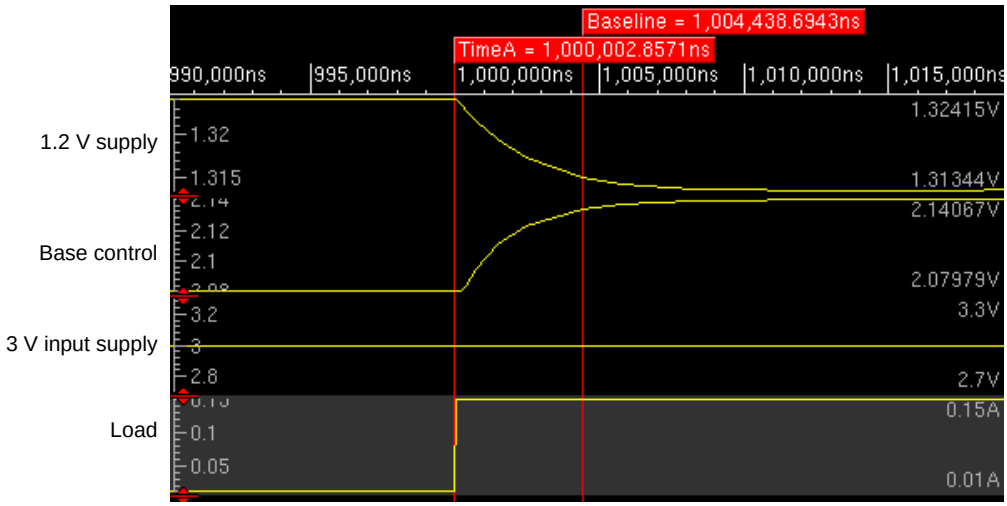


Figure 9. HPREG load regulation

3.8 I/O pad electrical characteristics

3.8.1 I/O pad types

The device provides five main I/O pad types:

- Slow pads — These are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads — These are provided in two types (M1 and M2) and provide transitions fast enough for the serial communication channels. M2 pads include slew rate control.
- Fast pads — These provide maximum speed. There are used for improved NEXUS debugging capability.
- SMD pads — These provide additional current capability to drive stepper motor loads.
- Digital I/O with analog (J) pad — These provide input and output digital features and analog input for ADC.

M2 and Fast pads can disable slew rate to reduce electromagnetic emission, at the cost of reducing AC performance.

3.8.2 I/O input DC characteristics

Table 28 provides input DC electrical characteristics as described in Figure 10.

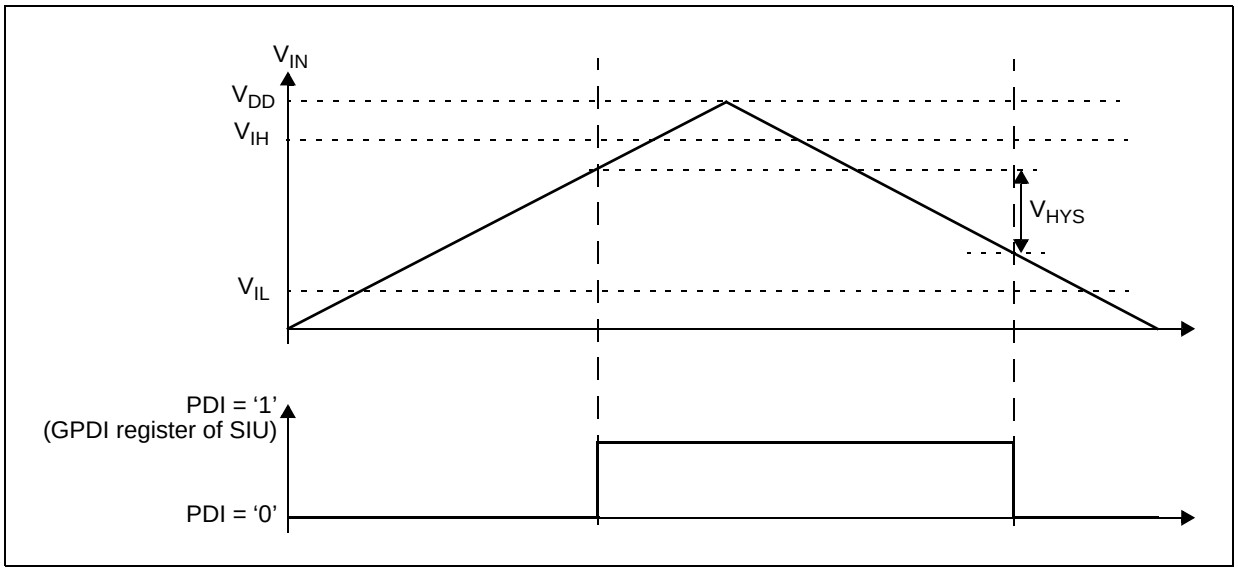


Figure 10. I/O input DC electrical characteristics definition

Table 28. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS Schmitt trigger	—	$0.65V_{DD}$	—	V_{DD} + 0.3	V
V_{IL}	SR	P	Input low level CMOS Schmitt trigger	—	–0.3	—	$0.35V_{DD}$	
V_{HYS}	CC	D	Input hysteresis CMOS Schmitt trigger	—	$0.1V_{DD}$	—	—	

Table 28. I/O input DC electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{LKG}	CC	P	Input leakage current	—	–1	—	1	µA
				T_A = -40°C	—	2	—	nA
				T_A = 25°C	—	2	—	nA
		C		T_A = 105°C	—	12	500	nA
		P		T_J = 150°C	—	70	1000	nA
R_{ON}	CC	D	Resistance of the analog switch inside the J pad type[2]	Supply range 3.3–5 V	—	—	1	kΩ

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C.
2 Applies to the J pad type only.

3.8.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 29 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 30 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 31 provides output driver characteristics for I/O pads when in MEDIUM configuration (applies to both M1 and M2 type pads).
- Table 32 provides output driver characteristics for I/O pads when in FAST configuration.
- Table 33 provides SMD pad characteristics.

Table 29. I/O pull-up/pull-down DC electrical characteristics [1]

Symbol		C	Parameter	Conditions[2]		Value			Unit
						Min	Typ	Max	
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	V_{IN} = V_{IL}, V_{DD} = 5.0V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[3]	10	—	250	
		P		V_{IN} = V_{IL}, V_{DD} = 3.3V ± 10%	PAD3V5V = 1	10	—	150	
$\|I_{WPD}\|$	CC	P	Weak pull-down current absolute value	V_{IN} = V_{IL}, V_{DD} = 5.0V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		V_{IN} = V_{IL}, V_{DD} = 3.3V ± 10%	PAD3V5V = 1	10	—	150	

NOTES:
1 The pull currents are dependent on the HVE settings.
2 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
3 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 30. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull, I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		D		Push Pull, I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C		Push Pull, I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		D		Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	T	Output transition time output pin[3] SLOW configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	100	
		T		C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	125	
		T		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
		T		C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	75	
ΔI_{tr50}	CC	D	Current slew at C_L = 50 pF SLOW configuration	recommended configuration at V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	2	mA/ns
		D		V_{DD} = 5.0 V ± 10%, PAD3V5V = 1	—	—	7	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified
2 This is a transient configuration during power-up. All pads but $\overline{\text{RESET}}$ and NEXUS output (MDOx, EVTO, MCK) are configured in input or in high impedance state.
3 C_L calculation should include device and package capacitances (C_{PKG} < 5 pF).

Table 31. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{OH}	CC	P	Output high level MEDIUM configuration	Push Pull, I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		D		Push Pull, I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C		Push Pull, I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level MEDIUM configuration	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		D		Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	T	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
		T		C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
		T		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
		T		C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
		T		C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
ΔI_{tr50}	CC	D	Current slew at C_L = 50 pF MEDIUM configuration	recommended configuration at V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	7	mA/ns
		D		V_{DD} = 5.0 V ± 10%, PAD3V5V = 1	—	—	16	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified
2 This is a transient configuration during power-up. All pads but $\overline{\text{RESET}}$ and NEXUS output (MDOx, EVTO, MCK) are configured in input or in high impedance state.
3 C_L includes device and package capacitance (C_{PKG} < 5 pF).

Table 32. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{OH}	CC	P	Output high level FAST configuration	Push Pull, I_{OH} = –14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		D		Push Pull, I_{OH} = –7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C		Push Pull, I_{OH} = –11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level FAST configuration	Push Pull, I_{OL} = 14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		D		Push Pull, I_{OL} = 7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	T	Output transition time output pin[3] FAST configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6	
		T		C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	12	
		T		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
		T		C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	7	
		T		C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
ΔI_{tr50}	CC	D	Current slew at C_L = 50 pF FAST configuration	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended configuration)	—	—	55	mA/ns
		D		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended configuration)	—	—	40	
		D		V_{DD} = 5.0 V ± 10%, PAD3V5V = 1	—	—	100	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified
2 This is a transient configuration during power-up. All pads but $\overline{\text{RESET}}$ and NEXUS output (MDOx, EVTO, MCK) are configured in input or in high impedance state.
3 C_L includes device and package capacitance (C_{PKG} < 5 pF).

Table 33. SMD pad electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IL}	CC	P	Low level input voltage	—	–0.4	—	$0.35 \times V_{DDM}$	V
V_{IH}	CC	P	High level input voltage	—	$0.65 \times V_{DDM}$	—	$V_{DDM}+0.4$	
V_{HYST}	CC	C	Schmitt trigger hysteresis	—	$0.1 \times V_{DDM}$	—	—	
V_{OL}	CC	P	Low level output voltage	I_{OL} = 20 mA[1]	—	—	0.32	
				I_{OL} = 30 mA[2]	—	—	0.48	
V_{OH}	CC	P	High level output voltage	I_{OH} = –20 mA[1]	V_{DDM}–0.32	—	—	
				I_{OH} = –30 mA[2]	V_{DDM}–0.48	—	—	
I_{PU}	CC	P	Internal pull-up device current	$V_{in}=V_{IL}$	–130	—	—	µA
				$V_{in}=V_{IH}$	—	—	–10	
I_{PD}	CC	P	Internal pull-down device current	$V_{in}=V_{IL}$	10	—	—	
				$V_{in}=V_{IH}$	—	—	130	
I_{IN}	CC	P	Input leakage current	—	-1	—	1	
R_{DSONH}	CC	C	SMD pad driver active high impedance	IOH ≤ –30 mA[2]	—	—	16	Ω
R_{DSONL}	CC	C	SMD pad driver active low impedance	IOL ≤ 30 mA[2]	—	—	16	Ω
V_{OMATCH}	CC	P	Output driver matching V_{OH} / V_{OL}	I_{OH} / I_{OL} ≤ 30 mA[2]	—	—	90	mV

NOTES:
1 VDD = 5.0 V ±10%, Tj = -40 to 150 °C.
2 VDD = 5.0 V ±10%, Tj = -40 to 130 °C.

3.8.4 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 34.

Table 35 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Table 34. I/O supply segment

Package	Supply segment				
	A[1]	B[2]	C[3,4]	D[5]	E[6]
144 LQFP	pins 1–21 pins 113–144	pins 22– 52	pins 53–72	pins 73–102	pins 103–112
176 LQFP	pins 1–21 pins 143–176	pins 22–68	pins 69–88	pins 89–118	pins 119–142

NOTES:
1 LCD pad segment containing pad supplies V_{DDE_A}
2 Miscellaneous pad segment containing pad supplies V_{DDE_B}
3 ADC pad segment containing pad supplies V_{DDE_C}
4 V_{DDE_C} should be the same as V_{DDA} with a 100 mV variation, i.e., $V_{DDE_C} = V_{DDA} \pm 100$ mV.
5 Stepper Motor pad segment containing I/O supplies V_{DDMA}, V_{DDMB}, V_{DDMC}
6 Miscellaneous pad segment containing pad supplies V_{DDE_E}

Table 35. I/O consumption

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{SWTSLW}	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
		D		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
		D		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
		D		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
		D		C_L = 25 pF, 4 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	3.2	
		D		C_L = 100 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	
		D		C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
		D		C_L = 25 pF, 4 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	2.3	
		D		C_L = 100 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4.7	

Table 35. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
		D		C_L = 25 pF, 4 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	13.4	
		D		C_L = 100 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	18.3	
		D		C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5.0	
		D		C_L = 25 pF, 4 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	8.5	
		D		C_L = 100 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	11.0	
I_{RMSFST}	CC	D	Root mean square I/O current for FAST configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22.0	mA
		D		C_L = 25 pF, 4 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	33.0	
		D		C_L = 100 pF, 2 MHz V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	56.0	
		D		C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14.0	
		D		C_L = 25 pF, 4 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	20.0	
		D		C_L = 100 pF, 2 MHz V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25.0	
I_{DYNSEG}	SR	D	Sum of all the dynamic and static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
		D		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	65	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	70	mA
		D		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	65	
$I_{DDMxAVG}$	SR	D	Sum of currents of two motors assigned to segment V_{DDMx}, V_{SSMx} pair	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 T_J = 130 °C	—	—	90	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 T_J = –40 °C	—	—	120	

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified

3.9 SSD specifications

3.9.1 Electrical characteristics

Table 36. SSD electrical characteristics

Symbol		C	Parameter	Value[1]			Unit
				Min	Typ	Max	
V_{VREF}	CC	P	Reference voltage (I_{VREF} = 0)	V_{DDM}/2 - 0.02	V_{DDM}/2	V_{DDM}/2 + 0.02	V
I_{VREF}	CC	P	Reference voltage output current	1.85	—	—	mA
R_{IN}	CC	D	Input resistance (against V_{DDM}/2)	0.8	1.0	1.2	MΩ
V_{IN}	CC	C	Input common mode range	V_{SSM}	—	V_{DDM}	V
SSD_{CONST}	CC	C	SSD constant	0.549	0.572	0.597	—
SSD_{OFFSET}	CC	C	SSD offset (unipolar, N_{sample} = 256)	–9	—	9	counts
			SSD offset (bipolar, N_{sample} = 256)	–8	—	8	
			SSD offset (bipolar with offset cancellation, N_{sample} = 256)	–5	—	5	
f_{SSDSMP}	CC	D	SSD cmpout sample rate	0.5	—	2.0	MHz

NOTES:
1 Vdd = 5.0V +/- 10%, Tj = -40C to +150C.

3.9.2 Accumulator values

Equation 5 describes the accumulator value in unipolar configuration. The voltage V_{in} is applied between the integrator input and V_{DDM}. The internal generated reference voltage is not connected. The accumulator value is a function of V_{DDM}, the number of samples (Nsample) taken and the SSD constant (SSDconst). The SSD constant and offset (SSDconst, SSDoffset) vary with temperature and process.

$$ACCval = \frac{V_{in} - (VDDM)/2}{VDDM \cdot SSDconst} \cdot Nsample + SSDoffset$$

Eqn. 5

Equation 6 describes the accumulator value in bipolar configuration. The voltage V_{in} is applied between the integrator input and the reference output. The accumulator value depends on the same parameters as in the unipolar case but the inaccuracy of the voltage reference (Vvref) is compensated.

$$ACCval = \frac{V_{in}}{VDDM \cdot SSDconst} \cdot Nsample + SSDoffset$$

Eqn. 6

3.10 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 11. Start-up reset requirements

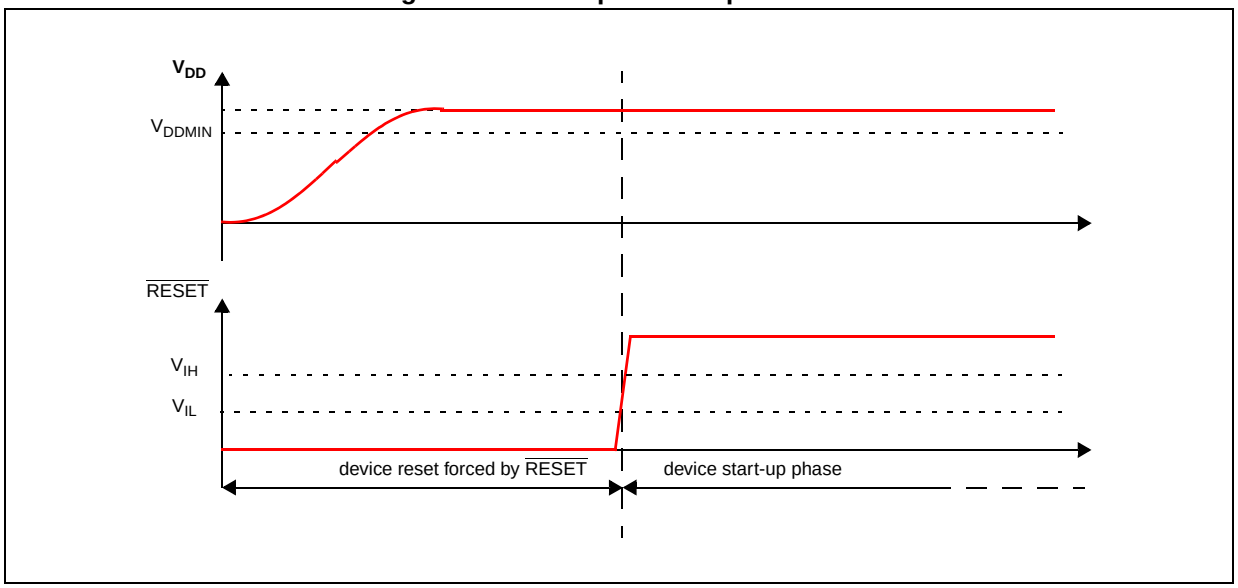


Figure 12. Noise filtering on reset signal

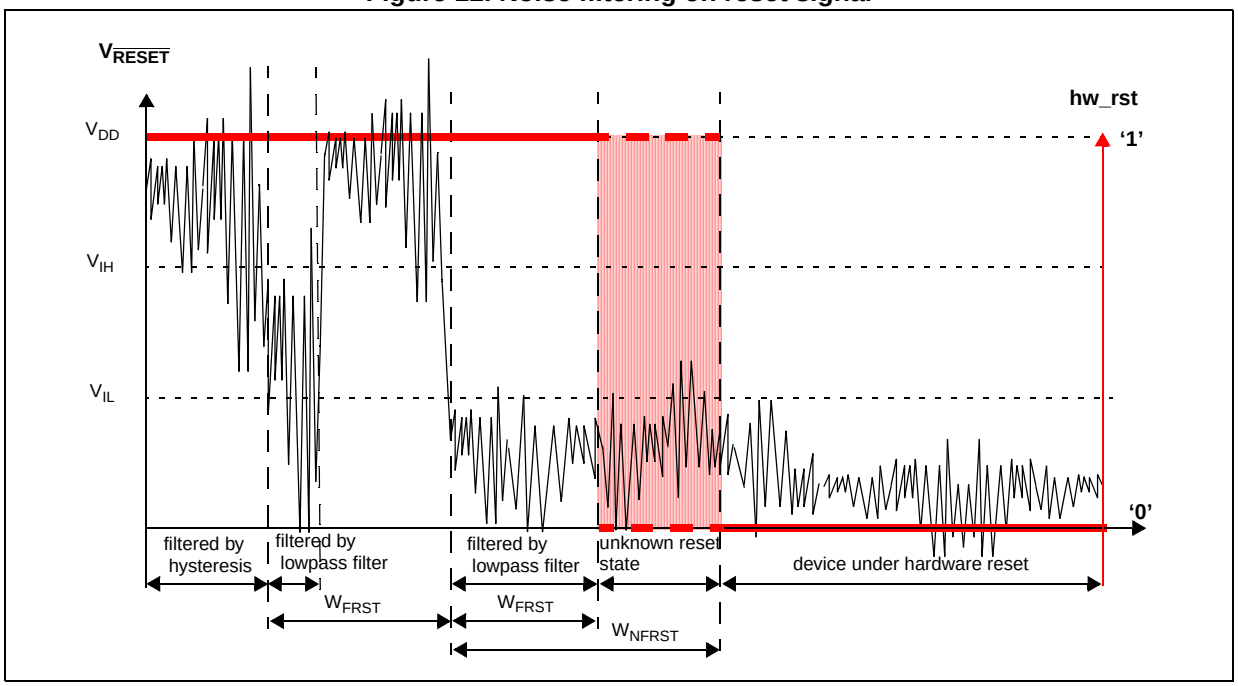


Table 37. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS Schmitt Trigger	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS Schmitt Trigger	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	D	Input hysteresis CMOS Schmitt Trigger	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		D		Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	T	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
		T		C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
		T		C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
		T		C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
		T		C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	1000	—	—	ns
I_{WPU}	CC	P	Weak pull-up current absolute value	—	10	—	150	µA
		D	RUN Current during RESET	Before Flash is ready	—	10	—	mA
				After Flash is ready	—	20	—	mA

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified
2. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to reset generation module (RGM) section of the device reference manual).
3. C_L includes device and package capacitance (C_{PKG} < 5 pF).

3.11 Fast external crystal oscillator (4–16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 13 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

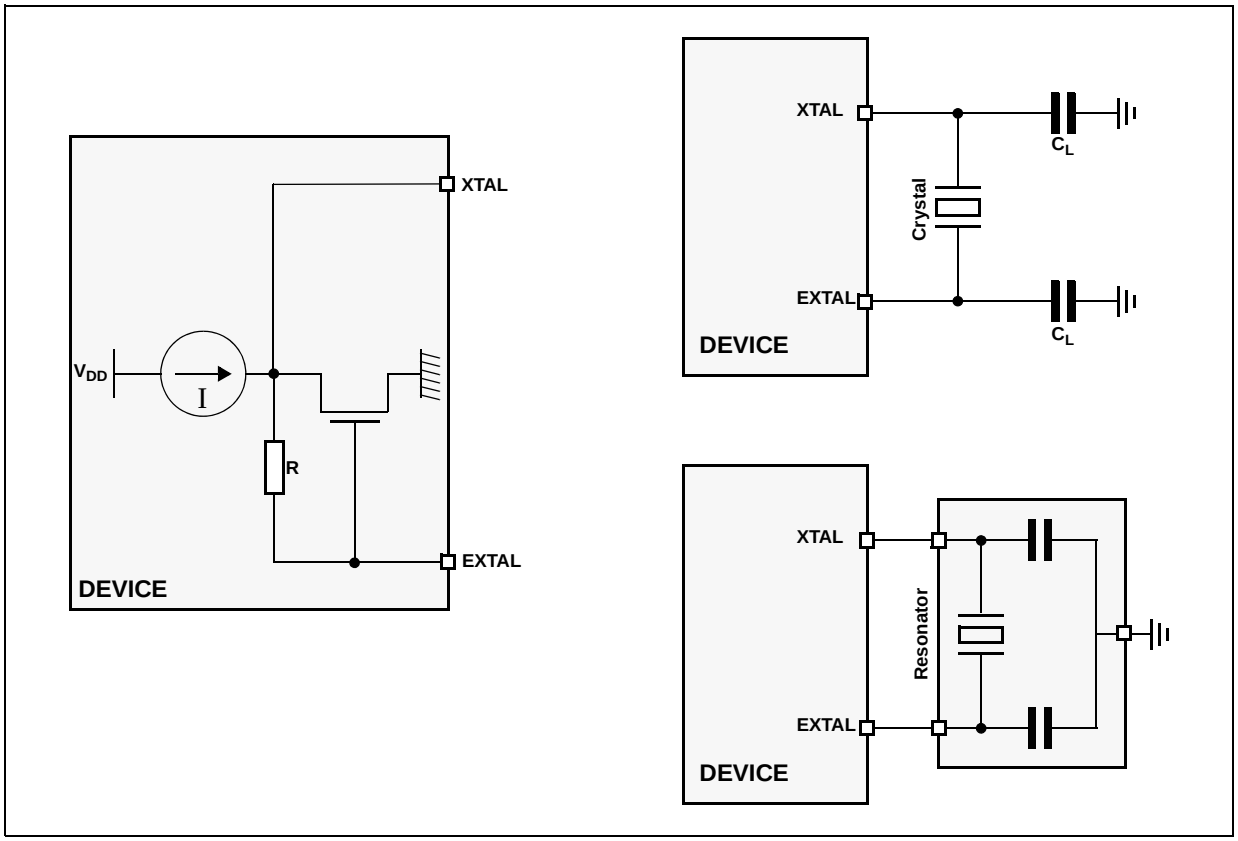


Figure 13. Crystal oscillator and resonator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 38. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout C1 = C2 (pF)[1]	Shunt capacitance between xtalout and xtalin C0[2] (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

NOTES:
1 The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.
2 The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

Table 39. Resonator description

	CSTCR4M00G53-R0	CSTCR4M00G55-R0
Vibration	Fundamental	
Fr (kHz)	3929.50	3898.00
Fa (kHz)	4163.25	4123.00
Fa–Fr (dF) (kHz)	233.75	225.00
Ra (kΩ)	372.41	465.03
R1 (Ω)	12.78	11.38
L1 (mH)	0.84443	0.88244
C1 (pF)	1.94268	1.88917
Co (pF)	15.85730	15.90537
Qm	1630.93	1899.77
CL1 (nominal) (pF)	15	39
CL2 (nominal) (pF)	15	39

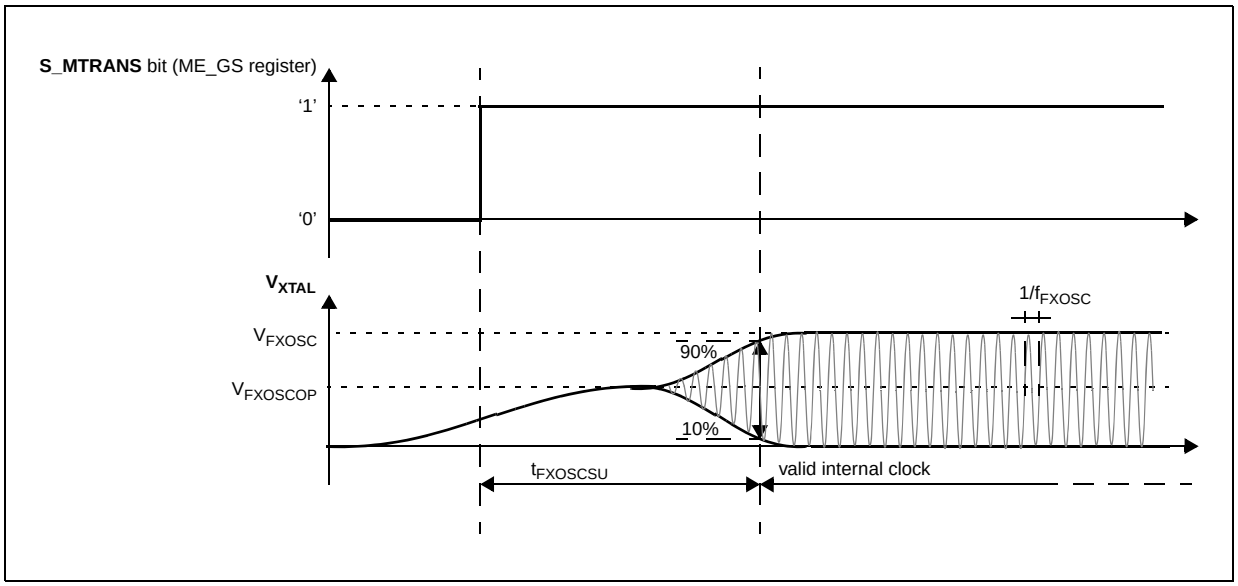


Figure 14. Fast external crystal oscillator (4–16 MHz) electrical characteristics

Table 40. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{FXOSC}	SR	—	Fast external crystal oscillator frequency	—	4.0	—	16.0	MHz
g_{mFXOSC}	CC	C	Fast external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0	2.2	—	8.2	mA/V
	CC	P		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0	2.0	—	7.4	
	CC	C		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1	2.7	—	9.7	
	CC	C		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1	2.5	—	9.2	
V_{FXOSC}	CC	T	Oscillation amplitude at EXTAL	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	1.3	—	—	V
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	1.3	—	—	
$V_{FXOSCOP}$	CC	C	Oscillation operating point	—	—	0.95	—	V
I_{FXOSC},[2]	CC	T	Fast external crystal oscillator consumption	—	—	2	3	mA
$T_{FXOSCSU}$	CC	T	Fast external crystal oscillator start-up time	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6	ms
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	$0.65V_{DD}$	—	V_{DD}+0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	–0.4	—	$0.35V_{DD}$	V

NOTES:
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified
2. Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals)

3.12 Slow external crystal oscillator (32 KHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

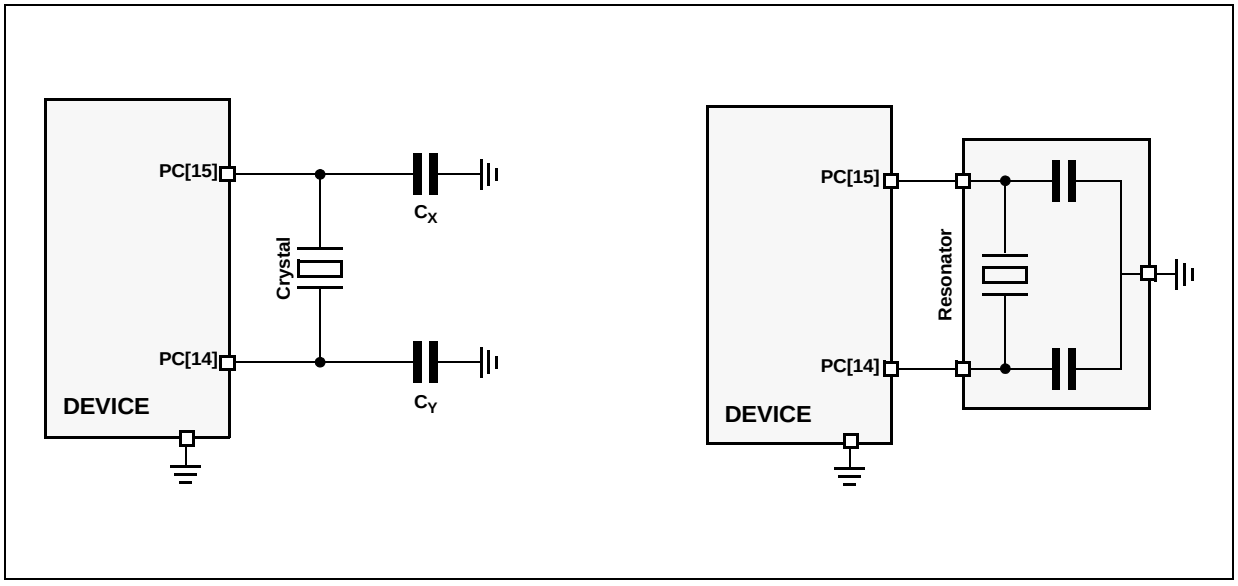


Figure 15. Crystal oscillator and resonator connection scheme

NOTE

PC[14]/PC[15] must not be directly used to drive external circuits.

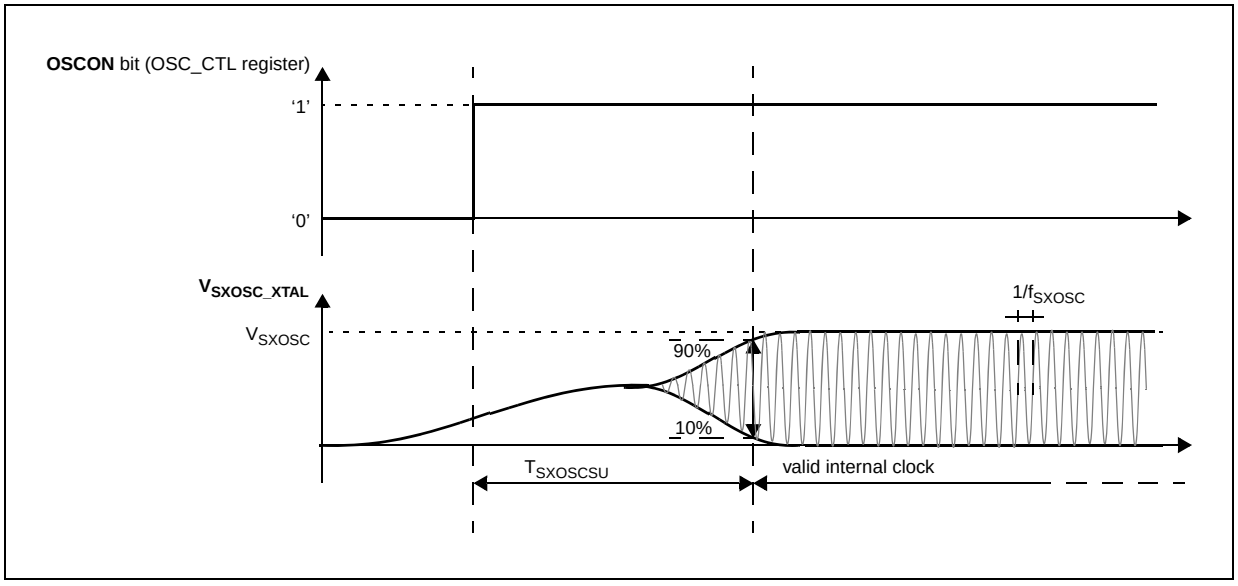


Figure 16. Slow external crystal oscillator (32 KHz) timing

Table 41. Slow external crystal oscillator (32 KHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	T	Slow external crystal oscillator frequency	—	32	—	40	kHz
V_{SXOSC}	CC	T	Oscillation amplitude	V_{DD} = 3.3 V ± 10%	1.12	1.33	1.74	V
		T		V_{DD} = 5.0 V ± 10%	1.12	1.37	1.74	
I_{SXOSC}	CC	D	Slow external crystal oscillator consumption	—	—	—	5	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2^2	s
V_{IH}	SR	D	Input high level CMOS Schmitt Trigger	Oscillator bypass mode	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	D	Input low level CMOS Schmitt Trigger	Oscillator bypass mode	–0.4	—	$0.35V_{DD}$	V

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified
2 The quoted figure is based on a board that is properly laid out and has no stray capacitances.

3.13 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 42. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	T	FMPLL reference clock[2]	—	4	—	64	MHz
Δ_{PLLIN}	SR	T	FMPLL reference clock duty cycle[2]	—	40	—	60	%
f_{PLLOUT}	CC	T	FMPLL output clock frequency	—	16	—	64	MHz
f_{CPU}	CC	T	System clock frequency	—	—	—	64[3]	MHz
t_{LOCK}	CC	T	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	—	200	µs
Δt_{PKJIT}	CC	T	FMPLL jitter (peak to peak)	f_{PLLIN} = 16 MHz (resonator)	—	—	220	ps
Δt_{LTJIT}	CC	T	FMPLL long term jitter	f_{PLLIN} = 16 MHz (resonator)	—	—	1.5	ns
I_{PLL}	CC	D	FMPLL consumption	T_A = 25 °C	—	—	4	mA

NOTES:
1 V_{DDPLL} = 1.2 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified.
2 PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
3 f_{CPU} 64 MHz can be achieved only at temperatures up to T_A = 105 °C with a maximum FM depth of 2%.

3.14 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz fast internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 43. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed			16		MHz
	SR	—		—		12		20	
$\Delta_{FIRCVAR}$	CC	C	Fast internal RC oscillator variation across temperature (T_A = -40°C to 105°C) and supply with respect to f_{FIRC} at T_A = 25 °C in high-frequency configuration	Trimmed	—	–5	—	+5	%
$I_{FIRCRUN}$	CC	D	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed	—	—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C	—	—	—	1	µA
$I_{FIRCSTOP}$	CC	D	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	0.3	—	mA
		D			sysclk = 2 MHz	—	2	—	
		D			sysclk = 4 MHz	—	2.5	—	
		D			sysclk = 8 MHz	—	3.3	—	
		D			sysclk = 16 MHz	—	5.2	—	
t_{FIRCSU}	CC	P	Fast internal RC oscillator start-up time		V_{DD} = 5.0 V ± 10%	—	1	2	µs

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified.

3.15 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz slow internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 44. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz
	SR	—		—	100		150	
$\Delta_{SIRCVAR}$	CC	C	Slow internal RC oscillator variation across temperature (T_A = -40°C to 105°C) and supply with respect to f_{SIRC} at T_A = 25 °C in high frequency configuration	Trimmed	-10%		+10%	kHz
I_{SIRC}	CC	D	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA
t_{SIRCSU}	CC	C	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs

NOTES:
1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified.

3.16 Flash memory electrical characteristics

Table 45. Program and erase specifications

Symbol		C	Parameter	Value			Unit
				Typ[1]	Initial max[2]	Max[3]	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	22	50	500	µs
$T_{16kpperase}$	CC	C	16 KB block pre-program and erase time	300	500	5000	ms
$T_{32kpperase}$	CC	C	32 KB block pre-program and erase time	400	600	5000	ms
$T_{128kpperase}$	CC	C	128 KB block pre-program and erase time	800	1300	7500	ms
T_{eslat}	CC	D	Erase suspend latency	—	30	30	µs

NOTES:
1 Typical program and erase times assume nominal supply values and operation at 25 °C.
2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4 Actual hardware programming times. This does not include software overhead.

Table 46. Flash module life

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Typ	
P/E	CC	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	cycles
P/E	CC	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	years
				Blocks with 10,000 P/E cycles	10	—	years
				Blocks with 100,000 P/E cycles	5	—	years

NOTES:
1 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 47. Flash memory read access timing

Symbol		C	Parameter	Condition[1]	Max value	Unit
f_{READ}	CC	P	Maximum frequency for flash memory reading	2 wait states	64	MHz
		C		1 wait state	40	
		C		0 wait states	20	

NOTES:
1 V_{DD} = 3.3 V ±10% / 5.0 V ±10%, T_A = –40 to 105 °C, unless otherwise specified

3.17 ADC electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) Analog to Digital Converter.

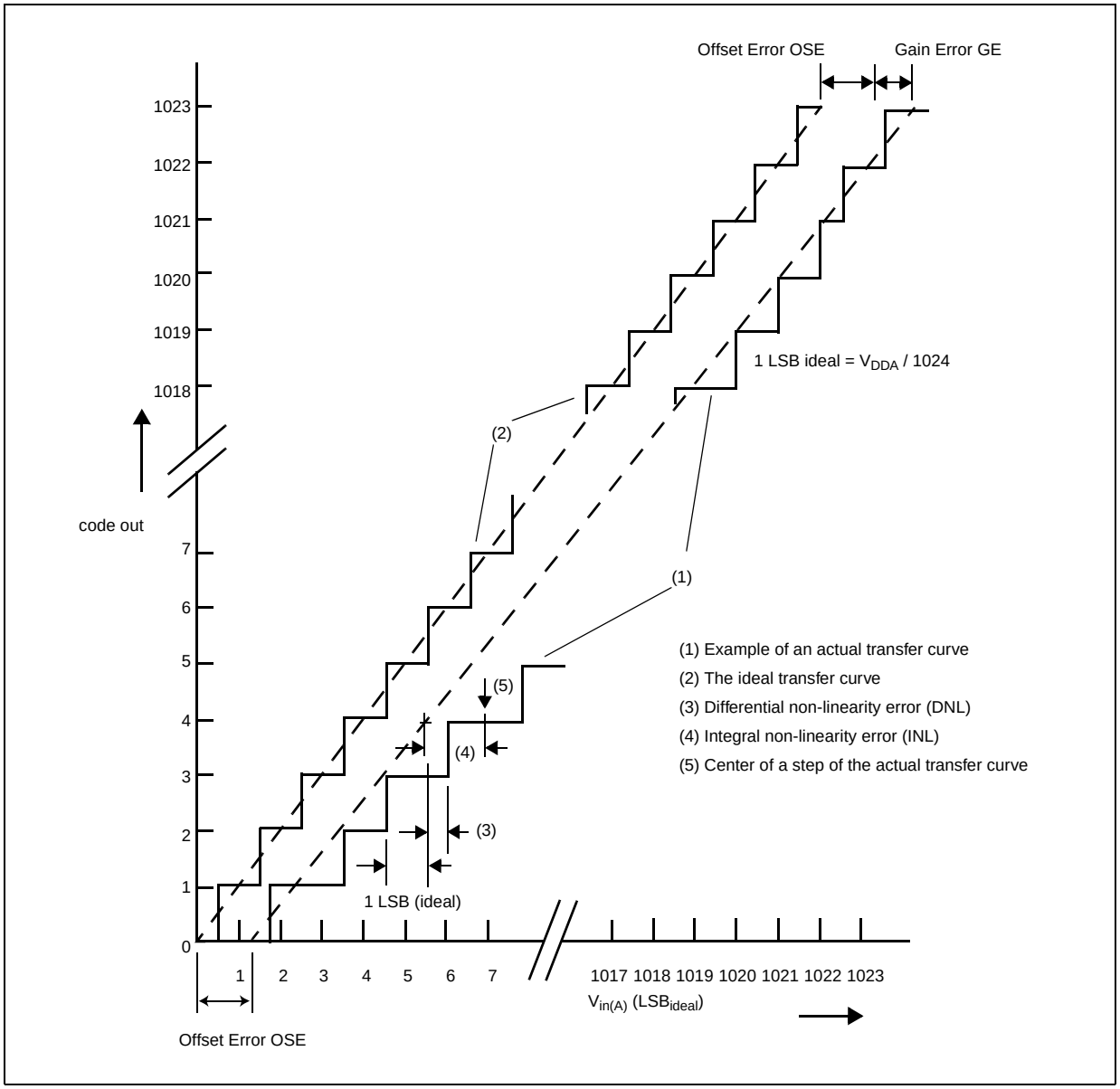


Figure 17. ADC Characteristics and Error Definitions

3.17.1 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer

or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_c \times C_S)$, where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 7:

Eqn. 7

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 7 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

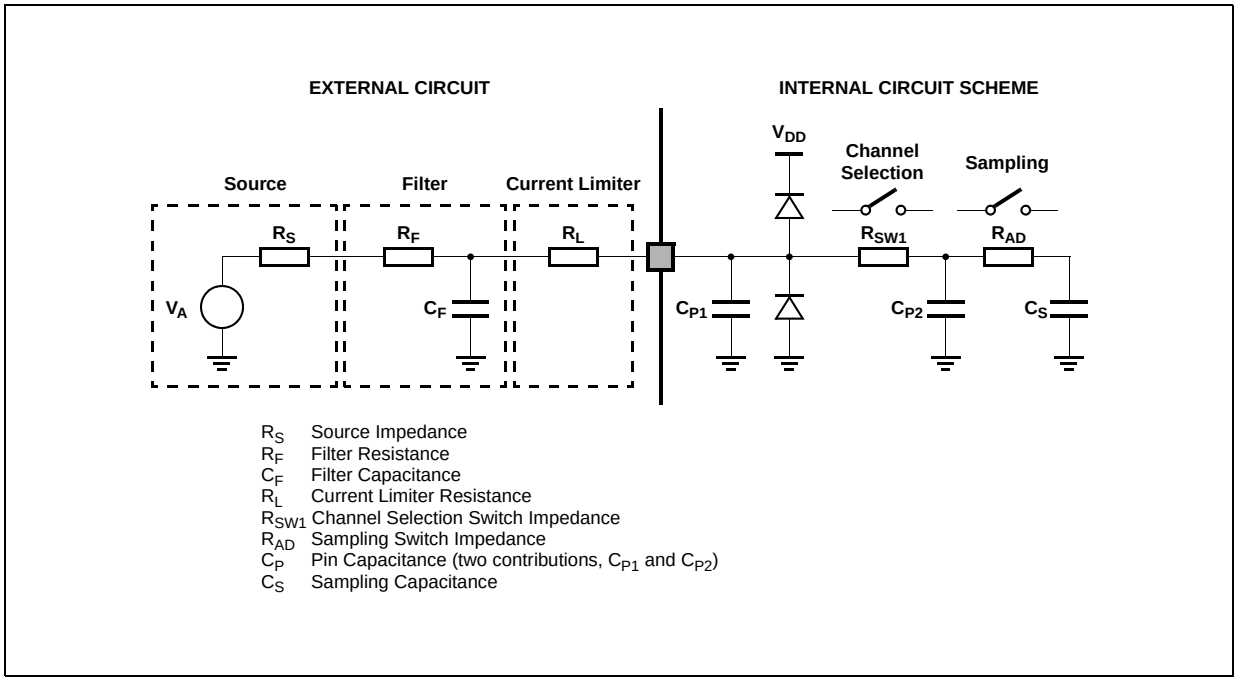


Figure 18. Input equivalent circuit (precise channels)

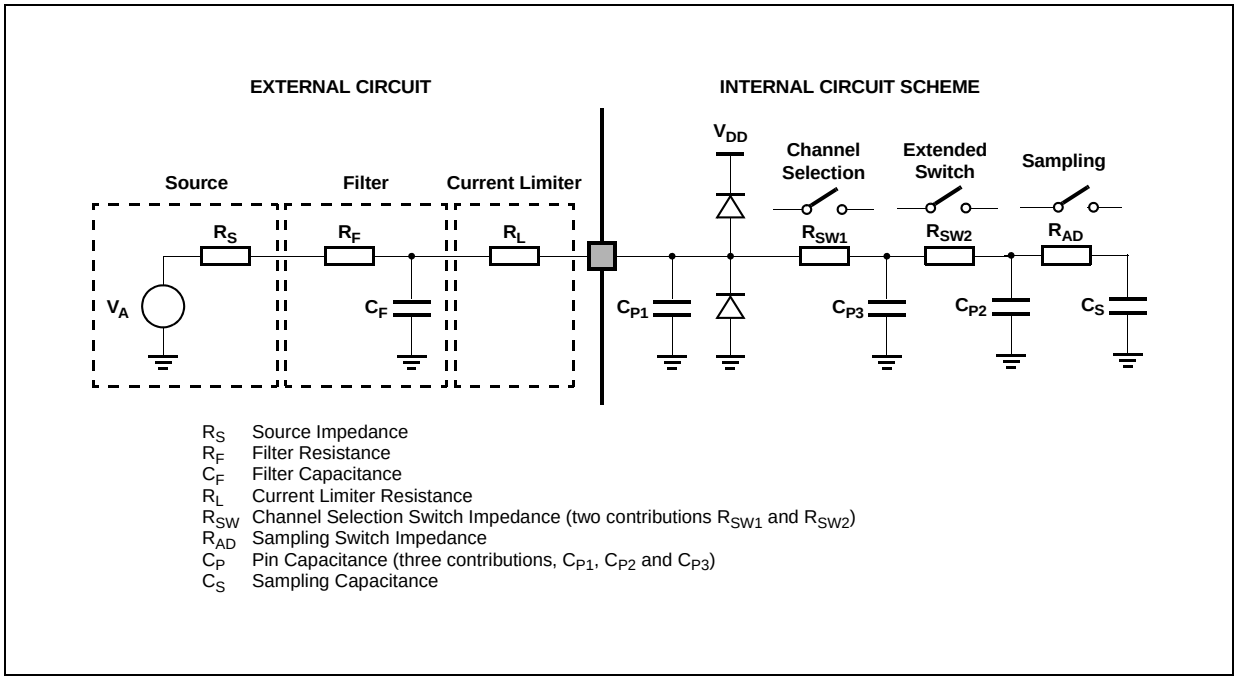


Figure 19. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 18): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

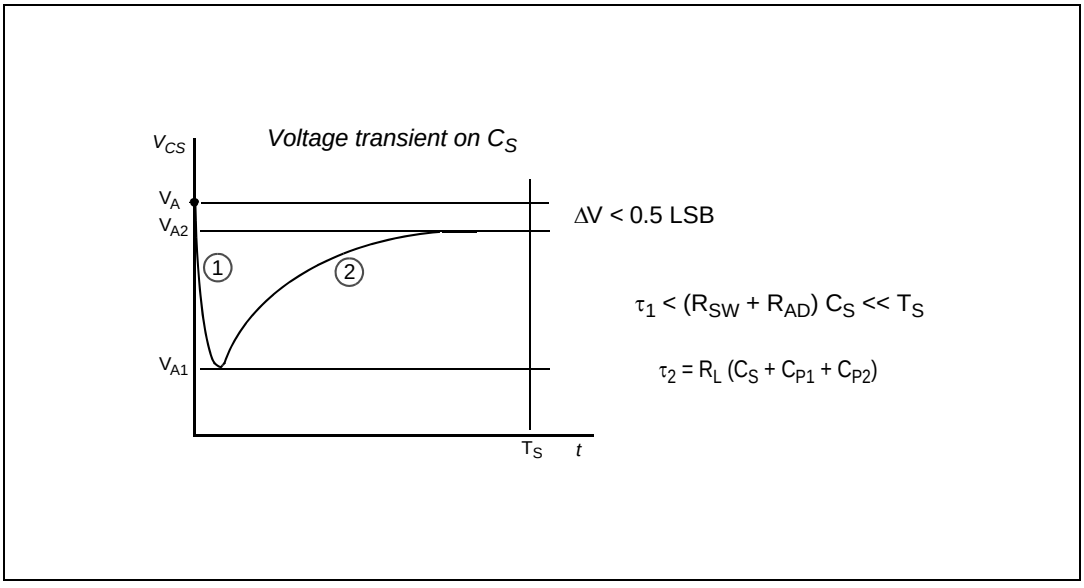


Figure 20. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case

(since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 8

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 8 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 9

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 10:

Eqn. 10

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 11

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Eqn. 12

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 13 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 13

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal

source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

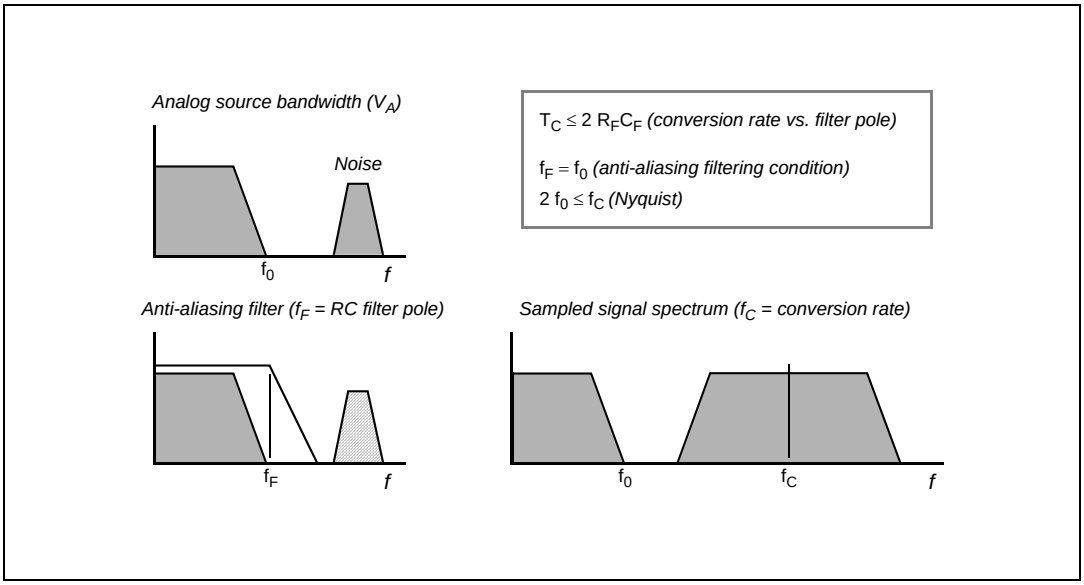


Figure 21. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 14 between the ideal and real sampled voltage on C_S:

Eqn. 14

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 15

$$C_F > 2048 \bullet C_S$$

3.17.2 ADC conversion characteristics

NOTE

For input leakage current specification, see Table 28.

Table 48. ADC conversion characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SSA}	SR	D	Voltage on VSSA (ADC reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DDA}	SR	D	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V
V_{AINx}	SR	D	Analog input voltage[3]	—	V_{SSA} – 0.1	—	V_{DDA} + 0.1	V
f_{ADC}	SR	D	ADC analog frequency	—	6	—	32	MHz
t_{ADC_PU}	SR	D	ADC power up delay	—	—	—	1.5	µs
t_{ADC_S}	CC	T	Sample time[4,5]	f_{ADC} = 32 MHz, ADC_conf_sample_input = 17	0.5	—	—	µs
		T		f_{ADC} = 6 MHz, ADC_conf_sample_input = 127	—	—	21	
t_{ADC_C}	CC	T	Conversion time[6]	f_{ADC} = 32 MHz, ADC_conf_comp = 2	0.625	—	—	µs
C_S	CC	D	ADC input sampling capacitance	—	—	—	3	pF
C_{P1}	CC	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC input pin capacitance 3	—	—	—	1	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—	—	—	0.1	kΩ
I_{INJ}	SR	T	Input current Injection	Current injection on one ADC input, different from the converted one	–5	—	5	mA
INL	CC	P	Integral Non Linearity	No overload	2.5	—	2.5	LSB
DNL	CC	P	Differential Non Linearity	No overload	–1.0	—	1.0	LSB

Table 48. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
OFS	CC	T	Offset error	After offset cancellation	—	0.5	—	LSB
GNE	CC	T	Gain error		—	0.6	—	LSB
TUEx	CC	P	Total unadjusted error for extended channel	Without current injection	–3	—	3	LSB
		T		With current injection	–4	—	4	

NOTES:
1 V_{DDA} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 105 °C, unless otherwise specified.

2 Analog and digital V_{SS} **must** be common (to be tied together externally).

3 V_{AINx} may exceed V_{SSA} and V_{DDA} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF

4 During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.

5 The maximum sample rate is 1 million samples per second, provided the source impedance and current limiter(>1 kΩ) are calculated adequately.

- Filter capacitor at analog source output must meet the criteria Cf (filter capacitor) > 2048*Cs (sampling capacitor which is 3 pF)

6 This parameter does not include the sample time t_{ADC_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

3.18 LCD driver electrical characteristics

Table 49. LCD driver specifications

Symbol		C	Parameter	Value[1]			Unit
				Min	Typ	Max	
VLCD	SR	C	Voltage on VLCD (LCD supply) pin with respect to VSS	0	—	VDDE + 0.3	V
$Z_{BP/FP}$	CC	T	LCD output impedance (BP[n-1:0],FP[m-1:0]) for output levels VLCD, VSS[2]	—	—	5.0	kΩ
$I_{BP/FP}$	CC	T	LCD output current (BP[n-1:0],FP[m-1:0]) for outputs charge/discharge voltage levels VLCD2/3, VLCD1/2, VLCD1/3)[2,3]	—	25	—	μA

NOTES:
1 V_{DD} = 5.0 V ± 10%, T_A = –40–105 °C, unless otherwise specified

2 Outputs measured one at a time, low impedance voltage source connected to the VLCD pin.

3 With PWR=10, BSTEN=0, and BSTAO=0

3.19 Pad AC specifications

Table 50. Pad AC specifications (5.0 V, PAD3V5V = 0)[1]

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	1.5	—	30	6	—	50	—	—	4	0.04	—	2	25
		1.5	—	30	9	—	100	—	—	2	0.04	—	2	50
		1.5	—	30	12	—	125	—	—	2	0.04	—	2	100
		1.5	—	30	16	—	150	—	—	2	0.04	—	2	200
2	Medium	1	—	15	3	—	10	—	—	40	2.5	—	7	25
		1	—	15	5	—	20	—	—	20	2.5	—	7	50
		1	—	15	9	—	40	—	—	13	2.5	—	8	100
		1	—	15	12	—	70	—	—	7	2.5	—	8	200
3	Fast	1	—	6	1	—	4	—	—	100	18	—	55	25
		1	—	6	1.5	—	6	—	—	80	18	—	55	50
		1	—	6	3	—	12	—	—	40	18	—	55	100
		1	—	6	5	—	16	—	—	25	18	—	55	200
4	Pull Up/Down (5.5 V max)	—	—	—	—	—	5000	—	—	—	—	—	—	50
Parameter Classification		D			C			C			C			n/a

NOTES:
1 Propagation delay from V_{DD}/2 of internal signal to Pchannel/Nchannel on condition
2 Slope at rising/falling edge

Table 51. Pad AC specifications (3.3 V, PAD3V5V = 1)[1]

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	3	—	40	4	—	40	—	—	4	0.01	—	2	25
		3	—	40	6	—	50	—	—	2	0.01	—	2	50
		3	—	40	10	—	75	—	—	2	0.01	—	2	100
		3	—	40	14	—	100	—	—	2	0.01	—	2	200
2	Medium	1	—	15	2	—	12	—	—	40	2.5	—	7	25
		1	—	15	4	—	25	—	—	20	2.5	—	7	50
		1	—	15	8	—	40	—	—	13	2.5	—	7	100
		1	—	15	14	—	70	—	—	7	2.5	—	7	200

Table 51. Pad AC specifications (3.3 V, PAD3V5V = 1)[1] (continued)

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
3	Fast	1	—	6	1	—	4	—	—	72	3	—	40	25
		1	—	6	1.5	—	7	—	—	55	3	—	40	50
		1	—	6	3	—	12	—	—	40	3	—	40	100
		1	—	6	5	—	18	—	—	25	3	—	40	200
4	Pull Up/Down (3.6 V max)	—	—	—	—	—	7500	—	—	—	—	—	—	50
Parameter Classification		D			C			C			C			n/a

NOTES:
1 Propagation delay from $V_{DD}/2$ of internal signal to Pchannel/Nchannel on condition
2 Slope at rising/falling edge

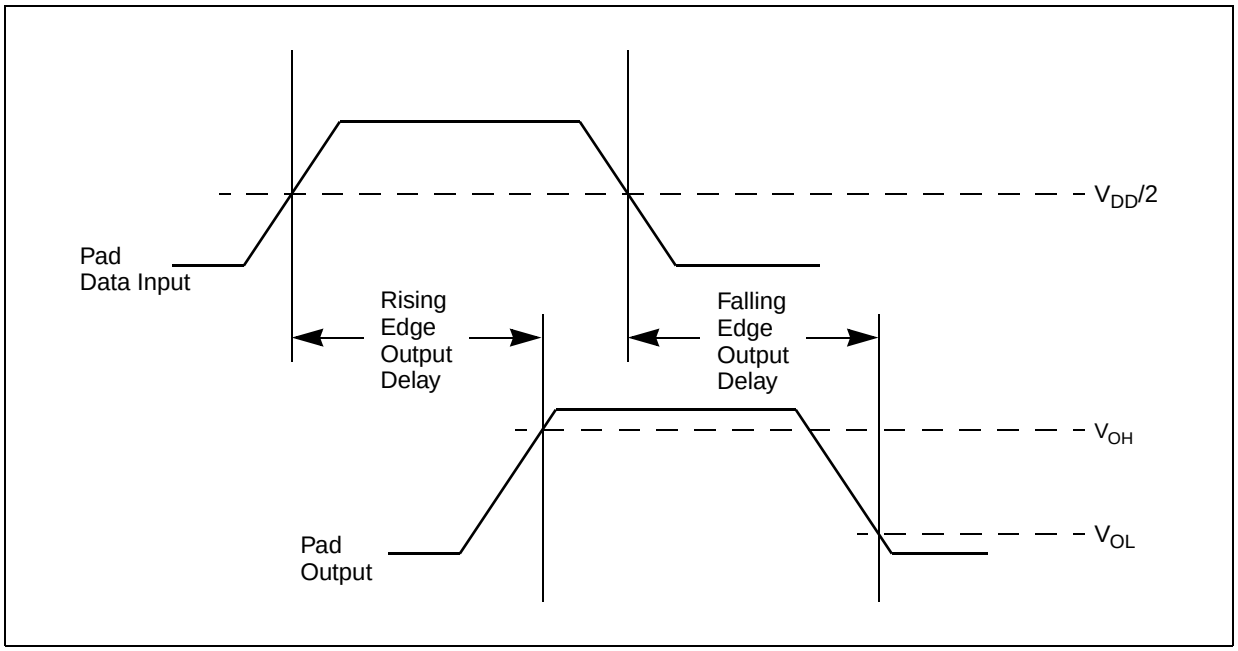


Figure 22. Pad output delay

Table 52. SMD pad delays

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	D	SMD pad delay	CL=50pf V_{DD}=5V±10% SRE=1	—	—	165	ns
				CL=50pf V_{DD}=5V±10% SRE=0	—	—	35	
—	CC	D	SMD pad delay	CL=50pf V_{DD}=3.3V±10% SRE=1	—	—	350	
				CL=50pf V_{DD}=3.3V±10% SRE=0	—	—	50	

3.20 AC timing

3.20.1 IEEE 1149.1 interface timing

Table 53. JTAG interface timing[1]

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{JCYC}	CC	D	TCK Cycle Time	100	—	ns
2	t_{JDC}	CC	D	TCK Clock Pulse Width (measured at V_{DD}/2)	40	60	
3	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times (40%–70%)	—	3	
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI Data Setup Time	5	—	
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI Data Hold Time	10	—	
6	t_{TDOV}	CC	D	TCK Low to TDO Data Valid	—	40	
7	t_{TDOI}	CC	D	TCK Low to TDO Data Invalid	0	—	
8	t_{TDOHZ}	CC	D	TCK Low to TDO High Impedance	—	30	

NOTES:
1 These specifications apply to JTAG boundary scan only. JTAG timing specified at V_{DD} = 3.0 V to 5.5 V, T_A = –40 to 105 °C, and C_L = 50 pF with SRC = 0b11.

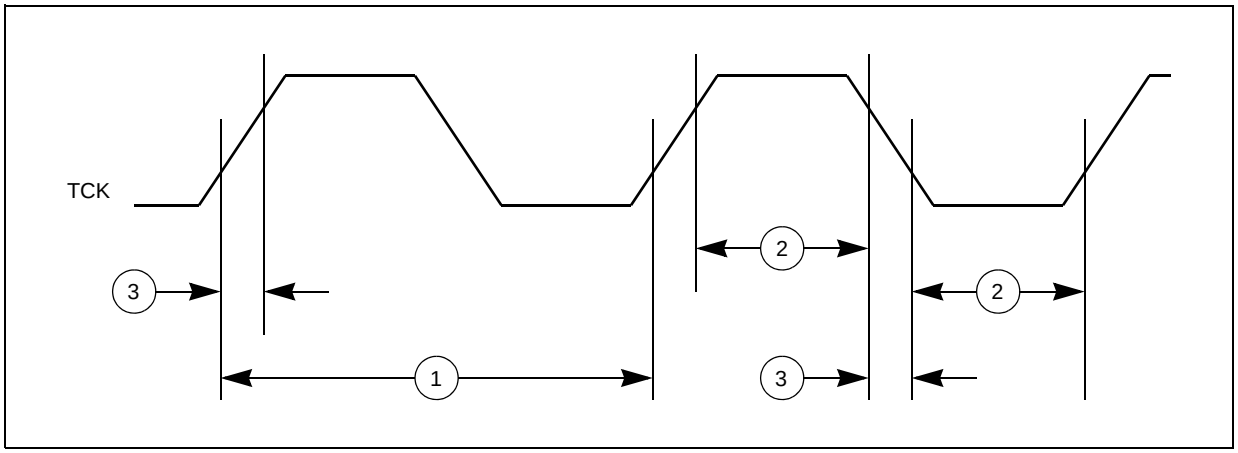


Figure 23. JTAG test clock input timing

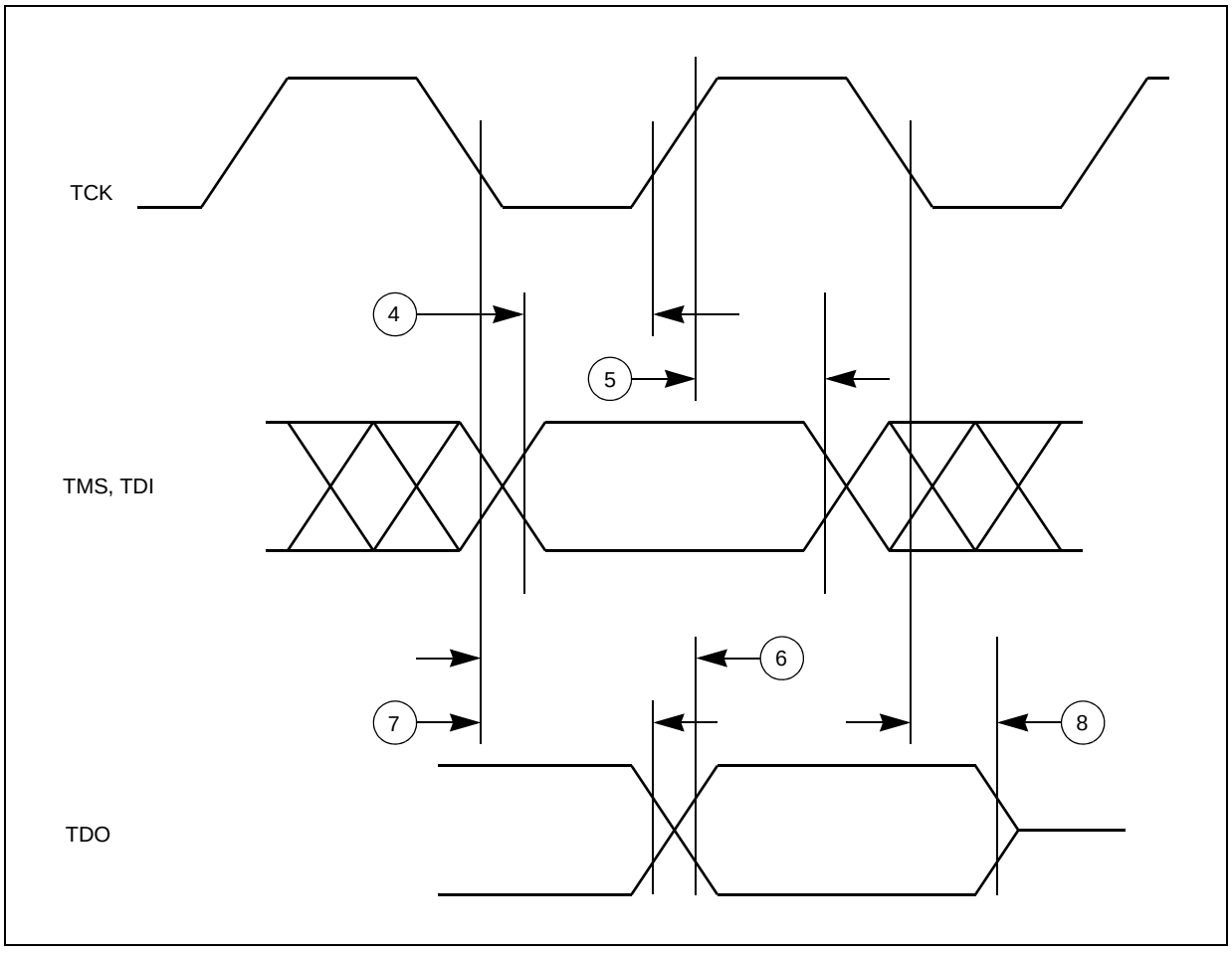


Figure 24. JTAG test access port timing

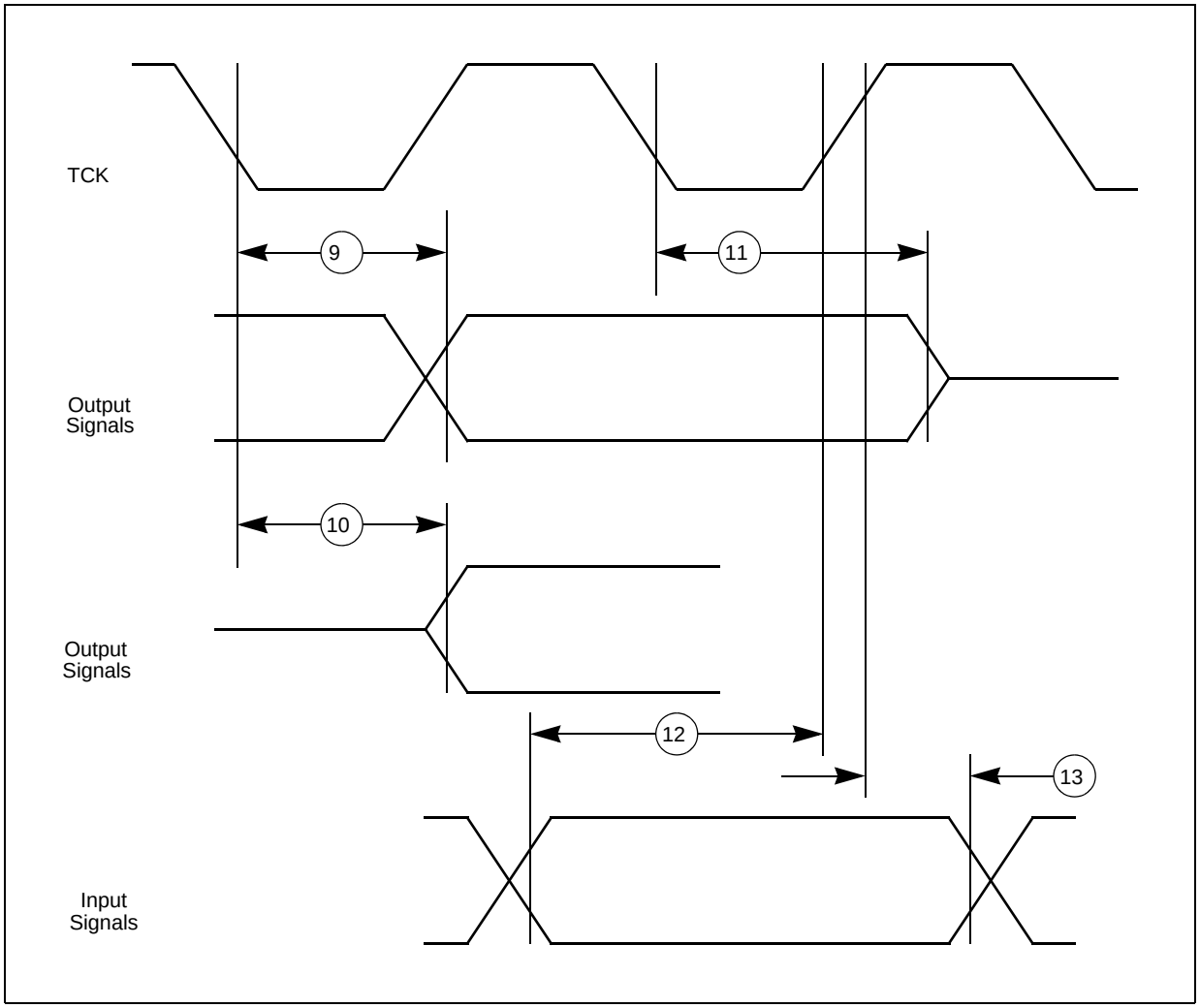


Figure 25. JTAG boundary scan timing

3.20.2 Nexus debug interface

Table 54. Nexus debug port timing[1]

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{MCYC}	CC	D	MCKO Cycle Time	22	—	ns
2	Δ_{MDC}	CC	D	MCKO Duty Cycle	40	60	%
3	t_{MDOV}	CC	D	MCKO Low to MDO Data Valid[2]	–2	14	ns
4	t_{MSEOV}	CC	D	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[2]	–2	14	ns
5	t_{EVTOV}	CC	D	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[2]	–2	14	ns
6	t_{EVTIPW}	CC	D	$\overline{\text{EVTI}}$ Pulse Width	4	—	t_{TCYC}

Table 54. Nexus debug port timing[1] (continued)

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
7	t_{EVTOPW}	CC	D	$\overline{EVTO}$ Pulse Width	1	—	t_{MCYC}
8	t_{TCYC}	CC	D	TCK Cycle Time[3]	100	—	ns
9	Δ_{TDC}	CC	D	TCK Duty Cycle	40	60	%
10	t_{NTDIS}, t_{NTMSS}	CC	D	TDI, TMS Data Setup Time	10	—	ns
11	t_{NTDIH}, t_{NTMSH}	CC	D	TDI, TMS Data Hold Time	5	—	ns
12	t_{JOV}	CC	D	TCK Low to TDO Data Valid	0	40	ns

NOTES:
1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 3.0 V to 5.5V, T_A = –40 to 105 °C, and C_L = 50 pF (C_L = 30 pF on MCKO), with SRC = 0b11.
2 MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.
3 The system clock frequency needs to be three times faster than the TCK frequency.

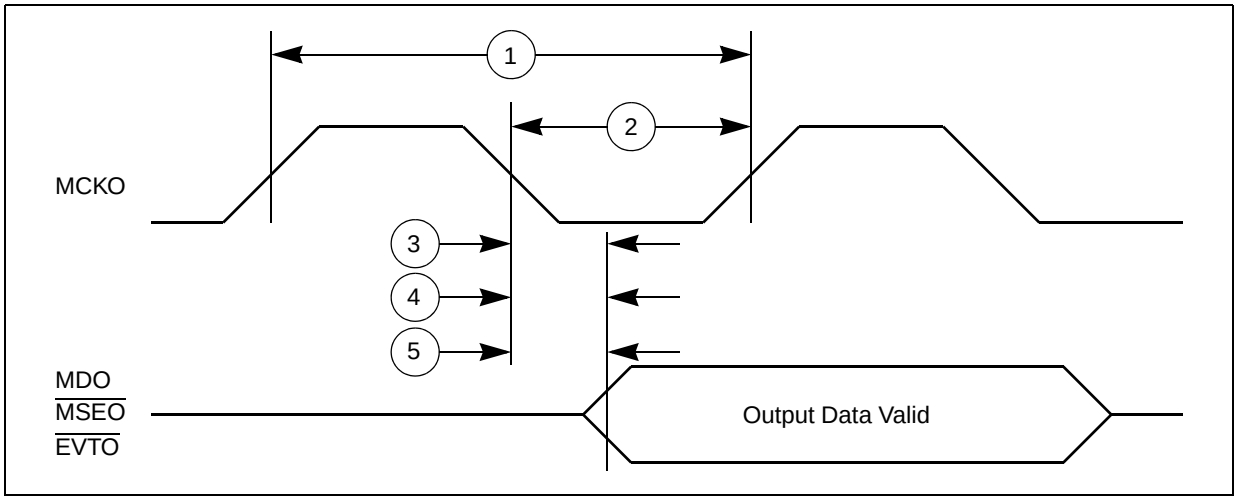


Figure 26. Nexus output timing

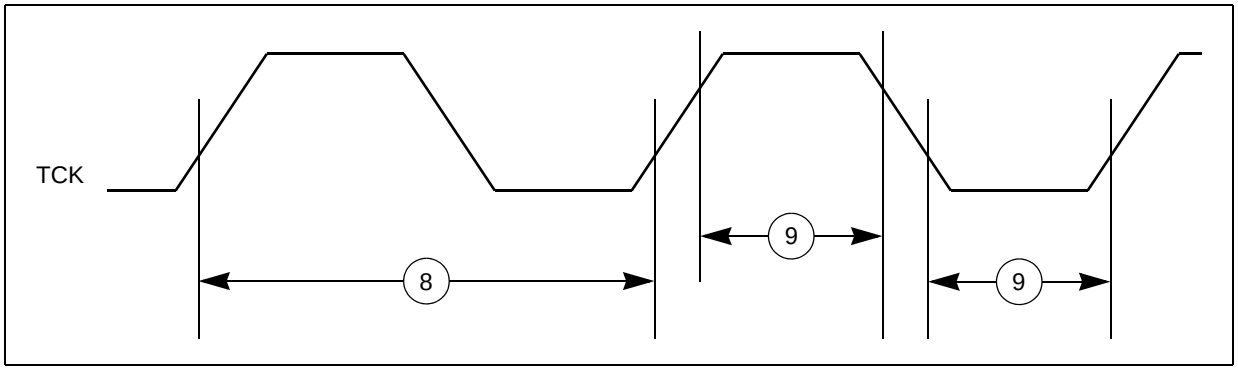


Figure 27. Nexus TCK timing

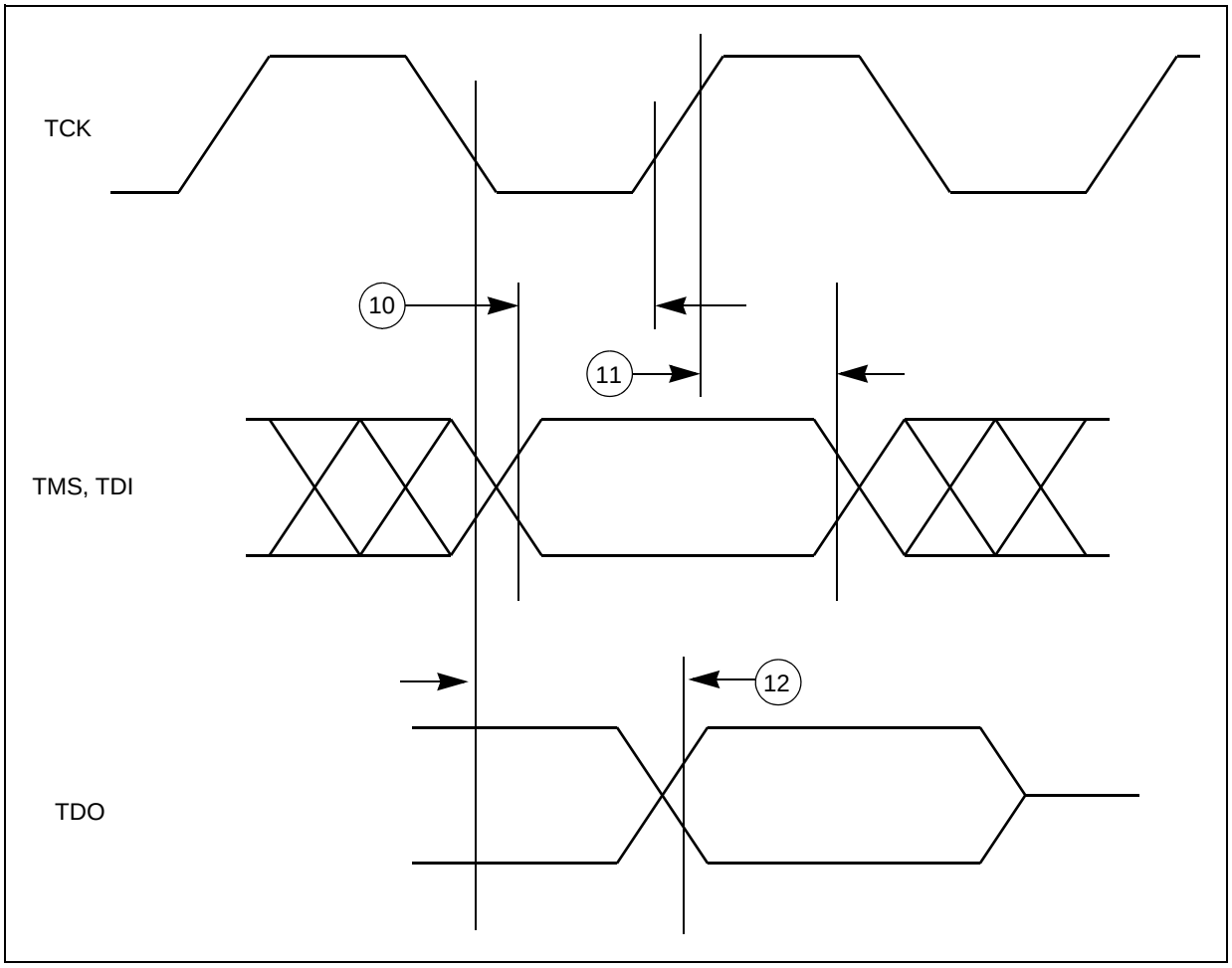


Figure 28. Nexus TDI, TMS, TDO timing

3.20.3 Interface to TFT LCD panels

Figure 29 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with positive polarity. The sequence of events for active matrix interface timing is:

1. DCU_CLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, DCU_CLK runs continuously.
2. DCU_HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
3. DCU_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
4. DCU_DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

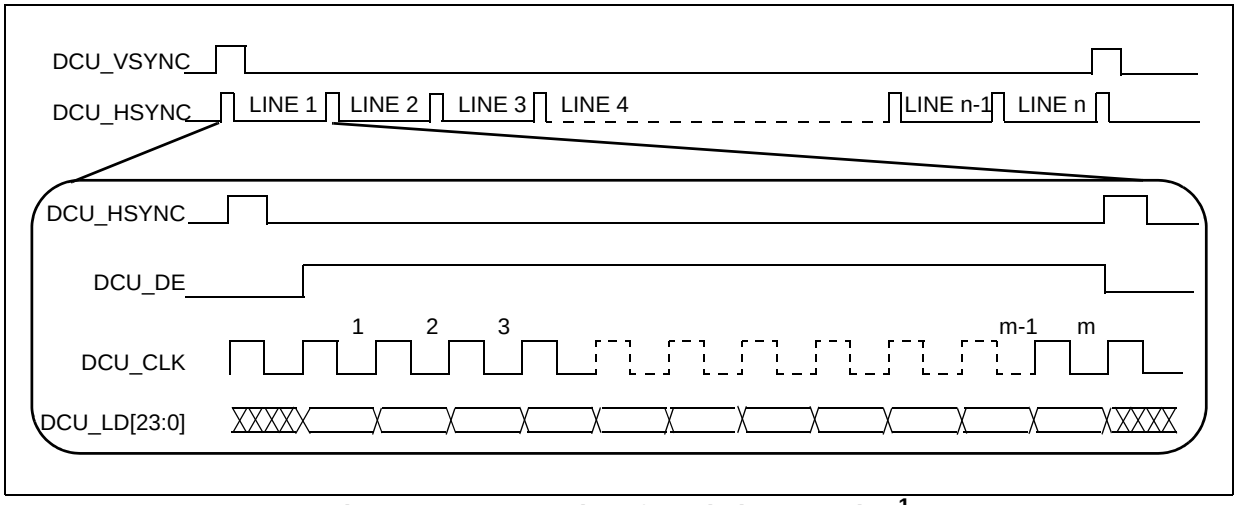


Figure 29. TFT LCD interface timing overview[1]

3.20.3.1 Interface to TFT LCD panels—pixel level timings

Figure 30 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the DCU_CLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the DCU_HSYNC, DCU_VSYNC and DCU_DE signals. The user can select the polarity of the DCU_HSYNC and DCU_VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DCU_DE signal is always active-high.

Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the DCU Clock Confide Register (DCCR) in the system clock module.

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

Table 55. LCD interface timing parameters—horizontal and vertical

Symbol		C	Parameter	Value	Unit
t_{PCP}	CC	D	Display pixel clock period	—	ns
t_{PWH}	CC	D	HSYNC pulse width	PW_H × t_{PCP}	ns
t_{BPH}	CC	D	HSYNC back porch width	BP_H × t_{PCP}	ns
t_{FPH}	CC	D	HSYNC front porch width	FP_H × t_{PCP}	ns
t_{SW}	CC	D	Screen width	DELTA_X × t_{PCP}	ns
t_{HSP}	CC	D	HSYNC (line) period	(PW_H + BP_H + FP_H + DELTA_X) × t_{PCP}	ns
t_{PWV}	CC	D	VSYNC pulse width	PWV × t_{HSP}	ns

1. In Figure 29, the “DCU_LD[23:0]” signal is an aggregation of the DCU’s RGB signals—DCU_R[0:7], DCU_G[0:7] and DCU_B[0:7].

Table 55. LCD interface timing parameters—horizontal and vertical (continued)

Symbol		C	Parameter	Value	Unit
t_{BPV}	CC	D	VSYNC back porch width	BP_V × t_{HSP}	ns
t_{FPV}	CC	D	VSYNC front porch width	FP_V × t_{HSP}	ns
t_{SH}	CC	D	Screen height	DELTA_Y × t_{HSP}	ns
t_{VSP}	CC	D	VSYNC (frame) period	(PW_V + BP_V + FP_V + DELTA_Y) × t_{HSP}	ns

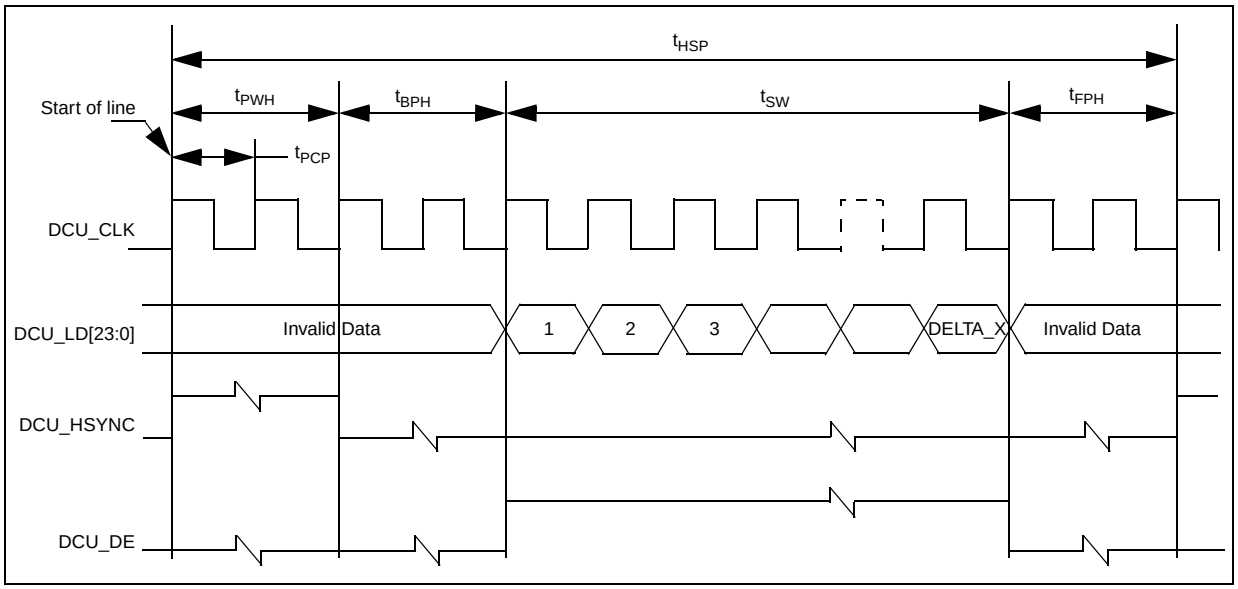


Figure 30. Horizontal sync timing

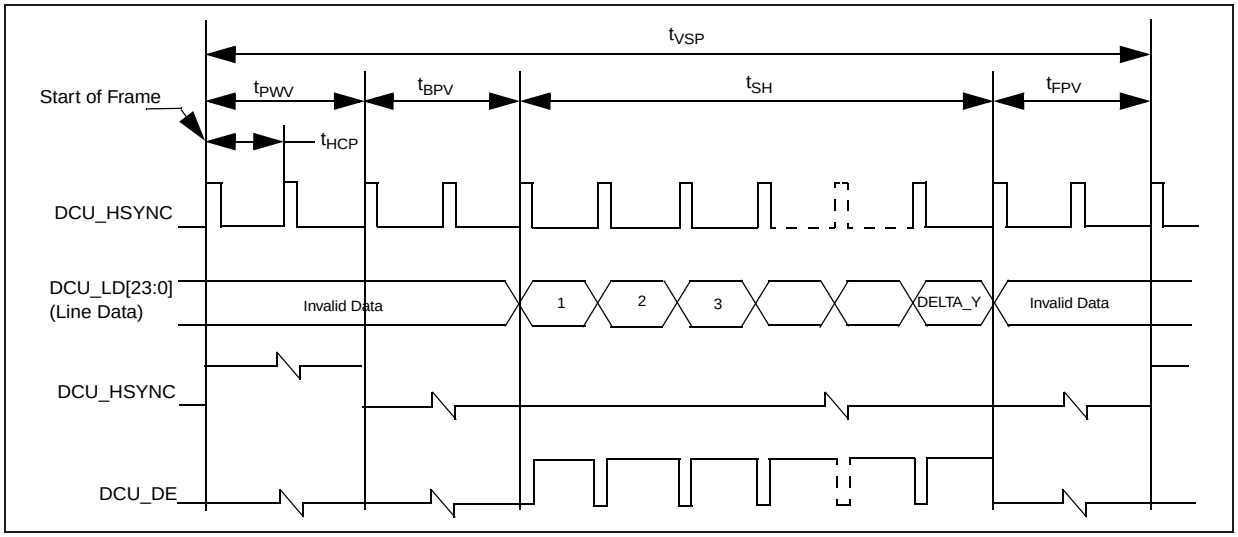


Figure 31. Vertical sync pulse

3.20.3.2 Interface to TFT LCD panels

Table 56. TFT LCD interface timing parameters[1,2,3,4]

Symbol		C	Parameter	Value			Unit
				Min	Typ	Max	
t_{CKP}	CC	D	PDI clock period	15.25	—	—	ns
Δ_{CK}	CC	D	PDI clock duty cycle	40	—	60	%
t_{DSU}	CC	D	PDI data setup time	9.5	—	—	ns
t_{DHD}	CC	D	PDI data access hold time	4.5	—	—	ns
t_{CSU}	CC	D	PDI control signal setup time	9.5	—	—	ns
t_{CHD}	CC	D	PDI control signal hold time	4.5	—	—	ns
	CC	D	TFT interface data valid after pixel clock	—	—	6	ns
	CC	D	TFT interface VSYNC valid after pixel clock	—	—	5.5	ns
	CC	D	TFT interface DE valid after pixel clock	—	—	5.6	ns
	CC	D	TFT interface hold time for data and control bits	2	—	—	ns
	CC	D	Relative skew between the data bits	—	—	3.7	ns

NOTES:
1 The characteristics in this table are based on the assumption that data is output at positive edge and displays latch data on negative edge
2 Intra bit skew is less than 2 ns
3 Load C_L = 50 pF for panel frequency up to 20 MHz
4 Load C_L = 25 pF for panel frequency from 20 to 32 MHz

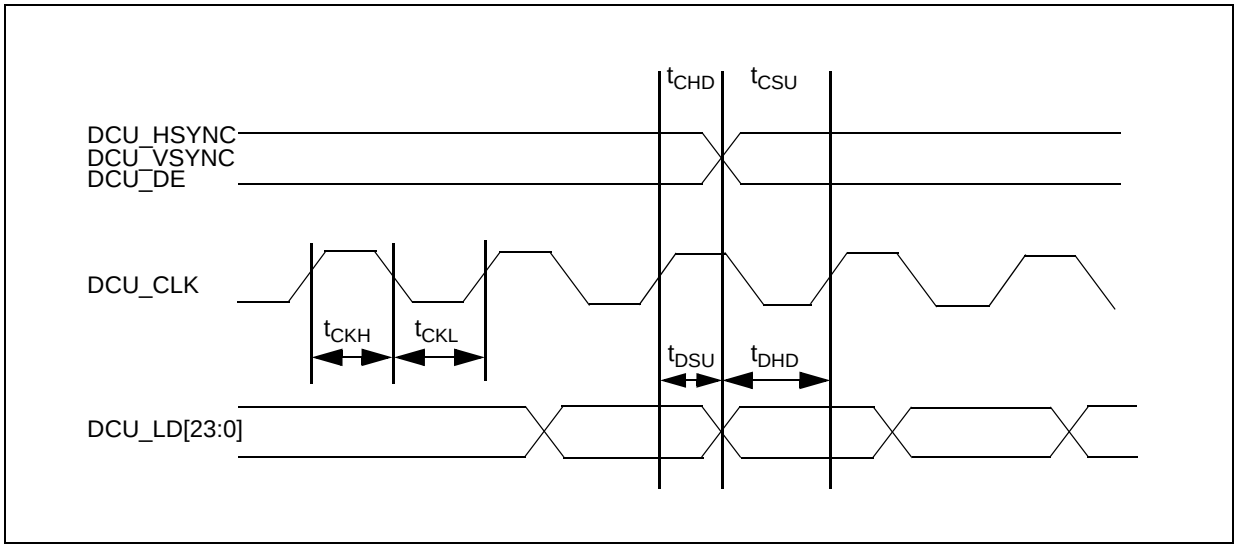


Figure 32. TFT LCD interface timing parameters

3.20.4 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) timing

Table 57. IRQ and NMI timing

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{IPWL}	CC	T	IRQ/NMI Pulse Width Low	200	—	ns
2	t_{IPWH}	CC	T	IRQ/NMI Pulse Width High	200	—	ns
3	t_{ICYC}	CC	T	IRQ/NMI Edge to Edge Time[1]	400	—	ns

NOTES:
1 Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

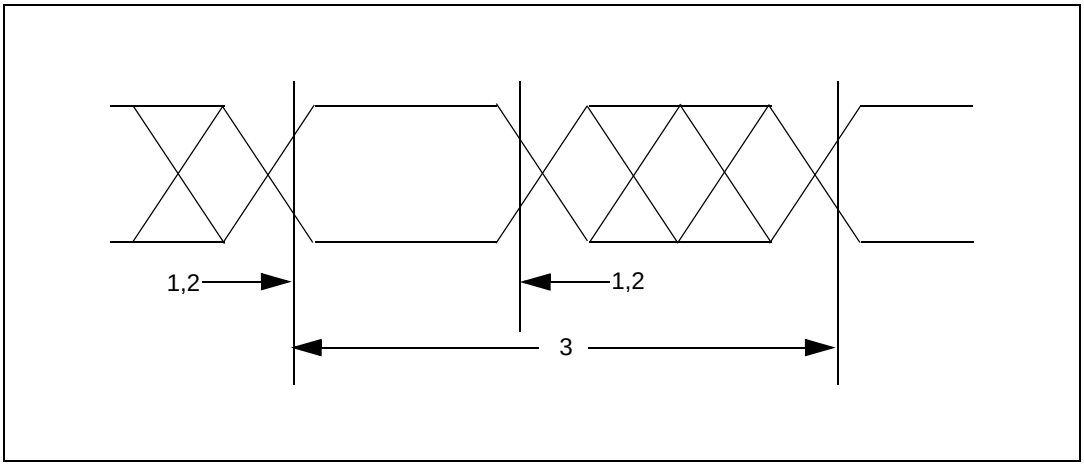


Figure 33. IRQ and NMI timing

3.20.5 eMIOS timing

Table 58. eMIOS timing[1]

No.	Symbol		C	Parameter	Value		Unit
					Min[2]	Max	
1	t_{MIPW}	CC	D	eMIOS input pulse width	4	—	t_{CYC}
2	t_{MOPW}	CC	D	eMIOS output pulse width	1	—	t_{CYC}

NOTES:
1 eMIOS timing specified at f_{SYS} = 64 MHz, V_{DD12} = 1.14 V to 1.32 V, VDDE_x = 3.0 V to 5.5 V, T_A = –40 to 105 °C, and C_L = 50 pF with SRC = 0b00

2 There is no limitation on the peripheral for setting the minimum pulse width, the actual width is restricted by the pad delays. Refer to the pad specification section for the details.

3.20.6 FlexCAN timing

The CAN functions are available as TX pins at normal IO pads and as RX pins at the always on domain. There is no filter for the wakeup dominant pulse. Any high-to-low edge can cause wakeup if configured.

Table 59. FlexCAN timing[1]

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{CANOV}	CC	D	CTNX Output Valid after CLKOUT Rising Edge (Output Delay)	—	22.48	ns
2	t_{CANSU}	CC	D	CNRX Input Valid to CLKOUT Rising Edge (Setup Time)	—	12.46	ns

NOTES:
1 FlexCAN timing specified at f_{SYS} = 64 MHz, V_{DD12} = 1.14 V to 1.32 V, VDDE_x = 3.0 V to 5.5 V, T_A = –40 to 105 °C, and C_L = 50 pF with SRC = 0b00.

3.20.7 Deserial Serial Peripheral Interface (DSPI)

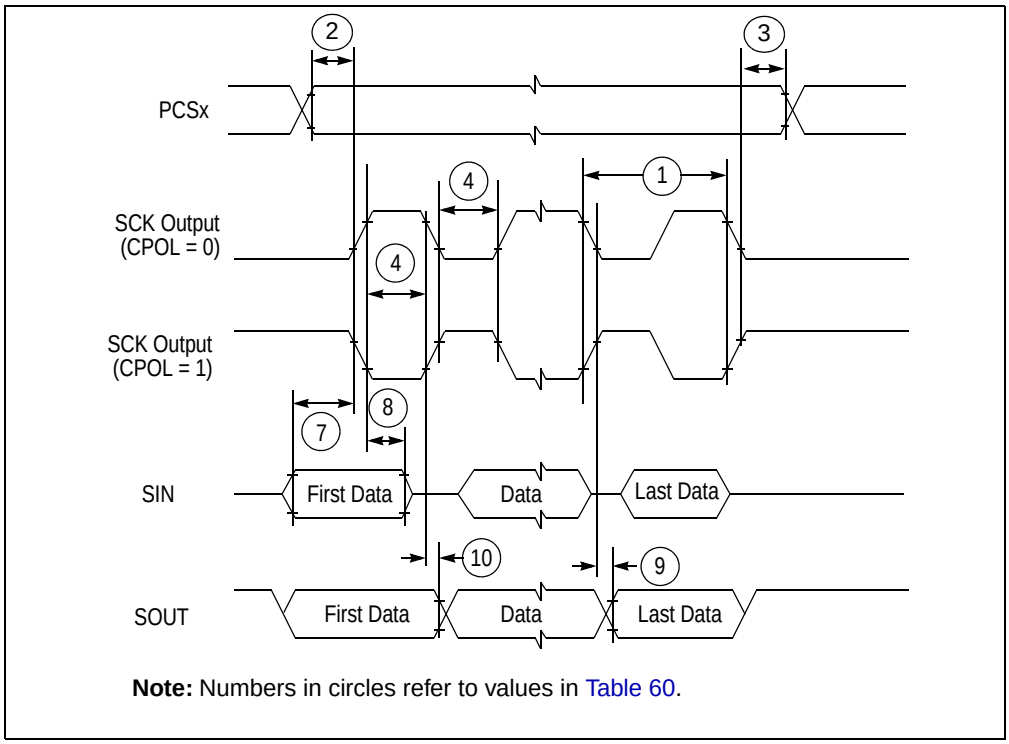
Table 60. DSPI timing[1]

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{SCK}	CC	D	DSPI Cycle TIme[2,3]	Master (MTFE = 0) Slave (MTFE = 0) Slave Receive Only Mode	62 62 62	— — —	ns ns ns
2	t_{CSC}	CC	D	PCS to SCK Delay[4]	—	20	—	ns
3	t_{ASC}	CC	D	After SCK Delay[5]	—	20	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle	—	0.4 x t_{SCK}	0.6 x t_{SCK}	ns
5	t_A	CC	D	Slave Access Time (PCSx active to SOUT driven)	SS active to SOUT valid	—	40	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time (PCSx inactive to SOUT High-Z or invalid)	SS inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}			PCSx to PCSS time	—	20	—	ns
8	t_{PASC}			PCSS to PCSx time	—	20	—	ns
9	t_{SUI}	CC	D	Data Setup Time for Inputs	Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	35 2 20 35	— — — —	ns ns ns ns
10	t_{HI}	CC	D	Data Hold Time for Inputs	Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	–5 5 10 –5	— — — —	ns ns ns ns

Table 60. DSPI timing[1] (continued)

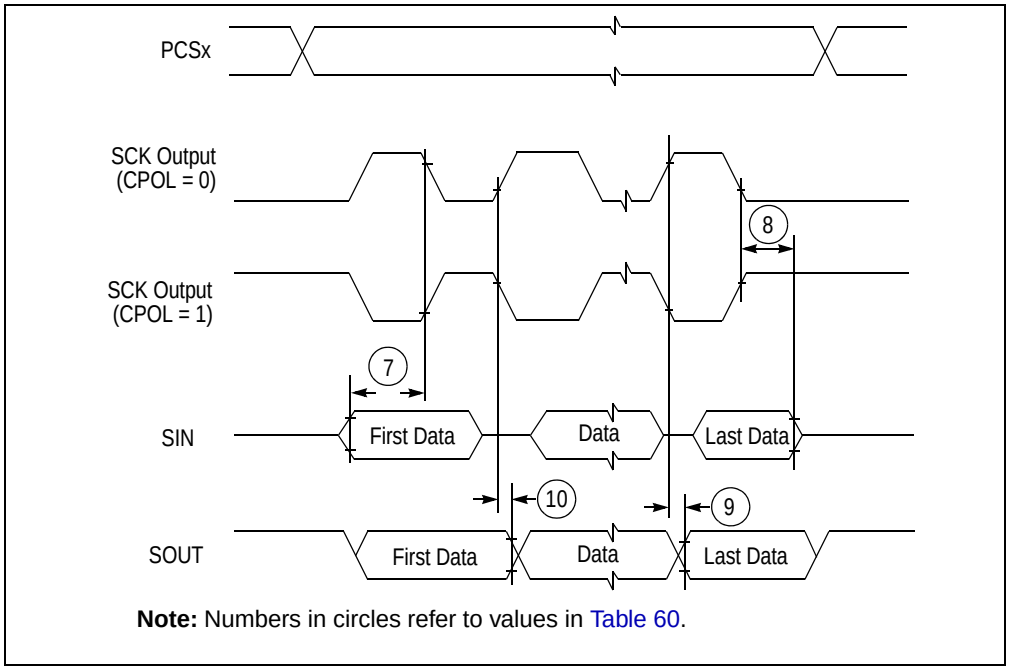
No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
11	t_{SUO}	CC	D	Data Valid (after SCK edge)	Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	— — — —	14 39 24 15	ns ns ns ns
12	t_{HO}	CC	D	Data Hold Time for Outputs	Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	–3 6 12 –3	— — — —	ns ns ns ns

NOTES:
1. DSPI timing specified at VDDE_x = 3.0 V to 5.5 V, T_A = –40 to 105 °C, and C_L = 50 pF with SRC = 0b11.
2. The minimum SCK Cycle Time restricts the baud rate selection for given system clock rate.
3. The actual minimum SCK Cycle Time is limited by pad performance.
4. The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK], program PSSCK = 2 and CSSCK = 2
5. The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC]
6. This delay value is corresponding to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR register.



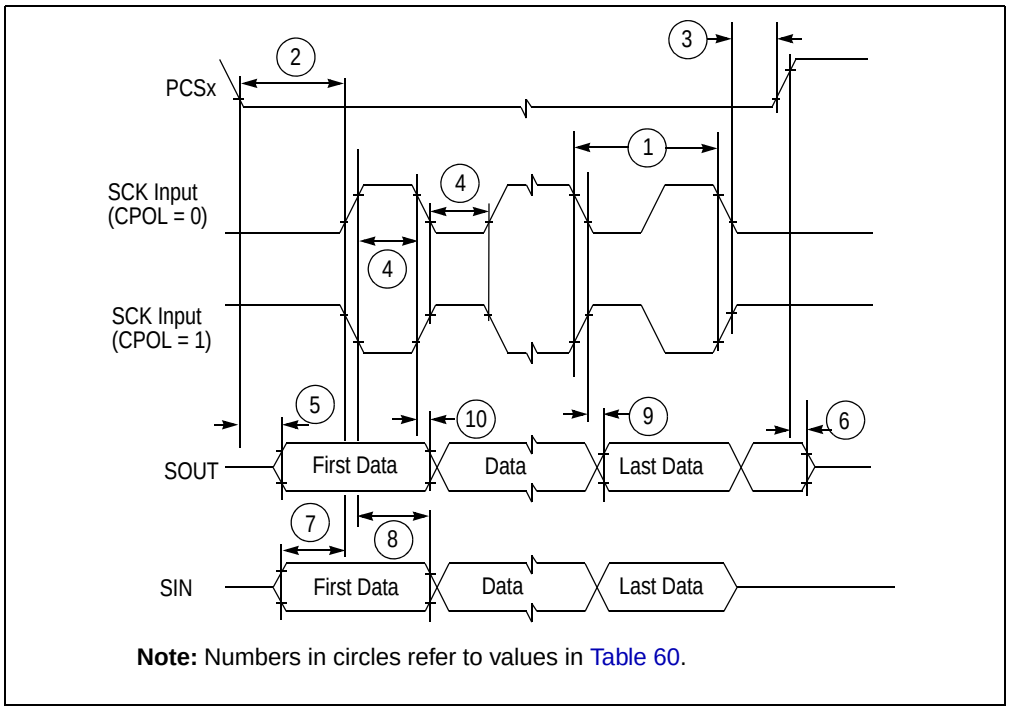
Note: Numbers in circles refer to values in Table 60.

Figure 34. DSPI classic SPI timing — master, CPHA = 0



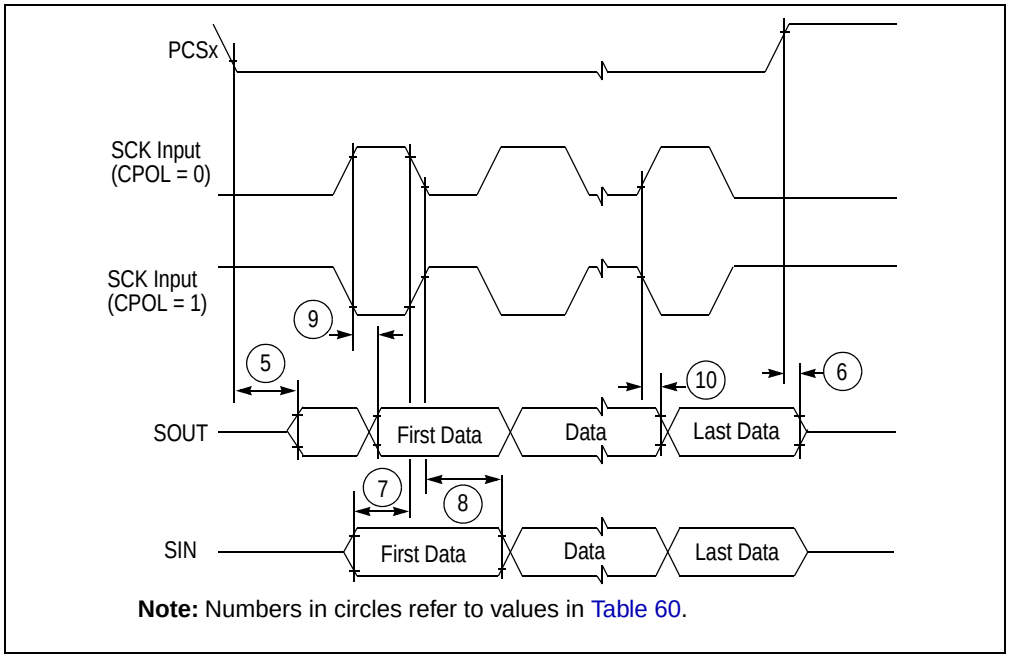
Note: Numbers in circles refer to values in Table 60.

Figure 35. DSPI classic SPI timing — master, CPHA = 1



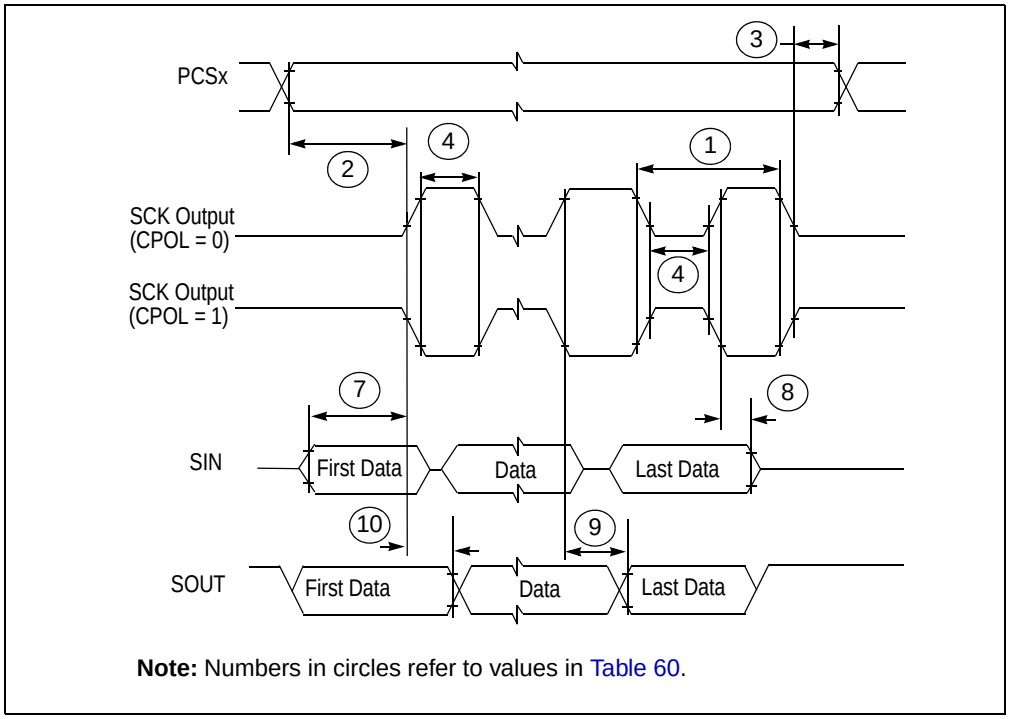
Note: Numbers in circles refer to values in Table 60.

Figure 36. DSPI classic SPI timing — slave, CPHA = 0



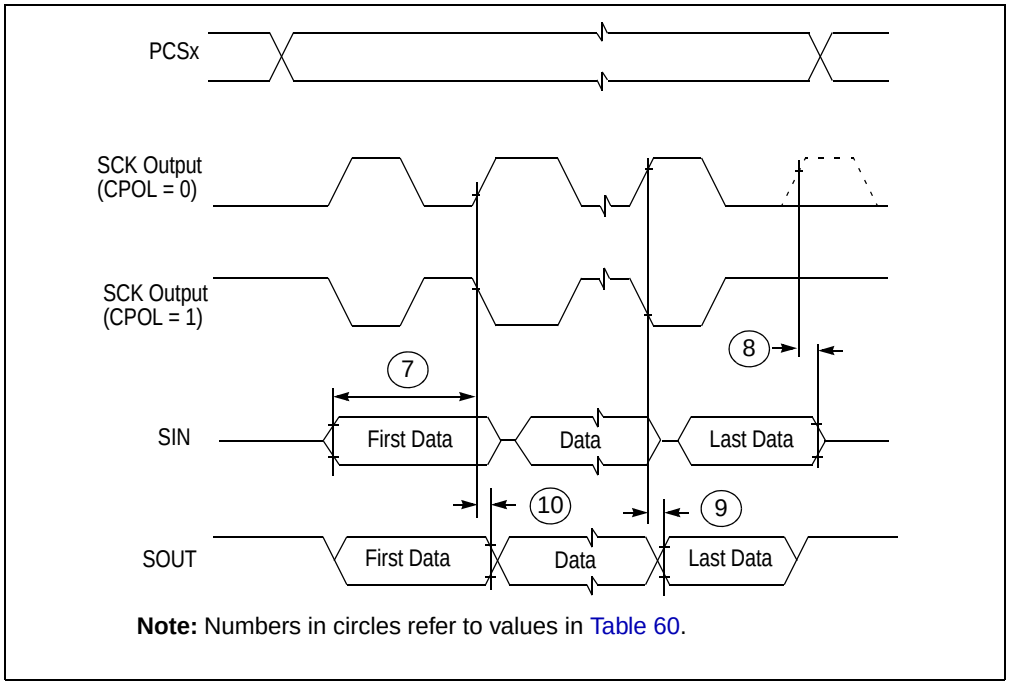
Note: Numbers in circles refer to values in Table 60.

Figure 37. DSPI classic SPI timing — slave, CPHA = 1



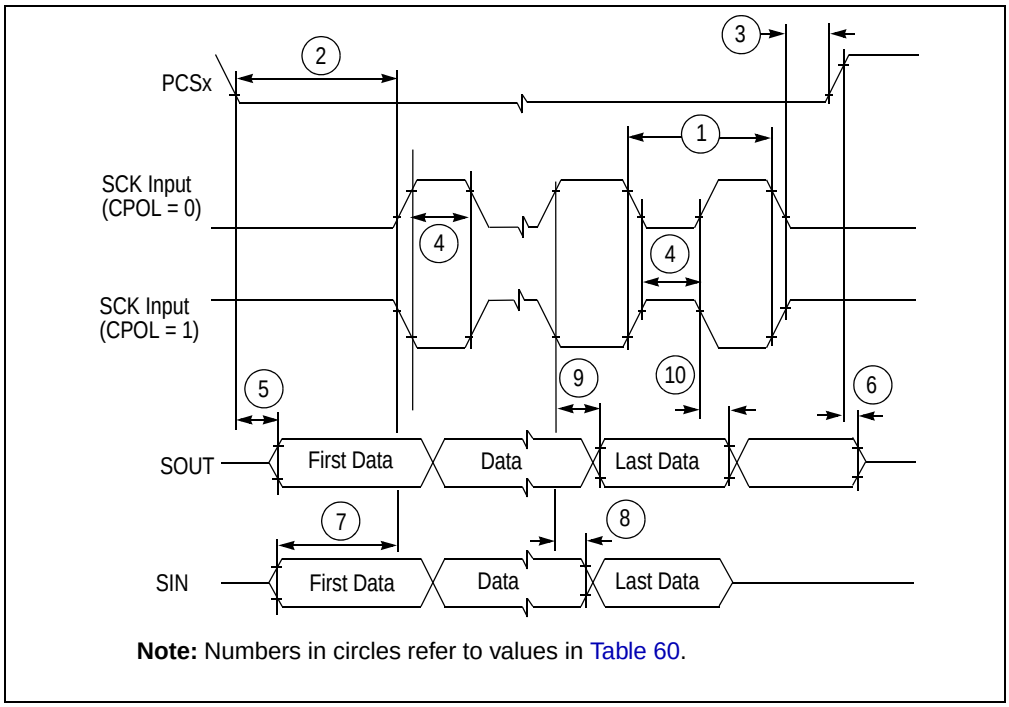
Note: Numbers in circles refer to values in Table 60.

Figure 38. DSPI modified transfer format timing — master, CPHA = 0



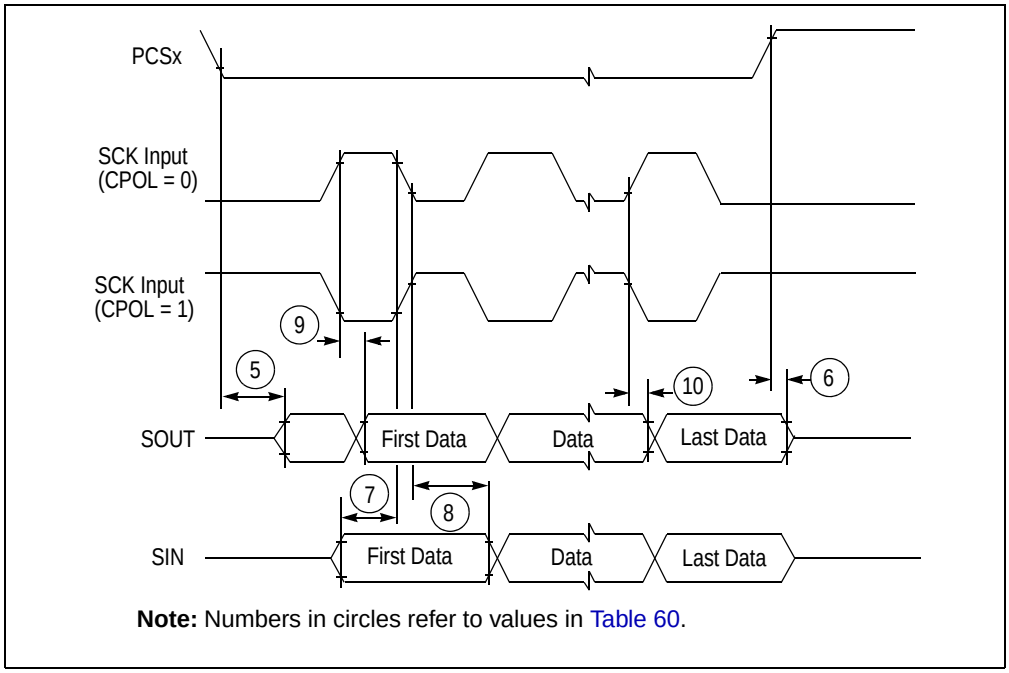
Note: Numbers in circles refer to values in Table 60.

Figure 39. DSPI modified transfer format timing — master, CPHA = 1



Note: Numbers in circles refer to values in Table 60.

Figure 40. DSPI modified transfer format timing — slave, CPHA = 0



Note: Numbers in circles refer to values in Table 60.

Figure 41. DSPI modified transfer format timing — slave, CPHA = 1

3.20.8 I^2C timing

Table 61. I^2C Input Timing Specifications — SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	2	—	IP-Bus Cycle[1]
2	—	CC	D	Clock low time	8	—	IP-Bus Cycle[1]
4	—	CC	D	Data hold time	0.0	—	ns
6	—	CC	D	Clock high time	4	—	IP-Bus Cycle[1]
7	—	CC	D	Data setup time	0.0	—	ns
8	—	CC	D	Start condition setup time (for repeated start condition only)	2	—	IP-Bus Cycle[1]
9	—	CC	D	Stop condition setup time	2	—	IP-Bus Cycle[1]

NOTES:
1 Inter Peripheral Clock is the clock at which the I^2C peripheral is working in the device

Table 62. I²C Output Timing Specifications — SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1[1]	—	CC	D	Start condition hold time	6	—	IP-Bus Cycle[2]
2[1]	—	CC	D	Clock low time	10	—	IP-Bus Cycle[1]
3[3]	—	CC	D	SCL/SDA rise time	—	99.6	ns
4[1]	—	CC	D	Data hold time	7	—	IP-Bus Cycle[1]
5[1]	—	CC	D	SCL/SDA fall time	—	99.5	ns
6[1]	—	CC	D	Clock high time	10	—	IP-Bus Cycle[1]
7[1]	—	CC	D	Data setup time	2	—	IP-Bus Cycle[1]
8[1]	—	CC	D	Start condition setup time (for repeated start condition only)	20	—	IP-Bus Cycle[1]
9[1]	—	CC	D	Stop condition setup time	10	—	IP-Bus Cycle[1]

NOTES:
1. Programming IBFD (I²C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.
2. Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device
3. Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

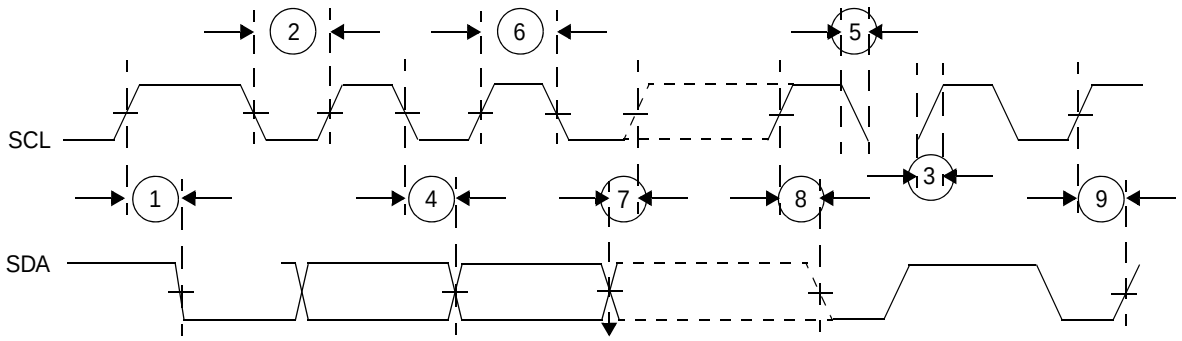


Figure 42. I²C input/output timing

3.20.9 QuadSPI timing

The following notes apply to Table 63:

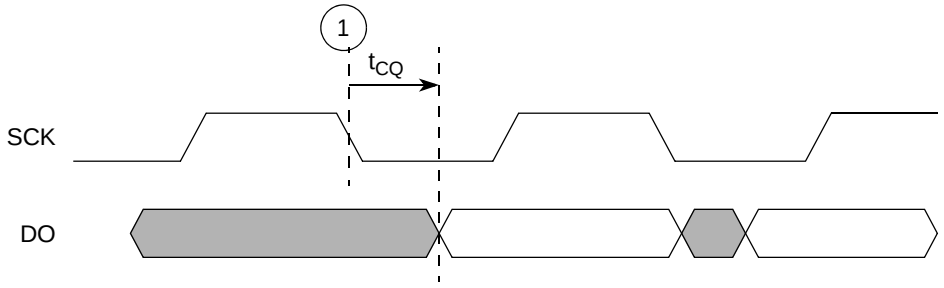
- All data are based on a negative edge data launch from PXD10 and a positive edge data capture as shown in the timing diagrams.
- Typical values are provided from center-split material at 25 °C and 3.3 V. Minimum and maximum values are from a temperature variation of –45 °C to 105 °C and the following supply conditions:
  - IO voltage: 3.2 V, core supply: 1.2 V

— IO voltage: 3.6 V, core supply: 1.2 V

- All measurements are taken at 70% of VDDE levels for clock pin and 50% of VDDE level for data pins.
- Timings correspond to QSPI_SMPR = 0x0000_000x. See the *PXD10 Microcontroller Reference Manual* for details.
- A negative value of hold is an indication of pad delay on the clock pad (delay between the edge capturing data inside the device and the edge appearing at the pin).
- Values are with a load of 15pF on the output pins.

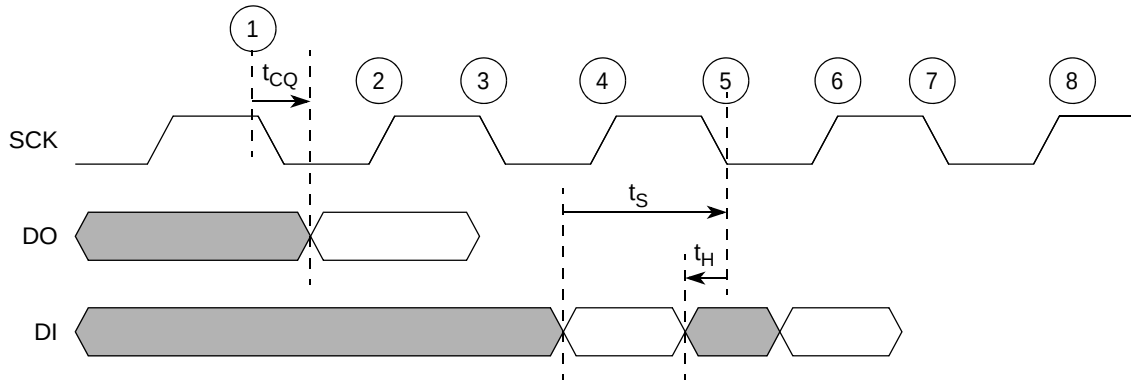
Table 63. QuadSPI timing

Symbol		C	Parameter	Value			Unit
				Min	Typ	Max	
t_{CQ}	CC	T	Clock to Q delay	1.60	2.4	5.33	ns
t_S	CC	T	Setup time for incoming data	6.1	9.4	12.1	ns
t_H	CC	T	Hold time requirement for incoming data	–12.5	–8.5	–7.5	ns
t_R	CC	T	Clock pad rise time	0.4	0.6	1.0	ns
t_F	CC	T	Clock pad fall time	0.3	0.5	0.9	ns



1. Last address out

Figure 43. QuadSPI output timing diagram



1. Last address out
2. Address captured at flash
3. Data out from flash
4. Ideal data capture edge
5. Delayed data capture edge with QSPI_SMPR=0x0000_000x
6. Delayed data capture edge with QSPI_SMPR=0x0000_002x
7. Delayed data capture edge with QSPI_SMPR=0x0000_004x
8. Delayed data capture edge with QSPI_SMPR=0x0000_006x

Figure 44. QuadSPI input timing diagram

The clock profile in Figure 45 is measured at 30% to 70% levels of VDDE.

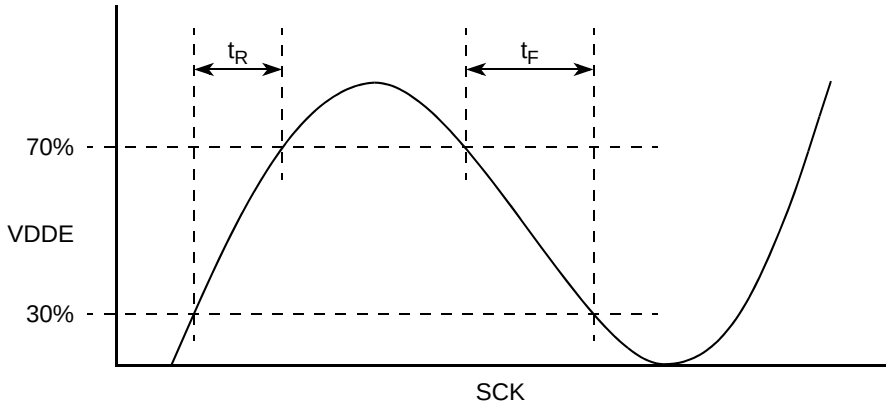
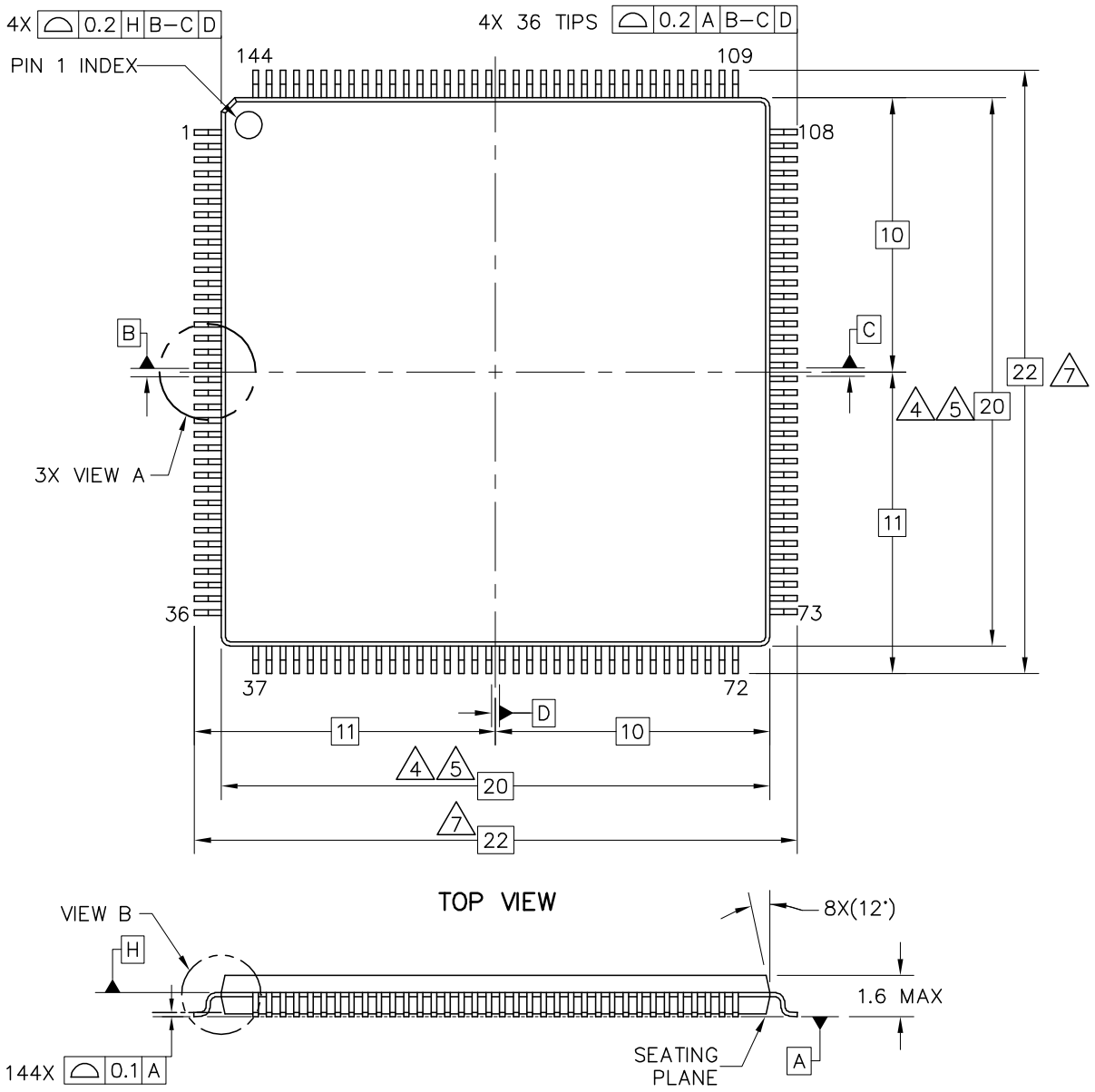


Figure 45. QuadSPI clock profile

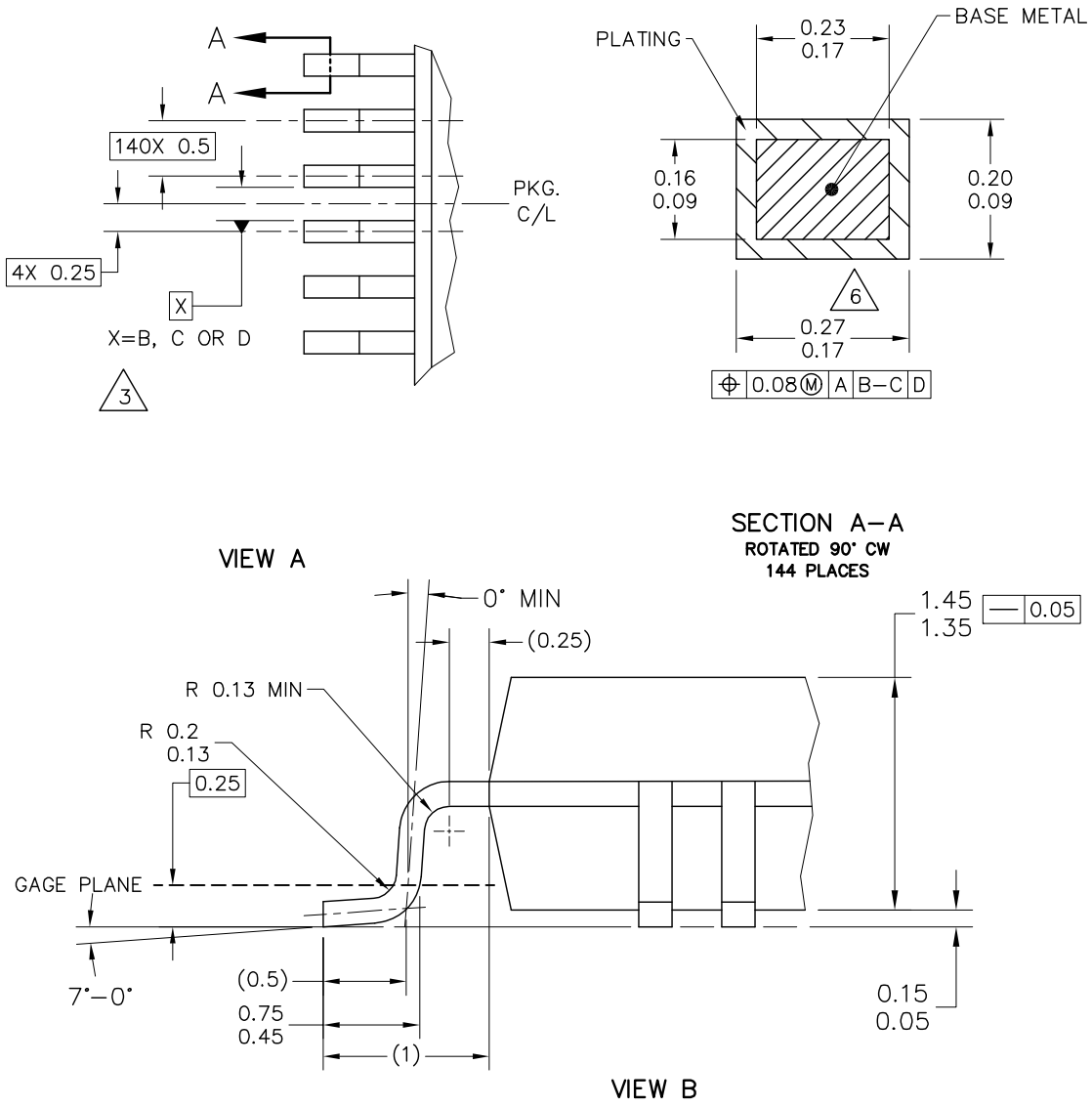
4 Package mechanical data

4.1 144 LQFP



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TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23177W	REV: F
	CASE NUMBER: 918–03	20 MAY 2005
	STANDARD: NON–JEDEC	

Figure 46. LQFP144 mechanical drawing (Part 1 of 3)



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TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23177W	REV: F
	CASE NUMBER: 918–03	20 MAY 2005
	STANDARD: NON–JEDEC	

Figure 47. LQFP144 mechanical drawing (Part 2 of 3)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.

5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

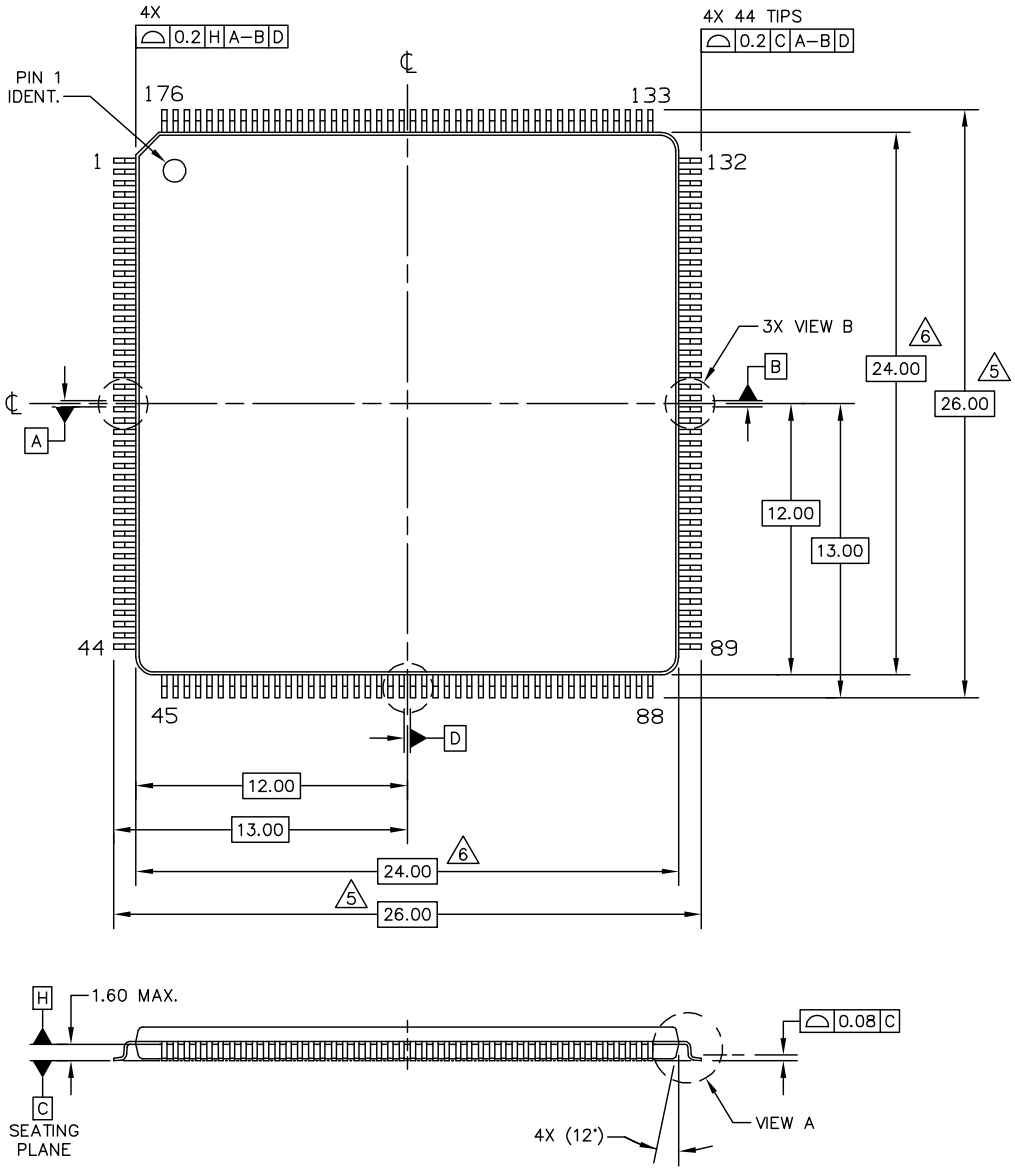
6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

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	CASE NUMBER: 918–03	20 MAY 2005
	STANDARD: NON–JEDEC	

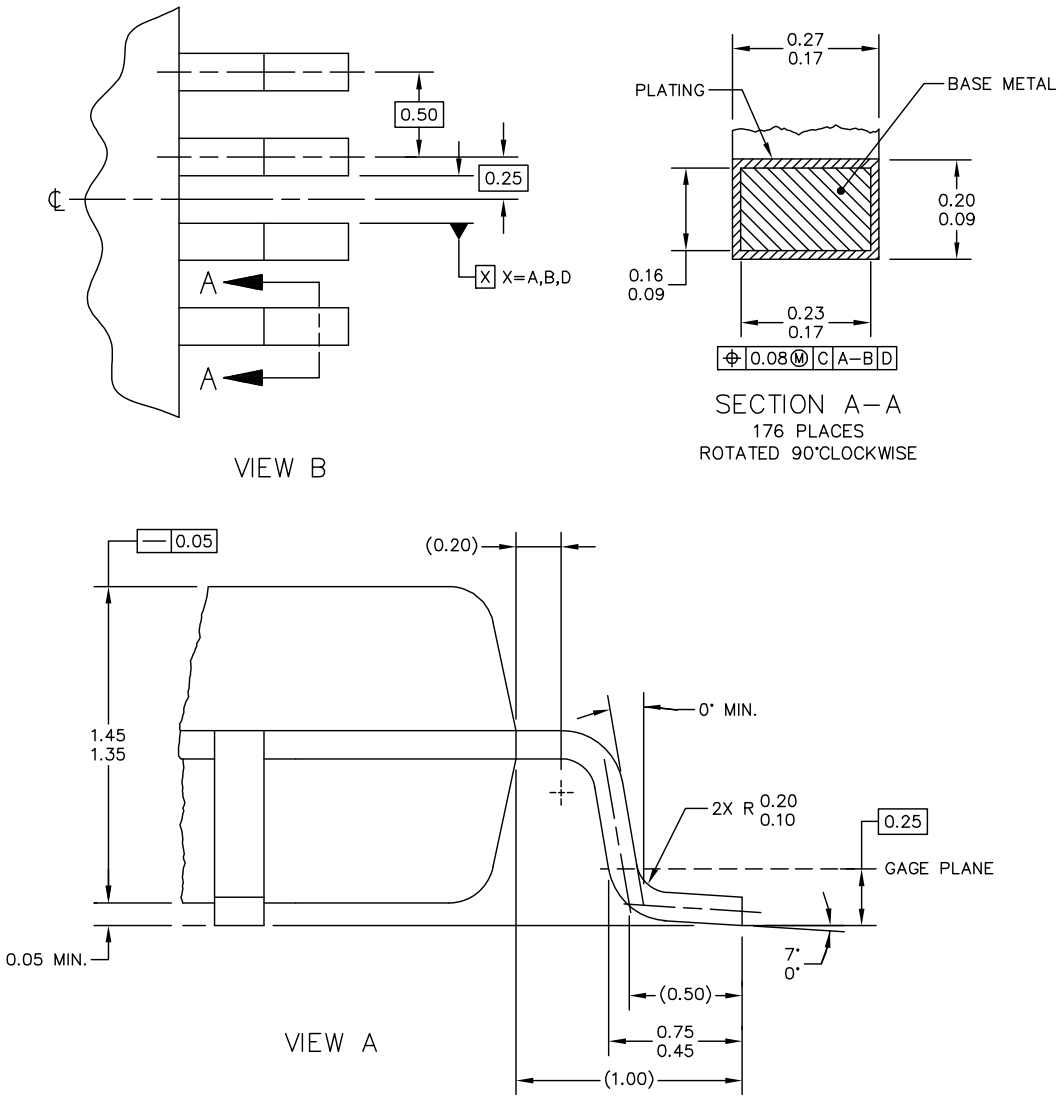
Figure 48. LQFP144 mechanical drawing (Part 3 of 3)

4.2 176 LQFP



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TITLE: 176 LD TQFP, 24 X 24 PKG, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23479W	REV: B
	CASE NUMBER: 1101–01	02 JUN 2005
	STANDARD: JEDEC MS–026 BGA	

Figure 49. LQFP176 mechanical drawing (Part 1 of 3)



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TITLE: 176 LD TQFP, 24 X 24 PKG, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23479W	REV: B
	CASE NUMBER: 1101–01	02 JUN 2005
	STANDARD: JEDEC MS–026 BGA	

Figure 50. LQFP176 mechanical drawing (Part 2 of 3)

NOTES:

1 DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.

2 DIMENSIONS IN MILLIMETERS.

3 DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4 DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

5 THIS DIMENSIONS TO BE DETERMINED AT SEATING PLANE, DATUM C.

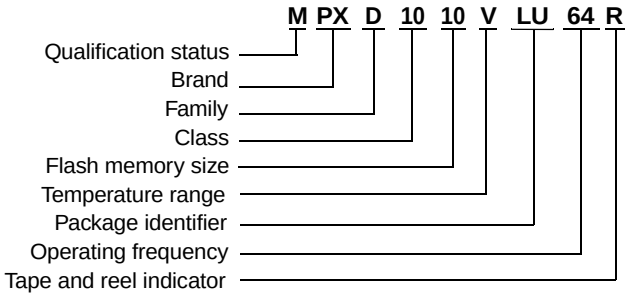
6 THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. THIS DIMENSIONS INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

7 THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD 0.07.

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TITLE: 176 LD TQFP, 24 X 24 PKG, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23479W	REV: B
	CASE NUMBER: 1101–01	02 JUN 2005
	STANDARD: JEDEC MS–026 BGA	

Figure 51. LQFP176 mechanical drawing (Part 3 of 3)

5 Ordering information



Qualification status
P = Pre-qualification (engineering samples)
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Family
D = Display Graphics
N = Connectivity/Network
R = Performance/Real Time Control
S = Safety

Flash Memory Size
05 = 512 KB
10 = 1 MB

Temperature range
V = –40 °C to 105 °C (ambient)

Package identifier
LQ = 144 LQFP
LU = 176 LQFP

Operating frequency
64 = 64 MHz
120 = 120 MHz

Tape and reel status
R = Tape and reel
(blank) = Trays

Note: Not all options are available on all devices. See Table 64 for more information.

Figure 52. PXD10 orderable part number description

Table 64. PXD10 orderable part number summary

Part number	Flash/SRAM	Package	Speed (MHz)
MPXD1005VLQ64	512 KB / 48 KB	144 LQFP (20 mm x 20 mm)	64
MPXD1010VLQ64	1 MB / 48 KB	144 LQFP (20 mm x 20 mm)	64
MPXD1010VLU64	1 MB / 48 KB	176 LQFP (24 mm x 24 mm)	64

6 Revision history

Table 65. Document revision history

Revision	Date	Substantive changes
1	30 Sep 2011	Initial release.

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