AK7735

Dual DSP with 4chADC + 4chDAC + 4chSRC

1. General Description

The AK7735 is a highly integrated digital signal processor, including a 24-bit stereo ADC with MIC gain amplifiers, a 24-bit stereo ADC with input selector, two 32-bit stereo DACs, 2 stereo sampling rate convertors supporting the sampling frequency up to 192kHz and dual DSPs for Audio/HF process. Each DSP has 3072step/fs (when fs=48kHz) parallel processing power. As the AK7735 is a RAM based DSP, it is freely programmable for user requirements, such as acoustic effects and proprietary high performance hands-free function. The AK7735 is available in a 48-pin LQFP package.

2. Features

□ Dual DSP: (DSP1 and DSP2 have the same specification. Memory areas are shared by them)
- **Word length: 28-bit (Simple floating point supported)**
- **Instruction cycle: Max. 6.8ns (3072fs at fs=48kHz)**
- **Multiplier: 24 x 24 → 48-bit (Double precision arithmetic available)**
- **Divider: 24 / 24 → 24-bit (Floating point normalization function)**
- **ALU: 52-bit Arithmetic Operation (with 4bits overflow margin)**
- **Program RAM: 4096-word x 36-bit**
- **Coefficient RAM: 6144-word x 24-bit**
- **Data RAM: 4096-word x 28-bit**
- **Delay RAM: 12288-word x 28-bit**
- **JX pins (Interrupt)**
- **Independent Power Management Function for DSP1, DSP2**

□ ADC1: 24-bit Stereo ADC with MIC Gain Amplifiers
- **Sampling Frequency: fs = 8kHz ~ 192kHz**
- **Channel Independent Analog Gain Amplifiers (0~18dB(2dB Step), 18~36dB(3dB Step))**
- **Differential Input or Single-ended Input**
- **ADC Characteristics S/N: 106dB (fs=48kHz, Differential Input, MIC Gain=0dB)**
- **Channel Independent Digital Volume Control (24dB〜-103dB, 0.5dB Step, Mute)**
- **Digital HPF for DC Offset Cancelling**
- **Low Noise MIC Power Output: 1ch**
- **4 types of Digital Filter for Sound Color Selection**

□ ADC2: 24-bit Stereo ADC with Input Selector
- **Sampling Frequency: fs = 8kHz ~ 192kHz**
- **Analog Input Selector: Differential Input x1 or Single-ended Input x2,**
- **ADC Characteristics S/N: 106dB (fs=48kHz, Differential Input)**
- **Channel Independent Digital Volume (24dB ~ -103dB, 0.5dB Step, Mute)**
- **Digital HPF for DC Offset Cancelling**
- **4 types of Digital Filter for Sound Color Selection**

□ DAC: Advanced 32bit DAC
- **2ch x 2**
- **Sampling Frequency: fs = 8kHz ~ 192kHz**
- **Single-ended Output**
- **DAC Characteristics S/N: 108dB (fs=48kHz)**
- **Channel Independent Digital Volume Control (12dB ~ -115dB, 0.5dB Step, Mute)**
- **4 types of Digital Filter for Sound Color Selection**

□ SRC:
- **2ch x 2**
- **FSI = 8kHz ~ 192kHz, FSO = 8kHz ~ 192kHz (FSO/FSI = 0.167 ~ 6.0)**

□ Digital Interfaces
- **Digital Input Port x 4 (Max 32ch, in TDM mode)**
- **Digital Output Port x 4 (Max 32ch, in TDM mode)**
- **Independent LRCK/BICK port x 3**
- **Data Format: MSB 32, 24bit / LSB 24, 20, 16bit / I^2S**
- **PCM Short / Long Frame Supported**
- **TDM Format Supported (Max:8ch / 256fs, fs=96kHz)**

□ PLL Circuit

□ µP Interface: SPI(Max 6MHz) / I^2C(400kHz Fast Mode, 1MHz Fast Mode Plus)

□ Power Supply:

Analog:	**AVDD:**	**3.0V ~ 3.6V (Typ. 3.3V)**
Digital:	**LVDD:**	**3.0V ~ 3.6V (Typ. 3.3V) (3.3V → 1.2V regulator integrated)**
I/F	**VDD33:**	**3.0V ~ 3.6V (Typ. 3.3V)**
	TVDD:	**1.7V ~ 3.6V (Typ. 3.3V)**

□Operating Temperature Range:

AK7735VQ: Ta = -40 ~ 85°C

AK7735EQ: Ta = -20 ~ 85°C

□Package: 48-pin LQFP (7mm x 7mm, 0.5mm pitch)

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4. Block Diagrams

■ Block Diagram

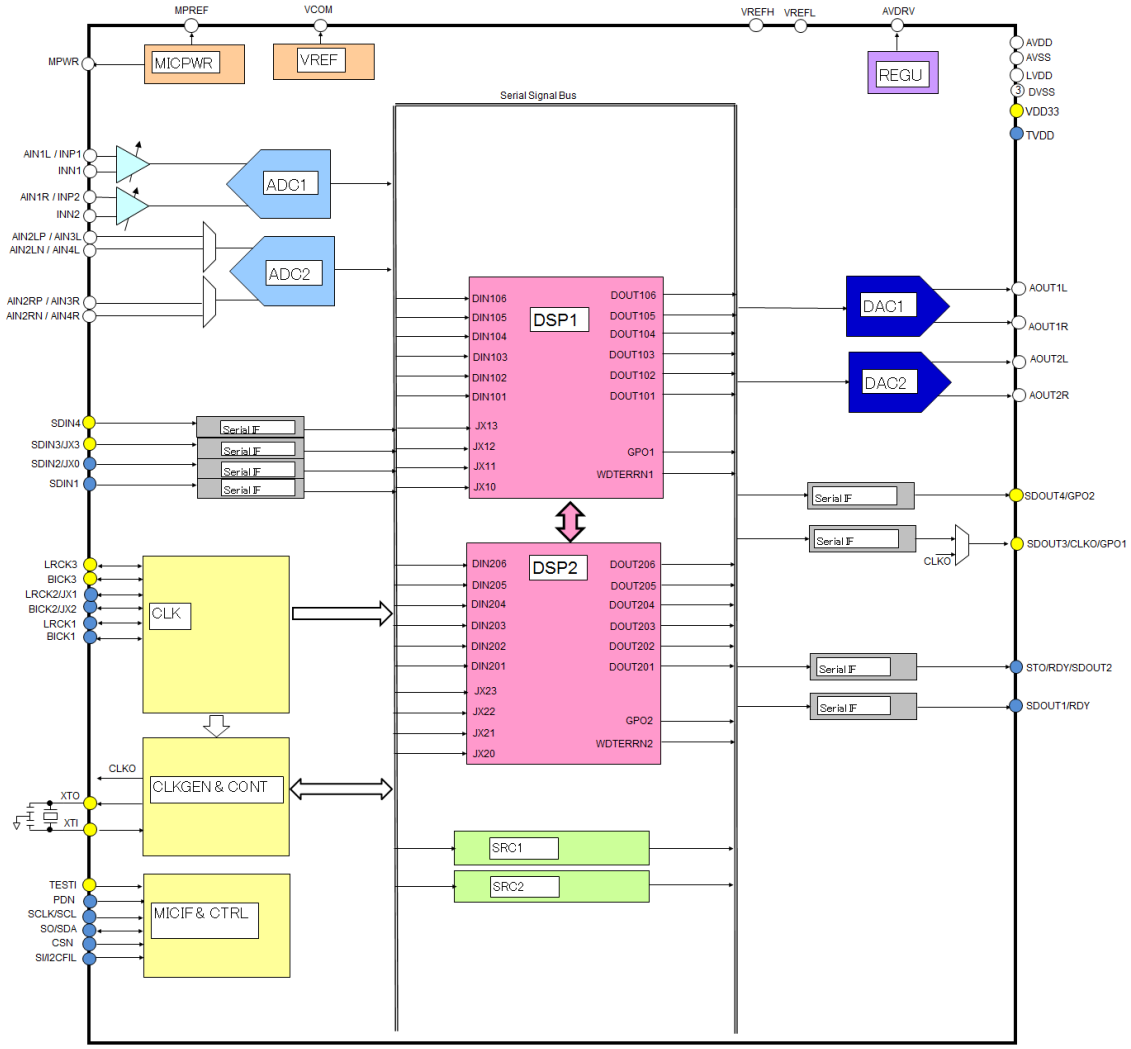


Figure 1. Block Diagram

■ DSP Block Diagram

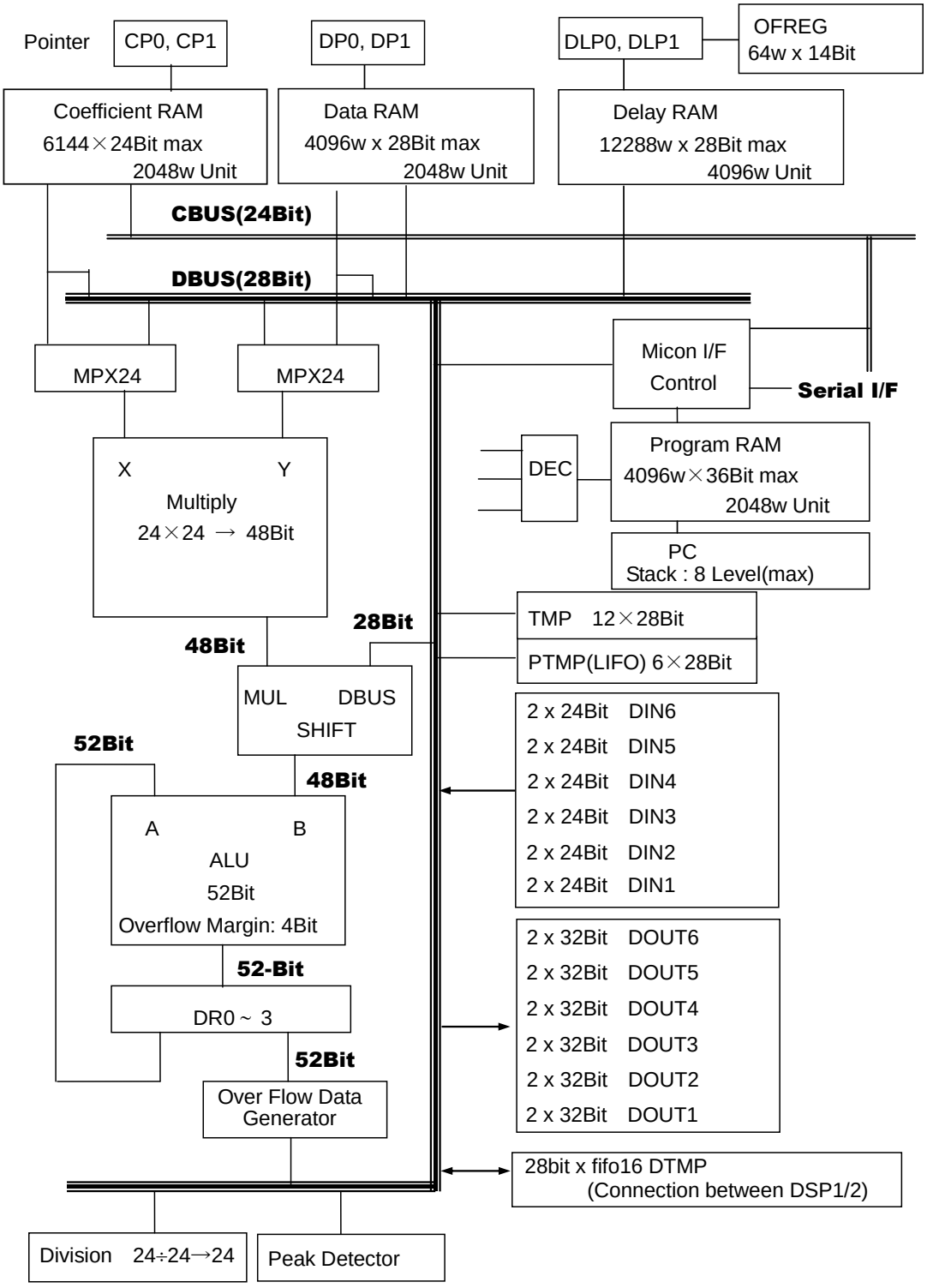


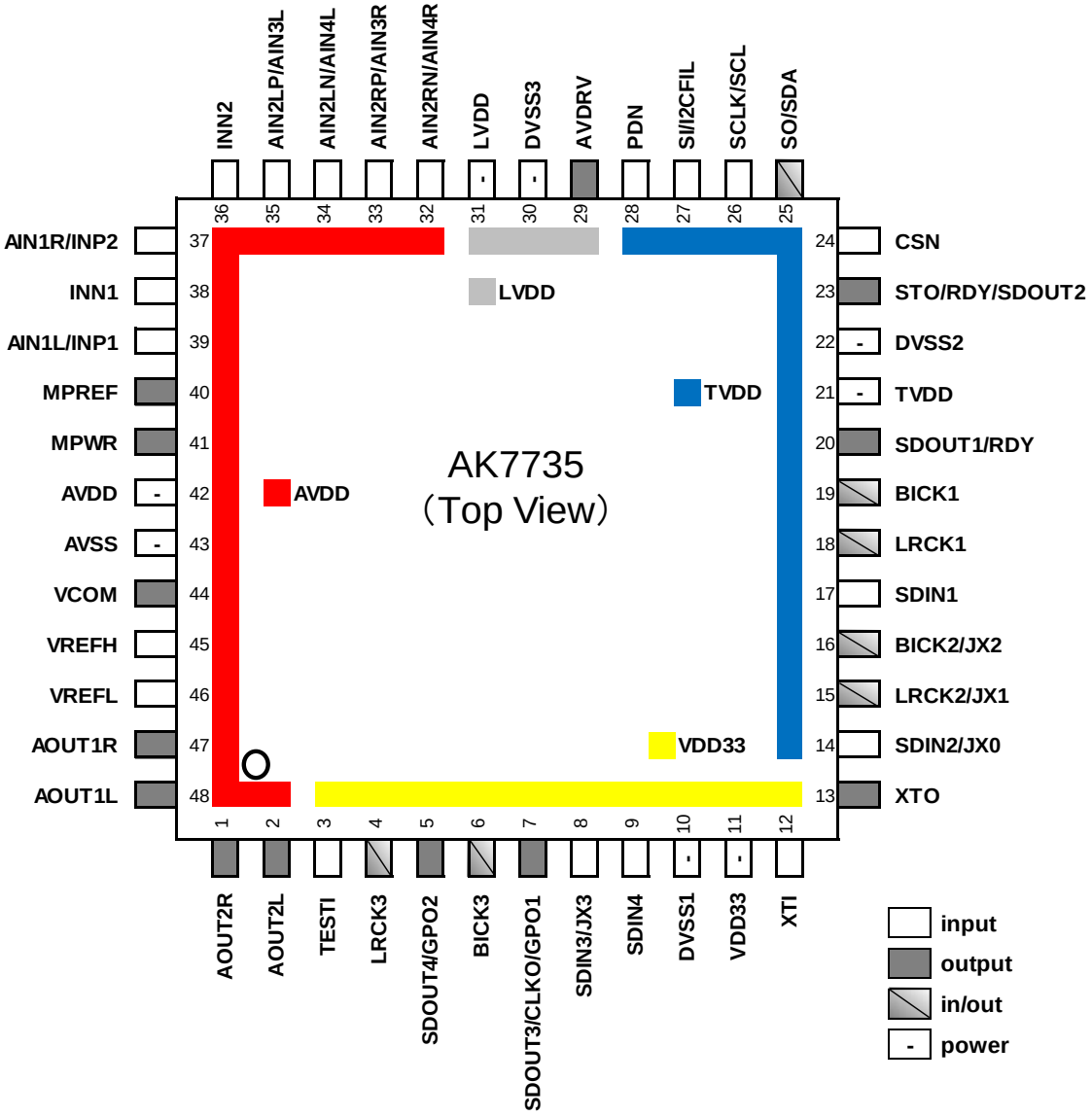
Figure 2. DSP Block Diagram

Note

* 1. Coefficient RAM, Data RAM, Delay RAM, Program RAM areas are shared by DSP1 and DSP2 and the sizes are configurable by control registers.

5. Pin Configurations and Functions

■ Pin Configurations



■ Pin Functions

No.	Pin Name	I/O	Function	Supply Power
1	AOUT2R	O	DAC2 Rch Analog Output Pin This pin outputs “Hi-Z” during power-down state.	AVDD
2	AOUT2L	O	DAC2 Lch Analog Output Pin This pin outputs “Hi-Z” during power-down state.	AVDD
3	TESTI	I	Test Input Pin It must be tied “L”.	VDD33
4	LRCK3	I/O	LR Channel Select Clock 3 Pin	VDD33
5	SDOUT4	O	Serial Data Output 4 Pin	VDD33
	GPO2	O	GPO Output 2 Pin (GPO Output of DSP2)	
6	BICK3	I/O	Serial Bit Clock 3 Pin	VDD33
7	SDOUT3	O	Serial Data Output 3 Pin	VDD33
	CLKO	O	Master Clock Output Pin	
	GPO1	O	GPO Output 1 Pin (GPO Output of DSP1)	
8	SDIN3	I	Serial Data Input 3 Pin	VDD33
	JX3	I	External Conditional Jump Input 3 Pin	
9	SDIN4	I	Serial Data Input 4 Pin	VDD33
10	DVSS1	-	Digital Ground 1 Pin 0V	-
11	VDD33	-	Digital I/F Power Supply Pin 3.0~3.6V (typ.3.3V)	-
12	XTI	I	Crystal Oscillator Input Pin When using a crystal oscillator, connect it between XTI and XTO. When not using XTI pin, leave this pin open.	VDD33
13	XTO	O	Crystal Oscillator Output Pin When using a crystal oscillator, connect it between XTI and XTO. When not using a crystal oscillator, leave this pin open.	VDD33
14	SDIN2	I	Serial Data Input 2 Pin	TVDD
	JX0	I	External Conditional Jump Input 0 Pin	
15	LRCK2	I/O	LR Channel Select Clock 1 Pin	TVDD
	JX1	I	External Conditional Jump Input 1 Pin	
16	BICK2	I/O	Serial Bit Clock 2 Pin	TVDD
	JX2	I	External Conditional Jump Input 2 Pin	
17	SDIN1	I	Serial Data Input 1 Pin	TVDD
18	LRCK1	I/O	LR Channel Select Clock 1 Pin	TVDD
19	BICK1	I/O	Serial Bit Clock 1 Pin	TVDD
20	SDOUT1	O	Serial Data Output 1 Pin	TVDD
	RDY	O	RDY Signal Output Pin	
21	TVDD	-	Digital I/F Power Supply Pin 1.7~3.6V (typ.3.3V)	-
22	DVSS2	-	Digital Ground 2 Pin 0V	-

No.	Pin Name	I/O	Function	Supply Power
23	STO	O	Status Output Pin This pin outputs “L” during power-down state.	TVDD
	RDY	O	RDY Signal Output Pin	
	SDOUT2	O	Serial Data Output 2 Pin	
24	CSN	I	SPI Mode SPI I/F Chip Select Pin During power-down state or when SPI I/F is not in use, leave this pin “H” level.	TVDD
		I	I^2C Mode I^2C I/F Chip Address Pin This pin must be pulled up or pulled down.	
25	SO	O	Serial Data Output Pin for SPI I/F This pin outputs “Hi-Z” during power-down state. This pin must be pulled up or pulled down.	TVDD
	SDA	I/O	Serial Data In/Output Pin for I^2C I/F This pin outputs “Hi-Z” during power-down state.	
26	SCLK	I	Serial Data Clock Input Pin for SPI I/F	TVDD
	SCL	I	Serial Data Clock Input Pin for I^2C I/F	
27	SI	I	Serial Data Input Pin for SPI I/F	TVDD
	I2CFIL	I	I^2C I/F Mode Select Input Pin I2CFIL = “L”: Fast Mode (400kHz) I2CFIL = “H”: Fast Mode Plus (1MHz) (should be fixed to TVDD2)	
28	PDN	I	Power-down Pin Use this pin to power down the AK7735. The PDN pin should be held “L” when power is supplied.	TVDD
29	AVDRV	O	VREG Output Pin Connect a 2.2uF(±30%) ceramic capacitor between this pin and DVSS3. Do not connect this pin to an external circuit.	LVDD
30	DVSS3	-	Digital Ground 3 Pin 0V	-
31	LVDD	-	Digital Core Power Supply Pin 3.0~3.6V (typ.3.3V)	-

No.	Pin Name	I/O	Function	Supply Power
32	AIN2RN	I	ADC2 Rch Inverted Differential Input 2 Pin	AVDD
	AIN4R	I	ADC2 Rch Single-ended Input 4 Pin	
33	AIN2RP	I	ADC2 Rch Non-inverted Differential Input 2 Pin	AVDD
	AIN3R	I	ADC2 Rch Single-ended Input 3 Pin	
34	AIN2LN	I	ADC2 Lch Inverted Differential Input 2 Pin	AVDD
	AIN4L	I	ADC2 Lch Single-ended Input 4 Pin	
35	AIN2LP	I	ADC2 Lch Non-inverted Differential Input 2 Pin	AVDD
	AIN3L	I	ADC2 Lch Single-ended Input 3 Pin	
36	INN2	I	ADC1 Rch Inverted Differential Input 2 Pin	AVDD
37	AIN1R	I	ADC1 Rch Single-ended Input 1 Pin	AVDD
	INP2	I	ADC1 Rch Non-inverted Differential Input 2 Pin	
38	INN1	I	ADC1 Lch Inverted Differential Input 1 Pin	AVDD
39	AIN1L	I	ADC1 Lch Single-ended Input 1 Pin	AVDD
	INP1	I	ADC1 Lch Non-inverted Differential Input 1 Pin	
40	MPREF	O	Ripple Filter Pin for Microphone Power Supply Connect a 1uF ceramic capacitor between this pin and AVSS. Do not connect this pin to an external circuit.	AVDD
41	MPWR	O	Power Supply Output Pin for Microphone This pin outputs “Hi-Z” during power-down state.	AVDD
42	AVDD	-	Analog Power Supply Pin 3.0~3.6V (typ.3.3V)	-
43	AVSS	-	Analog Ground Pin 0V	-
44	VCOM	O	Analog Common Voltage Output Pin Connect a 2.2uF ceramic capacitor between this pin and AVSS. Do not connect this pin to an external circuit. This pin outputs “L” during power-down state.	AVDD
45	VREFH	I	Analog High-level Reference Voltage Input Pin Connect this pin to AVDD.	AVDD
46	VREFL	I	Analog Low-level Reference Voltage Input Pin Connect this pin to AVSS.	AVDD
47	AOUT1R	O	DAC1 Rch Analog Output Pin This pin outputs “Hi-Z” during power-down state.	AVDD
48	AOUT1L	O	DAC1 Lch Analog Output Pin This pin outputs “Hi-Z” during power-down state.	AVDD

■ Handling of Unused Pins

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	MPREF, MPWR, AIN1L/INP1, INN1, AIN1R/INP2, INN2, AIN2LP/AIN3L, AIN2LN/AIN4L, AIN2RP/AIN3R, AIN2RN/AIN4R, AOUT1L, AOUT1R, AOUT2L, AOUT2R	Open
Digital	XTI, XTO, SDOUT1/RDY, STO/RDY/SDOUT2, SDOUT3/CLKO/GPO1, SDOUT4/GPO2	Open
	SDIN4, SDIN3/JX3, SDIN2/JX0, SDIN1, LRCK1, BICK1, LRCK2/JX1, BICK2/JX2, LRCK3, BICK3, TESTI	Connect to DVSS1/DVSS2

Table 1. Handling of Unused Pins

■ Internal Pulled-down Pins Status

No.	Pin Name	Power Down Status PDN pin = "L"	Power Down Release PDN pin = "H" (Slave mode)	Power Down Release PDN pin = "H" (Master mode)
3	TESTI	Pulled-down (25kΩ)	Pulled-down (25kΩ)	Pulled-down (25kΩ)
18	LRCK1	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
19	BICK1	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
15	LRCK2/JX1	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
16	BICK2/JX2	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
4	LRCK3	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
6	BICK3	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
20	SDOUT1/RDY	Pulled-down (50kΩ)	Output	Output
23	STO/RDY/SDOUT2	Pulled-down (50kΩ)	Output	Output
7	SDOUT3/CLKO/GPO1	Pulled-down (50kΩ)	Output	Output
5	SDOUT4/GPO2	Pulled-down (50kΩ)	Output	Output
29	AVDRV	Pulled-down (70Ω)	Output	Output

Table 2. Internal Pulled-down Pins Status

Note
* 2. Typical resistance value when LVDD=TVDD=VDD33=3.3V.

■ Power-down Status of Output Pins

No	Pin Name	I/O	Power-down Status	No	Pin Name	I/O	Power-down Status
44	VCOM	O	“L” Output	4	LRCK3	I/O	Input
40	MPREF	O	“L” Output	6	BICK3	I/O	Input
41	MPWR	O	“Hi-Z” Output	25	SO/SDA	I/O	“Hi-Z” Output
48	AOUT1L	O	“Hi-Z” Output	20	SDOUT1/RDY	O	“L” Output (Pulled-down)
47	AOUT1R	O	“Hi-Z” Output	23	STO/RDY/SDOUT2	O	“L” Output (Pulled-down)
2	AOUT2L	O	“Hi-Z” Output	7	SDOUT3/CLKO/GPO1	O	“L” Output (Pulled-down)
1	AOUT2R	O	“Hi-Z” Output	5	SDOUT4/GPO2	O	“L” Output (Pulled-down)
18	LRCK1	I/O	Input	13	XTO	O	“Hi-Z” Output
19	BICK1	I/O	Input	29	AVDRV	O	“L” Output (Pulled-down)
15	LRCK2/JX1	I/O	Input				
16	BICK2/JX2	I/O	Input				

Table 3. Power-down Status of Output Pins

6. Absolute Maximum Ratings

(AVSS=DVSS1=DVSS2=DVSS3=0V * 3)

Parameter	Symbol	Min.	Max.	Unit
Power Supplies				
Analog	AVDD	-0.3	4.3	V
Digital1(Core)	LVDD	-0.3	4.3	V
Digital2(I/F)	TVDD	-0.3	4.3	V
Digital3(I/F)	VDD33	-0.3	4.3	V
Difference (AVSS, DVSS1, DVSS2, DVSS3) * 3	ΔGND	-0.3	0.3	V
Input Current (except power supply pins)	IIN	—	±10	mA
Analog Input Voltage * 4	VINA	-0.3	(AVDD+0.3) or 4.3	V
Digital Input Voltage * 5	VIND1	-0.3	(TVDD+0.3) or 4.3	V
Digital Input Voltage * 6	VIND2	-0.3	(VDD33+0.3) or 4.3	V
Ambient Temperature (AK7735VQ)	Ta	-40	85	°C
Ambient Temperature (AK7735EQ)	Ta	-20	85	°C
Storage Temperature	Tstg	-65	150	°C

Notes

* 3. All voltages are with respect to ground. AVSS and DVSS1-3 must be connected to the same ground.
* 4. The maximum analog input voltage is smaller value between (AVDD+0.3)V and 4.3V.
* 5. The maximum digital input voltage of SDIN1, SDIN2/JX0, LRCK1, BICK1, LRCK2/JX1, BICK2/JX2, PDN, SCLK/SCL, CSN and SI/I2CFIL pins is smaller value between (TVDD+0.3)V and 4.3V.
* 6 . The maximum digital input voltage of SDIN3/JX3, SDIN4, LRCK3, BICK3, TESTI and XTI pins is smaller value between (VDD33+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS1=DVSS2=DVSS3=0V * 3)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supplies					
Analog	AVDD	3.0	3.3	3.6	V
Digital1(Core)	LVDD	3.0	3.3	3.6	V
Digital2(I/F)	TVDD	1.7	3.3	3.6	V
Digital3(I/F)	VDD33	3.0	3.3	3.6	V
Difference1	AVDD – LVDD	-0.1	0	0.1	V
Difference2	AVDD – VDD33	-0.1	0	0.1	V
Difference3	LVDD – VDD33	-0.1	0	0.1	V
Difference4	LVDD – TVDD	-0.1	-	-	V

Notes

* 7. The power-up sequence with AVDD, DVDD, TVDD and VDD33 is not critical. The PDN pin should be held “L” when power is supplied. The PDN pin is allowed to be “H” after all power supplies are applied and settled.
* 8. Do not turn off the power supply of the AK7735 with the power supply of the peripheral device turned on. When using the I^2C interface, pull-up resistors of SDA and SCL pins should be connected to TVDD or less voltage.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

8. Electrical Characteristics

■ Analog Characteristics

1. MIC AMP

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V;
ADC1VL/R bits="0")

	Parameter		Min.	Typ.	Max.	Unit
MIC AMP	Input Impedance		14	20	26	kΩ
	Gain	MGNL[3:0]bits=0h, MGNR[3:0]bits=0h	-1	0	1	dB
		MGNL[3:0]bits=1h, MGNR[3:0]bits=1h	1	2	3	
		MGNL[3:0]bits=2h, MGNR[3:0]bits=2h	3	4	5	
		MGNL[3:0]bits=3h, MGNR[3:0]bits=3h	5	6	7	
		MGNL[3:0]bits=4h, MGNR[3:0]bits=4h	7	8	9	
		MGNL[3:0]bits=5h, MGNR[3:0]bits=5h	9	10	11	
		MGNL[3:0]bits=6h, MGNR[3:0]bits=6h	11	12	13	
		MGNL[3:0]bits=7h, MGNR[3:0]bits=7h	13	14	15	
		MGNL[3:0]bits=8h, MGNR[3:0]bits=8h	15	16	17	
		MGNL[3:0]bits=9h, MGNR[3:0]bits=9h	17	18	19	
		MGNL[3:0]bits=Ah, MGNR[3:0]bits=Ah	20	21	22	
		MGNL[3:0]bits=Bh, MGNR[3:0]bits=Bh	23	24	25	
		MGNL[3:0]bits=Ch, MGNR[3:0]bits=Ch	26	27	28	
		MGNL[3:0]bits=Dh, MGNR[3:0]bits=Dh	29	30	31	
		MGNL[3:0]bits=Eh, MGNR[3:0]bits=Eh	32	33	34	
		MGNL[3:0]bits=Fh, MGNR[3:0]bits=Fh	35	36	37	

2. MIC Bias Output

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V;
Measurement Frequency =20Hz~20kHz)

	Parameter	Min.	Typ.	Max.	Unit
MIC Bias	Output Voltage * 9	2.3	2.5	2.7	V
	Load Resistance	2			kΩ
	Load Capaitance			30	pF
	Output Noise (A-weighted)		-114	-108	dBV

Note
* 9. Output voltage is proportional to AVDD (0.76 x AVDD).

3. MIC AMP + ADC1

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V; Signal Frequency =1kHz; 24bit Data; BICK=64fs; @fs=48kHz, Measurement Frequency BW=20Hz ~ 20kHz; @fs=96kHz,192kHz, BW=20Hz ~ 40kHz; ADC1VL/R bits="0"; MGNL/R[3:0] bits=0h (0dB); Differential Input, Unless otherwise specified.)

	Parameter		Min.	Typ.	Max.	Unit
MIC AMP + ADC1	Resolution				24	Bit
	Input Full Scale Voltage * 10	Differential Input * 13	±2.1	±2.3	±2.5	Vpp
		Differential Input * 14	±0.264	±0.290	±0.315	
		Differential Input * 15	±2.55	±2.83	±3.11	
	Input Full Scale Voltage * 11	Single-ended Input * 13	2.1	2.3	2.5	Vpp
		Single-ended Input * 14	0.264	0.290	0.315	
		Single-ended Input * 15	2.55	2.83	3.11	
	S/(N+D) (-1dBFS)	fs=48kHz * 13	85	95		dB
		fs=48kHz * 14		87		
		fs=96kHz * 13		92		
		fs=96kHz * 14		84		
		fs=192kHz * 13		92		
		fs=192kHz * 14		84		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted) * 13	98	106		dB
		fs=48kHz (A-weighted) * 14		95		
		fs=96kHz * 13		99		
		fs=96kHz * 14		89		
		fs=192kHz * 13		99		
		fs=192kHz * 14		89		
	S/N	fs=48kHz (A-weighted) * 13	98	106		dB
		fs=48kHz (A-weighted) * 14		95		
		fs=96kHz * 13		99		
		fs=96kHz * 14		89		
		fs=192kHz * 13		99		
		fs=192kHz * 14		89		
	Inter-Channel Isolation * 12		90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB
	CMRR * 16		60	80		dB

Notes

* 10. INP1, INN1, INP2 and INN2 pins
* 11. AIN1L and AIN1R pins
* 12. Inter-channel isolation with -1dBFS signal input.
* 13. ADC1VL/R bits = "0", MGNL/R[3:0] bits = 0h (0dB). Input full-scale voltage is proportional to AVDD (0.7 x AVDD).
* 14. ADC1VL/R bits = "0", MGNL/R[3:0] bits = 9h (+18dB). Input full-scale voltage is proportional to AVDD (0.088 x AVDD).
* 15. ADC1VL/R bits = "1", MGNL/R[3:0] bits = 0h (0dB). Input full-scale voltage is proportional to AVDD (0.86 x AVDD).
* 16. Common mode rejection ratio when inputting 1kHz, 100mVpp sine wave to both differential inputs. The value refers to the case when input a 1kHz, ±100mVpp sine wave as differential input.

4. ADC2

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V; Signal Frequency =1kHz; 24bit Data; BICK=64fs; @fs=48kHz, Measurement Frequency BW=20Hz ~ 20kHz; @fs=96kHz,192kHz, BW=20Hz ~ 40kHz; ADC2VL/R bits="0"; Differential Input, Unless otherwise specified.)

	Parameter		Min.	Typ.	Max.	Unit
ADC2	Resolution				24	bit
	Input Impedance		14	20	26	kΩ
	Input Full Scale Voltage * 17	Differential Input * 19	±2.1	±2.3	±2.5	Vpp
		Differential Input * 20	±2.55	±2.83	±3.11	
	Input Full Scale Voltage * 18	Single-ended Input * 19	2.1	2.3	2.5	Vpp
		Single-ended Input * 20	2.55	2.83	3.11	
	S/(N+D) (-1dBFS)	fs=48kHz	85	95		dB
		fs=96kHz		92		
		fs=192kHz		92		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	98	106		dB
		fs=96kHz		99		
		fs=192kHz		99		
	S/N	fs=48kHz (A-weighted)	98	106		dB
		fs=96kHz		99		
		fs=192kHz		99		
	Inter-Channel Isolation * 12		90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB
	CMRR * 16		60	80		dB

Notes

* 17. AIN2LP, AIN2LN, AIN2RP and AIN2RN pins
* 18. AIN3L, AIN3R, AIN4L and AIN4R pins
* 19. ADC2VL/R bits = "0". Input full-scale voltage is propotional to AVDD (0.7 x AVDD).
* 20. ADC2VL/R bits = "1". Input full-scale voltage is propotional to AVDD (0.86 x AVDD).

5. DAC

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V; Signal Frequency =1kHz; 32bit Data; BICK=64fs; @fs=48kHz, Measurement Frequency BW=20Hz ~ 20kHz; @fs=96kHz,192kHz, Measurement Frequency BW=20Hz ~ 40kHz)

	Parameter		Min.	Typ.	Max.	Unit
DAC1 DAC2	Resolution				32	bit
	Output Voltage * 21		2.55	2.83	3.11	Vpp
	S/(N+D) (0dBFS)	fs=48kHz	80	91		dB
		fs=96kHz		89		
		fs=192kHz		89		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	100	108		dB
		fs=96kHz		101		
		fs=192kHz		101		
	S/N	fs=48kHz (A-weighted)	100	108		dB
		fs=96kHz		101		
		fs=192kHz		101		
	Inter-Channel Isolation (fin=1kHz) * 22		90	110		dB
	Channel Gain Mismatch			0.0	0.7	dB
	Load Resistance * 23		10			kΩ
	Load Capaitance				30	pF

Notes

* 21. The output voltage when 0dBFS signal input. The output voltage is proportional to AVDD (0.86 x AVDD).
* 22. Inter-channel isolation between each DAC of Lch and Rch with 0dBFS signal input. (AOUT1L and AOUT1R, and AOUT2L and AOUT2R)
* 23. to AC load

6. SRC

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V; Signal Frequency =1kHz; 24bit Data; Measurement Frequency BW=20Hz ~ FSO/2)

	Parameter	Symbol	Min.	Typ.	Max.	Unit
SRC	Resolution				24	bit
	Input Sample Rate	FSI	8		192	kHz
	Output Sample Rate	FSO	8		192	kHz
	THD+N (Input=1kHz, 0dBFS)					
	Audio Mode					
	(SRCFAUD bit = “1”, SRCFEC bit = “0”)					
	FSO/FSI=192kHz/48kHz			-122		dB
	FSO/FSI=44.1kHz/48kHz			-125		dB
	FSO/FSI=48kHz/88.2kHz			-122		dB
	FSO/FSI=48kHz/96kHz			-133		dB
	FSO/FSI=44.1kHz/96kHz			-116		dB
	FSO/FSI=48kHz/192kHz			-133		dB
	FSO/FSI=8kHz/48kHz			-130		dB
	Voice Mode					
	(SRCFAUD bit = “0”, SRCFEC bit = “0”)					
	FSO/FSI=24kHz/32kHz			-95		dB
	FSO/FSI=16kHz/24kHz			-98		dB
	FSO/FSI=24kHz/44.1kHz			-78		dB
	FSO/FSI=16kHz/44.1kHz			-69		dB
	FSO/FSI=8kHz/32kHz			-130		dB
	Dynamic Range (Input=1kHz, -60dBFS)					
	Audio Mode					
	(SRCFAUD bit = “1”, SRCFEC bit = “0”)					
	FSO/FSI=192kHz/48kHz			132		dB
	FSO/FSI=44.1kHz/48kHz			136		dB
	FSO/FSI=48kHz/88.2kHz			136		dB
	FSO/FSI=48kHz/96kHz			135		dB
	FSO/FSI=44.1kHz/96kHz			136		dB
	FSO/FSI=48kHz/192kHz			136		dB
	FSO/FSI=8kHz/48kHz			130		dB
	Voice Mode					
	(SRCFAUD bit = “0”, SRCFEC bit = “0”)					
	FSO/FSI=24kHz/32kHz			134		dB
	FSO/FSI=16kHz/24kHz			137		dB
	FSO/FSI=24kHz/44.1kHz			132		dB
	FSO/FSI=16kHz/44.1kHz			128		dB
	FSO/FSI=8kHz/32kHz			130		dB
	Dynamic Range (Input=1kHz, -60dBFS, A-weighted)					
	FSO/FSI=44.1kHz/48kHz		-	137	-	dB
	Ratio between Input and Output Sample Rate	FSO/FSI	0.167		6	-

■ Power Consumption

(Ta=25°C; AVDD=LVDD=VDD33=3.0~3.6V(Typ=3.3V, Max=3.6V); TVDD=1.7~3.6V(Typ=3.3V, Max=3.6V); AVSS=DVSS1=DVSS2=DVSS3=0V; fs=192kHz; BICK=64fs; Master Mode; SDOUT1~4/LRCK1~3/BICK1~3=Output; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Up * 24 (PDN pin = "H")	AVDD		23	33	mA
	LVDD		55	98	mA
	TVDD		4	6	mA
	VDD33		5	8	mA
Power-Down (PDN pin = "L")	AVDD		0.01		mA
	LVDD		0.01		mA
	TVDD		0.01		mA
	VDD33		0.01		mA

Note

* 24. The current of LVDD changes depending on the system frequency and contents of DSP program.

9. Digital Filter Characteristics

■ ADC Block

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

1. Sharp Roll-Off Filter (ADSD bit = "0", ADSL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 25	0dB ~ -0.06dB	PB	0		22.1	kHz
	-3.0dB	PB		23.7		kHz
Stopband * 25		SB	27.8			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~20kHz		ΔGD		0		1/fs
Group Delay * 26		GD		20		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		0.9		Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 25	0dB ~ -0.06dB	PB	0		44.2	kHz
	-3.0dB	PB		47.5		kHz
Stopband * 25		SB	55.6			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD		0		1/fs
Group Delay * 26		GD		20		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		1.9		Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 25	0dB ~ -0.04dB	PB	0		83.7	kHz
	-3.0dB	PB		96.0		kHz
Stopband * 25		SB	122.9			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD		0		1/fs
Group Delay * 26		GD		16		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		3.8		Hz

2. Slow Roll-Off Filter (ADSD bit = "0", ADSL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 25	0dB ~ -0.074dB	PB	0		12.5	kHz
	-3.0dB	PB		19.2		kHz
Stopband * 25		SB	36.5			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~20kHz		ΔGD		0		1/fs
Group Delay * 26		GD		8		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		0.9		Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 25	0dB ~ -0.074dB	PB	0		25	kHz
	-3.0dB	PB		38.5		kHz
Stopband * 25		SB	73.0			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD		0		1/fs
Group Delay * 26		GD		8		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		1.9		Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 25	0dB ~ -0.1dB	PB	0		31.1	kHz
	-3.0dB	PB		62.3		kHz
Stopband * 25		SB	145.9			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD		0		1/fs
Group Delay * 26		GD		9		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		3.8		Hz

3. Short Delay Sharp Roll-Off Filter (ADSD bit = “1”, ADSL bit = “0”)

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 25	0dB ~ -0.06dB	PB	0		22.1	kHz
	-3.0dB	PB		23.7		kHz
Stopband * 25		SB	27.8			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~20kHz		ΔGD			2.6	1/fs
Group Delay * 26		GD		6		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		0.9		Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 25	0dB ~ -0.06dB	PB	0		44.2	kHz
	-3.0dB	PB		47.5		kHz
Stopband * 25		SB	55.6			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD			2.6	1/fs
Group Delay * 26		GD		6		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		1.9		Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 25	0dB ~ -0.04dB	PB	0		83.7	kHz
	-3.0dB	PB		96.0		kHz
Stopband * 25		SB	122.9			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD			0.2	1/fs
Group Delay * 26		GD		7		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		3.8		Hz

4. Short Delay Slow Roll-Off Filter (ADSD bit = "1", ADSL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 25	0dB ~ -0.074dB	PB	0		12.5	kHz
	-3.0dB	PB		19.2		kHz
Stopband * 25		SB	36.5			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~20kHz		ΔGD			2.6	1/fs
Group Delay * 26		GD		6		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		0.9		Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 25	0dB ~ -0.074dB	PB	0		25	kHz
	-3.0dB	PB		38.5		kHz
Stopband * 25		SB	73.0			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD			2.6	1/fs
Group Delay * 26		GD		6		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		1.9		Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 25	0dB ~ -0.1dB	PB	0		31.1	kHz
	-3.0dB	PB		63.2		kHz
Stopband * 25		SB	145.9			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD			0.5	1/fs
Group Delay * 26		GD		7		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		3.8		Hz

Notes

* 25. The passband and stopband frequencies are proportional to fs (sampling rate). High-pass filter characteristics are not included. A reference value of each gain amplitude is the maximum value of frequency response.

* 26. Delay time caused by the digital filter calculation. This time is measured from an analog signal input until 24-bit data of both channels are set into the output register. It includes group delay by HPF.

■ DAC Block

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

1. Sharp Roll-Off Filter (DASD bit = "0", DASL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 27	±0.05dB	PB	0		21.7	kHz
	−3.0dB	PB		23.4		kHz
Passband Ripple * 28		PR	-0.0032		0.0032	dB
Stopband * 27		SB	26.3			kHz
Stopband Attenuation * 30, * 31		SA	80.0			dB
Group Delay * 29		GD		27.3		1/fs
Digital Filter + SCF + SMF * 30						
Frequency Response : 0 ~ 20.0kHz			-0.3		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 27	±0.05dB	PB	0		43.5	kHz
	−3.0dB	PB		46.8		kHz
Passband Ripple * 28		PR	-0.0032		0.0032	dB
Stopband * 27		SB	52.5			kHz
Stopband Attenuation * 30, * 31		SA	80.0			dB
Group Delay * 29		GD		27.3		1/fs
Digital Filter + SCF + SMF * 30						
Frequency Response : 0 ~ 40.0kHz			-0.5		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 27	±0.05dB	PB	0		87.0	kHz
	−3.0dB	PB		93.6		kHz
Passband Ripple * 28		PR	-0.0032		0.0032	dB
Stopband * 27		SB	105.0			kHz
Stopband Attenuation * 30, * 31		SA	80.0			dB
Group Delay * 29		GD		27.3		1/fs
Digital Filter + SCF + SMF * 30						
Frequency Response : 0 ~ 80.0kHz			-1.9		0.1	dB

Notes

* 27. The passband and stopband frequencies are proportional to fs (sampling rate).
"PB = 0.4535 × fs, SB = 0.546 × fs"
* 28. Pass-band gain amplitude of double over sampling filter at the first step of Interpolator.
* 29. Delay time caused by the digital filter calculation. This time is measured from setting of the 16/20/24/32-bit impulse data to the input registers to output of the analog peak signal.
* 30. The output level with a 1kHz, 0dB sine wave input is defined as 0dB.
* 31. Band width of Stopband Attenuation ranges from 0Hz to fs.

2. Slow Roll-Off Filter (DASD bit = "0", DASL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 32	±0.05dB	PB	0		8.8	kHz
	−3.0dB	PB		19.8		kHz
Passband Ripple * 28		PR	-0.043		0.043	dB
Stopband * 32		SB	42.7			kHz
Stopband Attenuation * 30, * 31		SA	73.0			dB
Group Delay * 29		GD		6.8		1/fs
Digital Filter + SCF + SMF * 30						
Frequency Response : 0 ~ 20.0kHz			-5.0		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 32	±0.05dB	PB	0		17.7	kHz
	−3.0dB	PB		39.5		kHz
Passband Ripple * 28		PR	-0.043		0.043	dB
Stopband * 32		SB	85.3			kHz
Stopband Attenuation * 30, * 31		SA	73.0			dB
Group Delay * 29		GD		6.8		1/fs
Digital Filter + SCF + SMF * 30						
Frequency Response : 0 ~ 40.0kHz			-5.2		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 32	±0.05dB	PB	0		35.5	kHz
	−3.0dB	PB		79.0		kHz
Passband Ripple * 28		PR	-0.043		0.043	dB
Stopband * 32		SB	171.0			kHz
Stopband Attenuation * 30, * 31		SA	73.0			dB
Group Delay * 29		GD		6.8		1/fs
Digital Filter + SCF + SMF * 30						
Frequency Response : 0 ~ 80.0kHz			-5.9		0.1	dB

Note

* 32. The passband and stopband frequencies are proportional to fs (sampling rate).
"PB = 0.185 × fs, SB = 0.888 × fs"

3. Short Delay Sharp Roll-Off Filter (DASD bit = “1”, DASL bit = “0”)

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 27	±0.05dB	PB	0		21.7	kHz
	−3.0dB	PB		23.4		kHz
Passband Ripple * 28		PR	-0.0031		0.0031	dB
Stopband * 27		SB	26.3			kHz
Stopband Attenuation * 30, * 31		SA	80.0			dB
Group Delay * 29		GD		6.3		1/fs
Digital Filter + SCF + SMF * 30						
Frequency Response : 0 ~ 20.0kHz			-0.3		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 27	±0.05dB	PB	0		43.5	kHz
	−3.0dB	PB		46.8		kHz
Passband Ripple * 28		PR	-0.0031		0.0031	dB
Stopband * 27		SB	52.5			kHz
Stopband Attenuation * 30, * 31		SA	80.0			dB
Group Delay * 29		GD		6.3		1/fs
Digital Filter + SCF + SMF * 30						
Frequency Response : 0 ~ 40.0kHz			-0.5		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 27	±0.05dB	PB	0		87.0	kHz
	−3.0dB	PB		93.6		kHz
Passband Ripple * 28		PR	-0.0031		0.0031	dB
Stopband * 27		SB	105.0			kHz
Stopband Attenuation * 30, * 31		SA	80.0			dB
Group Delay * 29		GD		6.3		1/fs
Digital Filter + SCF + SMF * 30						
Frequency Response : 0 ~ 80.0kHz			-1.9		0.1	dB

4. Short Delay Slow Roll-Off Filter (DASD bit = "1", DASL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 33	±0.05dB	PB	0		12.0	kHz
	−3.0dB	PB		21.1		kHz
Passband Ripple * 28		PR	-0.05		0.05	dB
Stopband * 33		SB	41.5			kHz
Stopband Attenuation * 30, * 31		SA	82.0			dB
Group Delay * 29		GD		5.3		1/fs
Digital Filter + SCF + SMF * 30						
Frequency Response : 0 ~ 20.0kHz			-4.8		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 33	±0.05dB	PB	0		24.2	kHz
	−3.0dB	PB		42.1		kHz
Passband Ripple * 28		PR	-0.05		0.05	dB
Stopband * 33		SB	83.0			kHz
Stopband Attenuation * 30, * 31		SA	82.0			dB
Group Delay * 29		GD		5.3		1/fs
Digital Filter + SCF + SMF * 30						
Frequency Response : 0 ~ 40.0kHz			-5.0		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 33	±0.05dB	PB	0		48.4	kHz
	−3.0dB	PB		84.3		kHz
Passband Ripple * 28		PR	-0.05		0.05	dB
Stopband * 33		SB	165.9			kHz
Stopband Attenuation * 30, * 31		SA	82.0			dB
Group Delay * 29		GD		5.3		1/fs
Digital Filter + SCF + SMF * 30						
Frequency Response : 0 ~ 80.0kHz			-5.7		0.1	dB

Note

* 33. The passband and stopband frequencies are proportional to fs (sampling rate).
"PB = 0.252 × fs, SB = 0.864 × fs"

■ SRC Block

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

1. Audio Mode (SRCFAUD bit = "1", SRCFEC bit = "0")

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.980 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	-0.01dB	0.900 ≤ FSO/FSI < 0.990	PB	0		0.4167FSI	kHz
	-0.01dB	0.533 ≤ FSO/FSI < 0.909	PB	0		0.2182FSI	kHz
	-0.01dB	0.490 ≤ FSO/FSI < 0.539	PB	0		0.2177FSI	kHz
	-0.01dB	0.450 ≤ FSO/FSI < 0.495	PB	0		0.1948FSI	kHz
	-0.01dB	0.225 ≤ FSO/FSI < 0.455	PB	0		0.1312FSI	kHz
	-0.50dB	0.167 ≤ FSO/FSI < 0.227	PB	0		0.0658FSI	kHz
Stopband		0.980 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
		0.900 ≤ FSO/FSI < 0.990	SB	0.5021FSI			kHz
		0.533 ≤ FSO/FSI < 0.909	SB	0.2974FSI			kHz
		0.490 ≤ FSO/FSI < 0.539	SB	0.2812FSI			kHz
		0.450 ≤ FSO/FSI < 0.495	SB	0.2604FSI			kHz
		0.225 ≤ FSO/FSI < 0.455	SB	0.1802FSI			kHz
		0.167 ≤ FSO/FSI < 0.227	SB	0.0970FSI			kHz
Passband Ripple		0.225 ≤ FSO/FSI ≤ 6.000	PR			±0.01	dB
		0.167 ≤ FSO/FSI < 0.227	PR			±0.50	dB
Stopband Attenuation		0.450 ≤ FSO/FSI ≤ 6.000	SA	95.2			dB
		0.167 ≤ FSO/FSI < 0.455	SA	85.0			dB
Group Delay * 34 (Ts=1/fs)			GD		67 (55/FSI+12/FSO)		Ts

Note

* 34. This value is SRC block only. It is the time from a rising edge of input LRCK after data is input to a rising edge of output LRCK just before the data is output when there is no phase difference between input and output LRCK.

2. Voice Mode (SRCFAUD bit = “0”, SRCFEC bit = “0”)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.980 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	-0.01dB	0.900 ≤ FSO/FSI < 0.990	PB	0		0.4167FSI	kHz
	-0.50dB	0.711 ≤ FSO/FSI < 0.910	PB	0		0.3420FSI	kHz
	-0.50dB	0.653 ≤ FSO/FSI < 0.718	PB	0		0.3007FSI	kHz
	-0.50dB	0.450 ≤ FSO/FSI < 0.660	PB	0		0.2230FSI	kHz
	-0.50dB	0.327 ≤ FSO/FSI < 0.455	PB	0		0.1417FSI	kHz
	-0.50dB	0.225 ≤ FSO/FSI < 0.330	PB	0		0.1018FSI	kHz
	-0.50dB	0.167 ≤ FSO/FSI < 0.227	PB	0		0.0658FSI	kHz
Stopband		0.980 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
		0.900 ≤ FSO/FSI < 0.990	SB	0.5021FSI			kHz
		0.711 ≤ FSO/FSI < 0.910	SB	0.3735FSI			kHz
		0.653 ≤ FSO/FSI < 0.718	SB	0.3320FSI			kHz
		0.450 ≤ FSO/FSI < 0.660	SB	0.2490FSI			kHz
		0.327 ≤ FSO/FSI < 0.455	SB	0.1660FSI			kHz
		0.225 ≤ FSO/FSI < 0.330	SB	0.1248FSI			kHz
		0.167 ≤ FSO/FSI < 0.227	SB	0.0970FSI			kHz
Passband Ripple		0.900 ≤ FSO/FSI ≤ 6.000	PR			±0.01	dB
		0.167 ≤ FSO/FSI ≤ 0.910	PR			±0.50	dB
Stopband Attenuation		0.900 ≤ FSO/FSI ≤ 6.000	SA	95.2			dB
		0.653 ≤ FSO/FSI < 0.909	SA	90.0			dB
		0.450 ≤ FSO/FSI ≤ 0.660	SA	70.0			dB
		0.167 ≤ FSO/FSI < 0.455	SA	60.0			dB
Group Delay * 34 (Ts=1/fs)			GD		67 (55/FSI+12/FSO)		Ts

3. Echo Canceller Mode (SRCFEC bit = “1”)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.167 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
Stopband		0.167 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
Passband Ripple		0.167 ≤ FSO/FSI ≤ 6.000	PR			±0.01	dB
Stopband Attenuation		0.167 ≤ FSO/FSI ≤ 6.000	SA	95.2			dB
Group Delay * 34 (Ts=1/fs)			GD		67 (55/FSI+12/FSO)		Ts

10. DC Characteristics

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage 1 * 35		VIH1	75%TVDD			V
Low-Level Input Voltage 1 * 35		VIL1			25%TVDD	V
High-Level Input Voltage 2 * 36		VIH2	75%VDD33			V
Low-Level Input Voltage 2 * 36		VIL2			25%VDD33	V
SCL, SDA High-Level Input Voltage		VIH3	70%TVDD			V
SCL, SDA Low-Level Input Voltage		VIL3			30%TVDD	V
High-Level Output Voltage Iout= -100μA * 37		VOH1	TVDD-0.3			V
Low-Level Output Voltage Iout=100μA * 37		VOL1			0.3	V
High-Level Output Voltage Iout= -100μA * 38		VOH2	VDD33-0.3			V
Low-Level Output Voltage Iout=100μA * 38		VOL2			0.3	V
SDA Low-Level Output Voltage	Fast Mode					
	TVDD ≥ 2.0V (Iout=3mA)	VOL3			0.4	V
	TVDD < 2.0V (Iout=3mA)	VOL3			20%TVDD	V
	Fast Mode Plus					
	TVDD ≥ 2.0V (Iout=20mA)	VOL3			0.4	V
	TVDD < 2.0V (Iout=3mA)	VOL3			20%TVDD	V
Input Leak Current * 39		Iin			±10	μA
Input Leak Current, Pulled down pins Power Down * 40, * 42		Iid		66		μA
Input Leak Current, Pulled down pins Power Down Release * 41, * 42		Iid		72		μA
Input Leak Current, TESTI pin		Iid		132		μA
Input Leak Current, XTI pin		Iix		17		μA

Notes

* 35. SDIN1, SDIN2/JX0, LRCK1, BICK1, LRCK2/JX1, BICK2/JX2, PDN, SCLK/SCL, CSN and SI/I2CFIL pins. The SCL pin is not included.
* 36. SDIN3/JX3, SDIN4, LRCK3, BICK3, TESTI and XTI pins
* 37. SDOUT1/RDY, STO/RDY/SDOUT2 and SO/SDA pins. The SDA pin is not included.
* 38. SDOUT3/CLKO/GPO1 pin and SDOUT4/GPO2 pin
* 39. Except internal pulled-down pins and the XTI pin.
* 40. When the AK7735 is powered down (PDN pin = “L”), the pull down resistors of LRCK1, BICK1, LRCK2/JX1, BICK2/JX2, LRCK3 and BICK3 pins is 50kΩ (Typ. @3.3V).
* 41. When the AK7735 is powered up (PDN pin = “H”), the pull down resistors of LRCK1, BICK1, LRCK2/JX1, BICK2/JX2, LRCK3 and BICK3 pins is 46kΩ (Typ. @3.3V).
* 42. Leak current in case of inputting 3.3V when LVDD=TVDD=VDD33=3.3V.

11. Switching Characateristics

■ System Clock

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
XTI Input Timing					
a) X'tal Oscillator					
Input Frequency	fXTI	11.2896		18.432	MHz
b) XTI Clock Input					
Duty Cycle		40	50	60	%
Input Frequency	fXTI	0.256		24.576	MHz
CLKO Output Timing					
Output Frequency	fCLKO	2.048		24.576	MHz
Duty Cycle	dCLKO		50		%
LRCK/BICK Input Timing (Slave Mode)					
LRCK Input Timing					
Frequency	fs	8		192	kHz
BICK Input Timing					
Frequency * 43	fBCLK	0.256		24.576	MHz
Pulse Width Low	tBCLKL	0.4 / fBCLK			ns
Pulse Width High	tBCLKH	0.4 / fBCLK			ns
LRCK/BICK Output Timing (PLL Master Mode)					
LRCK Output Timing					
Frequency	fs	8		192	kHz
Pulse Width High PCM Mode Except PCM Mode	 tLRCKH tLRCKH		 1/fBCLK 50		 ns %
BICK Output Timing					
Frequency * 43	fBCLK	0.256		24.576	MHz
Duty	dBCLK		50		%

Note

* 43. Required to meet the following expression: fBCLK ≥ 2 x fs x (Input/Output Data Length).

■ Power Down

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
PDN Pulse Width * 44	tRST	600			ns

Note

* 44. The PDN pin must be "L" when power up the AK7735.

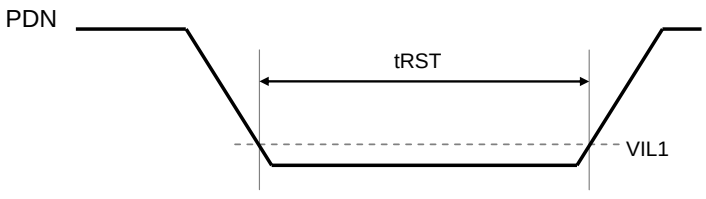


Figure 3. Reset Timing

■ **Serial Data Interface (SDIN1 ~ SDIN4, SDOUT1 ~ SDOUT4)**

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Slave Mode					
Delay Time from BICK "↑" to LRCK * 45	tBLRD	10			ns
Delay Time from LRCK to BICK "↑" * 45	tLRBD	10			ns
Serial Data Input Latch Setup Time	tBSIDS	10			ns
Serial Data Input Latch Hold Time	tBSIDH	5			ns
Delay Time from BICK "↓" to Serial Data Output * 46	tBSOD1			20	ns
Delay Time from BICK "↑"to Serial Data Output * 45, * 47	tBSOD2	5		30	ns
Master Mode					
BICK Frequency	fBCLK		32, 48, 64, 128, 256		fs
BICK Duty Cycle			50		%
Delay Time from BICK "↓" to LRCK * 46	tMBL	-10		10	ns
Serial Data Input Latch Setup Time	tBSIDS	10			ns
Serial Data Input Latch Hold Time	tBSIDH	10			ns
Delay Time from BICK "↓" to Serial Data Output * 46, * 47	tBSOD			10	ns

Notes

* 45. It is measured from BICK "↓" when the BICK polarity is inverted by setting BCKPx bit = "1".
* 46. It is measured from BICK "↑" when the BICK polarity is inverted by setting BCKPx bit = "1".
* 47. Set SDOPHx bit to "1" and the data from SDOUTx pin is output based on BICK "↑" when BICK speed is more than 12.288MHz such as when using TDM256 mode with 96kHz sampling frequency or TDM128 mode with 192kHz sampling frequency in slave mode. SDOPHx bit must be set to "0" in master mode.

1. Slave Mode

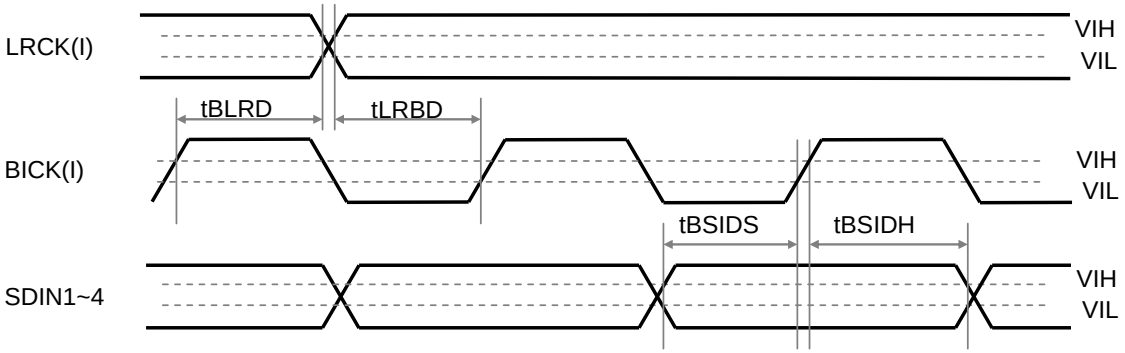


Figure 4. Serial Interface Input Timing in Slave Mode

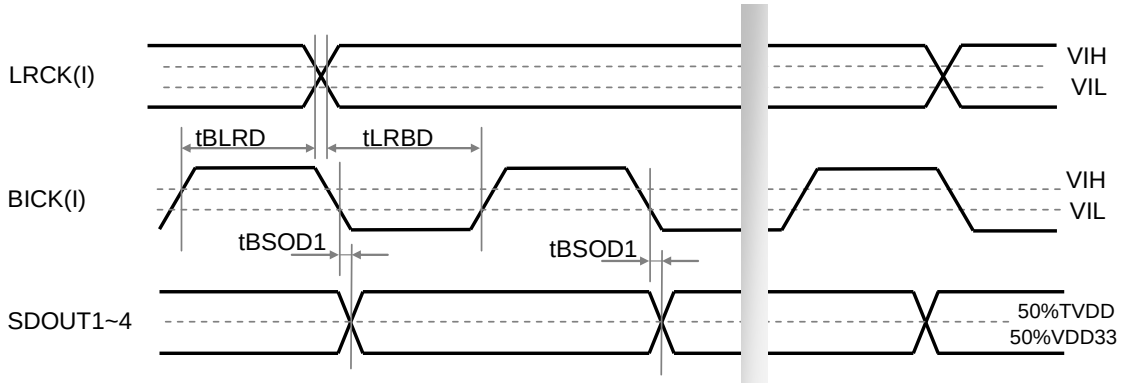


Figure 5. Serial Interface Output Timing in Slave Mode (SDOPHx bit = “0”)

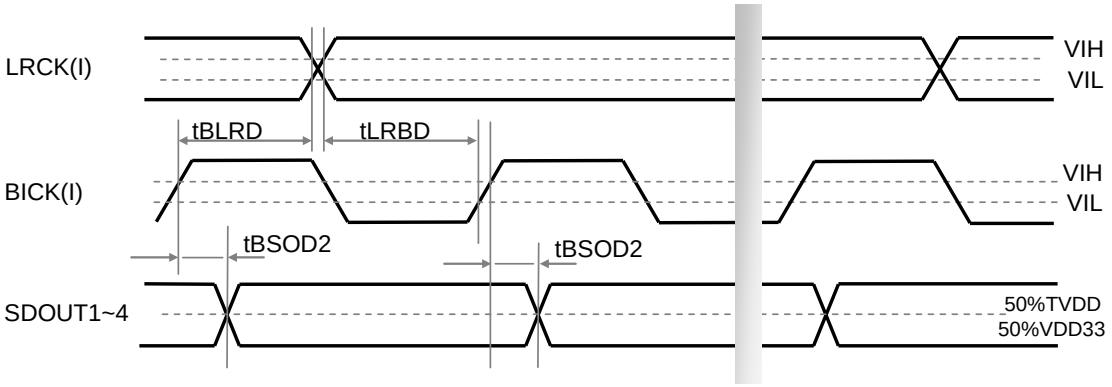


Figure 6. Serial Interface Output Timing in Slave Mode (SDOPHx bit = “1”)

2. Master Mode

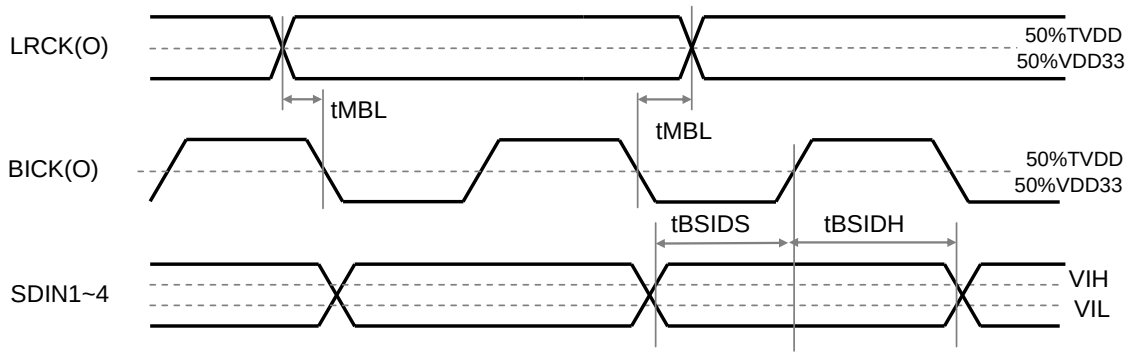


Figure 7. Serial Interface Input Timing in Master Mode

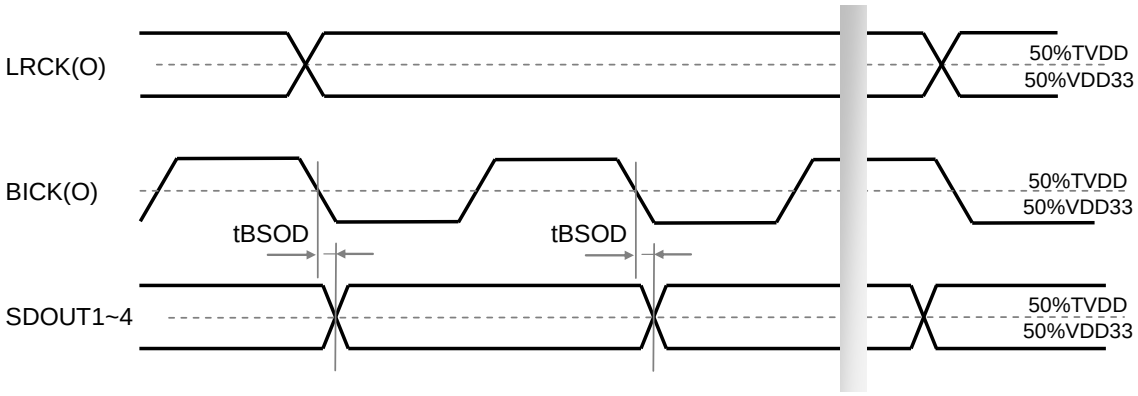


Figure 8. Serial Interface Output Timing in Master Mode (SDOPHx bit = “0”)

■ SPI Interface

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V; C_L=20pF)

1. SPI Low Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
µP Interface Signal					
SCLK Frequency * 49	fSCLK			3.0	MHz
SCLK Low-level Width	tSCLKL	160			ns
SCLK High-level Width	tSCLKH	160			ns
Microcontroller → AK7735					
CSN High-level Width	tWRQH	300			ns
From CSN "↑" to PDN "↑"	tRST	360			ns
From PDN "↑" to CSN "↓"	tIRRQ	1			ms
From CSN "↓" to SCLK "↓"	tWSC	300			ns
From SCLK "↑" to CSN "↑"	tSCW	480			ns
SI Latch Setup Time	tSIS	120			ns
SI Latch Hold Time	tSIH	120			ns
AK7735 → Microcontroller					
Delay Time from SCLK "↓" to SO Output	tSOS			120	ns
SO Output Hold Time from SCLK "↑" * 48	tSOH	120			ns

2. SPI High Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
µP Interface Signal					
SCLK Frequency * 49	fSCLK			6	MHz
SCLK Low-level Width	tSCLKL	72			ns
SCLK High-level Width	tSCLKH	72			ns
Microcontroller → AK7735					
CSN High-level Width	tWRQH	150			ns
From CSN "↑" to PDN "↑"	tRST	180			ns
From PDN "↑" to CSN "↓"	tIRRQ	1			ms
From CSN "↓" to SCLK "↓"	tWSC	150			ns
From SCLK "↑" to CSN "↑"	tSCW	240			ns
SI Latch Setup Time	tSIS	60			ns
SI Latch Hold Time	tSIH	60			ns
AK7735 → Microcontroller					
Delay Time from SCLK "↓" to SO Output	tSOS			60	ns
SO Output Hold Time from SCLK "↑" * 48	tSOH	60			ns

Notes

* 48. Except when writing the 24th bit (8 bits command + 16 bits address) of the command code. This will be the 8th bit (8 bits command) with "write preparation data read command (24H, 25H, 26H and 27H)".

* 49. Dummy command writing for switching to SPI interface from I^2C interface and control register access can always be made in SPI high speed mode (Max. 6MHz). DSP RAM area can be accessed in SPI low speed mode (Max. 3MHz) in clock reset state (CKRESETN bit = "0") and can also be accessed in SPI high speed mode (Max. 6MHz) when PLL is locked (CKRESETN bit = "1" and PLL is locked). It is necessary to set DLRDY bit to "1" when accessing to the DSP RAM area while PLL is unlocked (Figure 47).

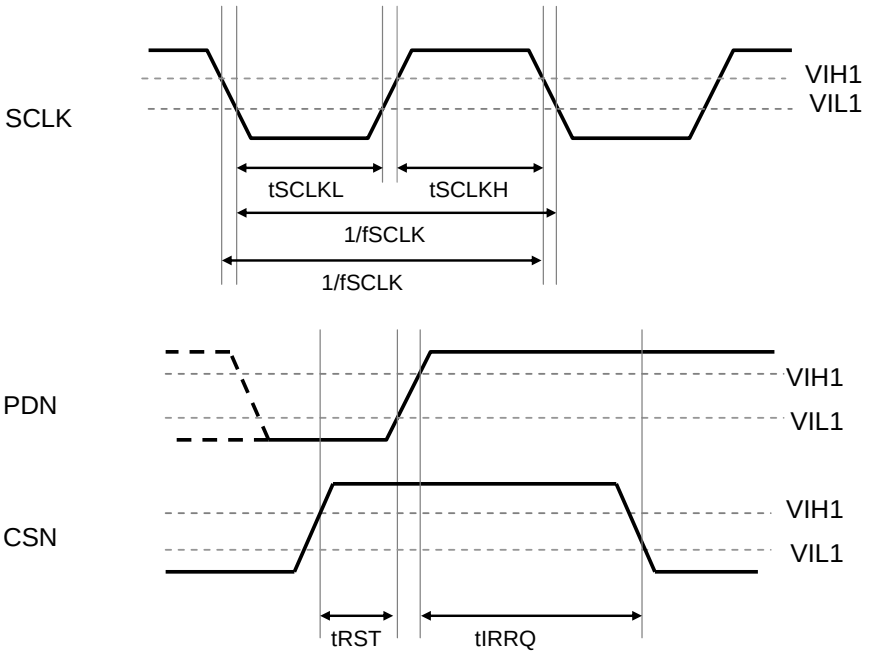


Figure 9. SPI Interface Timing 1

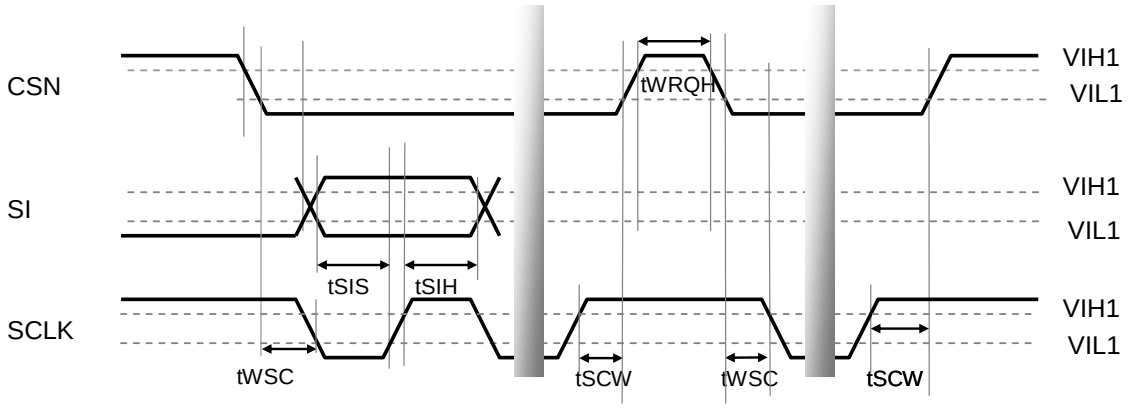


Figure 10. SPI Interface Timing 2 (Microcontroller → AK7735)

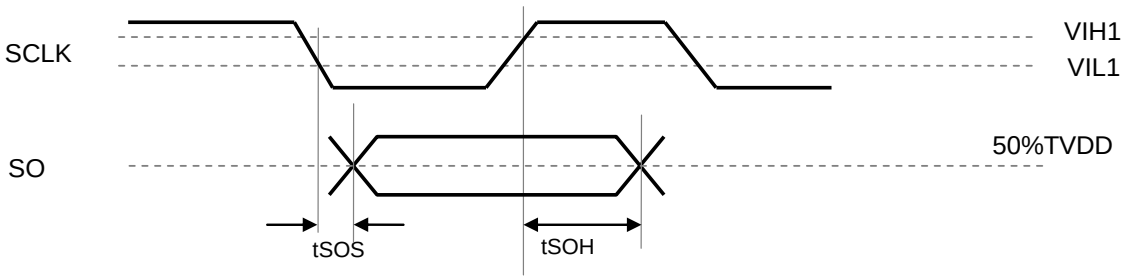


Figure 11. SPI Interface Timing 3 (AK7735 → Microcontroller)

■ I²C Interface

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

1. I²C: Fast Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF

2. I²C: Fast Mode Plus

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL	-	-	1	MHz
Bus Free Time Between Transmissions	tBUF	0.5	-	-	µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.26	-	-	µs
Clock Low Time	tLOW	0.5	-	-	µs
Clock High Time	tHIGH	0.26	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.26	-	-	µs
SDA Hold Time from SCL Falling	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.05	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.12	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.12	µs
Setup Time for Stop Condition	tSU:STO	0.26	-	-	µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	550	pF

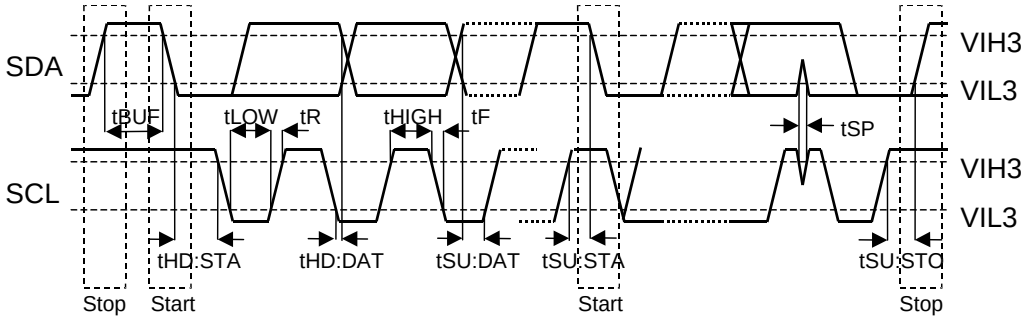


Figure 12. I²C Interface Timing

12. Functional Descriptions

■ System Clock

1. PLL Mode

The AK7735 has a PLL circuit to generate an internal operation clock. An input pin for the PLL reference clock is selected by REFSEL[1:0] bits. REFMODE[4:0] bits set the frequency of the reference clock. A reference clock input pin and the reference clock frequency must be changed during clock reset (CKRESETN bit = "0").

Mode	REFSEL[1:0] bits	Reference Clock Input Pin	Use of Crystal Oscillator	
0	00	XTI	Available	(default)
1	01	BICK1	N/A	
2	10	BICK2	N/A	
3	11	BICK3	N/A	

Table 4. PLL Reference Clock Input Pin Select

Mode	REFMODE[4:0] bits	Input Frequency		
		48kHz base	44.1kHz base	
0	00000	256kHz	235.2kHz	(default)
1	00001	384kHz	352.8kHz	
2	00010	512kHz	470.4kHz	
3	00011	768kHz	705.6kHz	
4	00100	1.024MHz	940.8kHz	
5	00101	1.152MHz	1.0584MHz	
6	00110	1.536MHz	1.4112MHz	
7	00111	2.048MHz	1.8816MHz	
8	01000	2.304MHz	2.1168MHz	
9	01001	3.072MHz	2.8224MHz	
10	01010	4.096MHz	3.7632MHz	
11	01011	4.608MHz	4.2336MHz	
12	01100	6.144MHz	5.6448MHz	
13	01101	8.192MHz	7.5264MHz	
14	01110	9.216MHz	8.4672MHz	
15	01111	12.288MHz	11.2896MHz	(X'tal available)
16	10000	18.432MHz	16.9344MHz	(X'tal available)
17	10001	24.576MHz	22.5792MHz	
Others	N/A	N/A	N/A	

Table 5. PLL Reference Clock Frequency Setting (N/A: Not Available)

The PLL block multiplies an input clock which is set by REFMODE[4:0] bits directly and generates a 147.456MHz/135.4752MHz master clock (PLLMCLK) for internal operation.

Master Clock (PLLMCLK)	48kHz base	44.1kHz base
	147.456MHz	135.4752MHz

Table 6. Internal Operation Master Clock

1-1. XTI Input

When using a crystal oscillator, connect it between XTI pin and XTO pin. Only 11.2896MHz, 12.288MHz, 16.9344MHz and 18.432MHz crystal oscillators are available. When using an external clock, the external clock must be input to the XTI pin and the XTO pin must be open. The XTI pin should also be open when not using XTI input.

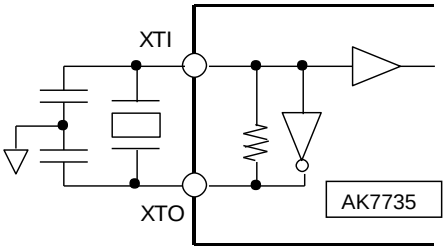


Figure 13. Using Crystal Oscillator

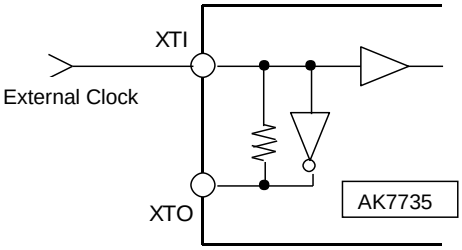


Figure 14. Using External System Clock

1-2. BICK Input

A stable BICK of single frequency is required when using clock input from BICKx (x=1~3) pin as reference clock.

■ Audio HUB

1. Audio HUB

Audio HUB provides simultaneous data transmitting and flexible path configuration for various audio sources by setting sample rate converters, input/output ports that support TDM mode and registers. Therefore the AK7735 is able to support various use cases of audio systems.

2. Definition of Clock Sync Domain

The AK7735 has four Clock Sync Domains (Figure 15). Reference clocks (LRCKSDx, BICKSDx, x=1~4) are output according to each register settings. The internal audio data and input/output data of the AK7735 must be synchronized with one of these four Clock Sync Domains.

When MSNx bit =“0”, clocks from input pins (LRCKx pin/BICKx pin) are selected as reference clock of clock sync domain 1~3. When MSNx bit = “1”, internal dividing clocks (MLRCKx/MBICKx) are selected as reference clock of clock sync domain 1~3. For clock sync domain 4, internal dividing clocks (MBICK4/MLRCK4) are selected as reference clock (BICKSD4/LRCKSD4) (Table 7).

Clock Sync Domain	MSNx bit	Reference Clock
Sync Domain x (x=1 ~ 3)	MSNx = 0	Clocks from Input Pins (BICKx pin/LRCKx pin)
	MSNx = 1	Internal Dividing Clocks (MBICKx/MLRCKx) Reference clock is generated internally by CKSx[2:0], BDVx[9:0] and SDVx[2:0] bits settings.
Sync Domain 4	-	Internal Dividing Clocks (MBICK4/MLRCK4) Reference clock is generated internally by CKS4[2:0], BDV4[9:0] and SDV4[2:0] bits settings.

Table 7. Reference Clock of Clock Sync Domain

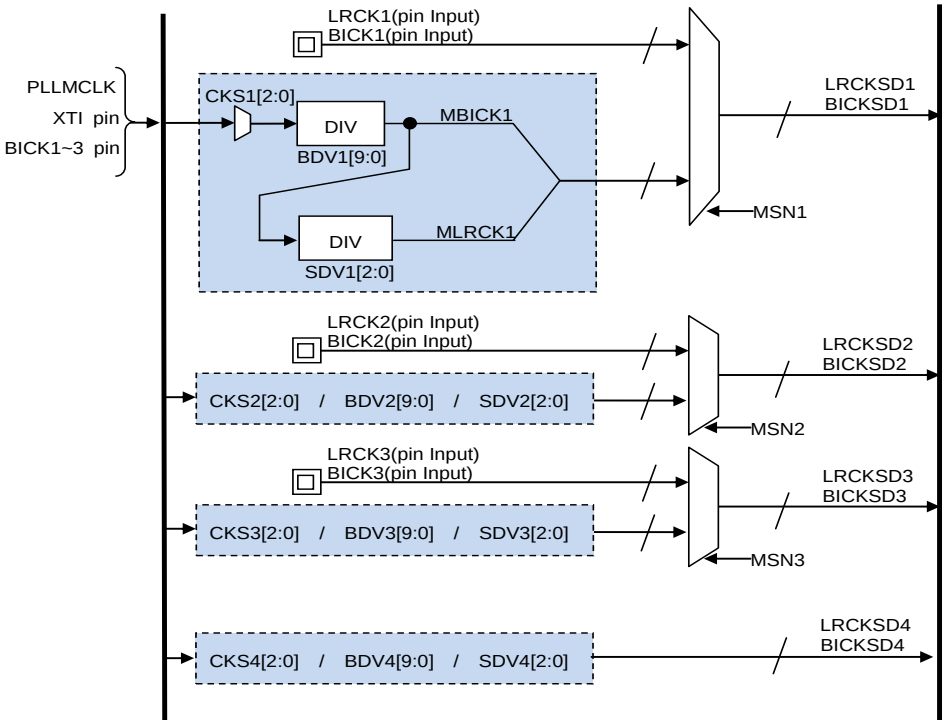


Figure 15. Definition of Clock Sync Domain

The clock source of internal dividing clock MBICKx is selected by CKSx[2:0] bits (Table 8). MBICKx is generated by dividing the selected clock source according to the BDVx[9:0] bits setting (Table 9). Additionally, MLRCKx is generated by dividing this MBICKx according to the SDVx[2:0] bits setting (Table 10).

CKSx[2:0] bits	Clock Source	
000	TieLow	(default)
001	PLLMCLK	
010	XTI pin	
011	BICK1 pin	
100	BICK2 pin	
101	BICK3 pin	
Others	N/A	

Table 8. Clock Source of Internal Dividing Clock (N/A: Not Available)

BDVx[9:0] bits	Divide by	
0x000	1	(default)
0x001 – 0x1FF	BDVx+1	

Table 9. MBICKx Setting

SDVx[2:0] bits	Divide by	
000	64	(default)
001	48	
010	32	
011	128	
100	256	
Others	N/A	

Table 10. MLRCKx Setting (N/A: Not Available)

Clock Sync Domain settings when PLLMCLK is selected as the clock source are shown in Table 11. When PLLMCLK is selected as the clock source, frequency settings other than shown in Table 11 are not available. Reference clocks for each setting are calculated as below.

PLLMCLK = 147.456MHz (48kHz base)/ 135.4752MHz (44.1kHz base)
MBICKx = PLLMCLK divided by BDVx[9:0] bits setting
MLRCKx = MBICKx divided by SDVx[2:0] bits setting

ex) When PLLMCLK = 147.456MHz, BDVx[9:0] bits = 0x02F(divide by 48) and SDVx[2:0] bits = “000”(divide by 64), MBICKx = 147.456MHz/48 = 3.072MHz, MLRCKx = 3.072MHz/64 = 48kHz.

BDVx[9:0] bits	MBICKx Dividing	MBICKx(MHz)		SDVx[2:0] bits	MLRCKx Dividing	MLRCKx(kHz)	
		48kHz Base	44.1kHz Base			48kHz Base	44.1kHz Base
0x23F	576	0.256	0.2352	010	32	8	N/A
0x17F	384	0.384	0.3528	001	48	8	N/A
0x11F	288	0.512	0.4704	000	64	8	N/A
0x08F	144	1.024	0.9408	011	128	8	N/A
0x047	72	2.048	1.8816	100	256	8	N/A
0x17F	384	0.384	0.3528	010	32	12	11.025
0x0FF	256	0.576	0.5292	001	48	12	11.025
0x0BF	192	0.768	0.7056	000	64	12	11.025
0x05F	96	1.536	1.4112	011	128	12	11.025
0x02F	48	3.072	2.8224	100	256	12	11.025
0x11F	288	0.512	0.4704	010	32	16	14.7
0x0BF	192	0.768	0.7056	001	48	16	14.7
0x08F	144	1.024	0.9408	000	64	16	14.7
0x047	72	2.048	1.8816	011	128	16	14.7
0x023	36	4.096	3.7632	100	256	16	14.7
0x0BF	192	0.768	0.7056	010	32	24	22.05
0x07F	128	1.152	1.0584	001	48	24	22.05
0x05F	96	1.536	1.4112	000	64	24	22.05
0x02F	48	3.072	2.8224	011	128	24	22.05
0x017	24	6.144	5.6448	100	256	24	22.05
0x08F	144	1.024	0.9408	010	32	32	29.4
0x05F	96	1.536	1.4112	001	48	32	29.4
0x047	72	2.048	1.8816	000	64	32	29.4
0x023	36	4.096	3.7632	011	128	32	29.4
0x011	18	8.192	7.5264	100	256	32	29.4
0x05F	96	1.536	1.4112	010	32	48	44.1
0x03F	64	2.304	2.1168	001	48	48	44.1
0x02F	48	3.072	2.8224	000	64	48	44.1
0x017	24	6.144	5.6448	011	128	48	44.1
0x00B	12	12.288	11.2896	100	256	48	44.1
0x02F	48	3.072	2.8224	010	32	96	88.2
0x01F	32	4.608	4.2336	001	48	96	88.2
0x017	24	6.144	5.6448	000	64	96	88.2
0x00B	12	12.288	11.2896	011	128	96	88.2
0x005	6	24.576	22.5792	100	256	96	88.2
0x017	24	6.144	5.6448	010	32	192	176.4
0x00F	16	9.216	8.4672	001	48	192	176.4
0x00B	12	12.288	11.2896	000	64	192	176.4
0x005	6	24.576	22.5792	011	128	192	176.4

Table 11. Clock Sync Domain Setting when PLLMCLK is Clock Source (N/A: Not Available)

For Clock Sync Domain, set BDVx[9:0] bits and SDVx[2:0] bits according to the input clock frequency when the XTI or BICK pin input is selected as the clock source, as well as the PLLMCLK.

MBICKx = XTI pin or BICKx pin frequency divided by BDVx[9:0] bits setting
MLRCKx = MBICKx divided by SDVx[2:0] bits setting

3. Sampling Frequency Setting of ADC and DAC Blocks

Available sampling modes for analog block of the AK7735 are shown below. Sampling frequency mode is set by FSMODE[4:0] bits. ADC1 can be operated by a different sampling frequency from ADC2, DAC1 and DAC2.

Mode	FSMODE[4:0] bits	ADC2, DAC1, DAC2	ADC1	
0	00000	8kHz	8kHz	(default)
1	00001	12kHz	12kHz	
2	00010	16kHz	16kHz	
3	00011	24kHz	24kHz	
4	00100	32kHz	32kHz	
5	00101	32kHz	16kHz	
6	00110	32kHz	8kHz	
7	00111	48kHz	48kHz	
8	01000	48kHz	24kHz	
9	01001	48kHz	16kHz	
10	01010	48kHz	8kHz	
11	01011	96kHz	96kHz	
12	01100	96kHz	48kHz	
13	01101	96kHz	32kHz	
14	01110	96kHz	24kHz	
15	01111	96kHz	16kHz	
16	10000	96kHz	8kHz	
17	10001	192kHz	192kHz	
18	10010	192kHz	96kHz	
19	10011	192kHz	48kHz	
20	10100	192kHz	32kHz	
21	10101	192kHz	16kHz	
Others	N/A	N/A	N/A	

Table 12. Sampling Frequency Settings of ADC and DAC Blocks (fs=48kHz base, N/A: Not Available)

Clock Sync Domain of the ADC1 (SDADC1) is selected by SDADC1[2:0] bits and Clock Sync Domain of the ADC2, DAC1 and DAC2 (SDCODEC) is selected by SDCODEC[2:0] bits (Table 18).
The sampling frequency of LRCKSDx for SDADC1 and the sampling frequency of the ADC1 should be the same. The sampling frequency of LRCKSDx for SDCODEC and the sampling frequency of the ADC2, DAC1 and DAC2 should also be the same. SDADC1 and SDCODEC must be synchronized with PLLMCLK.

Set SDADC1[2:0] bits to “000” (reference clock is fixed to “L”) when not using the ADC1. In the same manner, SDCODEC[2:0] bits should be set to “000” when not using the ADC2, DAC1 and DAC2.

4. Master Clock Output Setting

The master clock output frequency setting of the CLKO pin is controlled by CLKOSEL[2:0] bits.

Mode	CLKOSEL[2:0] bits	Output Frequency (fs=48kHz base)	Output Frequency (fs=44.1kHz base)	
0	000	12.288MHz	11.2896MHz	(default)
1	001	24.576MHz	22.5792MHz	
2	010	8.192MHz	7.5264MHz	
3	011	6.144MHz	5.6448MHz	
4	100	4.096MHz	3.7632MHz	
5	101	2.048MHz	1.8816MHz	
others	N/A	N/A	N/A	

Table 13. CLKO Output Frequency Setting (N/A: Not Available)

5. SDINx/BICKx/LRCKx pin Setting

The AK7735 has three BICK/LRCK pins and they are independent each other.
MSNx bit selects Master/Slave mode setting of the BICKx pin and the LRCKx pin (x=1~3). (Table 14)

MSNx bit (x=1~3)	BICKx pin, LRCKx pin	
0	Slave Mode (Input)	(default)
1	Master Mode (Output)	

Table 14. BICKx/LRCKx Pin Mode Selection

Note
* 50. Set MSNx bit to “0” when using the BICKx pin as PLL reference clock input pin.

When BICKx/LRCKx (x=1~3) pins are set to slave mode, the reference clocks of Clock Sync Domain x are the clocks from BICKx/LRCKx pins (Table 7). When BICKx/LRCKx pins are set to master mode, the output clocks of the BICKx/LRCKx pins can be selected from four Sync Domains by SDBCKx[2:0] bits (x= 1~3). (Table 15)

MSNx bit	SDBCKx[2:0] bits	BICKx pin/LRCKx pin	
1	000	TieLow	(default)
1	001	BICKSD1, LRCKSD1	
1	010	BICKSD2, LRCKSD2	
1	011	BICKSD3, LRCKSD3	
1	100	BICKSD4, LRCKSD4	
1	Others	N/A	

Table 15. Clock Sync Domain Setting of BICKx/LRCKx Pins in Master Mode (N/A: Not Available)

Note
***** 51. SDBCKx[2:0] bits can be in the default setting “000” (TIeLow) when BICKx pin/LRCKx pin (x=1~3) are in slave mode.

The AK7735 has four serial data input ports (SDINx pin). Synchronizing clock of SDINx pin can be selected from three BICKx/LRCKx pins by EXBCKx[1:0] bits.

EXBCKx[1:0] bits	BICK/LRCK Synchronizing with SDINx Pin	
00	TieLow	(default)
01	BICK1 pin, LRCK1 pin	
10	BICK2 pin, LRCK2 pin	
11	BICK3 pin, LRCK3 pin	

Table 16. BICK/LRCK Setting Synchronizing with SDINx Pin

6. Clock Sync Domain Setting of DSP

Clock sync domain of DSP1 is selected by SDDSP1[2:0] bits. The DSP1 input port inherits the sync domain of the input data. Clock sync domain of the output ports are set by SDDSP1O1[2:0] ~ SDDSP1O6[2:0] bits.

Clock sync domain of DSP2 is selected by SDDSP2[2:0] bits. The DSP2 input port inherits the sync domain of the input data. Clock sync domain of the output ports are set by SDDSP2O1[2:0] ~ SDDSP2O6[2:0] bits.

	DSP's Sync Domain	Input Port Sync Domain	Output Port Sync Domain
DSP1	SDDSP1[2:0] bits	Inherit the Sync Domain of Input data	Set by SDDSP1O1[2:0] bits ~ SDDSP1O6[2:0] bits
DSP2	SDDSP2[2:0] bits	Inherit the Sync Domain of Input data	Set by SDDSP2O1[2:0] bits ~ SDDSP2O6[2:0] bits

Table 17. Sync Domain Setting of DSP

Note
* 52. The sync domains of Input/Output ports should synchronize with the sync domain of DSP.

■ Audio Data Path Setting

1. Data Bus, In/Output Port

The AK7735 has a 32-bit serial audio stereo data bus (Figure 17). Inputs and outputs of each internal block and all input/output pins of the AK7735 are connected to this serial audio data bus. The port that data is input to this serial audio data bus is defined as “input port” and the port that data is output from the audio data bus is defined as “output port”. Each port selects Clock Sync Domain and inputs (outputs) audio data that synchronized to the reference clock of the Clock Sync domain to the data bus (Figure 17).

A stereo data on each port is defined as “data source”. All data sources are connected to the serial audio bus and a data source on any input port can be output to any output port. Data connection of the input port and the output port with the same sampling frequency via data bus is defined as “data path”. Input and output ports on the same data path should have the same Clock Sync Domain. If these ports have different Clock Sync Domains, reference clocks (BICKSDx, LRCKSDx) must be synchronized and the sampling frequency of LRCKSDx must be the same. However, phase synchronization of reference clocks is not necessary and frequencies of BICKSDx can be different.

An SRC is necessary for data transmission between two ports that have clock sync domain with different sampling frequencies or asynchronous reference clocks.

e.g.) Data Path Example (Figure 16)

It is an example of outputting data from the DAC1 after converting fs=8kHz input data from the SDIN1 pin to fs=48kHz by SRC. Path 1 is defined from the SDIN1 pin to SRC1. Path2 is defined from SRC1 to DAC1. Set the same clock sync domain for data ports of the Path1 (SDIN1 input and SRC1 output ports), and for the data ports of the Path2 (SRC1 input port and DAC1), independently.

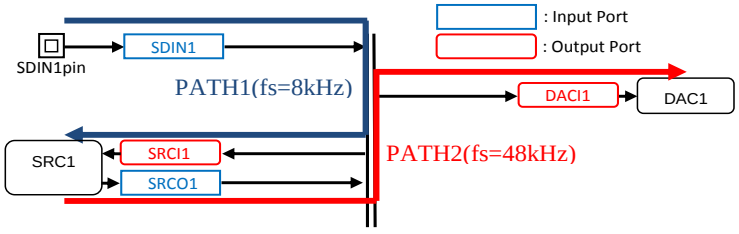


Figure 16. Data Path Example

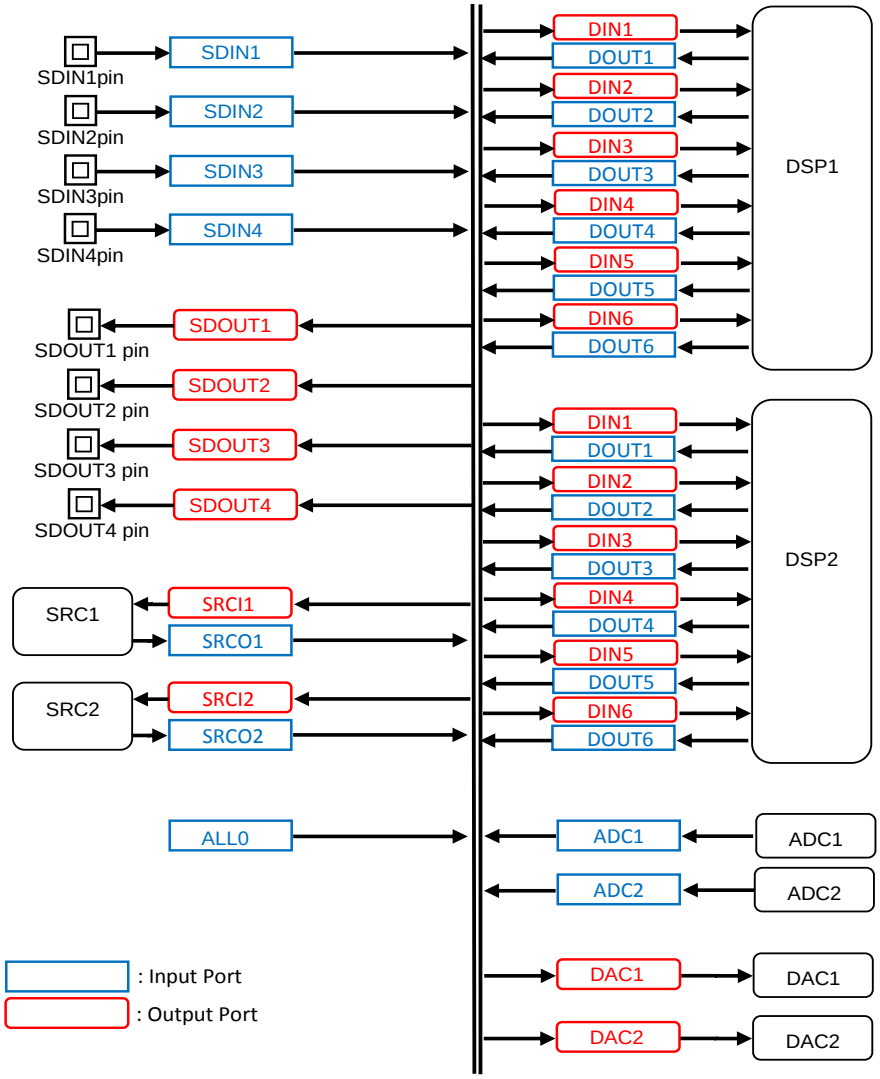


Figure 17. AK7735 Audio Data Path

2. Data Bus Group Delay

When the input and output ports with the same sampling frequency are connected via data bus, group delay of 2/fs occurs in total as audio data will have 1/fs group delay at each input and output port of the data bus (fs is the sampling frequency of the sync domain of the input and output ports).
Therefore, this group delay will increase as the number of times that the data goes through the data path increases.

In the example of Figure 16, 2/fs (fs=8kHz) group delay occurs when inputting the SDIN1 data to SRC via data bus and another 2/fs (fs=48kHz) group delay occurs when inputting the SRC1 output data to DAC1 via data bus.

3. Clock Sync Domain Setting of Input/output Port

Domain numbers are assigned to each Clock Sync Domain (Table 18). Each input/output port has setting registers for Clock Sync Domain (Figure 20). Set a domain number to clock sync domain setting registers for each input/output port. (Table 19, Table 20)

Domain Number	Clock Sync Domain
0x0	TieLow
0x1	LRCKSD1, BICKSD1 (SD1)
0x2	LRCKSD2, BICKSD2 (SD2)
0x3	LRCKSD3, BICKSD3 (SD3)
0x4	LRCKSD4, BICKSD4 (SD4)

Table 18. Clock Sync Domain Number

If the output port sync domain setting is in auto mode, the output port inherits the sync domain of the input data.

e.g.) Data Path Example
It is an example of outputting data from the DAC1 after converting fs=8kHz input data from the SDIN1 pin to fs=48kHz by SRC (Figure 16). The output port of SRC1 is in auto mode. Therefore the output port inherits the clock sync domain of SDIN1 input port.

Clock Sync Domain of the SDINx pin is automatically selected by setting EXBCKx[1:0] bits, MSN bit and SDBCKx[2:0] bits (Table 15, Table 16).

e.g.) Clock sync domain 3 is selected for the SDIN2 pin when EXBCK2[1:0] bits = “011” and MSN3 bit =“0” (Figure 18).

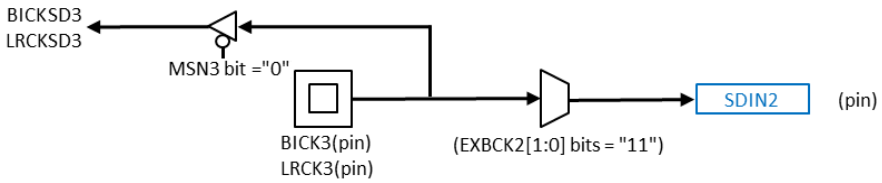


Figure 18. Clock Sync Domain Setting Example1 of SDINx Pin

e.g.) Clock sync domain 3 is selected for the SDIN1 pin when EXBCK1[1:0] bits = “001”, MSN2 bit =“1” and SDBCK2[2:0] bits = “011” (Figure 19).

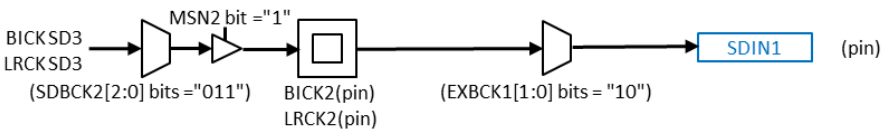


Figure 19. S Clock Sync Domain Setting Example2 of SDINx Pin

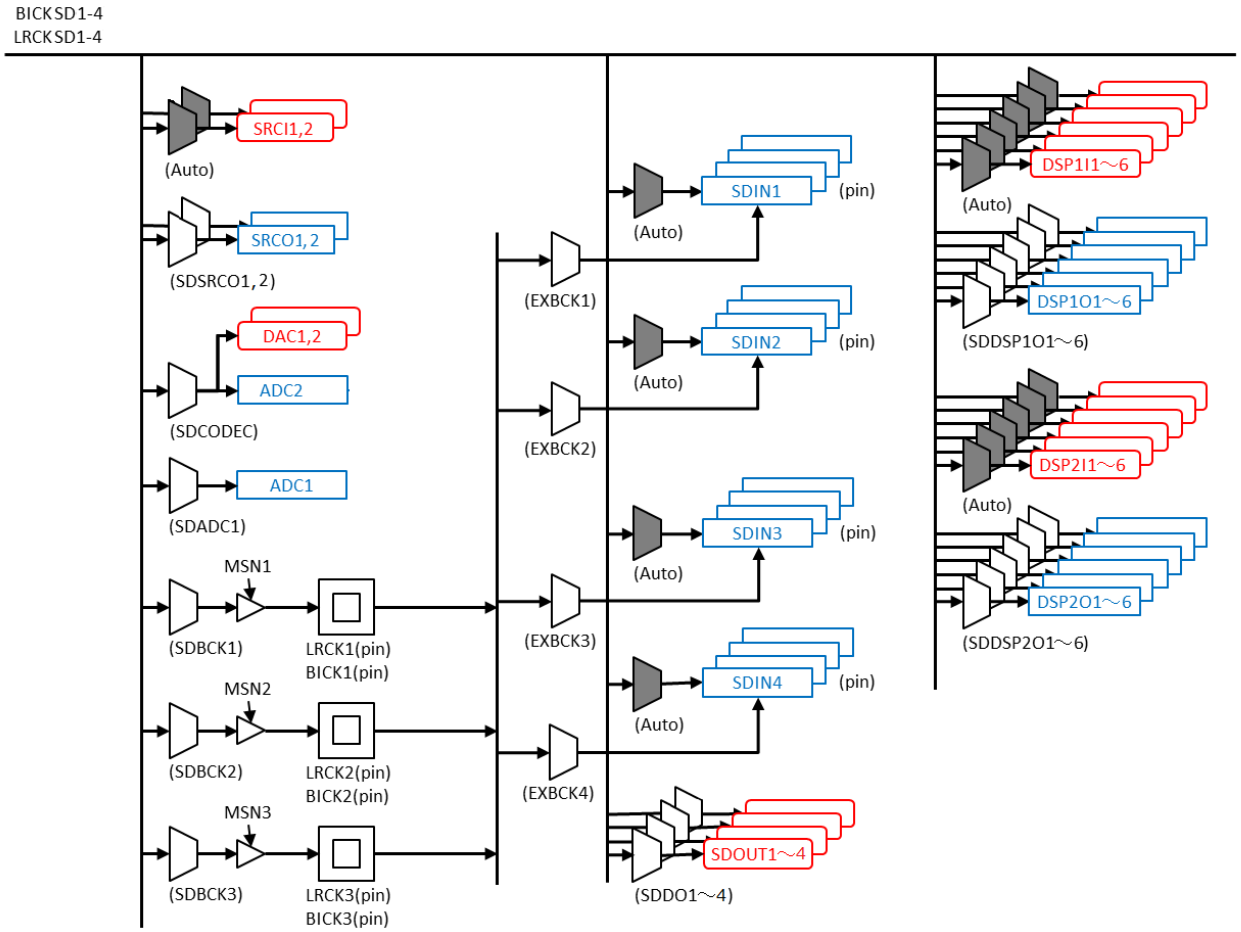


Figure 20. Clock Sync Domain Setting

4. Source Address, Source Selecting Registers

A source address is assigned to each input port source (Table 19). The output port can select any input port source by setting a source address to the source select register.

Source Address	Source Name	Source Contents	Input Port	Clock Sync Domain Setting Register
0x00	ALL0	0x0000 0000 fixed	ALL0	* 53
0x01	SDIN1 SDIN1A	SDIN1 (pin) Input TDMI1 Slot1, 2 Input	SDIN1	* 54
0x02	SDIN1B	TDMI1 Slot3, 4 Input		
0x03	SDIN1C	TDMI1 Slot5, 6 Input		
0x04	SDIN1D	TDMI1 Slot7, 8 Input		
0x05	SDIN2 SDIN2A	SDIN2 (pin) Input TDMI2 Slot1, 2 Input	SDIN2	* 54
0x06	SDIN2B	TDMI2 Slot3, 4 Input		
0x07	SDIN2C	TDMI2 Slot5, 6 Input		
0x08	SDIN2D	TDMI2 Slot7, 8 Input		
0x09	SDIN3 SDIN3A	SDIN3 (pin) Input TDMI3 Slot1, 2 Input	SDIN3	* 54
0x0A	SDIN3B	TDMI3 Slot3, 4 Input		
0x0B	SDIN3C	TDMI3 Slot5, 6 Input		
0x0C	SDIN3D	TDMI3 Slot7, 8 Input		
0x0D	SDIN4 SDIN4A	SDIN4 (pin) Input TDMI4 Slot1, 2 Input	SDIN4	* 54
0x0E	SDIN4B	TDMI4 Slot3, 4 Input		
0x0F	SDIN4C	TDMI4 Slot5, 6 Input		
0x10	SDIN4D	TDMI4 Slot7, 8 Input		
0x11	DOUT101	DSP1 Output 1	DOUT101	SDDSP1O1[2:0]
0x12	DOUT102	DSP1 Output 2	DOUT102	SDDSP1O2[2:0]
0x13	DOUT103	DSP1 Output 3	DOUT103	SDDSP1O3[2:0]
0x14	DOUT104	DSP1 Output 4	DOUT104	SDDSP1O4[2:0]
0x15	DOUT105	DSP1 Output 5	DOUT105	SDDSP1O5[2:0]
0x16	DOUT106	DSP1 Output 6	DOUT106	SDDSP1O6[2:0]
0x17	DOUT201	DSP2 Output 1	DOUT201	SDDSP2O1[2:0]
0x18	DOUT202	DSP2 Output 2	DOUT202	SDDSP2O2[2:0]
0x19	DOUT203	DSP2 Output 3	DOUT203	SDDSP2O3[2:0]
0x1A	DOUT204	DSP2 Output 4	DOUT204	SDDSP2O4[2:0]
0x1B	DOUT205	DSP2 Output 5	DOUT205	SDDSP2O5[2:0]
0x1C	DOUT206	DSP2 Output 6	DOUT206	SDDSP2O6[2:0]
0x1D	ADC1	ADC1 Output	ADC1	SDADC1[2:0]
0x1E	ADC2	ADC2 Output	ADC2	SDCODEC[2:0]
0x1F	SRCO1	SRC1 Output	SRCO1	SDSRCO1[2:0]
0x20	SRCO2	SRC2 Output	SRCO2	SDSRCO2[2:0]
Others	N/A	N/A	N/A	N/A

Table 19. Source Addresses of Input Ports (N/A: Not Available)

Source Select Registers	Contents	Output Port	Clock Sync Domain Setting Register
SELDO1A[5:0]	SDOUT1(pin) Output TDMO1 Slot1, Slot2	SDOUT1	SDDO1[2:0]
SELDO1B[5:0]	TDMO1 Slot3, Slot4		
SELDO1C[5:0]	TDMO1 Slot5, Slot6		
SELDO1D[5:0]	TDMO1 Slot7, Slot8		
SELDO2A[5:0]	SDOUT2(pin) Output TDMO2 Slot1, Slot2	SDOUT2	SDDO2[2:0]
SELDO2B[5:0]	TDMO2 Slot3, Slot4		
SELDO2C[5:0]	TDMO2 Slot5, Slot6		
SELDO2D[5:0]	TDMO2 Slot7, Slot8		
SELDO3A[5:0]	SDOUT3(pin) Output TDMO3 Slot1, Slot2	SDOUT3	SDDO3[2:0]
SELDO3B[5:0]	TDMO3 Slot3, Slot4		
SELDO3C[5:0]	TDMO3 Slot5, Slot6		
SELDO3D[5:0]	TDMO3 Slot7, Slot8		
SELDO4A[5:0]	SDOUT4(pin) Output TDMO4 Slot1, Slot2	SDOUT4	SDDO4[2:0]
SELDO4B[5:0]	TDMO4 Slot3, Slot4		
SELDO4C[5:0]	TDMO4 Slot5, Slot6		
SELDO4D[5:0]	TDMO4 Slot7, Slot8		
SELDA1[5:0]	DAC1 Input	DAC1	SDCODEC[2:0]
SELDA2[5:0]	DAC2 Input	DAC2	
D1SELDI1[5:0]	DSP1 Input 1	DIN101	(Auto)
D1SELDI2[5:0]	DSP1 Input 2	DIN102	(Auto)
D1SELDI3[5:0]	DSP1 Input 3	DIN103	(Auto)
D1SELDI4[5:0]	DSP1 Input 4	DIN104	(Auto)
D1SELDI5[5:0]	DSP1 Input 5	DIN105	(Auto)
D1SELDI6[5:0]	DSP1 Input 6	DIN106	(Auto)
D2SELDI1[5:0]	DSP2 Input 1	DIN201	(Auto)
D2SELDI2[5:0]	DSP2 Input 2	DIN202	(Auto)
D2SELDI3[5:0]	DSP2 Input 3	DIN203	(Auto)
D2SELDI4[5:0]	DSP2 Input 4	DIN204	(Auto)
D2SELDI5[5:0]	DSP2 Input 5	DIN205	(Auto)
D2SELDI6[5:0]	DSP2 Input 6	DIN206	(Auto)
SELSRCI1[5:0]	SRC1 Input	SRCI1	(Auto)
SELSRCI2[5:0]	SRC2 Input	SRCI2	(Auto)

Table 20. Source Select Registers of Output Ports

Notes

* 53. If the output port source is changed to ALL0 when the clock sync domain setting is “Auto”, the clock sync domain before changing the data source will be kept. This clock sync domain should not be stopped immediately after changing the data source otherwise the output data will not become ALL0 correctly.
* 54. Clock Sync Domain of the SDINx pin is automatically selected by setting EXBCKx[1:0] bits, MSNx bit and SDBCKx[2:0] bits (Table 14, Table 15, Table 16).
* 55. SDINxB~D are only valid in TDM mode. These ports are fixed to “0” if it is not in TDM mode.
* 56. Input data to the input port 1~6 of the DSP must be selected from a data based on a clock sync domain which is synchronized with PLLMCLK.

5. Input/Output Serial Interface Format

5-1. Data Clocks

The AK7735 has three LRCK/BICK pins that are input/output switchable to interface with external equipment. MSNx bit controls master and slave modes of LRCKx/BICKx pins (Table 14). DCFx[2:0] bits control each clock format of these pins independently. If LRCKx/BICKx pins are configured as slave mode, set DCFx[2:0] bits according to the input clock. If LRCKx/BICKx pins are configured as master mode, the output clock format is selected by DCFx[2:0] bits.

Mode	DCFx[2]	DCFx[1]	DCFx[0]	Clock Format	
0	0	0	0	I^2S Mode	(default)
1	1	0	1	DSP Mode	
2	1	1	0	PCM Short Frame	
3	1	1	1	PCM Long Frame	

Table 21. AK7735 Data Clock Format

BCKPx bit controls the relationship of BICKx and LRCKx edges.

BCKPx bit	BICKx edge referenced to LRCKx start edge	
0	Falling Edge	(default)
1	Rising Edge	

Table 22. Relationship of BICKx and LRCKx Edges

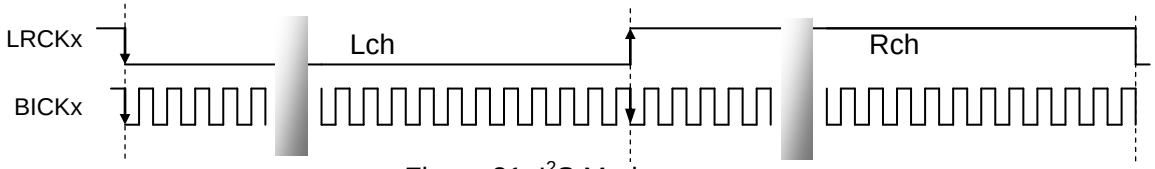


Figure 21. I^{2}S Mode

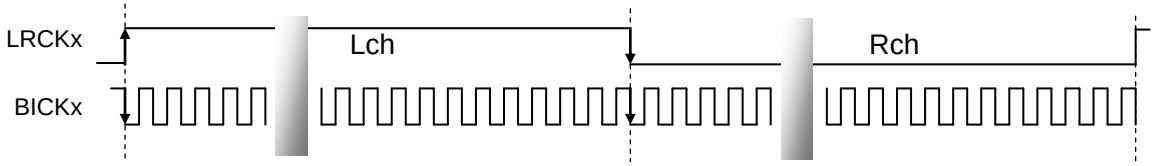


Figure 22. DSP Mode

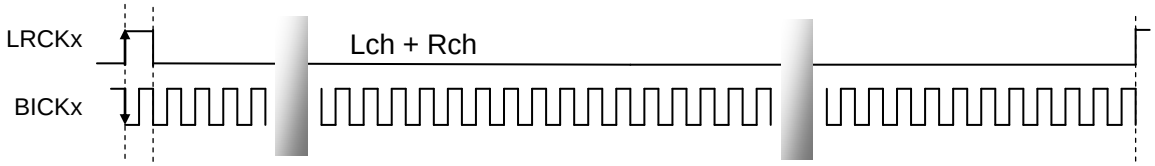


Figure 23. PCM Short Frame / PCM Long Frame (BCKPx bit = “0”)

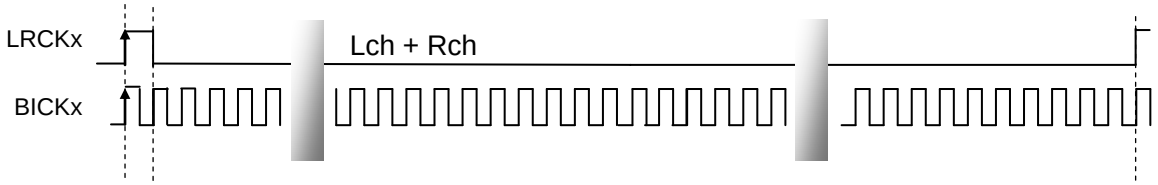


Figure 24. PCM Short Frame / PCM Long Frame (BCKPx bit = “1”)

5-2. Data Definitions

A serial bit stream that is sent or received by the AK7735 is a long sequence composed of “1” and “0”. This data sequence has hierarchical levels of slot, word and bit.

Bit: It is a smallest component in a serial data stream. The bit duration is one serial clock cycle.

Word: It is a group of multiple bits that composes transmitting data between external devices and the AK7735. Figure 25 shows an example of a word consists of eight bits.

Slot: It is composed of a word and adequate additional bits for interfacing to an external device. In Figure 25, the audio data is an 8-bit valid data and a 12-bit slot needs additional four zeroes to satisfy an interface protocol of the external device.
If the word length is shorter than the slot length, the data alignment of the word will be the beginning of the slot (MSB justified) or end of the slot (LSB justified). Figure 25 shows an example of MSB justified format.

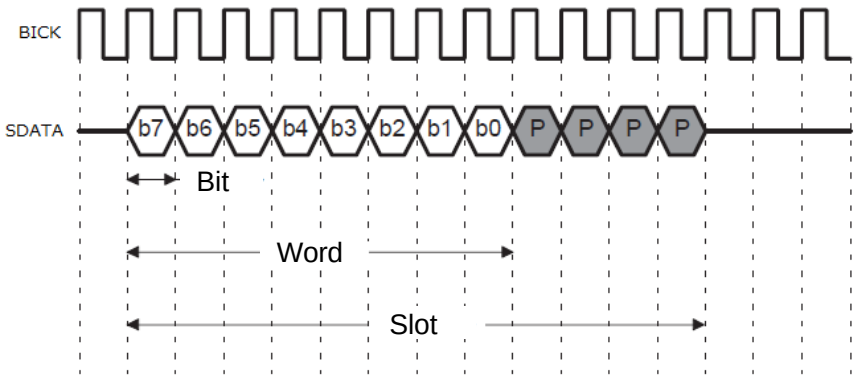


Figure 25. Bit, Word and Slot Definitions

5-3. Input/ Output Interface Format

The AK7735 has four digital input ports and four digital output ports. The data format can be set independently.
The input data format is determined by a combination of DISLx[1:0], DIEDGENx, DILSBEx and DIDLx[1:0] bits settings (x=1~4). The output data format is determined by a combination of DOSLx[1:0], DOEDGENx, DOLSBEx and DODLx[1:0] bits settings (x=1~4).

DISLx[1:0] bits / DOSLx[1:0] bits (x=1~4) control input/output data slot length.

Mode	DISLx[1] bit DOSLx[1] bit	DISLx[0] bit DOSLx[0] bit	Slot Length	
0	0	0	24bit	(default)
1	0	1	20bit	
2	1	0	16bit	
3	1	1	32bit	

Table 23. Slot Length Setting of Input/Output Data

DIDLx[1:0] bits / DODLx[1:0] bits (x=1~4) control input/output audio data word length.

Mode	DIDLx[1] bit DODLx[1] bit	DIDLx[0] bit DODLx[0] bit	Word Length	
0	0	0	24bit	(default)
1	0	1	20bit	
2	1	0	16bit	
3	1	1	32bit	

Table 24. Word Length Setting of Input/Output Audio Data

DILSBEx bit/ DOLSBEx bit (x=1~4) select the audio data format of a slot.

DILSBEx bit DOLSBEx bit	Slot Data Format	
0	MSB First	(default)
1	LSB First	

Table 25. Slot Data Format Setting

DIEDGENx bit / DOEDGENx bit (x=1~4) select data transmission start timing of the data after second channel

DIEDGENx bit DOEDGENx bit	Start Timing	
0	LRCK Edge Basis	(default)
1	Slot Length Basis	

Table 26. Data Transmission Start Timing Selection of The Data After Second Channel

If the data transmitting timing is set to Slot length basis, the next channel's data is transmitted immediately without waiting a LRCK edge after transmitted one slot data (Figure 29~ Figure 33).
If the data transmitting timing is set to LRCK edge basis, the next channel's data will not be transmitted until a LRCK edge even finished transmitting one slot data (Figure 26 ~ Figure 28).

5-3-1. Stereo Mode

AK7735 supports stereo mode. The BICKx pin should be set to arbitrary frequency more than “word length x 2fs” when DIEDGENx bit = “0”. The BICKx pin should be set to arbitrary frequency more than “slot length x 2fs” when DIEDGENx bit = “1”. BICK clock is supported up to 256fs (Max.24.576MHz).

The SDINx input pins of the AK7735 support stereo input mode. Two slots data input is available for each pin. A source address is assigned to each SDINx input pin when using stereo input mode (Table 19). DISLx[1:0] bits control input data slot length of the SDINx pin. DIDLx[1:0] bits control the input data word length of the SDINx pin. The slot data format is set by DILSBEx bit.
In stereo mode, DIEDGENx bit should be set to “0” if the data transmission timing of second channel is LRCK edge basis. In this case, DISLx[1:0] bits setting are ignored.

The SDOUTx output pins of the AK7735 support stereo output mode. Two slots data output is available for each pin. Each slot data can be assigned by setting SELDOxA[5:0] bits. DOSLx[1:0] bits control output data slot length of the SDOUTx pin. DODLx[1:0] bits control the output data word length of the SDOUTx pin. The slot data format is set by DOLSBEx bit.
In stereo mode, DOEDGENx bit must be set to “0” if the data transmission timing of second channel is LRCK edge basis. In this case, DOSLx[1:0] bits setting are ignored.

Setting example of stereo mode is shown in Table 27.

Mode	Data Format	DCFx[2:0]	DILSBEx DOLSBEx	DIEDGENx DOEDGENx	DISLx[1:0] DOSLx[1:0]	DIDLx[1:0] DODLx[1:0]
0	I^2S Compatible	000	0	0	-	Word Length
1	MSB Justified	101	0	0	-	Word Length
2	LSB Justified	101	1	0	-	Word Length
3	PCM Short Frame	110	0	1	Slot Length	Word Length
4	PCM Long Frame	111	0	1	Slot Length	Word Length
5	Irregular I^2S	000	0	1	Slot Length	Word Length

Table 27. Stereo Mode Setting Example (-: Do Not Care)

Mode 0: I²S Compatible Format

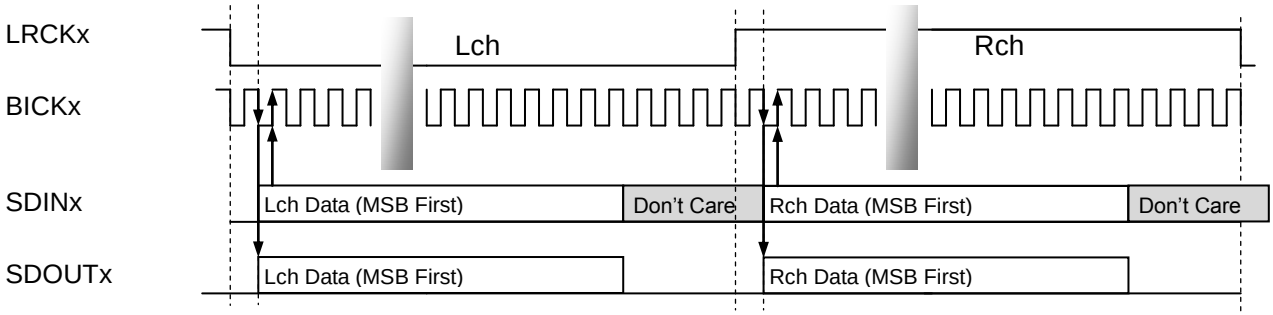


Figure 26. I²S Compatible Format

Mode 1: MSB Justified Format

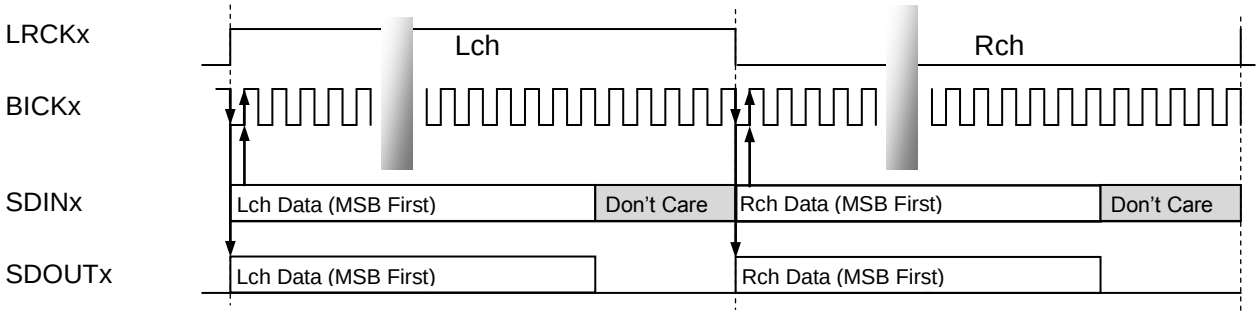


Figure 27. MSB Justified Format

Mode 2: LSB Justified Format

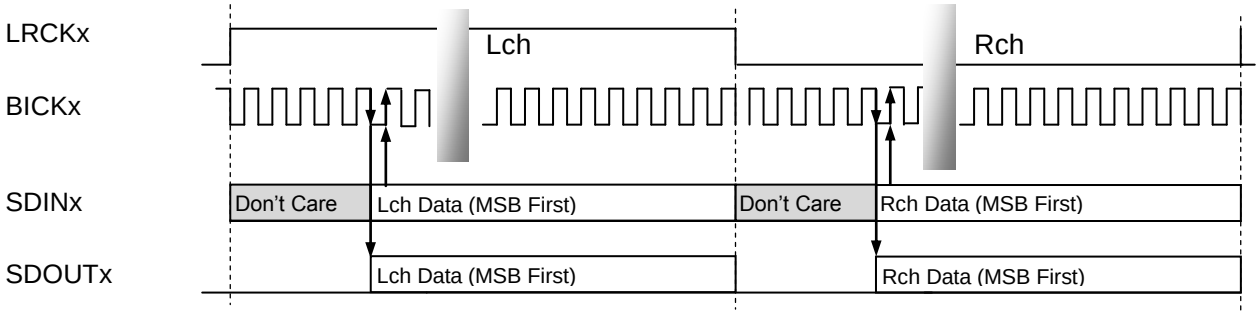


Figure 28. LSB Justified Format

Mode 3: PCM Short Frame Format

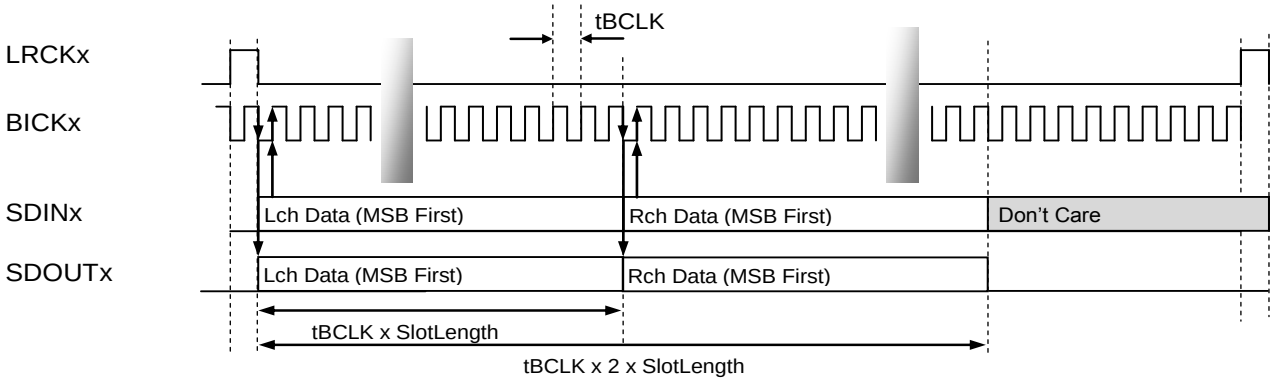


Figure 29. PCM Short Frame Format (BCKPx bit = "0")

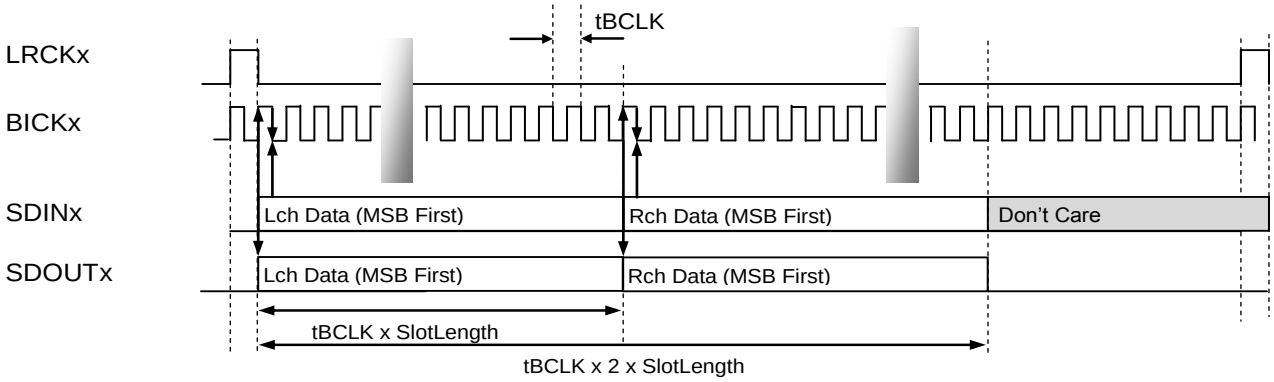


Figure 30. PCM Short Frame Format (BCKPx bit = "1")

Mode 4: PCM Long Frame Format

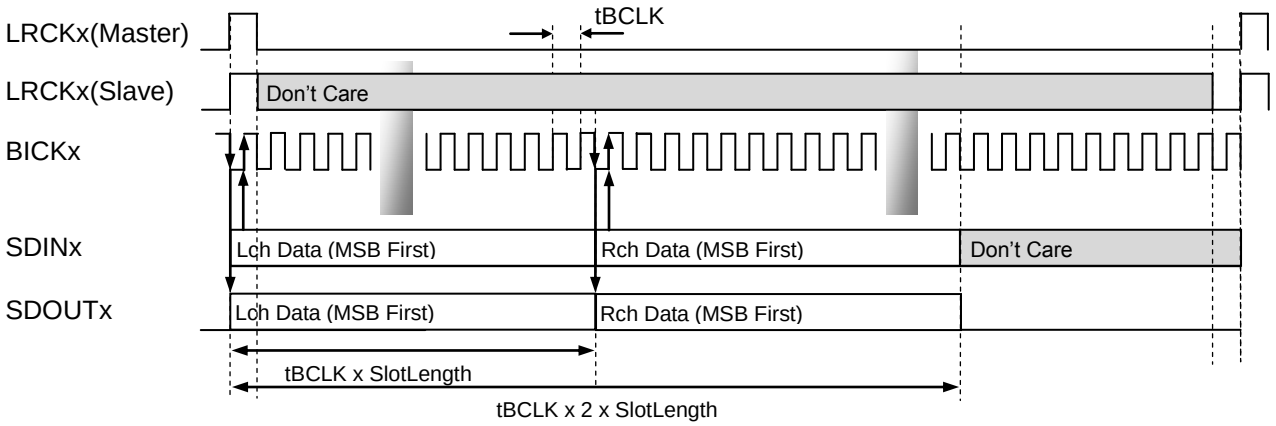


Figure 31. PCM Long Frame Format (BCKPx bit = "0")

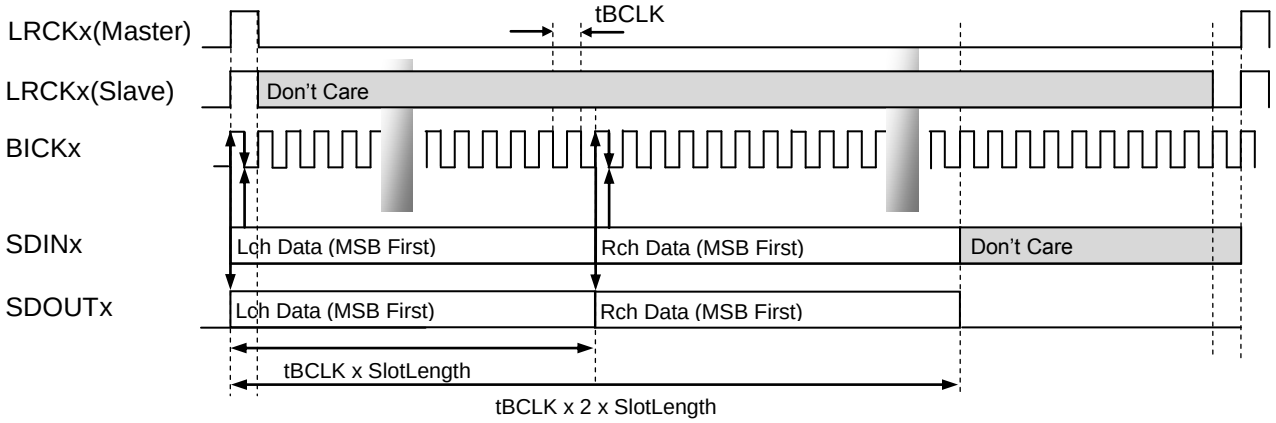


Figure 32. PCM Long Frame Format (BCKPx bit = "1")

Mode 5: Irregular I^2S Format

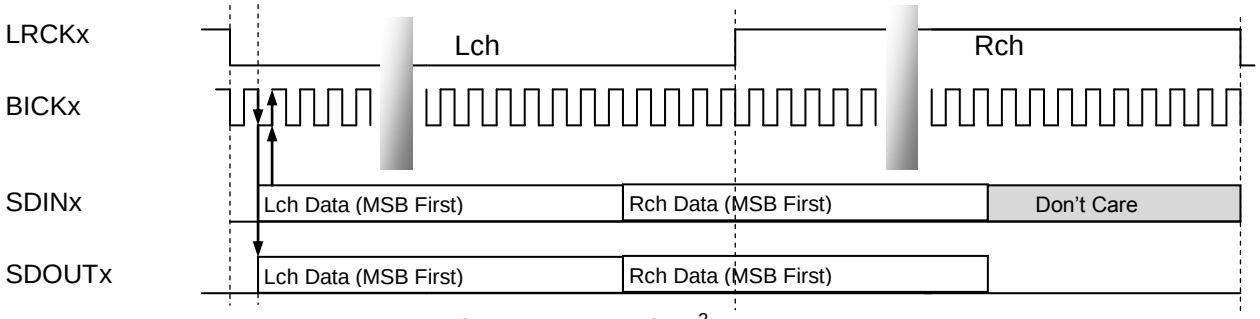


Figure 33. Irregular I^2S Format

5-3-2. TDM Mode

AK7735 supports TDM mode. BICK clock for data input/output should be set to 128fs, 192fs or 256fs when using TDM mode. Sampling frequency up to 192kHz in 128fs mode (max. fs=128kHz in 192 mode, max. fs=96kHz in 256 mode) is supported.

The SDINx input pins of the AK7735 support TDM mode. Eight slots data input is available at a maximum. A source address is assigned to each 2 slot of SDINx input pins when using TDM mode. (Table 19). DISLx[1:0] bits control input data slot length of the SDINx pin. DIDLx [1:0] bits control the input data word length of the SDINx pin. The slot data format is set by DILSBEx bit.
In TDM mode, DIEDGENx bit must be set to “1” since the data transmission timing after second channel is slot length basis. Slot length, word length and slot data format of each input data slot should be the same setting.

The SDOUTx output pins of the AK7735 support TDM mode. Eight slots data output is available for each pin at a maximum. Each slot data can be assigned independently by setting SELDOxA-D[5:0] bits in every two slots. DOSLx[1:0] bits control output data slot length of the SDOUTx pin. DODLx[1:0] bits control the output data word length of the SDOUTx pin. The slot data format is set by DOLSBEx bit. In TDM mode, DOEDGENx bit must be set to “1” since the data transmission timing after second channel is slot length basis. Slot length, word length and slot data format of each input data slot should be the same setting.

Setting example of TDM mode is shown in Table 28.

Mode	Data Format	DCFx[2:0]	DILSBEx DOLSBEx	DIEDGENx DOEDGENx	DISLx[1:0] DOSLx[1:0]	DIDLx[1:0] DODLx[1:0]
0	I^2S Compatible	000	0	1	11 (32bit)	Word Length
1	MSB Justified	101	0	1	11 (32bit)	Word Length
2	LSB Justified	101	1	1	11 (32bit)	Word Length
3	PCM Short Frame	110	0	1	Slot Length	Word Length
4	PCM Long Frame	111	0	1	Slot Length	Word Length
5	Irregular I^2S	000	0	1	Slot Length	Word Length

Table 28. TDM Mode Setting Example

Mode 0: I²S Compatible Format

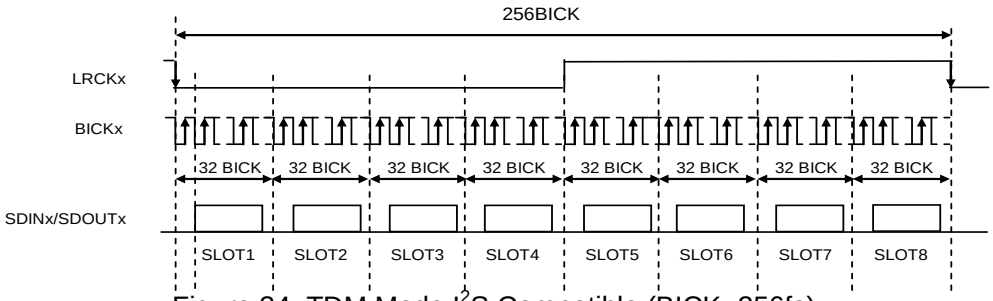


Figure 34. TDM Mode I²S Compatible (BICK=256fs)

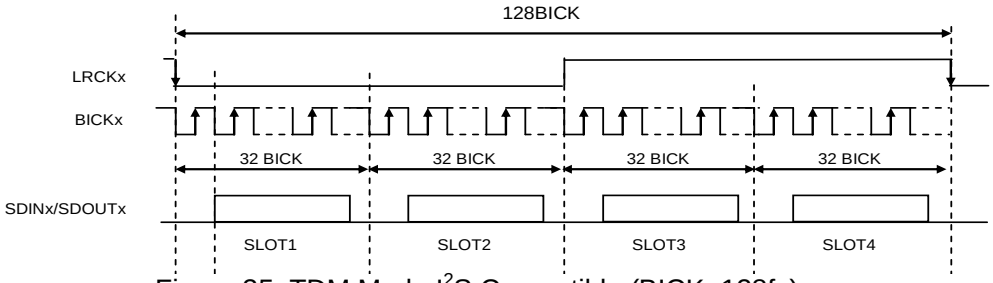


Figure 35. TDM Mode I²S Compatible (BICK=128fs)

Mode 1: MSB Justified Format

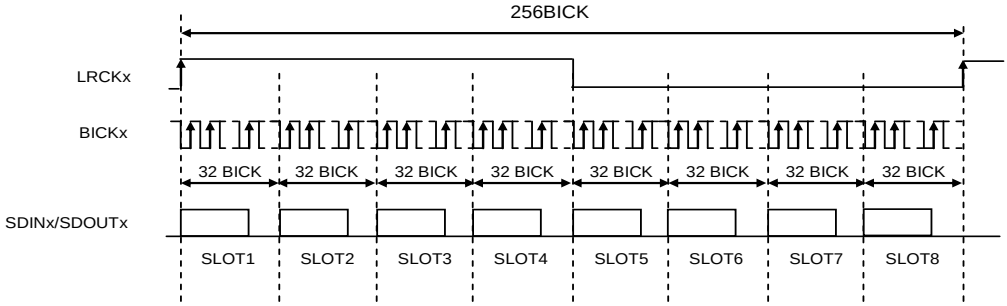


Figure 36. TDM Mode MSB Justified Format (BICK=256fs)

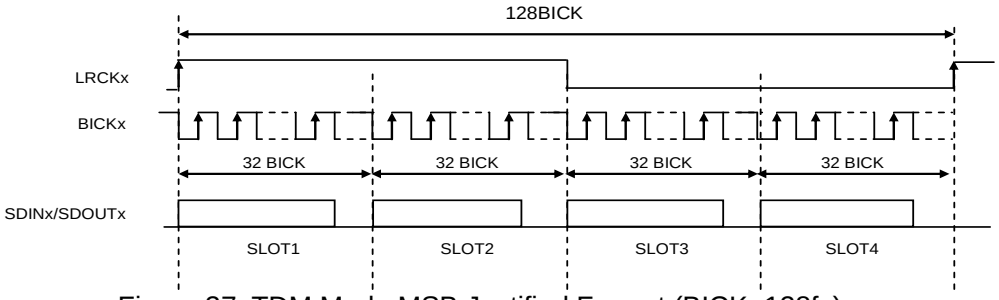


Figure 37. TDM Mode MSB Justified Format (BICK=128fs)

Mode 2: LSB Justified Format

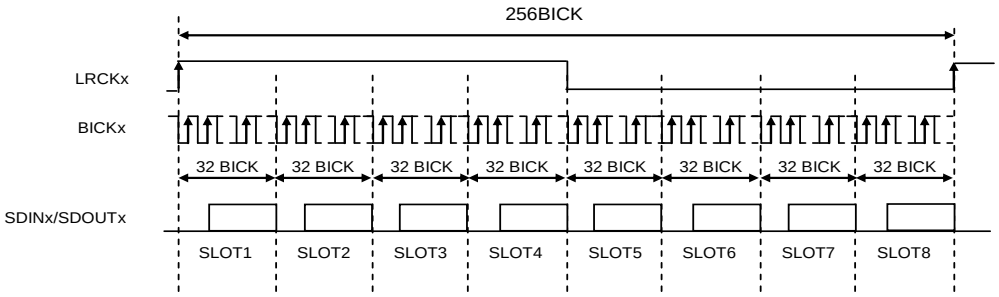


Figure 38. TDM Mode LSB Justified Format (BICK=256fs)

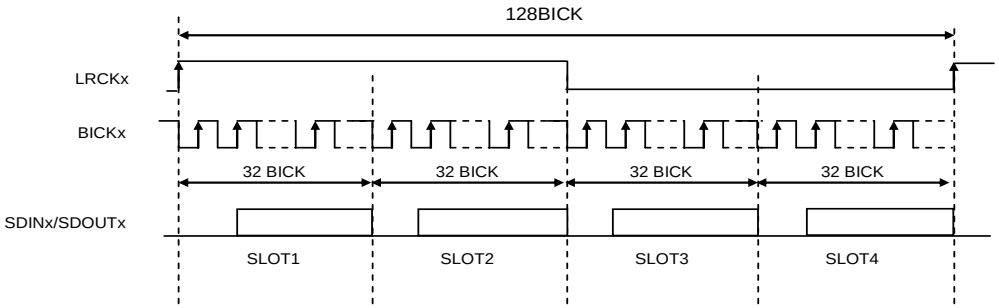


Figure 39. TDM Mode LSB Justified Format (BICK=128fs)

Mode 3: PCM Short Frame Format

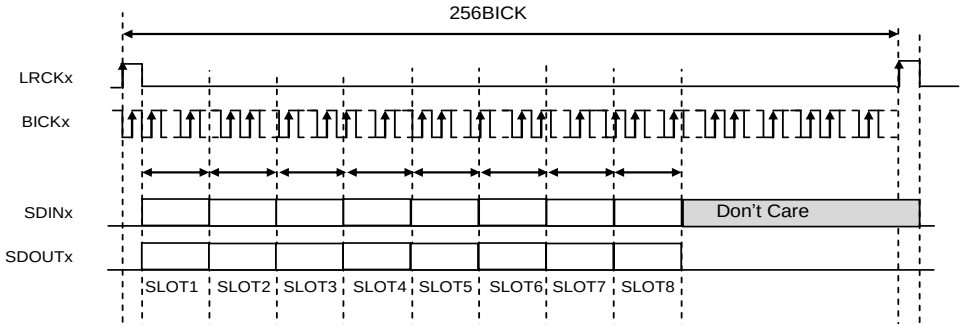


Figure 40. TDM Mode PCM Short Frame (BICK=256fs, BCKP bit = "0") * 57

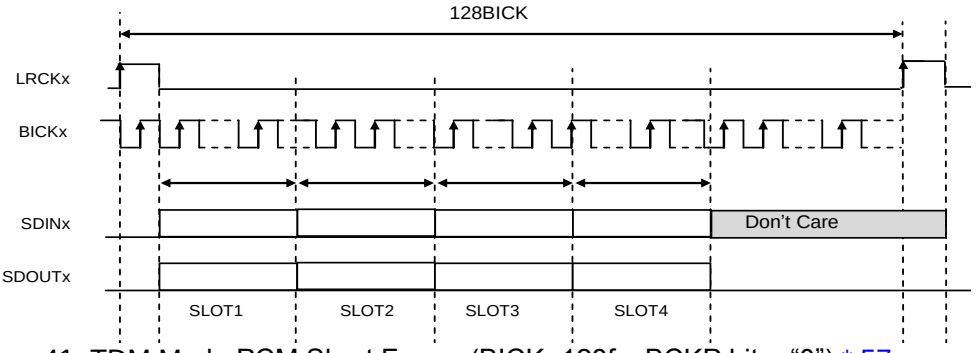


Figure 41. TDM Mode PCM Short Frame (BICK=128fs, BCKP bit = "0") * 57

Note

* 57. When BCKP bit = "1", a BICK rising edge "↑" corresponds to a LRCK rising edge "↑".

Mode 4: PCM Long Frame Format

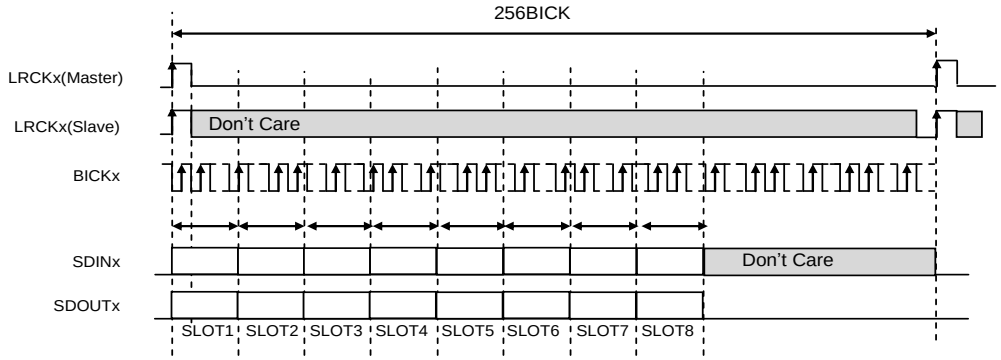


Figure 42. TDM Mode PCM Long Frame (BICK=256fs, BCKP bit = "0") * 58

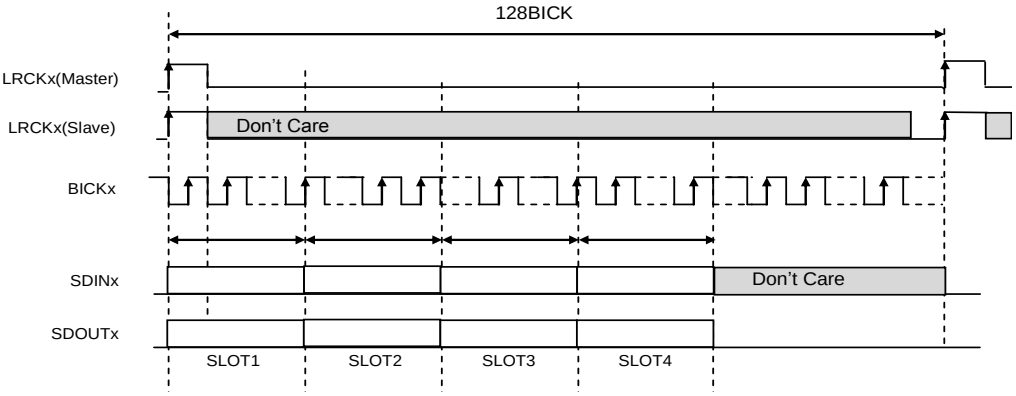


Figure 43. TDM Mode PCM Long Frame (BICK=128fs, BCKP bit = "0") * 58

Note

* 58. When BCKP bit = "1", a BICK rising edge "↑" corresponds to a LRCK rising edge "↑".

Mode 5: Irregular I^{2}S Format

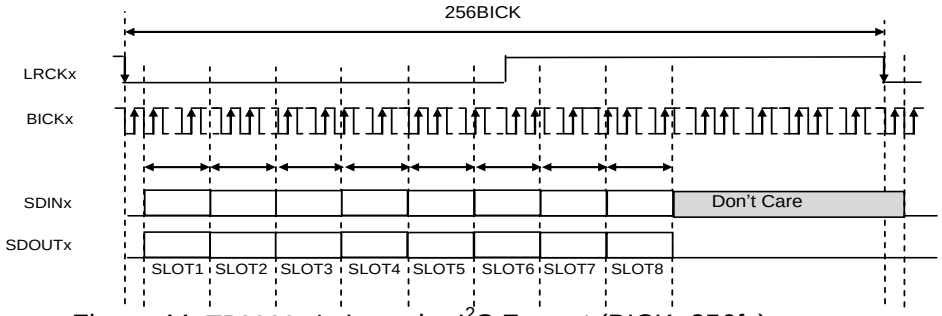


Figure 44. TDM Mode Irregular I^{2}S Format (BICK=256fs)

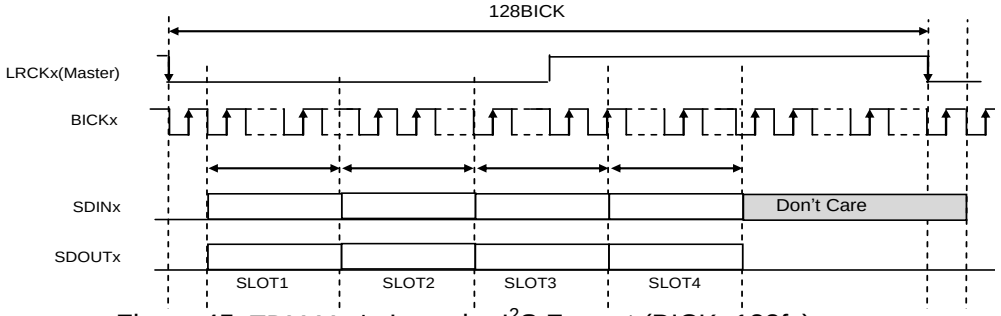


Figure 45. TDM Mode Irregular I^{2}S Format (BICK=128fs)

■ Power-up Sequence

The AK7735 should be powered up when the PDN pin = “L”. Set the PDN pin to “H” to start the power supply circuits for REF (reference voltage source) generator and digital circuits after all power supplies are fed. By setting the PDN pin to “H”, control registers are initialized. Control register settings should be made with an interval of 1ms or more after the PDN pin = “H”.

The PLL starts operation by a clock reset release (CKRESETN bit = “0” → “1”) and generates the internal master clock after setting control registers. Therefore, necessary system clock must be input before a clock reset release.

Interfacing with the AK7735 except control register settings should be made when PLL oscillation is stabilized after clock reset release (take a 10ms interval or confirm “H” output of PLLLOCK signal from the STO bit (Figure 46)). However, DSP program and coefficient data can be written even when the system clock is stopped or during clock reset (CKRESETN bit= “0”). DSP program and coefficient data can be written in 1ms by setting DLRDY bit “0” → “1”. DLRDY bit must be set to “0” after downloading programs or data (Figure 47).

When using a crystal oscillator, release clock reset after crystal oscillation is stabilized. The stabilizing time of crystal oscillation is dependent on the crystal and external circuits.

The system clock must not be stopped except during clock reset and power-down mode (PDN pin = “L”).

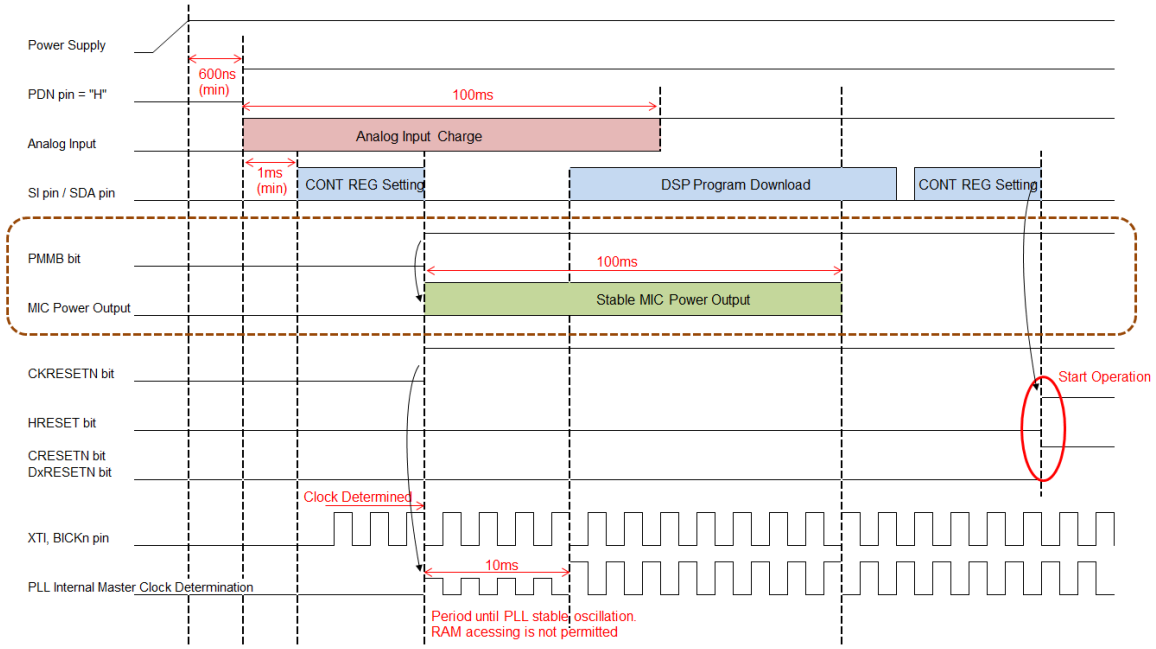


Figure 46. Power-up Sequence

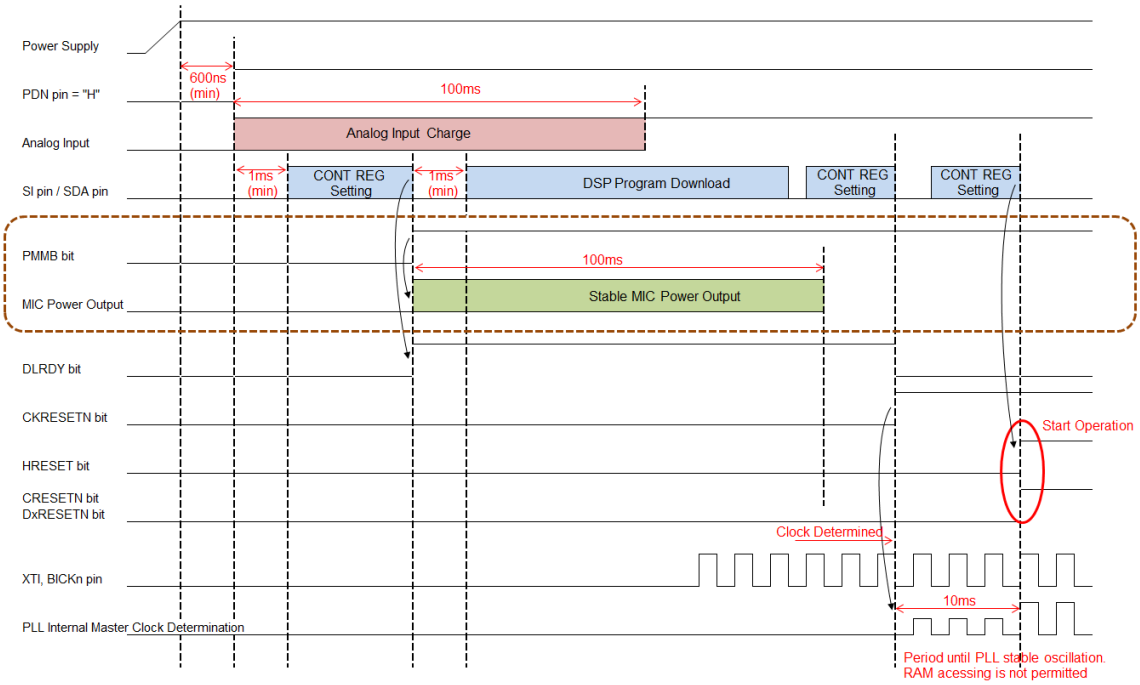


Figure 47. Power-up Sequence 2 (DLRDY bit Setting)

■ VREG (Internal Circuit Drive Regulator)

The AK7735 has a regulator for driving internal digital circuits (VREG). Connect a 2.2μF (±30%) capacitor between the AVDRV pin and the DVSS3 pin. The regulator starts operation by releasing power-down mode, and control register settings can be made 1ms after the power-down release (PDN pin="H").

The AK7735 has an overcurrent protection circuit to avoid abnormal heat of the device that is caused by a short of the AVDRV pin to VSS and etc., and an overvoltage protection circuit to protect from exceeded voltage when the voltage to the AVDRV pin gets too high. When these protection circuits perform, internal circuits are powered down. The internal circuit will not return to a normal operation until being reset by the PDN pin after removing the problems.

■ Power-down and Reset

1. AK7735 Power-down and Reset Statuses and Power Management

Power-down and power-down release of the AK7735 is controlled by the PDN pin. After power-down is released, the power management and reset of the AK7735 are controlled by registers such as CKRESETN bit (Clock Reset), HRESETN bit (HUB Reset), D1RESETN and D2RESETN bits (DSP reset), CRESETN bits (CODEC Reset) and power management bits for each block.

There are three states for the AK7735 other than normal operation: Power-down, Clock Reset and System Reset.

1) The power-down state means the status that the PDN pin is “L”. In this state, all blocks of the AK7735 stop the operation.
2) The clock reset state means the status that the PDN pin is “H” and CKRESETN bit is “0”. In this state, the DSP, ADC, DAC and SRC blocks are not in operation because the PLL circuit and internal clocks are stopped.
3) The system reset state means the status that the PDN pin is “H”, CKRESETN bit is “1”, HRESETN bit is “0”, CRESETN bit is “0” and DxRESETN bit (x= 1, 2) is “0”. In this state, the DSP, ADC, DAC and SRC blocks are not in operation although the PLL circuit and internal clocks are started. The system reset is released by setting either HRESETN bit or CRESETN bit or DxRESETN bit (x=1, 2) to “1”.

State	Setting				
	PDN pin	CKRESETN bit	DxRESETN bit (x=1, 2)	HRESETN bit	CRESETN bit
Power-down	L	x	x	x	x
Clock Reset	H	0	0	0	0
System Reset * 59	H	1	0	0	0
System Reset Release * 60	H	1	1	1	1

Table 29. Reset State Definitions of the AK7735 (x: Don’t Care)

Notes

* 59. A stable clock should be supplied before releasing clock reset (CKRESETN bit = “1”).
* 60. The system reset is released by setting either HRESETN bit or CRESETN bit or DxRESETN bit (x=1, 2) to “1”.

2. Power-down

The AK7735 can be powered down by bringing the PDN pin = “L”. Power-down status of output pins is shown in Table 3.

3. Power-down Release

The REF generation circuit (reference voltage source) and a power supply circuit for internal digital circuit are powered-up by bringing the PDN pin to “H” from “L” after an interval of 600ns or more when AVDD, LVDD, TVDD and VDD33 are powered up. Control register settings should be made with an interval of 1ms or more after setting the PDN pin = “H”.

4. Clock Reset

When CKRESETN bit = “0” after power-down mode is released (PDN pin = “H”), the AK7735 is in clock reset state. All blocks except the power supply circuits for REF generation and digital circuits are in power-save mode. Even the internal PLL for master clock generation is powered down.

Control register settings should be made with an interval of 1ms (min) after releasing the power-down mode. DSP program and coefficient data can be written in 1ms by setting DLRDY bit “0” → “1” during clock reset. DLRDY bit must be set to “0” after downloading (Figure 47).

Necessary system clocks (Table 4, Table 5) should be input before the clock reset is released. The internal PLL starts operation and the master clock is generated when clock reset is released (CKRESETN bit = “1”). DSP program and coefficient data should be sent 10ms after clock reset release or after confirming “H” output of PLLLOCK signal from the STO pin (Figure 46).

System clocks must be changed during clock reset or in power-down mode (PDN pin = “L”). The PLL and the internal clocks are stopped by this clock reset and the clock change can be done safely. Change register settings and system clock frequencies during the clock reset. After system clock is stabilized, the PLL starts operation by setting CKRESETN bit to “1”.

Clock operated blocks (ADC, DAC and SRC) must be powered down before executing clock reset. These blocks can be powered down simultaneously by setting HRESETN bit to “0” from “1”. Set HRESETN bit to “1” from “0” with an interval of 10ms for stabilization of PLL after clock reset is released.

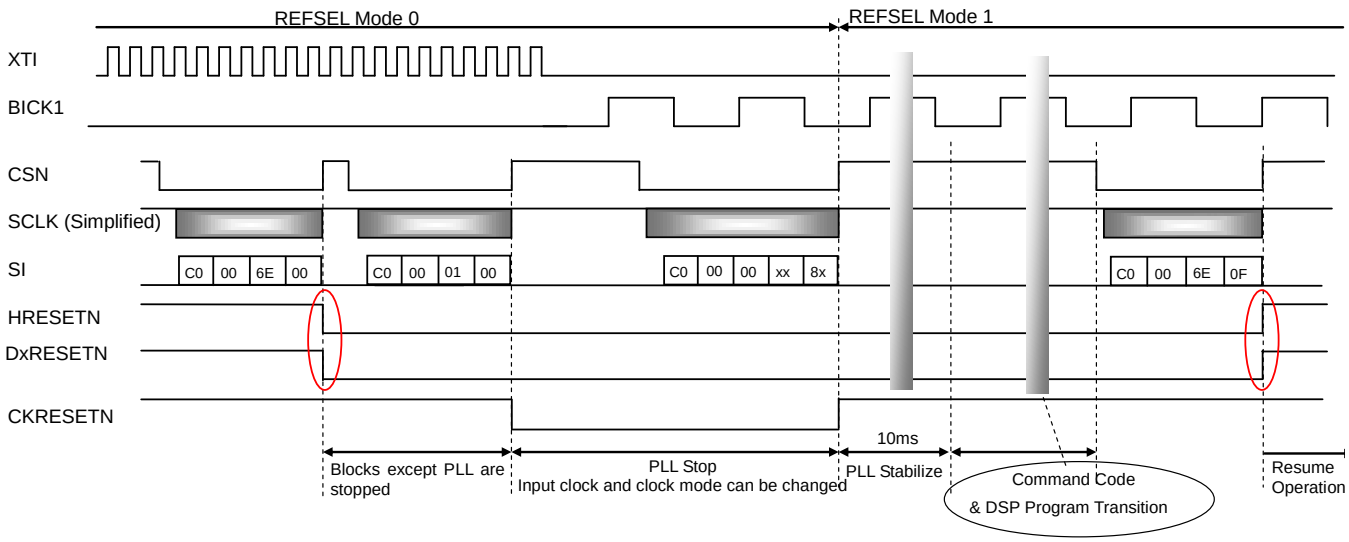


Figure 48. Clock Mode Switching Sequence

■ RAM Clear

The AK7735 has a RAM clear function. After a DSP reset release, DRAM and DLRAM are cleared by "0". The internal PLL must have stable oscillation before a DSP reset release.

A period of 8/fs (fs: DSP operating sampling rate) is required from a DSP reset release to the RAM clear start. The required time to clear RAM is about 112µs.

During the RAM clear period, it is possible to send a command to the DSP. (The DSP is stopped during RAM clear sequence. The sent command is accepted automatically after this sequence is completed.)

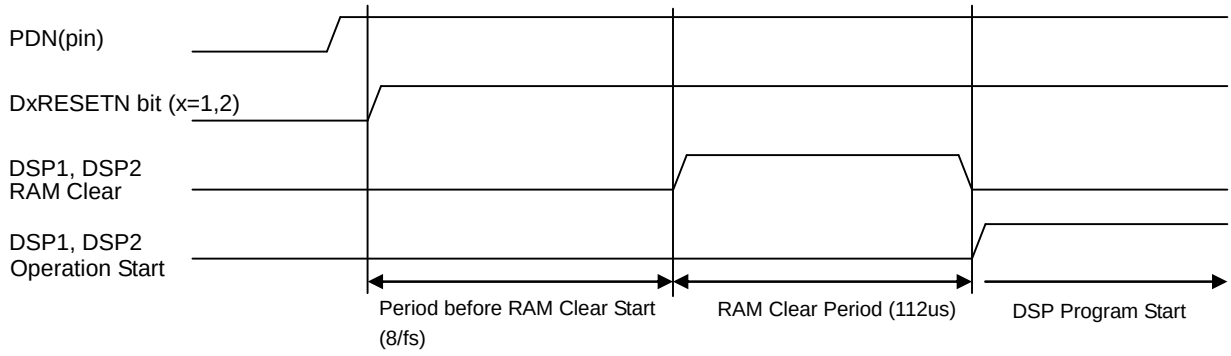


Figure 49. RAM Clear Sequence

Register and RAM settings of the AK7735 are not held if the PDN pin goes to "L". The DRAM and DLRAM are not held by a clock reset or a DSP reset.

State	Register	PRAM	CRAM	DRAM	DLRAM	OFREG
Power Down (PDN pin = "L")	x	x	x	x	x	x
Clock Reset (CKRESETN bit = "0")	Hold	Hold	Hold	x	x	Hold
DSP Reset (DxRESETN bit = "0")	Hold	Hold	Hold	x	x	Hold

Table 30. Register and RAM Setting Status by Reset (x: Not Hold)

■ STO pin Output Status

The No. 23 pin has the function of the STO (status output) pin, the RDY pin and the SDOUT2 pin. DO2SEL[1:0] bits control the function of this pin. The STO pin function is selected in the default setting. When SDOUT2EN bit = “0” (default), the STO pin output is enabled. When SDOUT2EN bit = “1”, the STO pin outputs “L”.

The STO pin outputs “L” when the AK7735 is powered up and the PDN pin is “L”. The STO pin outputs “H” when the internal digital power-supply circuit (VREG) is powered up after releasing the power-down (PDN pin = “H”).

After the power-down state is released, VREG shut down signal, PLL lock signal, WDT1 and WDT2 (watchdog timer) errors of the DSP, CRC error and SRC1~2 lock signal can be output from the STO pin by control register settings. The AK7735 is distinguished as error state when the PDN pin = “H”, DO2SEL[1:0] bits = “00”, SDOUT2EN bit = “0” and the STO pin = “L”.

VREG shut down status and WDT1-2 statuses, which are set by DSP instruction, are output from the STO pin when the control register settings are in the default value.

PDN pin	VREG	D1WDTEN bit D2WDTEN bit	CRCE bit	PLLLOCKE bit	SRCLOCKE1 bit SRCLOCKE2 bit	STO pin	Note
L	Power Down	-	-	-	-	L	
H	Error	-	-	-	-	L	
	Normal Operation	0	0	0	0	WDTnERR	(default) * 61, * 62
		1	1	0	0	CRCERR	
		1	0	1	0	PLLLOCKERR	
		1	0	0	1	SRCnLOCKERR	* 61
		0	1	1	1	WDTnERR & CRCERR & PLLLOCKERR & SRCLOCKERRn	* 61, * 62

Table 31. STO pin Output Setting (-: Not Care)

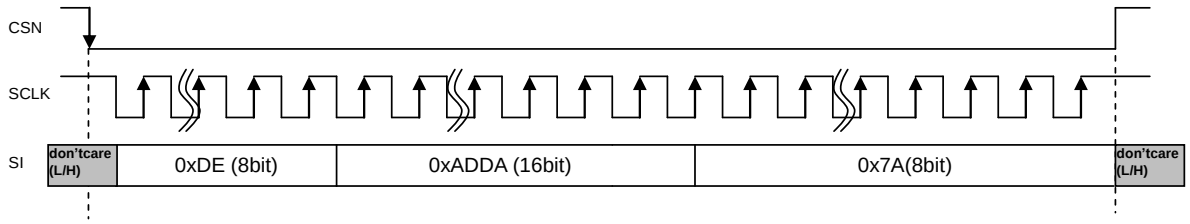
Notes

* 61. The STO pin outputs “L” if the one of status signal becomes “L” when setting multiple statuses to the STO pin.
* 62. A DSP instruction setting is necessary when using WDT1 and WDT2 (watchdog timer).

■ µP Interface Setting and Pin Statuses

The AK7735 supports both SPI and I^2C interfaces. When using SPI interface, release the power-down state of the AK7735 while the CSN pin is "H". When using I^2C interface, the CSN pin must be pulled up or down since it becomes a chip address pin. After a power-down release, the AK7735 is set to I^2C interface mode. SPI interface mode become enabled by sending the dummy command mentioned below.

Input "0xDE → 0xADDA → 0x7A" to the SI/I2CFIL pin while the CSN pin is "L" after a falling edge "↓" of the CSN pin for the dummy command. The data is in MSB first format.



Statuses of the CSN, SO/SDA, SCLK/SCL and SI/I2CFIL pins are changed depending on the PDN pin.

	PDN pin	CSN pin	SO/SDA pin	SCLK/SCL pin	SI/I2CFIL pin
SPI Interface	L	input ("H")	Hi-Z	input	input
	H	function	function (pull-up / pull-down)	function	function
I^2C Interface	L	pull-up / pull-down	"Hi-Z"→ pull-up	input	input
	H		function (pull-up)	function	"L": I^2C Fast Mode "H": I^2C Fast Mode Plus

Table 32. µP Interface Setting

Note

* 63. The CSN pin and the SI/I2CFIL pin should be fixed to "L" or "H" when using I^2C interface mode. The SO/SDA pin should be pulled-up/down when using SPI interface mode.

■ SPI Interface

1. Configuration

The access format consists of Command code (8bits) + Address (16bits) + Data (MSB first).

	Bit Length	Description
Command code	8	MSB bit is an R/W flag. The following 7 bits indicate access area such as PRAM/ CRAM/Registers.
Address	16	Address is fixed to 16bits.
Data	Mentioned in later section	Read/Write Data

Table 33. µP Interface Format

Write

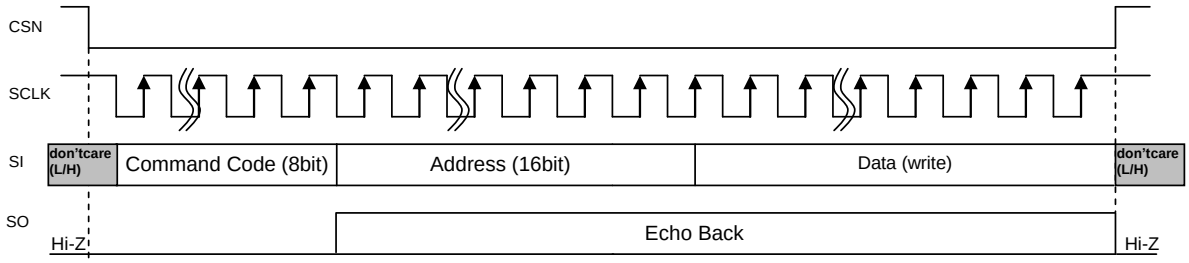


Figure 50. SPI Interface Timing (Write)

Read (Except Read Operation during Run）

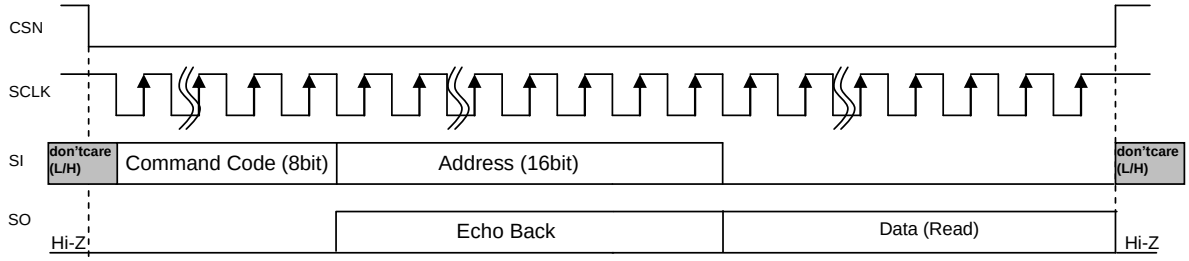


Figure 51. SPI Interface Timing (Read) (Except Command 24H, 25H, 26H and 27H)

Read (during Run)

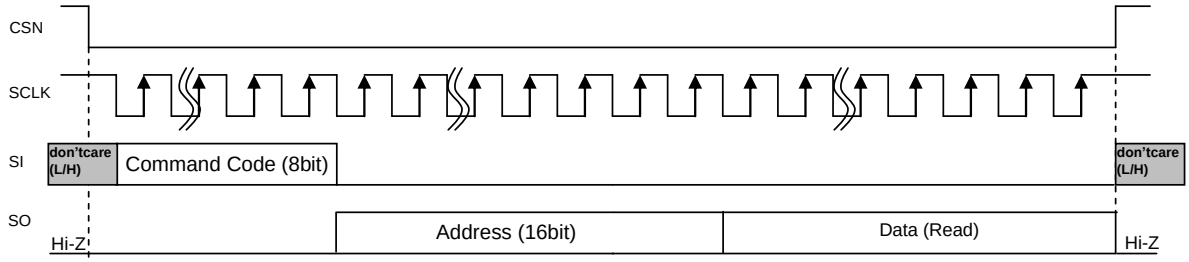


Figure 52. SPI Interface Timing (Read) (Command 24H, 25H, 26H and 27H)

1-1. Write

Command	Address	Data Length	Description
80H ~ 8FH	16bit	24bit x n	Write preparation to CRAM of DSP1/DSP2 during RUN (80H: write 1data, 81H: write 2data, ----, 8FH: write 16data) If the actual amount of write operations exceeds the defined amount, the data will be ignored.
90H ~ 9FH	16bit	24bit x n	Write preparation to OFREG of DSP1/DSP2 during RUN (90H: write 1data, 91H: write 2data, ----, 9FH: write 16data) If the actual amount of write operations exceeds the defined amount, the data will be ignored.
A2H	16bit	-	Write execution to OFREG of DSP1 during RUN. 0 address should be written.
A3H	16bit	-	Write execution to OFREG of DSP2 during RUN. 0 address should be written.
A4H	16bit	-	Write execution to CRAM of DSP1 during RUN. 0 address should be written.
A5H	16bit	-	Write execution to CRAM of DSP2 during RUN. 0 address should be written.
B2H	16bit	24bit x n	Write operation to OFREG of DSP1 (during DSP reset)
B3H	16bit	24bit x n	Write operation to OFREG of DSP2 (during DSP reset)
B4H	16bit	24bit x n	Write operation to CRAM of DSP1 (during DSP reset)
B5H	16bit	24bit x n	Write operation to CRAM of DSP2 (during DSP reset)
B8H	16bit	40bit x n	Write operation to PRAM of DSP1 (during DSP reset)
B9H	16bit	40bit x n	Write operation to PRAM of DSP2 (during DSP reset)
C0H	16bit	8bit x n	Sequential Control Register Write
F2H	16bit	16bit	CRC Result Write 0 address should be written.
F4H	16bit	8bit	Write operation of DSP1 JX code 0 address should be written.
F5H	16bit	8bit	Write operation of DSP2 JX code 0 address should be written.

The data length is defined by the command code which specifies the area to be accessed. Writing other than the above-mentioned command code is prohibited.

1-2. Read

Command	Address	Data Length	Description
24H	0bit	16bit + 24bit x n	Read CRAM write preparation data of DSP1
25H	0bit	16bit + 24bit x n	Read OFREG write preparation data of DSP1
26H	0bit	16bit + 24bit x n	Read CRAM write preparation data of DSP2
27H	0bit	16bit + 24bit x n	Read OFREG write preparation data of DSP2
32H	16bit	24bit x n	Read operation from OFREG of DSP1 (during DSP reset)
33H	16bit	24bit x n	Read operation from OFREG of DSP2 (during DSP reset)
34H	16bit	24bit x n	Read operation from CRAM of DSP1 (during DSP reset)
35H	16bit	24bit x n	Read operation from CRAM of DSP2 (during DSP reset)
38H	16bit	40bit x n	Read operation from PRAM of DSP1 (during DSP reset)
39H	16bit	40bit x n	Read operation from PRAM of DSP2 (during DSP reset))
40H	16bit	8bit x n	Sequential Control Register Read
40H	16bit	8bit	Device Identification No. (recognized as Register: Address = 0100H)
40H	16bit	8bit	Device Revision No. (recognized as Register: Address = 0101H)
72H	16bit	16bit	CRC result Read 0 address should be written.
76H	16bit	32bit x n	Sequential Read operation from MIR of DSP1. (max. 8) 0 address should be written. 28bits are upper-bit justified. Lower 4 bits are for validity flags. Valid at “0000”. * 64
77H	16bit	32bit x n	Sequential Read operation from MIR of DSP2. (max. 8) 0 address should be written. 28bits are upper-bit justified. Lower 4 bits are for validity flags. Valid at “0000”. * 64

Note

* 64. Lower 4 bits for validity flags are common in eight MIR data. If the MIR data is updated by a DSP program, all eight data flags become “0000”. If an MIR read command by a microcontroller is executed, all eight data flags become “1111”.

When accessing RAM or control registers, data may be read from sequential address locations by reading data continuously. Reading other than the above-mentioned command code is prohibited.

2. Echo-Back Mode

The AK7735 has Echo-back mode that outputs the writing data sequentially from the SO pin.

2-1. Write

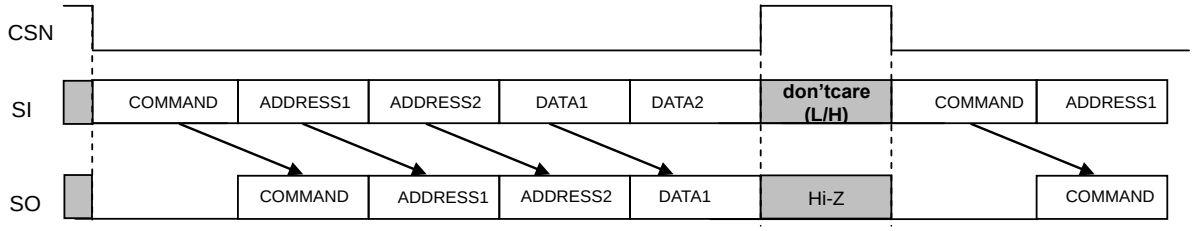


Figure 53. Echo-back Mode Writing (SPI)

The input data of the SI pin is echoed back on the SO pin by shifting 8-bits to the right. The last 1 byte written data is not echoed-back. The data will not echoed-back when writing dummy command.

2-2. Read

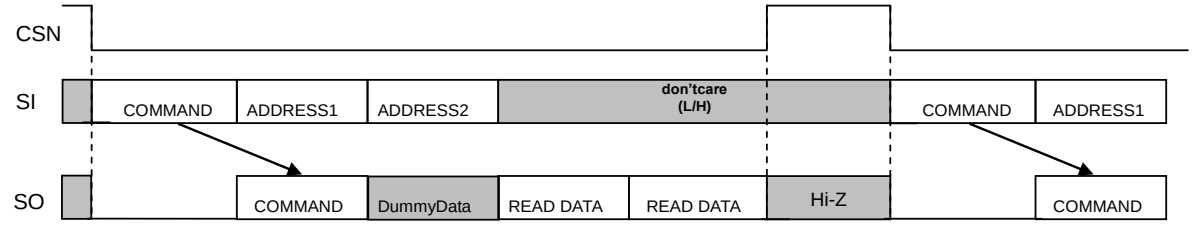


Figure 54. Echo-back Mode Reading (SPI)

Data of the address1/2 fields are not echoed back in read operation. The read data on the SO pin is output after writing to the address2 field.

3. Command Format

3-1. DSP RAM Write and Read

3-1-1. Write Operation during DSP Reset

(1) Program RAM (PRAM) Write (during DSP reset)

Field	Write data
(1) COMMAND Code	0xB8 (DSP1) / 0xB9 (DSP2)
(2) ADDRESS1	0 0 0 0 A11 A10 A9 A8
(3) ADDRESS2	A7 A6 A5 A4 A3 A2 A1 A0
(4) DATA1	0 0 0 0 D35 D34 D33 D32
(5) DATA2	D31~D24
(6) DATA3	D23~D16
(7) DATA4	D15~D8
(8) DATA5	D7~D0
	Five bytes of data may be written continuously for each address.

(2) Coefficient RAM (CRAM) Write (during DSP reset)

Field	Write data
(1) COMMAND Code	0xB4 (DSP1) / 0xB5 (DSP2)
(2) ADDRESS1	0 0 0 A12 A11 A10 A9 A8
(3) ADDRESS2	A7 A6 A5 A4 A3 A2 A1 A0
(4) DATA1	D23~D16
(5) DATA2	D15~D8
(6) DATA3	D7~D0
	Three bytes of data may be written continuously for each address.

(3) Offset REG (OFREG) Write (during system reset)

Field	Write data
(1) COMMAND Code	0xB2 (DSP1) / 0xB3 (DSP2)
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 A5 A4 A3 A2 A1 A0
(4) DATA1	0 0 0 0 0 0 0 0
(5) DATA2	0 0 D13 D12 D11 D10 D9 D8
(6) DATA3	D7~D0
	Three bytes of data may be written continuously for each address.

3-1-2. Write Operation during RUN中

(1) Coefficient RAM (CRAM) Write Preparation (during RUN)

Preparation	Write data
(1) COMMAND Code	0x80~0x8F (one data at 0x80, sixteen data at 0x8F)
(2) ADDRESS1	0 0 0 A12 A11 A10 A9 A8
(3) ADDRESS2	A7 A6 A5 A4 A3 A2 A1 A0
(4) DATA1	D23~D16
(5) DATA2	D15~D8
(6) DATA3	D7~D0
	Three bytes of data may be written continuously for each address.

(2) Coefficient RAM (CRAM) Write Operation (during RUN)

Execute	Write data
(1) COMMAND Code	0xA4 (DSP1) / 0xA5 (DSP2)
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 0 0 0 0 0 0

(3). Offset REG (OFREG) Write Preparation (during RUN)

Preparation	Write data
(1) COMMAND Code	0x90~0x9F (one data at 0x90, sixteen data at 0x9F)
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 A5 A4 A3 A2 A1 A0
(4) DATA1	0 0 0 0 0 0 0 0
(5) DATA2	0 0 D13 D12 D11 D10 D9 D8
(6) DATA3	D7~D0
	Three bytes of data may be written continuously for each address.

(4). Offset REG (OFREG) Write Operation (during RUN)

Execute	Write data
(1) COMMAND Code	0xA2 (DSP1) / 0xA3 (DSP2)
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 0 0 0 0 0 0

3-1-3. Read Operation during DSP Reset

(1) Program RAM (PRAM) Read (during DSP reset)

Field	Write data	Readout data
(1) COMMAND Code	0x38 (DSP1) / 0x39 (DSP2)	
(2) ADDRESS1	0 0 0 0 A11 A10 A9 A8	
(3) ADDRESS2	A7 A6 A5 A4 A3 A2 A1 A0	
(4) DATA1		0 0 0 0 D35 D34 D33 D32
(5) DATA2		D31~D24
(6) DATA3		D23~D16
(7) DATA4		D15~D8
(8) DATA5		D7~D0
	Five bytes of data may be read continuously for each address.	

(2) Coefficient RAM (CRAM) Read (during DSP reset)

Field	Write data	Readout data
(1) COMMAND Code	0x34 (DSP1) / 0x35 (DSP2)	
(2) ADDRESS1	0 0 0 A12 A11 A10 A9 A8	
(3) ADDRESS2	A7 A6 A5 A4 A3 A2 A1 A0	
(4) DATA1		D23~D16
(5) DATA2		D15~D8
(6) DATA3		D7~D0
	Three bytes of data may be read continuously for each address.	

(3) Offset REG (OFREG) Read (during DSP reset)

Field	Write data	Readout data
(1) COMMAND Code	0x32 (DSP1) / 0x33 (DSP2)	
(2) ADDRESS1	0 0 0 0 0 0 0 0	
(3) ADDRESS2	0 0 A5 A4 A3 A2 A1 A0	
(4) DATA1		0 0 0 0 0 0 0 0
(5) DATA2		0 0 D13 D12 D11 D10 D9 D8
(6) DATA3		D7~D0
	Three bytes of data may be read continuously for each address.	

3-1-4. Read Operation during RUN

(1) CRAM Write Preparation Read (during RUN)

Field	Write data	Readout data
(1) COMMAND Code	0x24 (DSP1) / 0x26 (DSP2)	
(2) ADDRESS1		0 0 0 A12 A11 A10 A9 A8
(3) ADDRESS2		A7 A6 A5 A4 A3 A2 A1 A0
(4) DATA1		D23~D16
(5) DATA2		D15~D8
(6) DATA3		D7~D0

(2) OFREG Write Preparation Read (during RUN)

Field	Write data	Readout data
(1) COMMAND Code	0x25 (DSP1) / 0x27 (DSP2)	
(2) ADDRESS1		0 0 0 0 0 0 0 0
(3) ADDRESS2		0 0 A5 A4 A3 A2 A1 A0
(4) DATA1		0 0 0 0 0 0 0 0
(5) DATA2		0 0 D13 D12 D11 D10 D9 D8
(6) DATA3		D7~D0

(3) MIR Register Read (during RUN)

Field	Write data	Readout data
(1) COMMAND Code	0x76 (DSP1) / 0x77 (DSP2)	
(2) ADDRESS1	0 0 0 0 0 0 0 0	
(3) ADDRESS2	0 0 0 0 0 0 0 0	
(4) DATA1		D27~D20
(5) DATA2		D19~D12
(6) DATA3		D11~D4
(7) DATA4		D3 D2 D1 D0 (flag3) (flag2) (flag1) (flag0)
	MIR register sequential read for DSP1/DSP2. Max 8 data (32 bytes) may be read continuously. The data is 28-bit MSB justified. Lower 4 bits are validity flags; the data is valid only when all flags are zero.	

3-2. Register Write and Read

3-2-1. Register Write

(1) Control Register Write

Field	Write data
(1) COMMAND Code	0xC0
(2) ADDRESS1	A15~A8
(3) ADDRESS2	A7~A0
(4) DATA	D7~D0
	One byte of data may be written continuously for each address.

(2) External Conditional Jump Code (JX register) Write

Field	Write data
(1) COMMAND Code	0xF4 (DSP1) / 0xF5 (DSP2)
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 0 0 0 0 0 0
(4) DATA	D7~D0

(3) CRC Code Write

Field	Write data
(1) COMMAND Code	0xF2
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 0 0 0 0 0 0
(4) DATA1	D15~D8
(5) DATA2	D7~D0

3-2-2. Register Read

(1) Control Register Read

Field	Write data	Readout data
(1) COMMAND Code	0x40	
(2) ADDRESS1	A15~A8	
(3) ADDRESS2	A7~A0	
(4) DATA		D7~D0
	One byte of data may be written continuously for each address.	

(2) CRC Code Read

Field	Write data	Readout data
(1) COMMAND Code	0x72	
(2) ADDRESS1	0 0 0 0 0 0 0 0	
(3) ADDRESS2	0 0 0 0 0 0 0 0	
(4) DATA1		D15~D8
(5) DATA2		D7~D0

4. RAM and Register Write/Read Timing

4-1. RAM Write Timing during DSP Reset

Write to Program RAM (PRAM), Coefficient RAM (CRAM) and Offset REG (OFREG) during DSP reset in the order of command code (8 bits), address (16 bits) and data. When writing the data to consecutive address locations, continue to input data only. Address is incremented by 1 automatically.

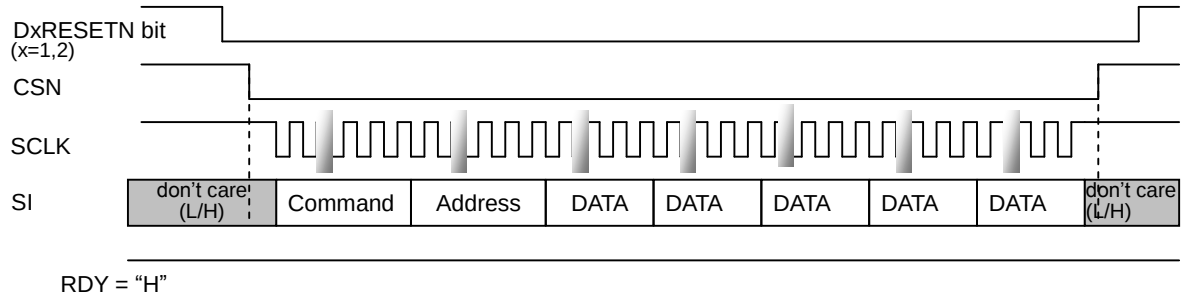


Figure 55. Writing to RAM at Consecutive Address Locations (SPI)

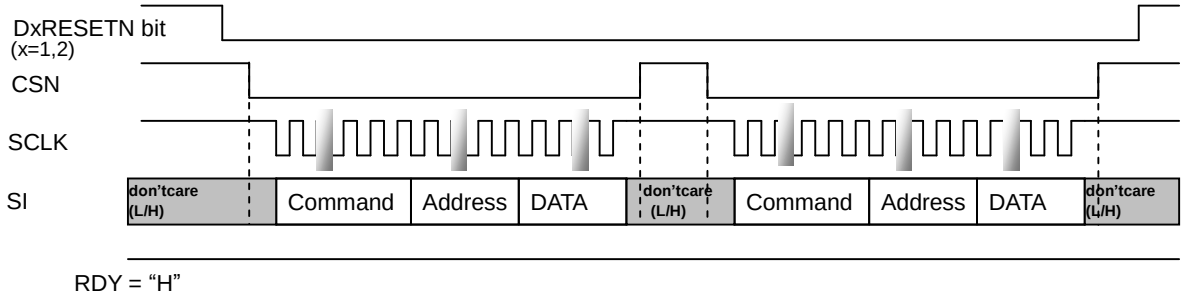


Figure 56. Writing to RAM at Random Address Locations (SPI)

4-2. RAM Write Timing during RUN

These operations described below are to rewrite the Coefficient RAM (CRAM) and Offset REG (OFREG) during RUN. Data writing is executed in two steps; write preparation and write execution. The written data can be confirmed by reading the write preparation data.

(1) Write Preparation
After inputting the assigned command code (8 bits) to select the number of data from 1 to 16, input the starting address of write (16 bits) and the number of data assigned by command code in this order.

(2) Write Preparation Data Confirmation
After write preparation, prepared data for writing can be confirmed. Address and Data are read in this order by write preparation data confirmation command “24H/26H” (CRAM) or “25H/27H” (OFREG). The data will be “0x000001” when reading more than write preparation data. Execute write preparation again when the address and data are disturbed by external noise.

(3) Write Execution
Upon completion of the above operation, execute a RAM write during RUN by inputting the corresponding command code and address (16 bits, all “0”) in this order.

Note
* 65. Execute Write Preparation and Write Preparation Data Confirmation before Write Execution. A Write Preparation Data Confirmation sequence can be skipped, but a malfunction occurs when executing Write Execution to RAM without a Write Preparation sequence. Access operation by a microcontroller is prohibited until RDY changes to “H”.

Write modification of the RAM content is executed whenever the RAM address for modification is accessed. For example, when 5 data are written, from RAM address “10”, it is executed as shown below.

RAM execution address	7	8	9	10	11	13	16	11	12	13	14	15
				↓	↓				↓	↓	↓	
Write execution position				○	○	wait			○	○	○	

Note
* 66. Address “13” is not executed until rewriting address “12”.

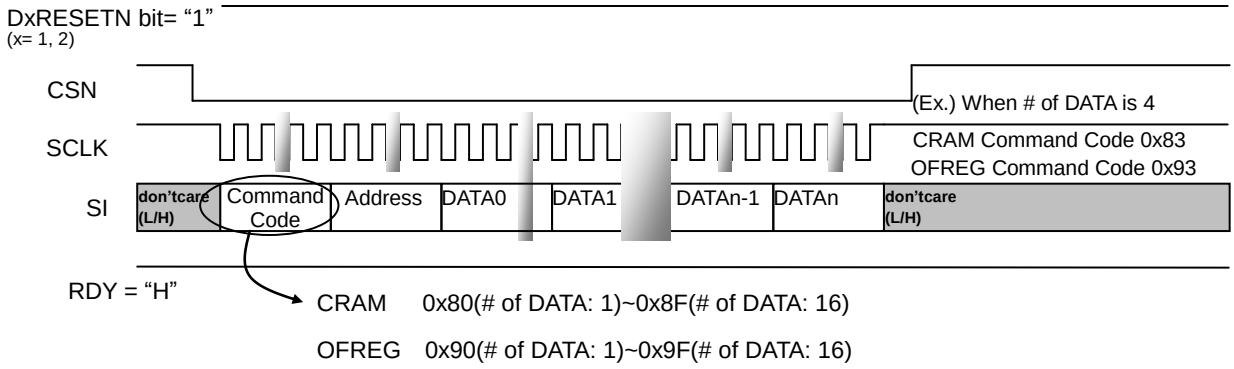


Figure 57. CRAM/OFREG Write Preparation (SPI)

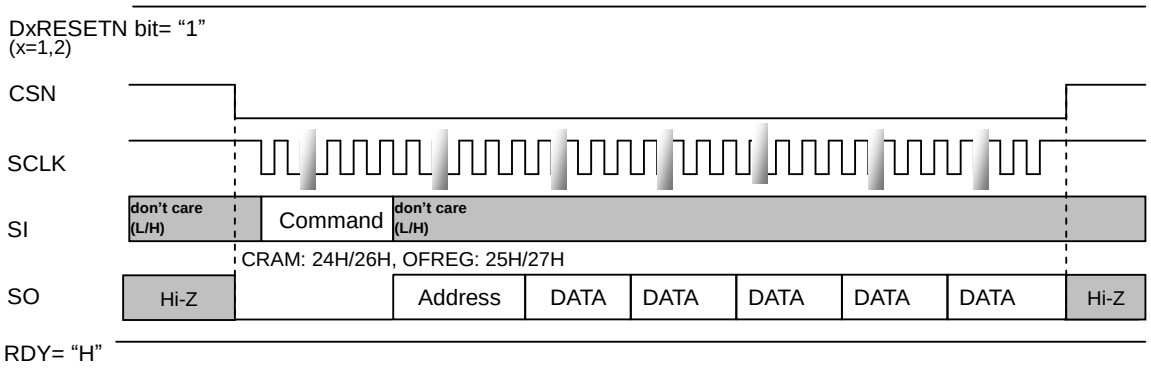


Figure 58. CRAM/OFREG Write Preparation Data Read (SPI)

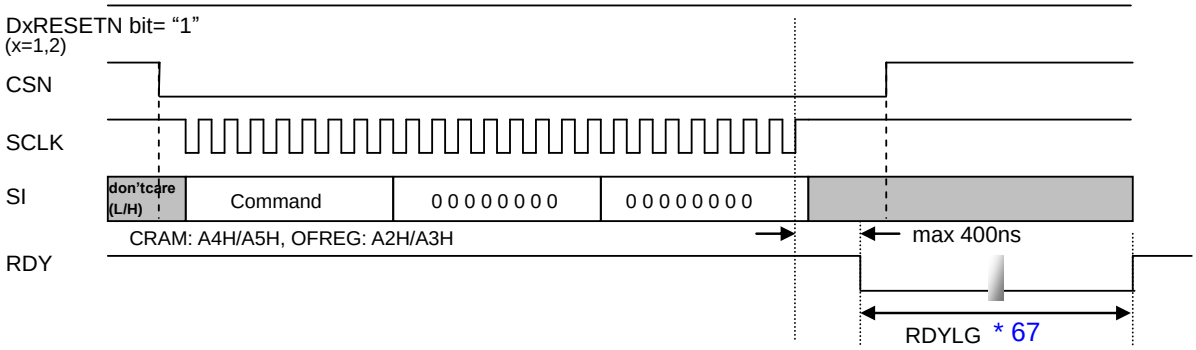


Figure 59. CRAM/OFREG Write (SPI)

Notes

* 67. The RDY pin rises to “H” in two LRCK cycles at maximum if the DSP program is designed to access the modification address in every sampling cycle. The RDY signal keeps “L” level even if a write command is completed internally while CSN is “L” level.

* 68. Writing to a CRAM or OFREG address that is not used in the DSP program is prohibited during RUN. If it is executed, the RDY pin keeps “L” output until the PDN pin becomes “L”. In the case of I^2C interface mode, communication will not be made correctly after that.

4-3. External Conditional Jump

External Conditional Jump Code Writing

(1) COMMAND	0xF4 (DSP1) / 0xF5 (DSP2)
(2) Address0	0 0 0 0 0 0 0 0
(3) Address1	0 0 0 0 0 0 0 0
(4) DATA	D7~D0

An External Conditional Jump code can be input during both DSP Reset and RUN. Input data is set to the designated register on the rising edge of LRCK assigned to the DSP. The RDY pin changes to “L” when the command code is transferred, and it changes to “H” when write operations are completed.

This Jump code is reset to 0 by setting the PDN pin to “L”, but it is not reset by DSP reset or Clock reset.

A DSP instruction setting is necessary when using external conditional jump code.

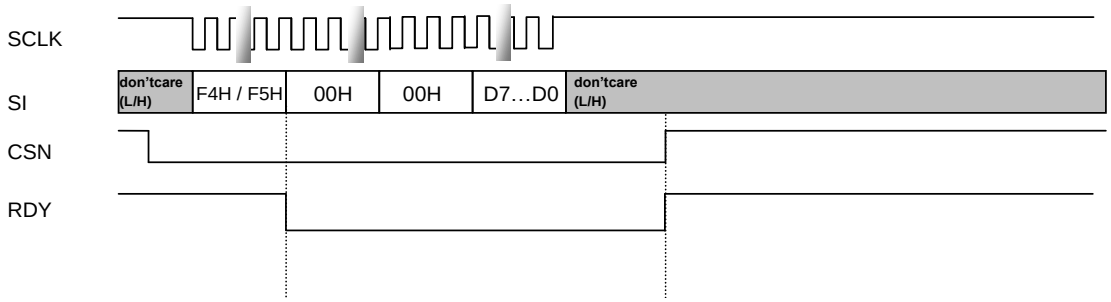


Figure 60. External Conditional Jump Timing (SPI)

■ I²C Interface

Access to the AK7735 registers and RAM can be controlled by an I²C bus. The AK7735 supports fast-mode I²C-bus (max: 400kHz) and fast-mode plus (max: 1MHz).

SI/I2CFIL pin	Bus Mode
L	Fast Mode
H	Fast Mode Plus

Table 34. I²C Bus Mode Setting

Note
* 69. The CSN pin and the SI/I2CFIL pin must be fixed to “L” or “H” when using I²C interface. The AK7735 does not support Hs mode (max: 3.4MHz).

1. Data Transfer

In order to access any IC devices on the I²C bus, input a start condition first, followed by one byte of Slave address which includes the Device Address. IC devices on the BUS compare this Device address with their own addresses and the IC device which has an identical address with the Device address generates an acknowledgement. An IC device with the identical address then executes either a read or a write operation. After the command execution, input a Stop condition.

1-1. Data Change

Change the data on the SDA line while the SCL line is “L”. The SDA line condition must be stable and fixed while the clock is “H”. Change the Data line condition between “H” and “L” only when the clock signal on the SCL line is “L”. Change the SDA line condition while the SCL line is “H” only when the start condition or stop condition is input.

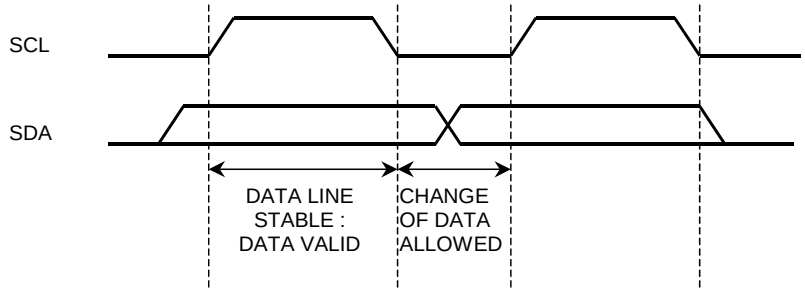


Figure 61. Data Change I²C)

1-2. Start Condition and Stop Condition

A start condition is generated by the transition of “H” to “L” on the SDA line while the SCL line is “H”. All instructions are initiated by a Start condition. A stop condition is generated by the transition of “L” to “H” on the SDA line while the SCL line is “H”. All instructions end by a Stop condition.

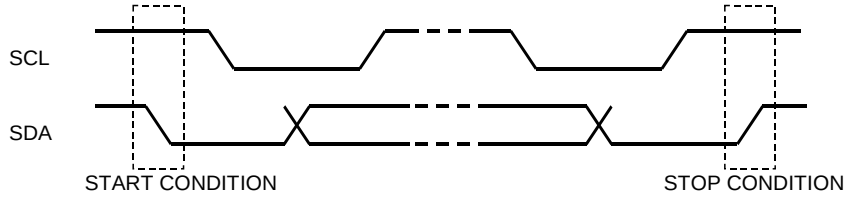


Figure 62. Start Condition and Stop Condition (I²C)

1-3. Repeated Start Condition

When a Start condition is received again instead of a Stop condition, the bus changes to a Repeated Start condition. A Repeated Start condition is functionally the same as a Start condition.

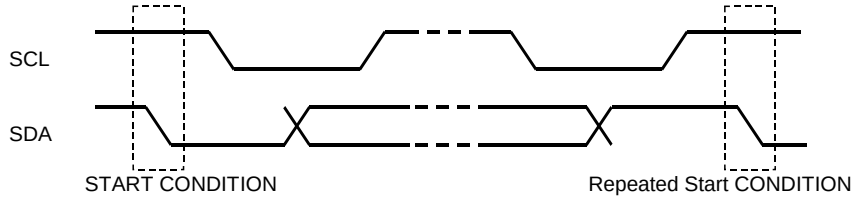


Figure 63. Repeated Start Condition (I^2C)

1-4. Acknowledge

The IC device that sends data releases the SDA line (“H”) after sending one byte of data. The IC device that receives data then sets the SDA line to “L” at the next clock. This operation is called “acknowledgement”, and it enables verification that the data transfer has been properly executed.

The AK7735 generates an acknowledgement upon receipt of a Start condition and a Slave address. For a write instruction, an acknowledgement is generated whenever receipt of each byte is completed. For a read instruction, succeeded by generation of an acknowledgement, the AK7735 releases the SDA line after outputting data at the designated address, and it monitors the SDA line condition. When the Master side generates an acknowledgement without sending a Stop condition, the AK7735 outputs data at the next address location. When no acknowledgement is generated, the AK7735 ends data output (not acknowledged).

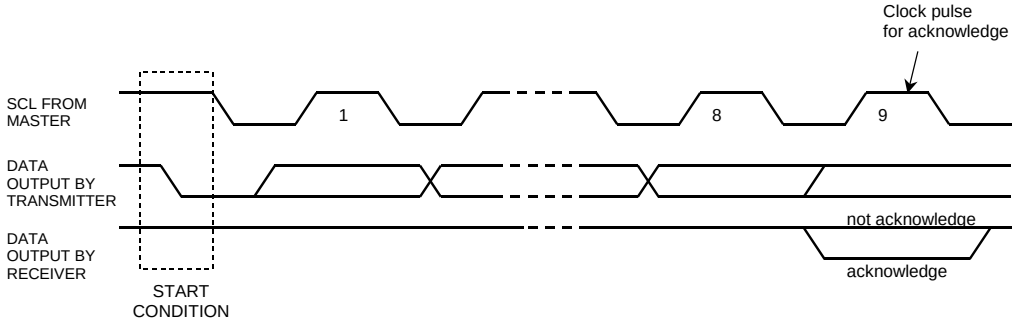


Figure 64. Generation of Acknowledgement (I^2C)

1-5. The First Byte

The First Byte, which includes the Slave-address, is input after the Start condition is set, and a target IC device that will be accessed on the bus is selected by the Slave-address.

When the Slave-address is inputted, an external device that has the identical device address generates an acknowledgement and instructions are then executed. The 8th bit of the First Byte (lowest bit) is allocated as the R/W Bit. When the R/W Bit is "1", the read instruction is executed, and when it is "0", the write instruction is executed.

The Slave-address of the AK7735 is set by the CSN pin.

CSN pin = "H"	0	0	1	1	0	0	0	R/W
CSN pin = "L"	0	0	1	1	1	0	0	R/W

Figure 65. First Byte Configuration (I^2C)

Note

* 70. In this document, there is a case that describes a "Write Slave-address assignment" when both address bits match and a Slave-address at R/W Bit = "0" is received. There is a case that describes "Read Slave-address assignment" when both address bits matches and a Slave-address at R/W Bit = "1" is received.

1-6. The Second and Succeeding Bytes

The data format of the second and succeeding bytes of the AK7735 Transfer / Receive Serial data (command code, address and data in microcontroller interface format) on the I^2C BUS are all configured with a multiple of 8-bits. When transferring or receiving those data on the I^2C BUS, they are divided into an 8-bit data stream segment and they are transferred / received with the MSB side data first with an acknowledgement in-between.

Example)
When transferring / receiving A1B2C3 (hex) 24-bit serial data in microprocessor interface format:

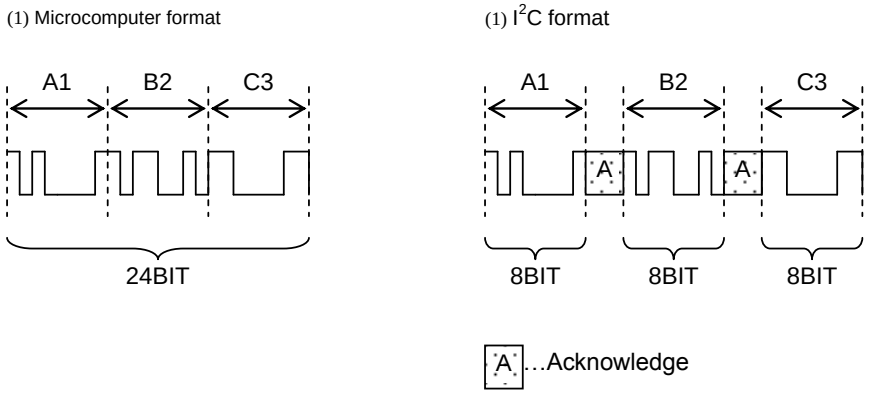


Figure 66. Division of Data (I^2C)

Note

* 71. In this document, there is a case that describes a write instruction command code which is received at the second byte as "Write Command". There is a case that describes a read instruction command code which is received at the second byte as "Read Command".

2. Write Sequence

In the AK7735, when a “Write-Slave-address assignment” is received at the first byte, the write command at the second byte, the address at the third and fourth bytes, and data at the fifth and succeeding bytes are received. The number of write data bytes is fixed by the received command code.

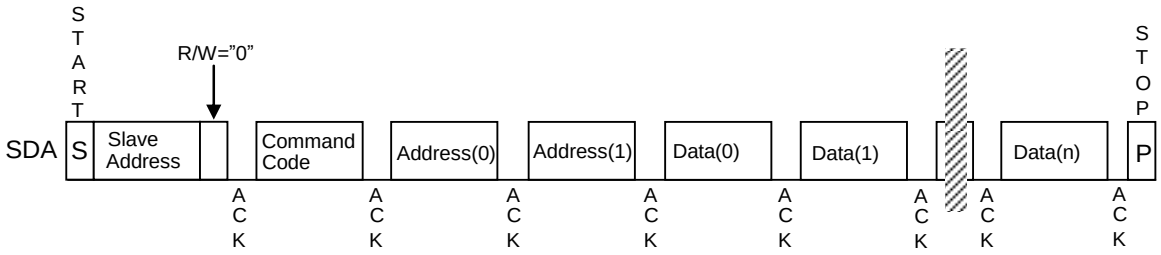


Figure 67. Write Sequence (I^2C)

3. Read Sequence

In the AK7735, when a “write- slave-address assignment” is received at the first byte, the read command at the second byte and the address at the third and fourth bytes are received. When the fourth byte is received and an acknowledgement is transferred, the read command waits for the next restart condition. When a “read slave-address assignment” is received at the first byte, data is transferred at the second and succeeding bytes. The number of readable data bytes is fixed by the received read command.

After reading the last byte, assure that a “not acknowledged” signal is received. If this “not acknowledged” signal is not received, the AK7735 continues to send data regardless whether data is present or not, and since it did not release the BUS, the stop condition cannot be properly received.

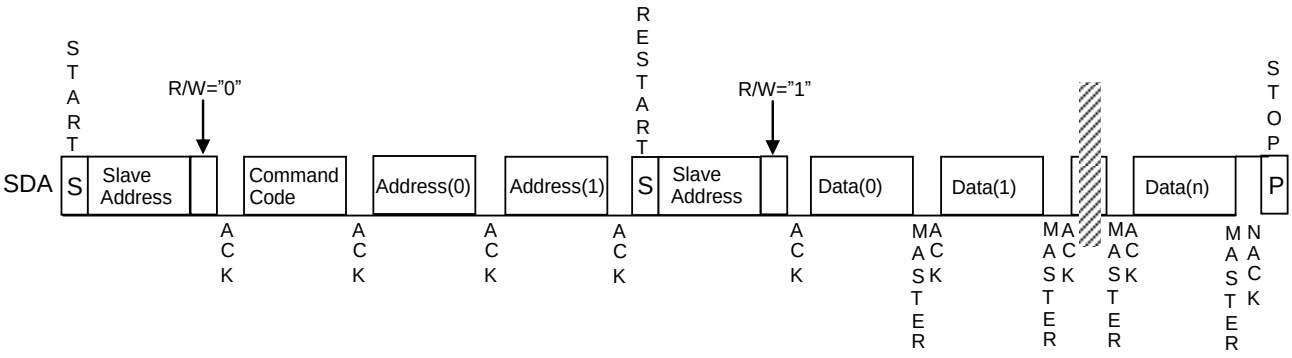


Figure 68. Read Sequence (I^2C)

4. Not Acknowledge

The AK7735 cannot receive instructions while the RDY pin (Data Write Ready pin) is at a low level. The maximum transition time of the RDY pin from low level to high level is 2 × LRCK. It is possible to confirm in a faster cycle than 2 x LRCK that the RDY pin becomes high by checking the AK7735 internal condition, which is made by verifying the acknowledgement.

4-1. Generation of "Not Acknowledge"

The AK7735 does not accept command codes until the RDY pin becomes high, when a command is received to set the RDY pin to a low level. In order to confirm the RDY pin condition, a "Write Slave-Address assignment" should be sent after the Start condition. If the RDY pin is then at a low level, "Acknowledgement" is not generated at the succeeding clock (generation of "Not Acknowledged").

After sending "Not Acknowledged", the BUS is released and all receiving data are ignored until the next start condition (behaves as if it received Slave address of other device).

4-2. When Read Slave-address assignment is received without receiving Read command code

Data read in the AK7735 can be made only in the previously documented Read sequence. Data cannot be read out without receiving a read command code. In the AK7735, a "Not Acknowledged" is generated when a "Read Slave-address Assignment" without proper receipt of read command is received.

5. Limitation in use of I2C Interface

The AK7735 does not operate in Hs Mode (max: 3.4MHz). The AK7735 supports Fast mode (max: 400kHz) and Fast plus mode (max: 1MHz).

Note

* 72. Do not turn off the power of the AK7735 whenever the power supplies of other devices of the same system are turned on. Pull-up resistors of SDA and SCL pins should be connected to TVDD or less voltage. (The diodes against TVDD exist in the SDA and SCL pins.)

■ Simple Write Error Check

The AK7735 have a cyclic redundancy check (CRC) function for a simple checking of writing data for RAM and registers.

1. Checked Data

1-1. SPI Interface

SI data during CSN = "L" is checked.

- Serial Data D(x): SI data which is input during a period from a falling edge to a rising edge of CSN
- Generator Polynomial $G(x)=x^{16}+x^{12}+x^5+1$ (Divisor=0x1021, Default=0, MSB-first, Not Inverted)
- The remainder of D(x) divided by G(x) is R(x).

1-2. I^2C Interface

Command code, address and data from the second byte are checked. (Acknowledge is not included. Therefore, the checked result will be the same as the SPI interface if the same command code, address and data are written.) The first byte which includes a slave address is not checked. It can be checked by Acknowledge.

- Serial Data D(x): Command Code, Address and Data (Slave Address is not included)
- Generator Polynomial $G(x)=x^{16}+x^{12}+x^5+1$ (Divisor=0x1021, Default=0, MSB-first, Not Inverted)
- The remainder of D(x) divided by G(x) is R(x).

2. Simple Write Error Check Sequence

There are two ways to check write error.

2-1. CRC Result

(1) Write serial data D(x) to be checked.
(2) Read out a CRC result (remainder R(x)) by the command code 72H.
(3) Check the result by a microprocessor.
(4) When checking other serial data, repeat the sequence from (1) to (3).
Note
* 73. The internal CRC result is not updated by command code 72H.

2-2. STO pin State

(1) Set control register CRCE bit to "1".
(2) Write serial data D(x) to be checked.
(3) Write the R(x) value to registers by the command code F2H.
(4) If the remainder of D(x) divided by G(x) is equal to R(x), the STO pin outputs "H". If not, it outputs "L".
(5) When checking other serial data, repeat the sequence from (2) to (4).
Note
* 74. The STO pin keeps outputting "L" until a correct value of R(x) is written in sequence (3).

■ DSP Block

1. Settings of DSP Memory

The AK7735 integrates two DSPs (DSP1 and DSP2) which have the same architecture. The DSP1 and the DSP2 share program RAM (PRAM), coefficient RAM (CRAM) data RAM (DRAM) and delay RAM (DLRAM). Assigned memory area for each DSP is set by register settings. Both DSPs must be in reset state when setting memory assignment.

PRAMDIV bit controls PRAM assignment for DSP1 and DSP2. CRAMDIV[1:0] bits control CRAM assignment, DRAMDIV bit controls DRAM assignment and DLRAMDIV[1:0] bits control DLRAM assignment.

Mode	PRAMDIV bit	DSP1	DSP2	
0	0	2048 word	2048 word	(default)
1	1	4096 word	Reset	

Table 35. PRAM Assignment for DSP1 and DSP2

Note
* 75. The DSP2 must be reset when setting to Mode 1 (PRAMDIV bit = “1”).

Mode	CRAMDIV[1:0] bits	DSP1	DSP2	
0	00	4096 word	2048 word	(default)
1	01	2048 word	4096 word	
2	10	6144 word	Reset	
3	11	N/A	N/A	

Table 36. CRAM Assignment for DSP1 and DSP2 (N/A: Not Available)

Note
* 76. The DSP2 must be reset when setting to Mode 2 (CRAMDIV[1:0] bits = “10”).

Mode	DRAMDIV bit	DSP1	DSP2	
0	0	2048 word	2048 word	(default)
1	1	4096 word	Reset	

Table 37. DRAM Assignment for DSP1 and DSP2

Note
* 77. The DSP2 must be reset when setting to Mode 1 (DRAMDIV bit = “1”).

Mode	DLRAMDIV[1:0] bits	DSP1	DSP2	
0	00	12288 word	Not Connected	(default)
1	01	8192 word	4096 word	
2	10	4096 word	8192 word	
3	11	Not Connected	12288 word	

Table 38. DLRAM Assignment for DSP1 and DSP2

Note
* 78. The DSP1 and DSP2 can be operated without connecting to DLRAM. However, program access to DLRAM is not permitted.

BANK size and BANK addressing mode of DRAM, that is assigned, can be set independently for the DSP1 and the DSP2.

DRAM BANK sizes for DSP1 and DSP2 are controlled by D1DRMBK[1:0] bits and D2DRMBK[1:0] bits, respectively.

Mode	D1DRMBK[1:0] bits D2DRMBK[1:0] bits	BANK 1 Size	BANK 0 Size	
0	00	1024	Rest of Area	(default)
1	01	2048	Rest of Area	
2	10	3072	Rest of Area	
3	11	N/A	N/A	

Table 39. DRAM BANK Size Setting for DSP1 and DSP2 (N/A: Not Available)

DRAM BANK addressing modes for DSP1 and DSP2 are controlled by D1DRMA[1:0] bits and D2DRMA[1:0] bits, respectively.

Mode	D1DRMA[1:0] bits D2DRMA[1:0] bits	BANK 1 (DP1)	BANK 0 (DP0)	
0	00	Ring	Ring	(default)
1	01	Ring	Linear	
2	10	Linear	Ring	
3	11	Linear	Linear	

Table 40. DRAM BANK Addressing Mode Setting for DSP1 and DSP2

BANK size and BANK addressing mode of DLRAM, that is assigned, can be set independently for the DSP1 and DSP2.

DLRAM BANK sizes for DSP1 and DSP2 are controlled by D1DLRMBK[2:0] bits and D2DLRMBK[2:0] bits, respectively.

Mode	D1DLRMBK [2:0] bits D2DLRMBK [2:0] bits	BANK 1 Size	BANK 0 Size	
0	000	0	Rest of Area	(default)
1	001	2048 word	Rest of Area	
2	010	4096 word	Rest of Area	
3	011	6144 word	Rest of Area	
4	100	8192 word	Rest of Area	
5	101	10240 word	Rest of Area	
6	110	12288 word	0	
7	111	N/A	N/A	

Table 41. DLRAM BANK Size Setting for DSP1 and DSP2 (N/A: Not Available)

DLRAM BANK addressing modes for DSP1 and DSP2 are controlled by D1DLRMA bit and D2DLRMA bit, respectively.

Mode	D1DLRMA bit D2DLRMA bit	BANK 1	BANK 0	
0	0	Ring	Ring	(default)
1	1	Linear	Ring	

Table 42. DLRAM BANK Addressing Mode Setting for DSP1 and DSP2

Sampling mode of DLRAM BANK 0 for the DSP1 and DSP2 are controlled by D1SS[1:0] bits and D2SS[1:0] bits, respectively.

Mode	D1SS[1:0] bits D2SS[1:0] bits	Sampling Mode of DLRAM BANK 0	
0	00	Update Address in Every Sampling	(default)
1	01	Update Address in Every 2 Samplings	
2	10	Update Address in Every 4 Samplings	
3	11	Update Address in Every 8 Samplings	

Table 43. DLRAM BANK0 Sampling Mode setting of DSP1/DSP2

The DSP1 and DSP2 are able to generate a trigonometric COS table for trigonometric processing. Input 1/4 cycle data of the COS table to CRAM and the DSP generates rest of 3/4 cycle data automatically. COS table length for CRAM input is variable according to the cycle resolution setting. The cycle resolution of DSP1 and DSP2 is controlled by D1WAVP[2:0] bits and D2WAVP[2:0] bits, respectively.

Mode	D1WAVP[2:0] bits D2WAVP[2:0] bits	Cycle Resolution	COS Table Length	
0	000	128 points	33 word	(default)
1	001	256 points	65 word	
2	010	512 points	129 word	
3	011	1024 points	257 word	
4	100	2048 points	513 word	
5	101	4096 points	1025 word	
6	110	N/A	N/A	
7	111	N/A	N/A	

Table 44. Cycle Resolution Setting of Trigonometric Table for DSP1/DSP2 (N/A: Not Available)

2. Soft SRC Function

DOUT1 port of DSP1 has a built-in FIFO to realize synchronous SRC program for sampling rate conversion. The output data of DOUT1 port of DSP1 can be up sampled by the FIFO.

A DSP filtering process is necessary when using the soft SRC function. The soft SRC is capable of integral multiple conversion of a sampling rate between two synchronized clock sync domains, supporting 6 times up sampling at maximum.

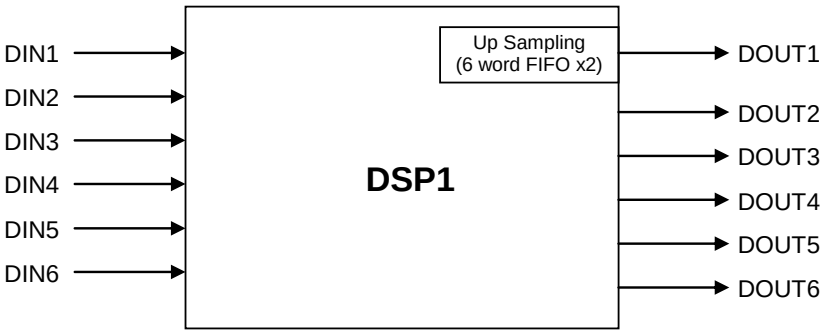


Figure 69. DSP1 Soft SRC Function

■ Analog Input Block

1. Microphone Input Gain

The AK7735 has gain amplifiers for microphone input. The gain of L and R channels can be independently selected by MGNL[3:0] and MGNR[3:0] bits (Table 45). The input impedance is typ. 20kΩ when ADC1VL/R bits is “0” and it is typ.25 kΩ when ADC1VL/R bits are “1”. This gain amplifier executes zero crossing detection when changing the gain by setting MICLZCE bit = “1” / MICRZCE bit = “1”. Zero crossing detection is executed independently for L and R channels. Zero crossing timeout period is 16ms (@fs=48kHz base). When MICLZCE bit = “0”/ MICRZCE bit = “0”, the volume is changed immediately by register settings.

When writing to MGNL/R[3:0] bits continuously, take an interval of zero crossing timeout period or more. If the MGNL/R[3:0] bits are changed before zero crossing, the volume of Lch and Rch may differ. When the volume level that is same as the present volume is set, the zero crossing counter is not reset and time outs according to the previous writing timing. Therefore, in this case, writing to MGNL/R [3:0] bits continuously is possible with a shorter interval of the zero crossing timeout period.

1-1. Microphone Gain

Mode	MGNL[3] MGNR[3]	MGNL[2] MGNR[2]	MGNL[1] MGNR[1]	MGNL[0] MGNR[0]	Input Gain	
0	0	0	0	0	0dB	(default)
1	0	0	0	1	2dB	
2	0	0	1	0	4dB	
3	0	0	1	1	6dB	
4	0	1	0	0	8dB	
5	0	1	0	1	10dB	
6	0	1	1	0	12dB	
7	0	1	1	1	14dB	
8	1	0	0	0	16dB	
9	1	0	0	1	18dB	
A	1	0	1	0	21dB	
B	1	0	1	1	24dB	
C	1	1	0	0	27dB	
D	1	1	0	1	30dB	
E	1	1	1	0	33dB	
F	1	1	1	1	36dB	

Table 45. Microphone Input Gain

1-2. Zero Crossing Timeout

The microphone gain is changed independently on the timing of zero crossing detection or zero crossing timeout.

	48kHz base	44.1kHz base
Zero Crossing Timeout Period	16ms	17.4ms

Table 46. Zero Crossing Timeout Period

1-3. Start-up Time of MIC Input Pin

The AK7735 starts to charge a DC cut capacitor when the PDN pin is set to “H” from “L”. Since the input impedance is 25kΩ, the time constant will be 25ms if the DC cut capacitor is 1μF. A wait time of about 100ms should be taken before power up the ADC to charge the DC cut capacitor sufficiently. A click noise may occur just after the ADC is powered up if this wait time is not enough.

2. Microphone Input Selector

The AK7735 has microphone input selectors. Each microphone amplifier input is selectable between single-ended input and differential input by AD1LSEL bit or AD1RSEL bit.

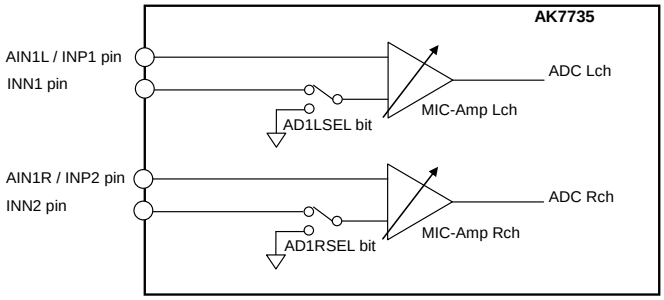


Figure 70. Microphone Input Selector

AD1LSEL bit	ADC Lch	
0	INP1/INN1	(default)
1	AIN1L	

AD1RSEL bit	ADC Rch	
0	INP2/INN2	(default)
1	AIN1R	

Table 47. Microphone Input Selector

Note

* 79. When using differential input mode, it is prohibited to input signal to only one side like pseudo differential input.

3. Microphone Bias Output

The AK7735 has a line of microphone bias output. The power supply of microphone is supplied from the MPWR pin by setting PMMB bit = “1”. The output voltage is 2.5V (AVDD=3.3V) and the load resistance is min. 2kΩ.

PMMB bit	MPWR pin	
0	Hi-Z	(default)
1	Output	

Table 48. Microphone Bias Output

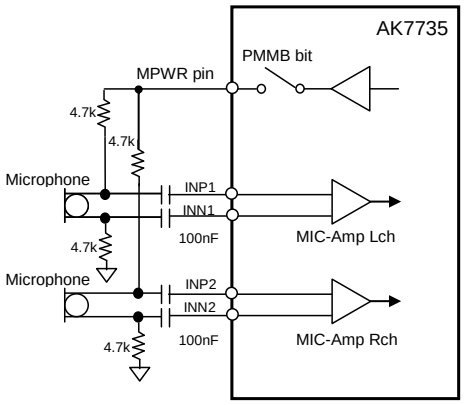


Figure 71. MIC Block Circuit (Differential Input)

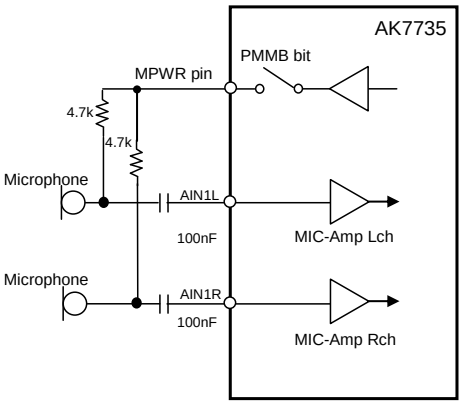


Figure 72. MIC Block Circuit (Single-end Input)

■ ADC Block

1. ADC Block High Pass Filter

The AK7735 has a digital high pass filter (HPF) for DC offset cancelling of each ADC. The cut-off frequency of the HPF is about 0.9Hz (fs=48kHz), depending on operation frequency.

2. ADC Digital Volume

The AK7735 has independent digital volume controls for Lch and Rch (256 levels, 0.5dB steps) of each ADC.

ADC1 VOLAD1L[7:0]	ADC1 VOLAD1R[7:0]	ADC2 VOLAD2L[7:0]	ADC2 VOLAD2R[7:0]	Attenuation Level	
00h	00h	00h	00h	+24.0dB	
01h	01h	01h	01h	+23.5dB	
02h	02h	02h	02h	+23.0dB	
:	:	:	:	:	
2Fh	2Fh	2Fh	2Fh	+0.5dB	
30h	30h	30h	30h	0.0dB	(default)
31h	31h	31h	31h	-0.5dB	
:	:	:	:	:	
FDh	FDh	FDh	FDh	-102.5dB	
FEh	FEh	FEh	FEh	-103.0dB	
FFh	FFh	FFh	FFh	Mute (-∞)	

Table 49. ADC Digital Volume Control Setting

The transition time between set values is selected by ATSPAD bit.

Mode	ATSPAD bit	Transition Time	
0	0	4/fs	(default)
1	1	16/fs	

Table 50. ADC Volume Level Transition Time

The transition between set values is soft transition. It takes 1020/fs (21.3ms@fs=48kHz) from 00h to FFh(MUTE) in Mode 0. If the PDN pin goes to “L”, the volume of each ADC channel is initialized to 30h.

ATSPAD bit	00h ⇔ FFh Transition Time				
	LRCK Cycle	fs=48kHz	fs=44.1kHz	fs=8kHz	
0	1020/fs	21.3ms	23.1ms	127.5ms	(default)
1	1020/fs x4	85.0ms	92.5ms	510.0ms	

Table 51. ADC Volume Transition Time from 00h to FFh

code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	dB
00h	24.0	20h	8.0	40h	-8.0	60h	-24.0	80h	-40.0	A0h	-56.0	C0h	-72.0	E0h	-88.0
01h	23.5	21h	7.5	41h	-8.5	61h	-24.5	81h	-40.5	A1h	-56.5	C1h	-72.5	E1h	-88.5
02h	23.0	22h	7.0	42h	-9.0	62h	-25.0	82h	-41.0	A2h	-57.0	C2h	-73.0	E2h	-89.0
03h	22.5	23h	6.5	43h	-9.5	63h	-25.5	83h	-41.5	A3h	-57.5	C3h	-73.5	E3h	-89.5
04h	22.0	24h	6.0	44h	-10.0	64h	-26.0	84h	-42.0	A4h	-58.0	C4h	-74.0	E4h	-90.0
05h	21.5	25h	5.5	45h	-10.5	65h	-26.5	85h	-42.5	A5h	-58.5	C5h	-74.5	E5h	-90.5
06h	21.0	26h	5.0	46h	-11.0	66h	-27.0	86h	-43.0	A6h	-59.0	C6h	-75.0	E6h	-91.0
07h	20.5	27h	4.5	47h	-11.5	67h	-27.5	87h	-43.5	A7h	-59.5	C7h	-75.5	E7h	-91.5
08h	20.0	28h	4.0	48h	-12.0	68h	-28.0	88h	-44.0	A8h	-60.0	C8h	-76.0	E8h	-92.0
09h	19.5	29h	3.5	49h	-12.5	69h	-28.5	89h	-44.5	A9h	-60.5	C9h	-76.5	E9h	-92.5
0Ah	19.0	2Ah	3.0	4Ah	-13.0	6Ah	-29.0	8Ah	-45.0	AAh	-61.0	CAh	-77.0	EAh	-93.0
0Bh	18.5	2Bh	2.5	4Bh	-13.5	6Bh	-29.5	8Bh	-45.5	ABh	-61.5	CBh	-77.5	EBh	-93.5
0Ch	18.0	2Ch	2.0	4Ch	-14.0	6Ch	-30.0	8Ch	-46.0	ACh	-62.0	CCh	-78.0	ECh	-94.0
0Dh	17.5	2Dh	1.5	4Dh	-14.5	6Dh	-30.5	8Dh	-46.5	ADh	-62.5	CDh	-78.5	EDh	-94.5
0Eh	17.0	2Eh	1.0	4Eh	-15.0	6Eh	-31.0	8Eh	-47.0	AEh	-63.0	CEh	-79.0	EEh	-95.0
0Fh	16.5	2Fh	0.5	4Fh	-15.5	6Fh	-31.5	8Fh	-47.5	AFh	-63.5	CFh	-79.5	EFh	-95.5
10h	16.0	30h	0.0	50h	-16.0	70h	-32.0	90h	-48.0	B0h	-64.0	D0h	-80.0	F0h	-96.0
11h	15.5	31h	-0.5	51h	-16.5	71h	-32.5	91h	-48.5	B1h	-64.5	D1h	-80.5	F1h	-96.5
12h	15.0	32h	-1.0	52h	-17.0	72h	-33.0	92h	-49.0	B2h	-65.0	D2h	-81.0	F2h	-97.0
13h	14.5	33h	-1.5	53h	-17.5	73h	-33.5	93h	-49.5	B3h	-65.5	D3h	-81.5	F3h	-97.5
14h	14.0	34h	-2.0	54h	-18.0	74h	-34.0	94h	-50.0	B4h	-66.0	D4h	-82.0	F4h	-98.0
15h	13.5	35h	-2.5	55h	-18.5	75h	-34.5	95h	-50.5	B5h	-66.5	D5h	-82.5	F5h	-98.5
16h	13.0	36h	-3.0	56h	-19.0	76h	-35.0	96h	-51.0	B6h	-67.0	D6h	-83.0	F6h	-99.0
17h	12.5	37h	-3.5	57h	-19.5	77h	-35.5	97h	-51.5	B7h	-67.5	D7h	-83.5	F7h	-99.5
18h	12.0	38h	-4.0	58h	-20.0	78h	-36.0	98h	-52.0	B8h	-68.0	D8h	-84.0	F8h	-100.0
19h	11.5	39h	-4.5	59h	-20.5	79h	-36.5	99h	-52.5	B9h	-68.5	D9h	-84.5	F9h	-100.5
1Ah	11.0	3Ah	-5.0	5Ah	-21.0	7Ah	-37.0	9Ah	-53.0	BAh	-69.0	DAh	-85.0	FAh	-101.0
1Bh	10.5	3Bh	-5.5	5Bh	-21.5	7Bh	-37.5	9Bh	-53.5	BBh	-69.5	DBh	-85.5	FBh	-101.5
1Ch	10.0	3Ch	-.6.0	5Ch	-22.0	7Ch	-38.0	9Ch	-54.0	BCh	-70.0	DCh	-86.0	FCh	-102.0
1Dh	9.5	3Dh	-6.5	5Dh	-22.5	7Dh	-38.5	9Dh	-54.5	BDh	-70.5	DDh	-86.5	FDh	-102.5
1Eh	9.0	3Eh	-7.0	5Eh	-23.0	7Eh	-39.0	9Eh	-55.0	BEh	-71.0	DEh	-87.0	FEh	-103.0
1Fh	8.5	3Fh	-7.5	5Fh	-23.5	7Fh	-39.5	9Fh	-55.5	BFh	-71.5	DFh	-87.5	FFh	Mute

Table 52. ADC Digital Volume Settings

3. ADC Soft Mute

The ADC block has a digital soft mute circuit. The soft mute operation is performed at digital domain. The output signal is attenuated to -∞ in “ATT setting level x ATT transition time” from the current ADC digital volume setting level by setting AD1MUTE bit or AD2MUTE bit to “1”. When the AD1MUTE bit or AD2MUTE bit returns to “0”, the mute is cancelled and the output attenuation level gradually changes to ATT setting level in “ATT setting level x ATT transition time”. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and the volume level returns to original volume setting level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

The attenuation level transition takes 828/fs from 0dB to -∞ and from -∞ to 0dB. Soft mute function is available when each ADC is in operation. The attenuation value is initialized by setting the PDN pin = “L”.

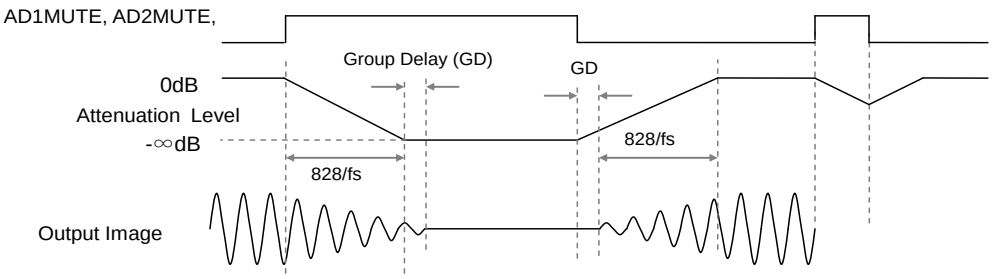


Figure 73. ADC Soft Mute

4. ADC2 Input Selector

ADC2 of the AK7735 has an input selector for 1 stereo differential input and 2 stereo single-ended inputs. These inputs are selected by AD2SEL[1:0] bits. In the case that these registers are changed during operation, mute output signal to reduce switching noise as needed.

Mode	AD2SEL[1:0] bits	Selected Pin	
0	00	AIN2LP, AIN2LN, AIN2RP, AIN2RN	(default)
1	01	AIN3L, AIN3R	
2	10	AIN4L, AIN4R	
3	11	N/A	

Table 53. ADC2 Input Select (N/A: Not Available)

Note

* 80. When using differential input mode, it is prohibited to input signal to only one side like pseudo differential input.

4-1. Input Selector Switching Sequence

The input selector should be changed after enabling soft mute function to avoid the switching noise of the input selector.

ADC2 Input selector switching sequence:
1) Enable Soft Mute Function before Changing Channel
2) Change Channel
3) Disable Soft Mute Function

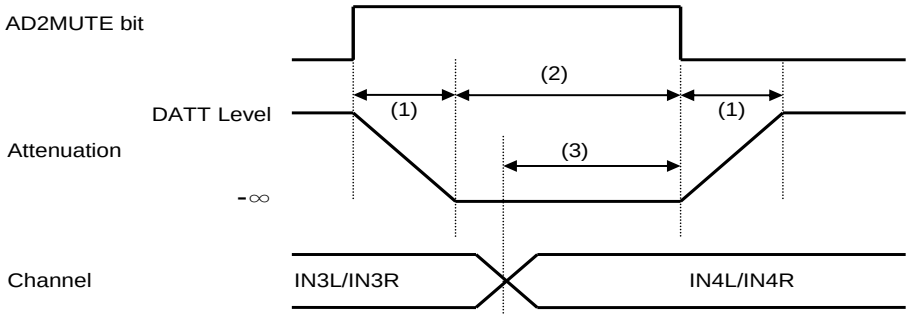


Figure 74. ADC2 Input Channel Switching Sequence Example

The period of (1) varies according to the setting value of the DATT level. Transition time of attenuation level from 0dB to -∞ is shown below.

ATSPAD bit	(1) Period (Max)				
	LRCK Cycle	fs=48kHz	fs=44.1kHz	fs=8kHz	
0	828/fs	17.25ms	18.78ms	103.5ms	(default)
1	828/fs x 4	69ms	75.10ms	414ms	

The input channel should be changed during the period (2). An interval around 200ms is needed before releasing the soft mute after changing the channel (period (3)).

5. ADC Digital Filter Select

The AK7735 has four kinds of digital filters in ADC block. ADSD and ADSL bits select a digital filter. ADC1 and ADC2 have a common setting for digital filter.

Mode	ADSD bit	ADSL bit	Digital Filter	
0	0	0	Sharp Roll-Off Filter	(default)
1	0	1	Slow Roll-Off Filter	
2	1	0	Short Delay Sharp Roll-Off Filter	
3	1	1	Short Delay Slow Roll-Off Filter	

Table 54. ADC Digital Filter Select

6. ADC Input Volume Selection

Single-ended input amplitude (differential input amplitude) of ADC1 L/Rch and ADC2 L/Rch can be switched between 2.3Vpp (±2.3Vpp) and 2.83Vpp (±2.83Vpp) by ADC1VL/R bit and ADC2VL/R bit, respectively.

Mode	ADC1VL bit / ADC1VR bit ADC2VL bit / ADC2VR bit	Input Full Scale Voltage		
		Single-end Input	Differential Input	
0	0	2.3Vpp	±2.3Vpp	(default)
1	1	2.83Vpp	±2.83Vpp	

Table 55. ADC Input Full Scale Voltage Selection

■ DAC Block

1. DAC Digital Volume

The AK7735 has channel-independent digital volume controls in DAC block. (256 levels, 0.5 steps)

DAC1 Lch VOLDA1L[7:0]	DAC1 Rch VOLDA1R[7:0]	DAC2 Lch VOLDA2L[7:0]	DAC2 Rch VOLDA2R[7:0]	Attenuation Level	
00h	00h	00h	00h	+12.0dB	
01h	01h	01h	01h	+11.5dB	
02h	02h	02h	02h	+11.0dB	
:	:	:	:	:	
17h	17h	17h	17h	+0.5dB	
18h	18h	18h	18h	0.0dB	(default)
19h	19h	19h	19h	-0.5dB	
:	:	:	:	:	
FDh	FDh	FDh	FDh	-114.5dB	
FEh	FEh	FEh	FEh	-115.0dB	
FFh	FFh	FFh	FFh	Mute (-∞)	

Table 56. DAC Digital Volume Setting

Transition time between set values can be selected by ATSPDA bit.

MODE	ATSPDA	Transition Time	
0	0	4/fs	(default)
1	1	16/fs	

Table 57. DAC Volume Transition Time Setting

The transition between set values is soft transition. It takes 1020/fs (21.3ms@fs=48kHz) from 00h to FFh (MUTE) in Mode 0. If the PDN pin is set to “L”, the VOLDA1L[7:0], VOLDA1R[7:0], VOLDA2L[7:0] and VOLDA2R[7:0] bits are initialized to 18h.

ATSPDA bit	00h ↔ FFh Transition Time				
	LRCK Cycle	fs=48kHz	fs=44.1kHz	fs=8kHz	
0	1020/fs	21.3ms	23.1ms	127.5ms	(default)
1	1020/fs x4	85.0ms	92.5ms	510.0ms	

Table 58. DAC Volume Transition Time (00h ↔ FFh)

code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	DB	code	dB
00h	12.0	20h	-4.0	40h	-20.0	60h	-36.0	80h	-52.0	A0h	-68.0	C0h	-84.0	E0h	-100.0
01h	11.5	21h	-4.5	41h	-20.5	61h	-36.5	81h	-52.5	A1h	-68.5	C1h	-84.5	E1h	-100.5
02h	11.0	22h	-5.0	42h	-21.0	62h	-37.0	82h	-53.0	A2h	-69.0	C2h	-85.0	E2h	-101.0
03h	10.5	23h	-5.5	43h	-21.5	63h	-37.5	83h	-53.5	A3h	-69.5	C3h	-85.5	E3h	-101.5
04h	10.0	24h	-.6.0	44h	-22.0	64h	-38.0	84h	-54.0	A4h	-70.0	C4h	-86.0	E4h	-102.0
05h	9.5	25h	-6.5	45h	-22.5	65h	-38.5	85h	-54.5	A5h	-70.5	C5h	-86.5	E5h	-102.5
06h	9.0	26h	-7.0	46h	-23.0	66h	-39.0	86h	-55.0	A6h	-71.0	C6h	-87.0	E6h	-103.0
07h	8.5	27h	-7.5	47h	-23.5	67h	-39.5	87h	-55.5	A7h	-71.5	C7h	-87.5	E7h	-103.5
08h	8.0	28h	-8.0	48h	-24.0	68h	-40.0	88h	-56.0	A8h	-72.0	C8h	-88.0	E8h	-104.0
09h	7.5	29h	-8.5	49h	-24.5	69h	-40.5	89h	-56.5	A9h	-72.5	C9h	-88.5	E9h	-104.5
0Ah	7.0	2Ah	-9.0	4Ah	-25.0	6Ah	-41.0	8Ah	-57.0	AAh	-73.0	CAh	-89.0	EAh	-105.0
0Bh	6.5	2Bh	-9.5	4Bh	-25.5	6Bh	-41.5	8Bh	-57.5	ABh	-73.5	CBh	-89.5	EBh	-105.5
0Ch	6.0	2Ch	-10.0	4Ch	-26.0	6Ch	-42.0	8Ch	-58.0	ACh	-74.0	CCh	-90.0	ECh	-106.0
0Dh	5.5	2Dh	-10.5	4Dh	-26.5	6Dh	-42.5	8Dh	-58.5	ADh	-74.5	CDh	-90.5	EDh	-106.5
0Eh	5.0	2Eh	-11.0	4Eh	-27.0	6Eh	-43.0	8Eh	-59.0	AEh	-75.0	CEh	-91.0	EEh	-107.0
0Fh	4.5	2Fh	-11.5	4Fh	-27.5	6Fh	-43.5	8Fh	-59.5	AFh	-75.5	CFh	-91.5	EFh	-107.5
10h	4.0	30h	-12.0	50h	-28.0	70h	-44.0	90h	-60.0	B0h	-76.0	D0h	-92.0	F0h	-108.0
11h	3.5	31h	-12.5	51h	-28.5	71h	-44.5	91h	-60.5	B1h	-76.5	D1h	-92.5	F1h	-108.5
12h	3.0	32h	-13.0	52h	-29.0	72h	-45.0	92h	-61.0	B2h	-77.0	D2h	-93.0	F2h	-109.0
13h	2.5	33h	-13.5	53h	-29.5	73h	-45.5	93h	-61.5	B3h	-77.5	D3h	-93.5	F3h	-109.5
14h	2.0	34h	-14.0	54h	-30.0	74h	-46.0	94h	-62.0	B4h	-78.0	D4h	-94.0	F4h	-110.0
15h	1.5	35h	-14.5	55h	-30.5	75h	-46.5	95h	-62.5	B5h	-78.5	D5h	-94.5	F5h	-110.5
16h	1.0	36h	-15.0	56h	-31.0	76h	-47.0	96h	-63.0	B6h	-79.0	D6h	-95.0	F6h	-111.0
17h	0.5	37h	-15.5	57h	-31.5	77h	-47.5	97h	-63.5	B7h	-79.5	D7h	-95.5	F7h	-111.5
18h	0.0	38h	-16.0	58h	-32.0	78h	-48.0	98h	-64.0	B8h	-80.0	D8h	-96.0	F8h	-112.0
19h	-0.5	39h	-16.5	59h	-32.5	79h	-48.5	99h	-64.5	B9h	-80.5	D9h	-96.5	F9h	-112.5
1Ah	-1.0	3Ah	-17.0	5Ah	-33.0	7Ah	-49.0	9Ah	-65.0	BAh	-81.0	DAh	-97.0	FAh	-113.0
1Bh	-1.5	3Bh	-17.5	5Bh	-33.5	7Bh	-49.5	9Bh	-65.5	BBh	-81.5	DBh	-97.5	FBh	-113.5
1Ch	-2.0	3Ch	-18.0	5Ch	-34.0	7Ch	-50.0	9Ch	-66.0	BCh	-82.0	DCh	-98.0	FCh	-114.0
1Dh	-2.5	3Dh	-18.5	5Dh	-34.5	7Dh	-50.5	9Dh	-66.5	BDh	-82.5	DDh	-98.5	FDh	-114.5
1Eh	-3.0	3Eh	-19.0	5Eh	-35.0	7Eh	-51.0	9Eh	-67.0	BEh	-83.0	DEh	-99.0	FEh	-115.0
1Fh	-3.5	3Fh	-19.5	5Fh	-35.5	7Fh	-51.5	9Fh	-67.5	BFh	-83.5	DFh	-99.5	FFh	Mute

Table 59. DAC Digital Volume Level Setting

2. DAC Soft Mute

The DAC block has a digital soft mute circuit. The soft mute operation is performed at digital domain. The output signal is attenuated to -∞ in “ATT setting level x ATT transition time” from the current DAC digital volume setting level by setting DA1MUTE bit or DA2MUTE bit to “1”. When the DA1MUTE bit or DA2MUTE bit returns to “0”, the mute is cancelled and the output attenuation level gradually changes to ATT setting level in “ATT setting level x ATT transition time”. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and the volume level returns to original volume setting level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

The attenuation level transition takes 924/fs from 0dB to -∞ and from -∞ to 0dB. Soft mute function is available when each DAC is in operation. The attenuation value is initialized by setting the PDN pin = “L”.

The DAC1 (DAC2) is reset by setting PMDA1 bit (PMDA2 bit) to “0”. A click noise may occur when reset the DAC block and releasing the reset. The output signal should be muted externally if the click noise adversely affects the system performance.

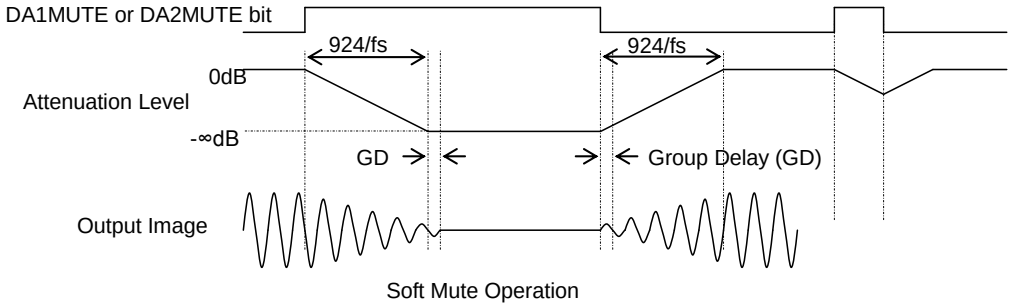


Figure 75. DAC Soft Mute Operation

Analog ouptut pins will output VCOM voltage by setting HRESETN bit = “1” → “0” while PMDAx bit is “1”. Use this mode when changing system clock during DAC operation to prevent a click noise caused by resuming DAC operation after changing the system clock (Figure 76, CASE1).
Analog outputs goes to Hi-z state by setting HRESETN bi = “1” → “0” while PMDAx bit is “0”. Therefore a click noise may occur when resuming DAC operation after changing the system clock (Figure 76, CASE2). The output signal should be muted externally if the click noise adversely affects the system performance.

PMDAx bit	HRESETN bit	Analog Output
0	0	Hi-Z Output
0	1	Hi-Z Output
1	0	VCOM Voltage Output
1	1	Normal Operation

Table 60. Analog Output Status during HUB Reset

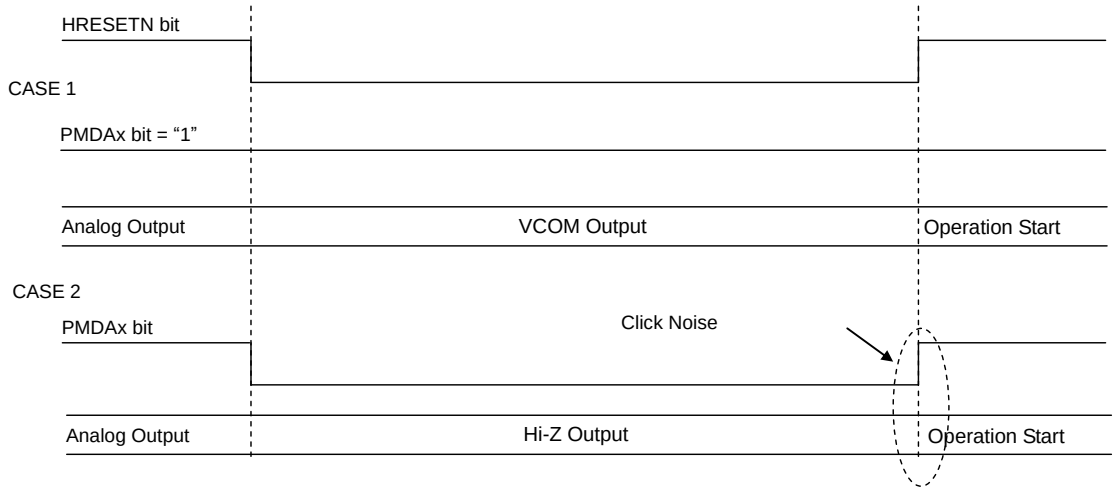


Figure 76. Analog Output Status during HUB Reset

3. DAC Digital Filter Select

The AK7735 has four kinds of digital filters in DAC block. DASD and DASL bits select a digital filter. DAC1 and DAC2 have a common digital filter setting.

Mode	DASD bit	DASL bit	Digital Filter	
0	0	0	Sharp Roll-Off Filter	(default)
1	0	1	Slow Roll-Off Filter	
2	1	0	Short Delay Sharp Roll-Off Filter	
3	1	1	Short Delay Slow Roll-Off Filter	

Table 61. DAC Digital Filter Select

4. DAC De-emphasis Filter Control

The AK7735 has a digital de-emphasis filter (tc=50/15µs) that corresponds to three sampling frequencies (32kHz, 44.1kHz and 48kHz) by IIR filter. The de-emphasis filter frequency is selected by DEMx[1:0] bits (x=1, 2) (Table 62).

The de-emphasis filer only corresponds to the frequencies shown in Table 62. DEMx[1:0] bits must be set to the default setting “01” when the AK7735 is operated with other sampling frequencies.

DEMx[1] bit	DEMx[0] bit	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 62. DAC De-emphasis Filter Control

■ SRC Block

1. Sampling Rate

The AK7735 includes two stereo digital sampling rate converters (SRC). The input sampling rate (FSI) and the output sampling rate (FSO) are supported from 8kHz to 192kHz. Available sampling rate ratio is FSO/FSI = 0.167~6.0.

1-1. Up Sampling (1.00 ≤ FSO/FSI ≤ 6.00)

Supported sampling rates are shown below. (Passband and Stopband are proportional to FSI when the FSO/FSI ratios are same.)

FSO	FSI	FSO/FSI	Passband	Stopband
192kHz	48kHz	4.00	22.00kHz	26.00kHz
48kHz	48kHz	1.00	22.00kHz	26.00kHz
48kHz	44.1kHz	1.09	20.21kHz	23.89kHz
48kHz	32kHz	1.50	14.67kHz	17.33kHz
48kHz	24kHz	2.00	11.00kHz	13.00kHz
48kHz	16kHz	3.00	7.33kHz	8.67kHz
48kHz	12kHz	4.00	5.50kHz	6.50kHz
48kHz	8kHz	6.00	3.67kHz	4.33kHz
192kHz	44.1kHz	4.35	20.21kHz	23.89kHz
44.1kHz	44.1kHz	1.00	20.21kHz	23.89kHz
44.1kHz	32kHz	1.38	14.67kHz	17.33kHz
44.1kHz	24kHz	1.84	11.00kHz	13.00kHz
44.1kHz	16kHz	2.76	7.33kHz	8.67kHz
44.1kHz	12kHz	3.68	5.50kHz	6.50kHz
44.1kHz	8kHz	5.51	3.67kHz	4.33kHz
16kHz	16kHz	1.00	7.33kHz	8.67kHz
16kHz	8kHz	2.00	3.67kHz	4.33kHz
8kHz	8kHz	1.00	3.67kHz	4.33kHz

Table 63. Up Sampling Example

1-2. Down Sampling (0.167 ≤ FSO/FSI < 1.00)

Three kinds of filter mode can be selected by SRCFAUD bit and SRCFEC bit when down sampling. Supported sampling rates are shown below. (Passband and Stopband are proportional to FSI when the FSO/FSI ratios are same.)

1) Audio Mode (SRCFAUD bit = “1”, SRCFEC bit = “0”)

FSO	FSI	FSO/FSI	Passband	Stopband
44.1kHz	48kHz	0.919	20.00kHz	24.10kHz
48kHz	88.2kHz	0.544	19.25kHz	26.23kHz
48kHz	96kHz	0.5	20.90kHz	27.00kHz
44.1kHz	88.2kHz	0.5	19.20kHz	24.81kHz
44.1kHz	96kHz	0.459	18.70kHz	25.00kHz
16kHz	44.1kHz	0.363	5.79kHz	7.95kHz
48kHz	192kHz	0.25	25.19kHz	34.60kHz
44.1kHz	192kHz	0.229	25.19kHz	34.60kHz
8kHz	48kHz	0.167	3.16kHz	4.66kHz
8kHz	44.1kHz	0.181	2.90kHz	4.28kHz

Table 64. Down Sampling Example (Audio Mode)

2) Voice Mode (SRCFAUD bit = “0”, SRCFEC bit = “0”)

FSO	FSI	FSO/FSI	Passband	Stopband
24kHz	32kHz	0.75	10.94kHz	11.95kHz
16kHz	24kHz	0.667	7.22kHz	7.97kHz
16kHz	32kHz	0.5	7.14kHz	7.97kHz
8kHz	16kHz	0.5	3.57kHz	3.98kHz
16kHz	48kHz	0.333	6.80kHz	7.97kHz
8kHz	32kHz	0.25	3.26kHz	3.99kHz

Table 65. Down Sampling Example (Voice Mode)

3) Echo Canceller Mode (SRCFEC bit = “1”)

In echo canceller mode, the input signal should be attenuated sufficiently for more than FSO/2 frequency.

FSO	FSI	FSO/FSI	Passband	Stopband
32kHz	44.1kHz	0.726	20.21kHz	23.89kHz
32kHz	48kHz	0.667	22.00kHz	26.00kHz
24kHz	44.1kHz	0.544	20.21kHz	23.89kHz
24kHz	48kHz	0.5	22.00kHz	26.00kHz
16kHz	44.1kHz	0.363	20.21kHz	23.89kHz
16kHz	48kHz	0.333	22.00kHz	26.00kHz

Table 66. Down Sampling Example (Echo Canceller Mode)

2. SRC Input/Output

Input sources of SRC1~2 are selected by SELSRCI1[5:0] and SELSRCI2[5:0] bits (Table 19, Table 20). The input clock sync domains are inherited from the input data. The output clock sync domains are set by SDSRCO1[2:0] and SDSRCO2[2:0] bits (Table 19, Table 20). Then the output data is sent to the data bus.

3. SRC Soft Mute

The SRC1 and SRC2 have soft mute function independently.

3-1. Manual Mode

When SMUTEx bit (x=1, 2) is set to “1”, the SRC output data are attenuated to −∞ in 1024 FSO cycles. When the SMUTEx bit is set to “0”, the mute is cancelled and the output attenuation level gradually changes to 0dB in 1024 FSO cycles. If the soft mute is cancelled before mute state, the attenuation is discontinued and the attenuation level returns to 0dB by the same cycles. The soft mute is effective for changing the signal source without stopping the signal.

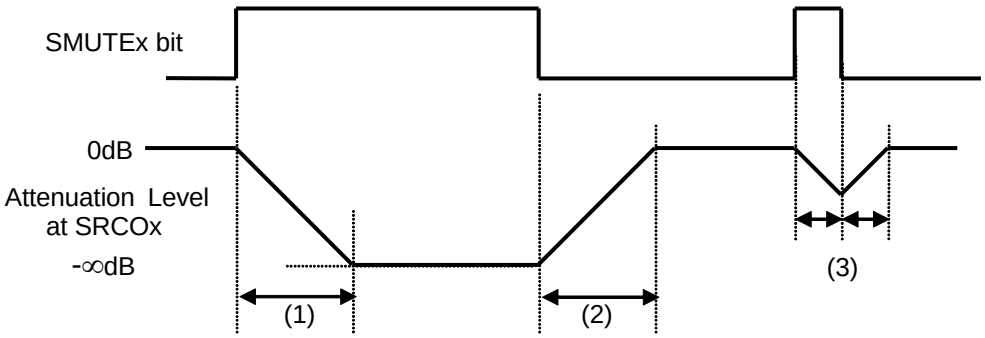


Figure 77. Soft Mute Manual Mode

(1) SMUTEx bit (x=1, 2) = “0”→“1”: The output data is attenuated to −∞ during 1024 FSO cycles.
(2) SMUTEx bit (x=1, 2) =“1”→“0”: The output attenuation level gradually changes to 0dB from −∞ in 1024 FSO cycles.
(3) If the soft mute is cancelled within 1024 FSO cycles, the attenuation is discontinued and the attenuation level returns to 0dB by the same number of clock cycles.

3-2. Semi-Auto Mode

Semi-automatic soft mute mode is set by SAUTOx bit (x=1, 2) = “1”. In this mode, soft mute is released within 21.25ms after continuing the mute when PMSRCx bit (x=1, 2) is set to “1”. If SMUTEx bit is “1” when PMSRCx bit is released (“0” → “1”), the soft mute is not cancelled.

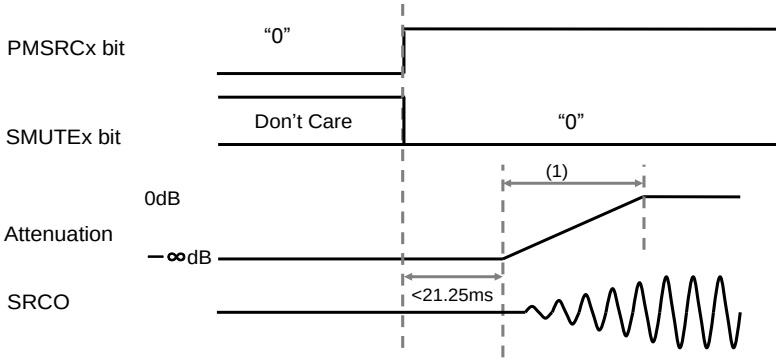


Figure 78. Soft Mute Semi-Auto Mode

(1) The attenuation level of the output data is changed to 0dB by 1024 FSO cycles.

4. SRC Reset

Bringing PMSRCx bit (x= 1, 2) to “0” resets the SRC of the AK7735 and initializes the digital filters. When PMSRCx bit = “0”, the SRC output is “L”. The SRC outputs data within 21ms by releasing the SRC reset (PMSRCx bit = “1”) after inputting a clock. Until then, the SRC outputs “L”. Before releasing the PMSRCx bit to “1”, the SRC settings should be completed.

Case 1

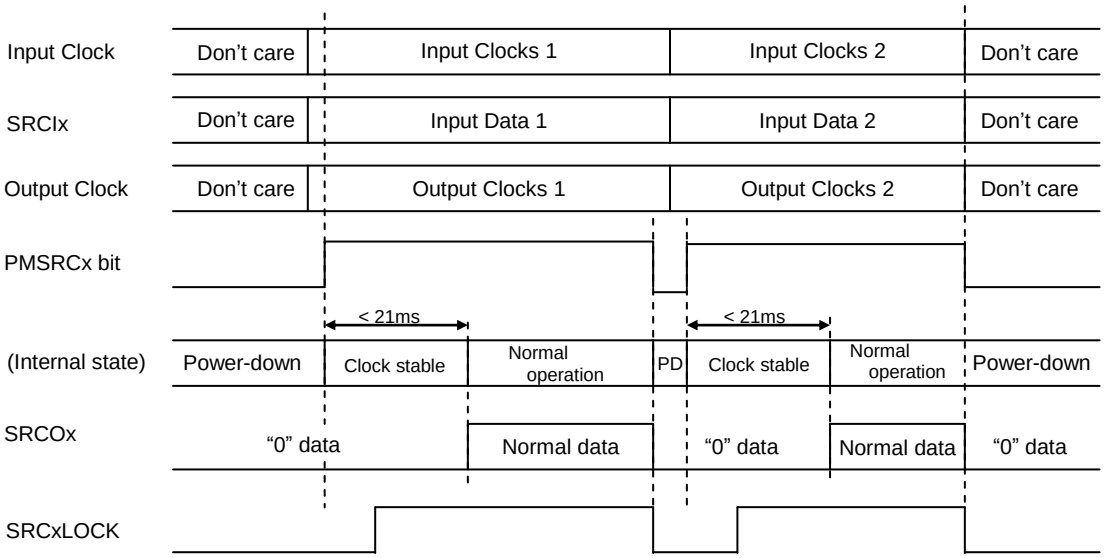


Figure 79. SRC Reset Example 1

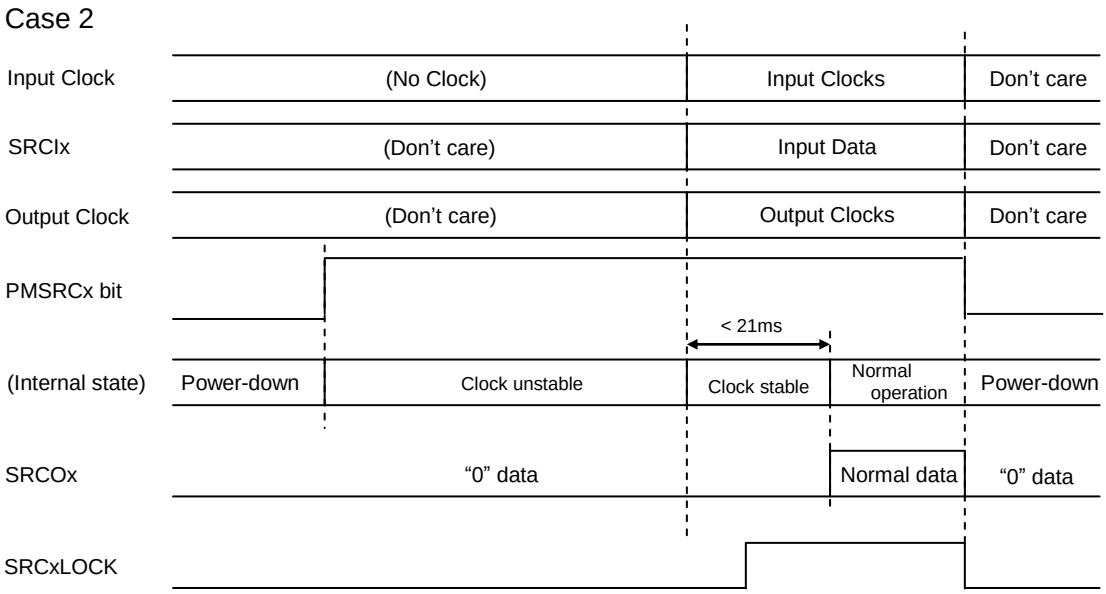


Figure 80. SRC Reset Example 2

5. SRC Clock Change

5-1. Internal Reset Function for Clock Change

The SRC block executes internal reset automatically when an input or output clock is stopped. Normal data will be output within 21ms after the clock is restarted.

5-2. Clock Change Sequence

A clock change sequence of SRC is shown in Figure 81.

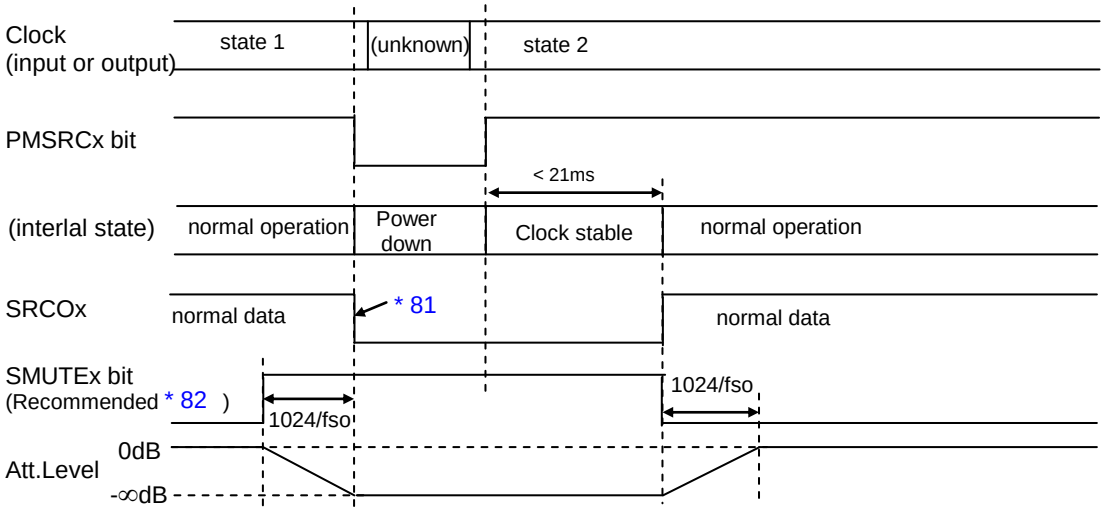


Figure 81. SRC Clock Change Sequence

Notes

* 81. The data on SRC output may cause a clicking noise. To prevent this, input "0" data to SRC input (SRCIx) before PMSRCx bit (x= 1, 2) is set to "0", that will keep the data on SRC output as "0".
* 82. This click noise (* 81) can also be removed by setting SMUTEx bit (x= 1, 2).

6. SRC Lock

The STO pin outputs the SRC status by setting SRCLOCKEx bit (x= 1, 2) to “1”. The STO pin outputs “H” if the SRC is locked, and outputs “L” when the SRC is unlocked or when the SRC is in reset state (PMSRCx bit = “0”).

7. Group Delay when using SRCs in the Same Rate

When SRC1 and SRC2 use the same Sync Domain for input clock (FSI) and the same Sync Domain for output clock (FSO), a maximum 2xFSO mismatch of group delay may occur between them. This group delay mismatch can be avoided by setting PMSRC1 and PMSRC2 bits to “1” simultaneously after setting SRCPHGR bit to “1”. A click noise may occur if PMSRC1/2 bits are not set to “1” at the same time when SRCPHGR bit is “1”.

■ Register Map

Control registers can be initialized by a power-down release (PDN pin = “L” → “H”).

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	default
0000	System Clock Setting 1	0	REFSEL[1:0]		REFMODE[4:0]					00
0001	System Clock Setting 2	CKRESETN	0	0	FSMODE[4:0]					00
0002	Mic Bias Power Management	0	0	0	0	0	0	0	PMMB	00
0003	Sync Domain 1 Setting 1	BDV1[9]	BDV1[8]	CKS1[2:0]			SDV1[2:0]			00
0004	Sync Domain 1 Setting 2	BDV1[7:0]								00
0005	Sync Domain 2 Setting 1	BDV2[9]	BDV2[8]	CKS2[2:0]			SDV2[2:0]			00
0006	Sync Domain 2 Setting 2	BDV2[7:0]								00
0007	Sync Domain 3 Setting 1	BDV3[9]	BDV3[8]	CKS3[2:0]			SDV3[2:0]			00
0008	Sync Domain 3 Setting 2	BDV3[7:0]								00
0009	Sync Domain 4 Setting 1	BDV4[9]	BDV4[8]	CKS4[2:0]			SDV4[2:0]			00
000A	Sync Domain 4 Setting 2	BDV4[7:0]								00
000B	Sync Domain M/S Setting	0	0	0	0	0	MSN3	MSN2	MSN1	00
000C	Reserved	0	0	0	0	0	0	0	0	00
000D	CLKO Output Setting	0	0	0	0	CLKOE	CLKOSEL[2:0]			00
000E	Reserved	0	0	0	0	0	0	0	0	00
000F	Sync Domain Select 1	0	SDBCK1[2:0]			0	SDBCK2[2:0]			00
0010	Sync Domain Select 2	0	SDBCK3[2:0]			0	0	0	0	00
0011	Sync Domain Select 3	0	SDDSP1[2:0]			0	SDDSP2[2:0]			00
0012	Sync Domain Select 4	0	SDDSP1O1[2:0]			0	SDDSP1O2[2:0]			00
0013	Sync Domain Select 5	0	SDDSP1O3[2:0]			0	SDDSP1O4[2:0]			00
0014	Sync Domain Select 6	0	SDDSP1O5[2:0]			0	SDDSP1O6[2:0]			00
0015	Sync Domain Select 7	0	SDDSP2O1[2:0]			0	SDDSP2O2[2:0]			00
0016	Sync Domain Select 8	0	SDDSP2O3[2:0]			0	SDDSP2O4[2:0]			00
0017	Sync Domain Select 9	0	SDDSP2O5[2:0]			0	SDDSP2O6[2:0]			00
0018	Sync Domain Select 10	0	SDSRCO1[2:0]			0	SDSRCO2[2:0]			00
0019	Sync Domain Select 11	0	SDADC1[2:0]			0	SDCODEC[2:0]			00
001A	Sync Domain Select 12	0	SDDO1[2:0]			0	SDDO2[2:0]			00
001B	Sync Domain Select 13	0	SDDO3[2:0]			0	SDDO4[2:0]			00
001C	External Clock Domain Select	EXBCK4[1:0]		EXBCK3[1:0]		EXBCK2[1:0]		EXBCK1[1:0]		00
001D	Reserved	0	0	0	0	0	0	0	0	00
001E	Reserved	0	0	0	0	0	0	0	0	00
001F	SDOUT1A Output Data Select	0	0	SELDO1A[5:0]						00
0020	SDOUT1B Output Data Select	0	0	SELDO1B[5:0]						00
0021	SDOUT1C Output Data Select	0	0	SELDO1C[5:0]						00
0022	SDOUT1D Output Data Select	0	0	SELDO1D[5:0]						00
0023	SDOUT2A Output Data Select	0	0	SELDO2A[5:0]						00
0024	SDOUT2B Output Data Select	0	0	SELDO2B[5:0]						00
0025	SDOUT2C Output Data Select	0	0	SELDO2C[5:0]						00
0026	SDOUT2D Output Data Select	0	0	SELDO2D[5:0]						00
0027	SDOUT3A Output Data Select	0	0	SELDO3A[5:0]						00
0028	SDOUT3B Output Data Select	0	0	SELDO3B[5:0]						00
0029	SDOUT3C Output Data Select	0	0	SELDO3C[5:0]						00
002A	SDOUT3D Output Data Select	0	0	SELDO3D[5:0]						00
002B	SDOUT4A Output Data Select	0	0	SELDO4A[5:0]						00
002C	SDOUT4B Output Data Select	0	0	SELDO4B[5:0]						00
002D	SDOUT4C Output Data Select	0	0	SELDO4C[5:0]						00
002E	SDOUT4D Output Data Select	0	0	SELDO4D[5:0]						00
002F	DAC1 Input Data Select	0	0	SELDA1[5:0]						00

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	default
0030	DAC2 Input Data Select	0	0	SELDA2[5:0]						00
0031	DSP1 DIN1 Input Data Select	0	0	D1SELDI1[5:0]						00
0032	DSP1 DIN2 Input Data Select	0	0	D1SELDI2[5:0]						00
0033	DSP1 DIN3 Input Data Select	0	0	D1SELDI3[5:0]						00
0034	DSP1 DIN4 Input Data Select	0	0	D1SELDI4[5:0]						00
0035	DSP1 DIN5 Input Data Select	0	0	D1SELDI5[5:0]						00
0036	DSP1 DIN6 Input Data Select	0	0	D1SELDI6[5:0]						00
0037	DSP2 DIN1 Input Data Select	0	0	D2SELDI1[5:0]						00
0038	DSP2 DIN2 Input Data Select	0	0	D2SELDI2[5:0]						00
0039	DSP2 DIN3 Input Data Select	0	0	D2SELDI3[5:0]						00
003A	DSP2 DIN4 Input Data Select	0	0	D2SELDI4[5:0]						00
003B	DSP2 DIN5 Input Data Select	0	0	D2SELDI5[5:0]						00
003C	DSP2 DIN6 Input Data Select	0	0	D2SELDI6[5:0]						00
003D	SRC1 Input Data Select	0	0	SELSRCI1[5:0]						00
003E	SRC2 Input Data Select	0	0	SELSRCI2[5:0]						00
003F	Reserved	0	0	0	0	0	0	0	0	00
0040	Reserved	0	0	0	0	0	0	0	0	00
0041	Clock Format Setting 1	BCKP1	DCF1[2:0]			BCKP2	DCF2[2:0]			00
0042	Clock Format Setting 2	BCKP3	DCF3[2:0]			0	0	0	0	00
0043	SDIN1 Digital Input Format	DIEDGEN1	0	DISL1[1:0]		DILSBE1	0	DIDL1[1:0]		00
0044	SDIN2 Digital Input Format	DIEDGEN2	0	DISL2[1:0]		DILSBE2	0	DIDL2[1:0]		00
0045	SDIN3 Digital Input Format	DIEDGEN3	0	DISL3[1:0]		DILSBE3	0	DIDL3[1:0]		00
0046	SDIN4 Digital Input Format	DIEDGEN4	0	DISL4[1:0]		DILSBE4	0	DIDL4[1:0]		00
0047	SDOUT1 Digital Output Format	DOEDGEN1	0	DOSL1[1:0]		DOLSBE1	0	DODL1[1:0]		00
0048	SDOUT2 Digital Output Format	DOEDGEN2	0	DOSL2[1:0]		DOLSBE2	0	DODL2[1:0]		00
0049	SDOUT3 Digital Output Format	DOEDGEN3	0	DOSL3[1:0]		DOLSBE3	0	DODL3[1:0]		00
004A	SDOUT4 Digital Output Format	DOEDGEN4	0	DOSL4[1:0]		DOLSBE4	0	DODL4[1:0]		00
004B	SDOUT Phase Setting	0	0	0	0	SDOPH4	SDOPH3	SDOPH2	SDOPH1	00
004C	Output Port Enable Setting	0	0	0	0	SDOUT4E	SDOUT3E	SDOUT2EN	SDOUT1E	00
004D	Shared Input Port Select	0	0	0	0	DI3SEL	DI2SEL	LCK2SEL	BCK2SEL	00
004E	Shared Output Port Select	0	0	DO4SEL	DO3SEL[1:0]		DO2SEL[1:0]		DO1SEL	00
004F	Reserved	0	0	0	0	0	0	0	0	00
0050	MIC AMP Gain	MGNL[3:0]				MGNR[3:0]				00
0051	MIC AMP Gain Control	0	0	0	0	0	0	MICLZCE	MICRZCE	00
0052	ADC1 Lch Digital Volume	VOLAD1L[7:0]								30
0053	ADC1 Rch Digital Volume	VOLAD1R[7:0]								30
0054	ADC2 Lch Digital Volume	VOLAD2L[7:0]								30
0055	ADC2 Rch Digital Volume	VOLAD2R[7:0]								30
0056	Analog Input Select Setting	ADSD	ADSL	0	0	AD1LSEL	AD1RSEL	AD2SEL[1:0]		00
0057	ADC Mute & HPF Control	ATSPAD	AD1MUTE	AD2MUTE	0	0	0	AD1HPFN	AD2HPFN	00
0058	ADC FullScale Control	0	0	0	0	ADC1VL	ADC1VR	ADC2VL	ADC2VR	00
0059	DAC1 Lch Digital Volume	VOLDA1L[7:0]								18
005A	DAC1 Rch Digital Volume	VOLDA1R[7:0]								18
005B	DAC2 Lch Digital Volume	VOLDA2L[7:0]								18
005C	DAC2 Rch Digital Volume	VOLDA2R[7:0]								18
005D	DAC Mute & Filter Setting	ATSPDA	DA1MUTE	DA2MUTE	0	0	0	DASD	DASL	00
005E	DAC De-Emphasis Setting	0	0	0	0	DEM2[1:0]		DEM1[1:0]		05
005F	Reserved	0	0	0	0	0	0	0	0	00

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	default
0060	SRC Filter Setting	SRCFEC	SRCFAUD	0	SRCPHGR	0	0	0	0	00
0061	SRC Mute Setting	0	0	0	0	SMUTE1	SMUTE2	SAUTO1	SAUTO2	00
0062	Reserved	0	0	0	0	0	0	0	0	00
0063	Reserved	0	0	0	0	0	0	0	0	00
0064	DSP Memory Assignment	DLRAMDIV[1:0]		0	0	CRAMDIV[1:0]		DRAMDIV	PRAMDIV	00
0065	DSP1/2 DRAM Setting	D1DRMA[1:0]		D1DRMBK[1:0]		D2DRMA[1:0]		D2DRMBK[1:0]		00
0066	DSP1 DLRAM Setting	D1SS[1:0]		D1DLRMA	0	0	D1DLRMBK[2:0]			00
0067	DSP2 DLRAM Setting	D2SS[1:0]		D2DLRMA	0	0	D2DLRMBK[2:0]			00
0068	WAVP & DLP0 Setting	D1DLP0	D1WAVP[2:0]			D2DLP0	D2WAVP[2:0]			00
0069	JX Setting	D1JX0E	D1JX1E	D1JX2E	D1JX3E	D2JX0E	D2JX1E	D2JX2E	D2JX3E	00
006A	Reserved	0	0	0	0	0	0	0	0	00
006B	Reserved	0	0	0	0	0	0	0	0	00
006C	STO Flag Setting	CRCE	0	0	PLLLOCKE	SRCLOCKE1	SRCLOCKE2	D1WDTEN	D2WDTEN	00
006D	Power Management	0	0	PMSRC1	PMSRC2	PMAD1	PMAD2	PMDA1	PMDA2	00
006E	Reset Control	DLRDY	0	0	0	D1RESETN	D2RESETN	CRESETN	HRESETN	00
006F	Reserved	0	0	0	0	0	0	0	0	00
0070	Reserved	0	0	0	0	0	0	0	0	00

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	default
0100	Device ID	DEVID[7:0]								35
0101	Revision Num	REVNUM[7:0]								00
0102	DSP Error Status	CRCERRN	WDT1ERRN	WDT2ERRN	PLLLOCK	0	0	GPO1	GPO0	E0
0103	SRC Status	0	0	SRC2LOCK	SRC1LOCK	0	0	0	0	00
0104	STO Read Out	STO	0	0	0	0	0	0	0	80

Note

* 83. The bits defined as “0” must contain a “0” value. Do not write to the address other than 0000H ~ 0070H.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0000	System Clock Setting 1	0	REFSEL[1:0]		REFMODE[4:0]				
R/W		R/W	R/W		R/W				
Default		0	00		00H				

REFSEL[1:0]: PLL Reference Clock Input Pin Setting (Table 4)
Default: “00” (XTI)

REFMODE[4:0]: PLL Reference Clock Frequency Setting (Table 5)
Default: 00H (256kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0001	System Clock Setting 2	CKRESETN	0	0	FSMODE[4:0]				
R/W		R/W	R/W	R/W	R/W				
Default		0	0	0	00H				

CKRESETN: Clock Reset
0: Clock Reset (default)
1: Clock Reset Release

FSMODE[4:0]: Operation Sampling Frequency Mode Setting for Analog Block (Table 12)
Default: 00H (ADC2, DAC1, DAC2=8kHz, ADC1=8kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0002	Mic Bias Power Management	0	0	0	0	0	0	0	PMMB
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMMB: Power Management Setting for MIC Bias Output
0: Power-Off (default)
1: Normal Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0003	Sync Domain 1 Setting 1	BDV1[9]	BDV1[8]		CKS1[2:0]			SDV1[2:0]	
0004	Sync Domain 1 Setting 2	BDV1[7:0]							
0005	Sync Domain 2 Setting 1	BDV2[9]	BDV2[8]		CKS2[2:0]			SDV2[2:0]	
0006	Sync Domain 2 Setting 2	BDV2[7:0]							
0007	Sync Domain 3 Setting 1	BDV3[9]	BDV3[8]		CKS3[2:0]			SDV3[2:0]	
0008	Sync Domain 3 Setting 2	BDV3[7:0]							
0009	Sync Domain 4 Setting 1	BDV4[9]	BDV4[8]		CKS4[2:0]			SDV4[2:0]	
000A	Sync Domain 4 Setting 2	BDV4[7:0]							
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

CKSx[2:0]: Internal Divider Clock Source Setting of Sync Domain x (Table 8)
Default: “000” (TieLow)

SDVx[2:0]: MLRCK Divider Setting of Sync Domain x (Table 10)
Default: “000” (Divided by 64)

BDVx[9:0]: MBICK Divider Setting of Sync Domain x (Table 9)
Default: 000H (Divided by 1)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
000B	Sync Domain M/S Setting	0	0	0	0	0	MSN3	MSN2	MSN1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MSN3: Slave/Master Mode Setting of LRCKSD3/BICKSD3 (Table 7, Table 14)
- 0: Slave Mode (default)
- 1: Master Mode

MSN2: Slave/Master Mode Setting of LRCKSD2/BICKSD2 (Table 7, Table 14)
- 0: Slave Mode (default)
- 1: Master Mode

MSN1: Slave/Master Mode Setting of LRCKSD1/BICKSD1 (Table 7, Table 14)
- 0: Slave Mode (default)
- 1: Master Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
000D	CLKO Output Setting	0	0	0	0	CLKOE	CLKOSEL[2:0]		
R/W		R/W	R/W	R/W	R/W	R/W	R/W		
Default		0	0	0	0	0	000		

CLKOE: Output Enable of the CLKO Pin
- 0: CLKO pin = “L” (default)
- 1: CLKO pin Output Enable

CLKOSEL[2:0]: CLKO Pin Output Clock Frequency Setting (Table 13)
Default: “000” (12.288MHz / 11.2896MHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
000F	Sync Domain Select 1	0	SDBCK1[2:0]			0	SDBCK2[2:0]		
0010	Sync Domain Select 2	0	SDBCK3[2:0]			0	0	0	0
0011	Sync Domain Select 3	0	SDDSP1[2:0]			0	SDDSP2[2:0]		
0012	Sync Domain Select 4	0	SDDSP1O1[2:0]				SDDSP1O2[2:0]		
0013	Sync Domain Select 5	0	SDDSP1O3[2:0]			0	SDDSP1O4[2:0]		
0014	Sync Domain Select 6	0	SDDSP1O5[2:0]			0	SDDSP1O6[2:0]		
0015	Sync Domain Select 7	0	SDDSP2O1[2:0]			0	SDDSP2O2[2:0]		
0016	Sync Domain Select 8	0	SDDSP2O3[2:0]			0	SDDSP2O4[2:0]		
0017	Sync Domain Select 9	0	SDDSP2O5[2:0]			0	SDDSP2O6[2:0]		
0018	Sync Domain Select 10	0	SDSRCO1[2:0			0	SDSRCO2[2:0		
0019	Sync Domain Select 11		SDADC1[2:0]			0	SDCODEC[2:0]		
001A	Sync Domain Select 12	0	SDDO1[2:0]			0	SDDO1[2:0]		
001B	Sync Domain Select 13	0	SDDO3[2:0]			0	SDDO4[2:0]		
R/W		R/W	R/W			R/W	R/W		
Default		0	000			0	000		

SDxxxx[2:0]: Sync Domain Setting of Input/Output Port for Data and Clocks (Table 19, Table 20)
Default: “000” (TieLow)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
001C	External Clock Domain Select	EXBCK4[1:0]		EXBCK3[1:0]		EXBCK2[1:0]		EXBCK1[1:0]	
R/W		R/W		R/W		R/W		R/W	
Default		00		00		00		00	

EXBCK4[1:0]: Synchronizing BICK/LRCK Pin Setting with SDIN4 Pin (Table 16)
Default: “00” (TieLow)

EXBCK3[1:0]: Synchronizing BICK/LRCK Pin Setting with SDIN3 Pin (Table 16)
Default: “00” (TieLow)

EXBCK2[1:0]: Synchronizing BICK/LRCK Pin Setting with SDIN2 Pin (Table 16)
Default: “00” (TieLow)

EXBCK1[1:0]: Synchronizing BICK/LRCK Pin Setting with SDIN1 Pin (Table 16)
Default: “00” (TieLow)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
001F	SDOUT1A Output Data Select	0	0	SELDO1A[5:0]					
0020	SDOUT1B Output Data Select	0	0	SELDO1B[5:0]					
0021	SDOUT1C Output Data Select	0	0	SELDO1C[5:0]					
0022	SDOUT1D Output Data Select	0	0	SELDO1D[5:0]					
0023	SDOUT2A Output Data Select	0	0	SELDO2A[5:0]					
0024	SDOUT2B Output Data Select	0	0	SELDO2B[5:0]					
0025	SDOUT2C Output Data Select	0	0	SELDO2C[5:0]					
0026	SDOUT2D Output Data Select	0	0	SELDO2D[5:0]					
0027	SDOUT3A Output Data Select	0	0	SELDO3A[5:0]					
0028	SDOUT3B Output Data Select	0	0	SELDO3B[5:0]					
0029	SDOUT3C Output Data Select	0	0	SELDO3C[5:0]					
002A	SDOUT3D Output Data Select	0	0	SELDO3D[5:0]					
002B	SDOUT4A Output Data Select	0	0	SELDO4A[5:0]					
002C	SDOUT4B Output Data Select	0	0	SELDO4B[5:0]					
002D	SDOUT4C Output Data Select	0	0	SELDO4C[5:0]					
002E	SDOUT4D Output Data Select	0	0	SELDO4D[5:0]					
002F	DAC1 Input Data Select	0	0	SELDA1[5:0]					
0030	DAC2 Input Data Select	0	0	SELDA2[5:0]					
0031	DSP1 DIN1 Input Data Select	0	0	D1SELDI1[5:0]					
0032	DSP1 DIN2 Input Data Select	0	0	D1SELDI2[5:0]					
0033	DSP1 DIN3 Input Data Select	0	0	D1SELDI3[5:0]					
0034	DSP1 DIN4 Input Data Select	0	0	D1SELDI4[5:0]					
0035	DSP1 DIN5 Input Data Select	0	0	D1SELDI5[5:0]					
0036	DSP1 DIN6 Input Data Select	0	0	D1SELDI6[5:0]					
0037	DSP2 DIN1 Input Data Select	0	0	D2SELDI1[5:0]					
0038	DSP2 DIN2 Input Data Select	0	0	D2SELDI2[5:0]					
0039	DSP2 DIN3 Input Data Select	0	0	D2SELDI3[5:0]					
003A	DSP2 DIN4 Input Data Select	0	0	D2SELDI4[5:0]					
003B	DSP2 DIN5 Input Data Select	0	0	D2SELDI5[5:0]					
003C	DSP2 DIN6 Input Data Select	0	0	D2SELDI6[5:0]					
003D	SRC1 Input Data Select	0	0	SELSRCI1[5:0]					
003E	SRC2 Input Data Select	0	0	SELSRCI2[5:0]					
R/W		R/W	R/W	R/W					
Default		0	0	00H					

SELxxxx[5:0]/D1SELxxxx[5:0]/D2SEL[5:0]: Source Data Select of Each Port (Table 19, Table 20)
Default: 00H (ALL0)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0041	Clock Format Setting 1	BCKP1	DCF1[2:0]			BCKP2	DCF2[2:0]		
R/W		R/W	R/W			R/W	R/W		
Default		0	000			0	000		

BCKP1: Relationship of LRCK1 and BICK1 Edges (Table 22)
0: LRCK1 Starts on a BICK1 Falling Edge (default)
1: LRCK1 Starts on a BICK1 Rising Edge

DCF1[2:0]: LRCK1/BICK1 Clock Format Setting (Table 21)
Default: "000" (I^2S Mode)

BCKP2: Relationship of LRCK2 and BICK2 Edges (Table 22)
0: LRCK2 Starts on a BICK2 Falling Edge (default)
1: LRCK2 Starts on a BICK2 Rising Edge

DCF2[2:0]: LRCK2/BICK2 Clock Format Setting (Table 21)
Default: "000" (I^2S Mode)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0042	Clock Format Setting 2	BCKP3	DCF3[2:0]			0	0	0	0
R/W		R/W	R/W			R/W	R/W	R/W	R/W
Default		0	000			0	0	0	0

BCKP3: Relationship of LRCK3 and BICK3 Edges (Table 22)
- 0: LRCK3 Starts on a BICK3 Falling Edge (default)
- 1: LRCK3 Starts on a BICK3 Rising Edge

DCF3[2:0]: LRCK3/BICK3 Clock Format Setting (Table 21)
Default: “000” (I^2S Mode)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0043	SDIN1 Digital Input Format	DIEDGEN1	0	DISL1[1:0]		DILSBE1	0	DIDL1[1:0]	
0044	SDIN2 Digital Input Format	DIEDGEN2	0	DISL2[1:0]		DILSBE2	0	DIDL2[1:0]	
0045	SDIN3 Digital Input Format	DIEDGEN3	0	DISL3[1:0]		DILSBE3	0	DIDL3[1:0]	
0046	SDIN4 Digital Input Format	DIEDGEN4	0	DISL4[1:0]		DILSBE4	0	DIDL4[1:0]	
R/W		R/W	R/W	R/W		R/W	R/W	R/W	
default		0	0	00		0	0	00	

DIEDGENx: Start Timing Setting of Data Transferring for Second and Succeeding Channels of SDINx (Table 26)
- 0: LRCK Edge Basis (default)
- 1: Slot Length Basis

DISLx[1:0]: SDINx Data Slot Length Setting (Table 23)
Default: “00” (24bit)

DILSBEx: MSB/LSB Setting of Audio Data in SDINx Data Slot (Table 25)
- 0: MSB (default)
- 1: LSB

DIDLx[1:0]: Audio Data Word Length Setting of SDINx (Table 24)
Default: “00” (24bit)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0047	SDOUT1 Digital Output Format	DOEDGEN1	0	DOSL1[1:0]		DOLSBE1	0	DODL1[1:0]	
0048	SDOUT2 Digital Output Format	DOEDGEN2	0	DOSL2[1:0]		DOLSBE2	0	DODL2[1:0]	
0049	SDOUT3 Digital Output Format	DOEDGEN3	0	DOSL3[1:0]		DOLSBE3	0	DODL3[1:0]	
004A	SDOUT4 Digital Output Format	DOEDGEN4	0	DOSL4[1:0]		DOLSBE4	0	DODL4[1:0]	
R/W		R/W	R/W	R/W		R/W	R/W	R/W	
Default		0	0	00		0	0	00	

DOEDGENx: Start Timing Setting of Data Transferring for Second and Succeeding Channels of SDOUTx (Table 26)
- 0: LRCK Edge Basis (default)
- 1: Slot Length Basis

DOSLx[1:0]: SDOUTx Data Slot Length Setting (Table 23)
Default: “00” (24bit)

DOLSBEx: MSB/LSB Setting of Audio Data in SDOUTx Data Slot (Table 25)
- 0: MSB (default)
- 1: LSB

DODLx[1:0]: Audio Data Word Length Setting of SDOUTx (Table 24)
Default: “00” (24bit)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
004B	SDOUT Phase Setting	0	0	0	0	SDOPH4	SDOPH3	SDOPH2	SDOPH1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SDOPH4: SDOUT4 Fast Mode Setting for Data Output in Slave Mode (* 47)
0: Slow mode (default)
1: Fast Mode

SDOPH3: SDOUT3 Fast Mode Setting for Data Output in Slave Mode (* 47)
0: Slow mode (default)
1: Fast Mode

SDOPH2: SDOUT2 Fast Mode Setting for Data Output in Slave Mode (* 47)
0: Slow mode (default)
1: Fast Mode

SDOPH1: SDOUT1 Fast Mode Setting for Data Output in Slave Mode (* 47)
0: Slow mode (default)
1: Fast Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
004C	Output Port Enable Setting	0	0	0	0	SDOUT4E	SDOUT3E	SDOUT2EN	SDOUT1E
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SDOUT4E: SDOUT4/GPO2 Pin Output Setting
0: SDOUT4/GPO2 pin = “L” (default)
1: SDOUT4/GPO2 pin Output Enable

SDOUT3E: SDOUT3/CLKO/GPO1 Pin Output Setting
0: SDOUT3/CLKO/GPO1 pin = “L” (default)
1: SDOUT3/CLKO/GPO1 pin Output Enable

SDOUT2EN: STO/RDY/SDOUT2 Pin Output Setting
0: STO/RDY/SDOUT2 pin Output Enable (default)
1: STO/RDY/SDOUT2 pin = “L”

SDOUT1E: SDOUT1/RDY Pin Output Setting
0: SDOUT1/RDY pin = “L” (default)
1: SDOUT1/RDY pin Output Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
004D	Shared Input Port Select	0	0	0	0	DI3SEL	DI2SEL	LCK2SEL	BCK2SEL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DI3SEL: SDIN3/JX3 Pin Input Function Setting
- 0: SDIN3 Input (default)
- 1: JX3 Input

DI2SEL: SDIN2/JX0 Pin Input Function Setting
- 0: SDIN2 Input (default)
- 1: JX0 Input

LCK2SEL: LRCK2/JX1 Pin Input Function Setting
- 0: LRCK2 Input (default)
- 1: JX1 Input (Set MSN2 bit to “0”)

BCK2SEL: BICK2/JX2 Pin Input Function Setting
- 0: BICK2 Input (default)
- 1: JX2 Input (Set MSN2 bit to “0”)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
004E	Shared Output Port Select	0	0	DO4SEL	DO3SEL[1:0]		DO2SEL[1:0]		DO1SEL
R/W		R/W	R/W	R/W	R/W		R/W		R/W
Default		0	0	0	00		00		0

DO4SEL: SDOUT4/GPO2 Pin Output Function Setting
- 0: SDOUT4 Output (default)
- 1: GPO2 Output (GPO Output of DSP2)

DO3SEL: SDOUT3/CLKO/GPO1 Pin Output Function Setting
- 00: SDOUT3 Output (default)
- 01: CLKO Output
- 10: GPO1 Output (GPO Output of DSP1)

DO2SEL: STO/RDY/SDOUT2 Pin Output Function Setting
- 00: STO Output (default)
- 01: RDY Output
- 10: SDOUT2 Output

DO1SEL: SDOUT1/RDY Pin Output Function Setting
- 0: SDOUT1 Output (default)
- 1: RDY Output

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0050	MIC AMP Gain	MGNL[3:0]				MGNR[3:0]			
R/W		R/W				R/W			
Default		0000				0000			

MGNL[3:0]: Lch Gain Setting of Microphone Input (Table 45)
Default: “0000” (0dB)

MGNR[3:0]: Rch Gain Setting of Microphone Input (Table 45)
Default: “0000” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0051	MIC AMP Gain Control	0	0	0	0	0	0	MICLZCE	MICRZCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MICLZCE: Zero Cross Enable of Lch Microphone Gain
0: Lch Zero Crossing Detection is OFF (default)
1: Lch Zero Crossing Detection is ON

MICRZCE: Zero Cross Enable of Rch Microphone Gain
0: Rch Zero Crossing Detection is OFF (default)
1: Rch Zero Crossing Detection is ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0052	ADC1 Lch Digital Volume	VOLAD1L[7:0]							
0053	ADC1 Rch Digital Volume	VOLAD1R[7:0]							
0054	ADC2 Lch Digital Volume	VOLAD2L[7:0]							
0055	ADC2 Rch Digital Volume	VOLAD2R[7:0]							
R/W		R/W							
Default		30H							

VOLAD1L[7:0]: Lch Digital Volume Setting of ADC1 (Table 49)
Default: 30H (0dB)

VOLAD1R[7:0]: Rch Digital Volume Setting of ADC1 (Table 49)
Default: 30H (0dB)

VOLAD2L[7:0]: Lch Digital Volume Setting of ADC2 (Table 49)
Default: 30H (0dB)

VOLAD2R[7:0]: Rch Digital Volume Setting of ADC2 (Table 49)
Default: 30H (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0056	Analog Input Select Setting	ADSD	ADSL	0	0	AD1LSEL	AD1RSEL	AD2SEL[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Default		0	0	0	0	0	0	00	

ADSD, ADSL: ADC Digital Filter Select (Table 54)
- 00: Sharp Roll-Off Filter (default)
- 01: Slow Roll-Off Filter
- 10: Short Delay Sharp Roll-Off Filter
- 11: Short Delay Slow Roll-Off Filter

AD1LSEL: ADC1 Lch Input Pin Select (Table 47)
- 0: INP1/INN1 (default)
- 1: AIN1L

AD1RSEL: ADC1 Rch Input Pin Select (Table 47)
- 0: INP2/INN2 (default)
- 1: AIN1R

AD2SEL[1:0]: ADC2 Input Pin Select (Table 53)
- 00: AIN2LP, AIN2LN, AIN2RP, AIN2RN (default)
- 01: AIN3L, AIN3R
- 10: AIN4L, AIN4R

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0057	ADC Mute & HPF Control	ATSPAD	AD1MUTE	AD2MUTE	0	0	0	AD1HPFN	AD2HPFN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATSPAD: ADC Digital Volume Transition Time Setting (Table 50)
- 0: 4/fs (default)
- 1: 16/fs

AD1MUTE: ADC1 Soft Mute Enable
- 0: Soft Mute Disable (default)
- 1: Soft Mute Enable

AD2MUTE: ADC2 Soft Mute Enable
- 0: Soft Mute Disable (default)
- 1: Soft Mute Enable

AD1HPFN: ADC1 HPF Enable for DC Offset Cancelling
- 0: HPF Enable (default)
- 1: HPF Disable

AD2HPFN: ADC2 HPF Enable for DC Offset Cancelling
- 0: HPF Enable (default)
- 1: HPF Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0058	ADC FullScale Control	0	0	0	0	ADC1VL	ADC1VR	ADC2VL	ADC2VR
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ADC1VL: Lch Input Voltage Full Scale Setting of ADC1
- 0: 2.3Vpp (±2.3Vpp) (default)
- 1: 2.83Vpp (±2.83Vpp)

ADC1VR: Rch Input Voltage Full Scale Setting of ADC1
- 0: 2.3Vpp (±2.3Vpp) (default)
- 1: 2.83Vpp (±2.83Vpp)

ADC2VL: Lch Input Voltage Full Scale Setting of ADC2
- 0: 2.3Vpp (±2.3Vpp) (default)
- 1: 2.83Vpp (±2.83Vpp)

ADC2VR: Rch Input Voltage Full Scale Setting of ADC2
- 0: 2.3Vpp (±2.3Vpp) (default)
- 1: 2.83Vpp (±2.83Vpp)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0059	DAC1 Lch Digital Volume	VOLDA1L[7:0]							
005A	DAC1 Rch Digital Volume	VOLDA1R[7:0]							
005B	DAC2 Lch Digital Volume	VOLDA2L[7:0]							
005C	DAC2 Rch Digital Volume	VOLDA2R[7:0]							
R/W		R/W							
Default		18H							

VOLDA1L[7:0]: Lch Digital Volume Setting of DAC1 (Table 56)
Default: 18H (0dB)

VOLDA1R[7:0]: Rch Digital Volume Setting of DAC1 (Table 56)
Default: 18H (0dB)

VOLDA2L[7:0]: Lch Digital Volume Setting of DAC2 (Table 56)
Default: 18H (0dB)

VOLDA2R[7:0]: Rch Digital Volume Setting of DAC2 (Table 56)
Default: 18H (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
005D	DAC Mute & Filter Setting	ATSPDA	DA1MUTE	DA2MUTE	0	0	0	DASD	DASL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATSPDA: DAC Digital Volume Transition Time Setting (Table 57)
- 0: 4/fs (default)
- 1: 16/fs

DA1MUTE: DAC1 Soft Mute Enable
- 0: Soft Mute Disable (default)
- 1: Soft Mute Enable

DA2MUTE: DAC2 Soft Mute Enable
- 0: Soft Mute Disable (default)
- 1: Soft Mute Enable

DASD, DASL: DAC Digital Filter Select (Table 61)
- 00: Sharp Roll-Off Filter (default)
- 01: Slow Roll-Off Filter
- 10: Short Delay Sharp Roll-Off Filter
- 11: Short Delay Slow Roll-Off Filter

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
005E	DAC De-Emphasis Setting	0	0	0	0	DEM2[1:0]		DEM1[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	0	1

DEM2[1:0]: De-emphasis Filter Setting of DAC2 (Table 62)
- 00: 44.1kHz
- 01: off (default)
- 10: 48kHz
- 11: 32kHz

DEM1[1:0]: De-emphasis Filter Setting of DAC1 (Table 62)
- 00: 44.1kHz
- 01: off (default)
- 10: 48kHz
- 11: 32kHz

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0060	SRC Filter Setting	SRCFEC	SRCFAUD	0	SRCPHGR	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SRCFEC, SRCFAUD: SRC Digital Filter Setting
- 00: Voice Mode (default)
- 01: Audio Mode
- 1x: Echo Canceller Mode

SRCPHGR: Group Delay Matching Function for Multiple SRCs on the Same Sampling Rate
- 0: Disable (default)
- 1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0061	SRC Mute Setting	0	0	0	0	SMUTE1	SMUTE2	SAUTO1	SAUTO2
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SMUTE1: SRC1 Soft Mute Enable
- 0: Soft Mute Disable (default)
- 1: Soft Mute Enable

SMUTE2: SRC2 Soft Mute Enable
- 0: Soft Mute Disable (default)
- 1: Soft Mute Enable

SAUTO1: Semi-Auto Mode Setting of SRC1 Soft Mute Function
- 0: Manual Mode (default)
- 1: Semi-Auto Mode

SAUTO2: Semi-Auto Mode Setting of SRC2 Soft Mute Function
- 0: Manual Mode (default)
- 1: Semi-Auto Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0064	DSP Memory Assignment	DLRAMDIV[1:0]		0	0	CRAMDIV[1:0]		DRAMDIV	PRAMDIV
R/W		R/W		R/W	R/W	R/W		R/W	R/W
Default		00		0	0	00		0	0

DLRAMDIV[1:0]: DLRAM Memory Assignment for DSP1 and DSP2 (Table 38)
Default: “00” (DSP1 = 12288 words, DSP2 = Not Connected)

CRAMDIV[1:0]: CRAM Memory Assignment for DSP1 and DSP2 (Table 36)
Default: “00” (DSP1 = 4096 words, DSP2 = 2048 words)

DRAMDIV: DRAM Memory Assignment for DSP1 and DSP2 (Table 37)
- 0: DSP1 = 2048 words, DSP2 = 2048 words (default)
- 1: DSP1 = 4096 words, DSP2 = Reset

PRAMDIV: PRAM Memory Assignment for DSP1 and DSP2 (Table 35)
- 0: DSP1 = 2048 words, DSP2 = 2048 words (default)
- 1: DSP1 = 4096 words, DSP2 = Reset

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0065	DSP1/2 DRAM Setting	D1DRMA[1:0]		D1DRMBK[1:0]		D2DRMA[1:0]		D2DRMBK[1:0]	
R/W		R/W		R/W		R/W		R/W	
Default		00		00		00		00	

D1DRMA[1:0]: BANK Addressing Mode Setting of Each BANK of DRAM for DSP1 (Table 40)
Default: “00” (BANK 1 = Ring, BANK 0 = Ring)

D1DRMBK[1:0]: DRAM BANK Size Setting of DSP1 (Table 39)
Default: “00” (BANK 1 = 1024 words, BANK 0 = DSP1 DRAM Size – 1024 words)

D2DRMA[1:0]: BANK Addressing Mode Setting of Each BANK of DRAM for DSP2 (Table 40)
Default: “00” (BANK 1 = Ring, BANK 0 = Ring)

D2DRMBK[1:0]: DRAM BANK Size Setting of DSP2 (Table 39)
Default: “00” (BANK 1 = 1024 words, BANK 0 = DSP2 DRAM Size – 1024 words)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0066	DSP1 DLRAM Setting	D1SS[1:0]		D1DLRMA	0	0	D1DLRMBK[2:0]		
R/W		R/W		R/W	R/W	R/W	R/W		
Default		00		0	0	0	000		

D1SS[1:0]: Sampling Mode Setting of DLRAM BANK 0 for DSP1 (Table 43)
Default: “00” (Update Every Sampling)

D1DLRMA: DLRAM Memory BANK1 Addressing Mode Setting of DSP1 (Table 42)
0: Ring (default)
1: Linear

D1DLRMBK[2:0]: DLRAM BANK Size Setting of DSP1 (Table 41)
Default: “000” (BANK 1 = 0 word, BANK 0 = DSP1 DLRAM Size)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0067	DSP2 DLRAM Setting	D2SS[1:0]		D2DLRMA	0	0	D2DLRMBK[2:0]		
R/W		R/W		R/W	R/W	R/W	R/W		
Default		00		0	0	0	000		

D2SS[1:0]: Sampling Mode Setting of DLRAM BANK 0 for DSP2 (Table 43)
Default: “00” (Update Every Sampling)

D2DLRMA: DLRAM Memory BANK1 Addressing Mode Setting of DSP2 (Table 42)
0: Ring (default)
1: Linear

D2DLRMBK[2:0]: DLRAM BANK Size Setting of DSP2 (Table 41)
Default: “000” (BANK 1 = 0 word, BANK 0 = DSP2 DLRAM Size)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0068	WAVP & DLP0 Setting	D1DLP0	D1WAVP[2:0]			D2DLP0	D2WAVP[2:0]		
R/W		R/W	R/W			R/W	R/W		
Default		0	000			0	000		

D1DLP0: Operation Mode Setting of DLRAM Pointer (DLP0) of DSP1
0: OFREG (default)
1: DBUS Immediate Data

D1WAVP[2:0]: Cycle Resolution Setting of Trigonometric Table for DSP1 (Table 44)
Default: “000” (128 points)

D2DLP0: Operation Mode Setting of DLRAM Pointer (DLP0) of DSP2
0: OFREG (default)
1: DBUS Immediate Data

D2WAVP[2:0]: Cycle Resolution Setting of Trigonometric Table for DSP2 (Table 44)
Default: “000” (128 points)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0069	JX Setting	D1JX0E	D1JX1E	D1JX2E	D1JX3E	D2JX0E	D2JX1E	D2JX2E	D2JX3E
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

D1JX0E: DSP1 JX0 Enable
0: Disable (default)
1: Enable

D1JX1E: DSP1 JX1 Enable
0: Disable (default)
1: Enable

D1JX2E: DSP1 JX2 Enable
0: Disable (default)
1: Enable

D1JX3E: DSP1 JX3 Enable
0: Disable (default)
1: Enable

D2JX0E: DSP2 JX0 Enable
0: Disable (default)
1: Enable

D2JX1E: DSP2 JX1 Enable
0: Disable (default)
1: Enable

D2JX2E: DSP2 JX2 Enable
0: Disable (default)
1: Enable

D2JX3E: DSP2 JX3 Enable
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
006C	STO Flag Setting	CRCE	0	0	PLLLOCKE	SRCLOCKE1	SRCLOCKE2	D1WDTEN	D2WDTEN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

CRCE: STO pin Output Setting of Cyclic Redundancy Check Error Signal
- 0: Do Not Output to STO pin (default)
- 1: Output to STO pin

PLLLOCKE: STO pin Output Setting of PLL Lock Signal
- 0: Do Not Output to STO pin (default)
- 1: Output to STO pin

SRCLOCKE1: STO pin Output Setting of SRC1 Lock Signal
- 0: Do Not Output to STO pin (default)
- 1: Output to STO pin

SRCLOCKE2: STO pin Output Setting of SRC2 Lock Signal
- 0: Do Not Output to STO pin (default)
- 1: Output to STO pin

D1WDTEN: STO Pin Output Setting of DSP1 Watch Dog Timer Error Signal
- 0: Output to STO pin (default)
- 1: Do Not Output to STO pin

D2WDTEN: STO pin Output Setting of DSP2 Watch Dog Time Error Signal
- 0: Output to STO pin (default)
- 1: Do Not Output to STO pin

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
006D	Power Management	0	0	PMSRC1	PMSRC2	PMAD1	PMAD2	PMDA1	PMDA2
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMSRC1: SRC1 Power Management Setting
- 0: Power-Off (default)
- 1: Normal Operation

PMSRC2: SRC2 Power Management Setting
- 0: Power-Off (default)
- 1: Normal Operation

PMAD1: ADC1 Power Management Setting
- 0: Power-Off (default)
- 1: Normal Operation

PMAD2: ADC2 Power Management Setting
- 0: Power-Off (default)
- 1: Normal Operation

PMDA1: DAC1 Power Management Setting
- 0: Power-Off (default)
- 1: Normal Operation

PMDA2: DAC2 Power Management Setting
- 0: Power-Off (default)
- 1: Normal Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
006E	Reset Control	DLRDY	0	0	0	D1RESETN	D2RESETN	CRESETN	HRESETN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DLRDY: DSP Data Downloading Function without Clock Input
0: OFF, Normal Operation (default)
1: ON, Program downloading is available without inputting a clock.
Note
* 84. DSP programs and coefficient data can be downloaded while the main clock is stopped or during clock reset (CKRESETN bit = “0”) by setting this bit to “1”. This bit must be set to “0” after downloading.

D1RESETN: DSP1 Reset
0: DSP1 Reset (default)
1: DSP1 Reset Release

D1RESETN: DSP2 Reset
0: DSP2 Reset (default)
1: DSP2 Reset Release

CRESETN: CODEC Reset
0: CODEC Reset (default)
ADC1, ADC2, DAC1 and DAC2 are Reset.
1: CODEC Reset Release

HRESETN: HUB Reset
0: HUB Reset (default)
ADC1, ADC2, DAC1, DAC2, SRC1 and SRC2 are Reset.
1: HUB Reset Release

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0100	Device ID	DEVID[7:0]							
R/W		R							
Fixed Value		35H							

DEVID[7:0]: AK7735's Device ID Read
Fixed Value: 35H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0101	Revision Num	REVNUM[7:0]							
R/W		R							
Fixed Value		00H							

REVNUM[7:0]: AK7735's Device Revision Read
Fixed Value: 00H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0102	DSP Error Status	CRCERRN	WDT1ERRN	WDT2ERRN	PLLLOCK	0	0	GPO2	GPO1
R/W		R	R	R	R	R	R	R	R
Default		1	1	1	0	0	0	0	0

CRCERRN: Cyclic Redundancy Check Error Status
0: Error
1: Normal Operation (default)

WDT1ERRN: DSP1 Watchdog Timer Error Status
0: Error
1: Normal Operation (default)

WDT2ERRN: DSP2 Watchdog Timer Error Status
0: Error
1: Normal Operation (default)

PLLLOCK: PLL Lock Status
0: PLL Unlock (default)
1: PLL Lock

GPO2: GPO Output Level Status of DSP2
0: "L" Output (default)
1: "H" Output

GPO1: GPO Output Level Status of DSP1
0: "L" Output (default)
1: "H" Output

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0103	SRC Status	0	0	SRC2LOCK	SRC1LOCK	0	0	0	0
	R/W	R	R	R	R	R	R	R	R
	Default	0	0	0	0	0	0	0	0

SRC2LOCK: SRC2 Lock Status Read
- 0: Unlock (default)
- 1: Lock

SRC1LOCK: SRC1 Lock Status Read
- 0: Unlock (default)
- 1: Lock

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0104	STO Read Out	STO	0	0	0	0	0	0	0
	R/W	R	R	R	R	R	R	R	R
	Default	1	0	0	0	0	0	0	0

STO: STO pin Status Read
- 0: Error
- 1: Normal Operation (default)

13. Recommended External Circuits

■ Connection Diagram

1. I²C Interface

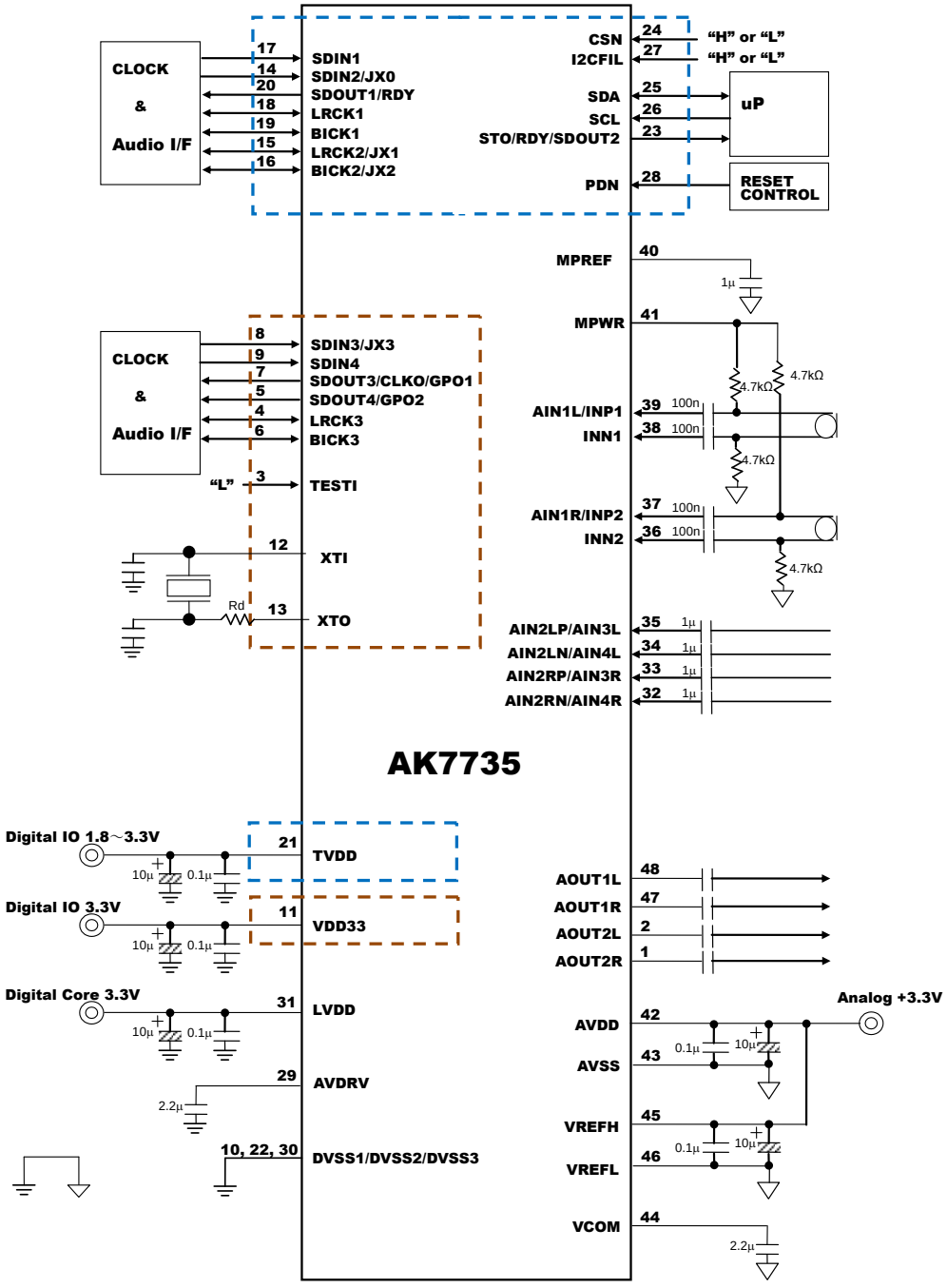


Figure 82. I²C Interface Connection Example

2. SPI Interface

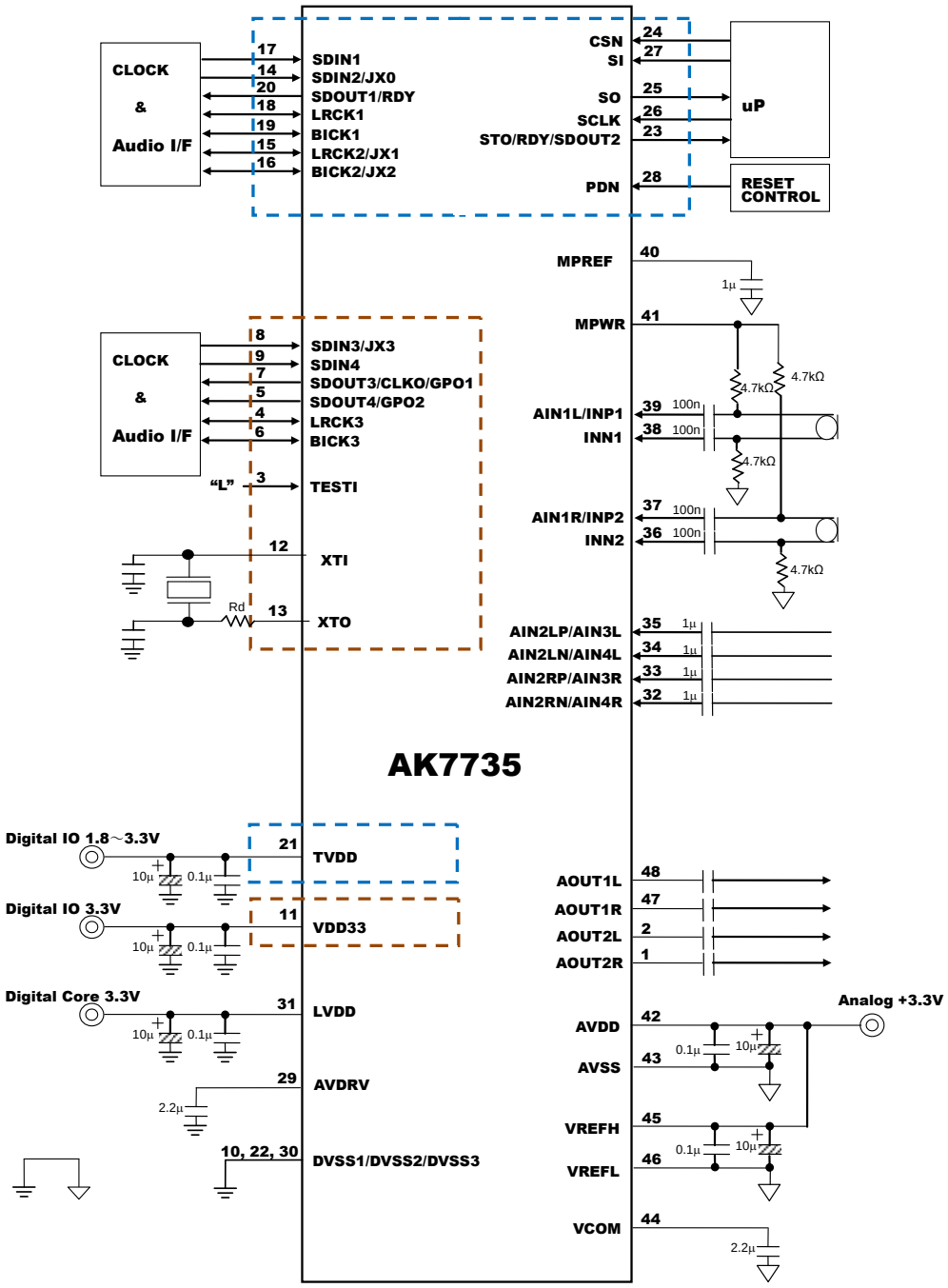


Figure 83. SPI Interface Connection Example

■ Peripheral Circuit

1. Ground

AVSS, DVSS1, DVSS2 and DVSS3 should be connected to the same ground. Decoupling capacitors, particularly ceramic capacitors of small capacity, should be placed at positions as close as possible to the AK7735.

2. Reference Voltage

VCOM is a common voltage of this chip and the VCOM pin outputs AVDD/2. A 2.2µF ceramic capacitor should be connected between the VCOM pin and AVSS.

Do not connect the VCOM pin to any external devices. Digital signal lines, especially clock signal line should be kept away as far as possible from this pin in order to avoid unwanted coupling into the AK7735.

3. Analog Input

The analog input signal is input to the analog modulator of the AK7735. The maximum input voltage at differential input pins is ±2.30Vpp (Typ.) or ±2.83Vpp (Typ.). The maximum input voltage at single-ended input pins is 2.30Vpp (Typ.) or 2.83Vpp (Typ.). The output code format is 2's complements. The internal HPF removes the DC offset.

After power-down is released, the internal operating point level AVDD/2 occurs on analog input pins of the AK7735. Concerning the internal operating point formation circuit, each input pin has impedance of 25kΩ (Typ.). The pins that are connected to AC coupling capacitors require start-up time (time constant).

The AK7735 samples the analog inputs at 6.144MHz when fs=48kHz, 96kHz or 192kHz. The AK7735 includes an anti-aliasing filter (RC filter), and no external low-pass filter is necessary in front of the ADC. However, an external low-pass filter should be connected before the ADC for the signal which has large out-of-band noise such as D/A converted signals.

The analog power supply to the AK7735 is +3.3V (Typ.). Voltage of AVDD + 0.3V or larger, voltage of AVSS - 0.3V or smaller, and current of 10mA or larger must not be applied to analog input pins. Excessive current will damage the internal protection circuit and will cause latch-up, damaging the IC. Accordingly, if the external analog circuit voltage is ±15V, the analog input pins must be protected from signals which are equal or larger than absolute maximum ratings.

When using differential input mode, it is prohibited to input signal to only one side like pseudo differential input.

4. Analog Output

The analog output is single-ended and the output signal range is typically 0.857 x AVDD Vpp centered on VCOM. The digital input data format is two’s compliment. Positive full-scale output corresponds to 7FFFFFFFH (@32bit) input code, Negative full scale is 80000000H (@32bit) and VCOM voltage ideally is 00000000H (@32bit). The Out-of-Band noise (shaping noise) generated by the internal delta-sigma modulator is attenuated by an integrated switched capacitor filter (SCF) and a continuous time filter (CTF).

5. Crystal Oscillator

The resistor and capacitor values for the oscillator RC circuit are shown blow.

Oscillator	R1 (Max)	C0 (Max)	XTI, XTO pin Capacity
12.288MHz	120Ω	2.5pF	22pF
18.432MHz	80Ω	2.5pF	15pF

Table 67. Recommended Resistance and Capacitance with Crystal Oscillator

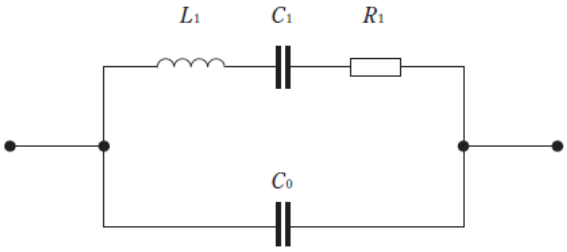
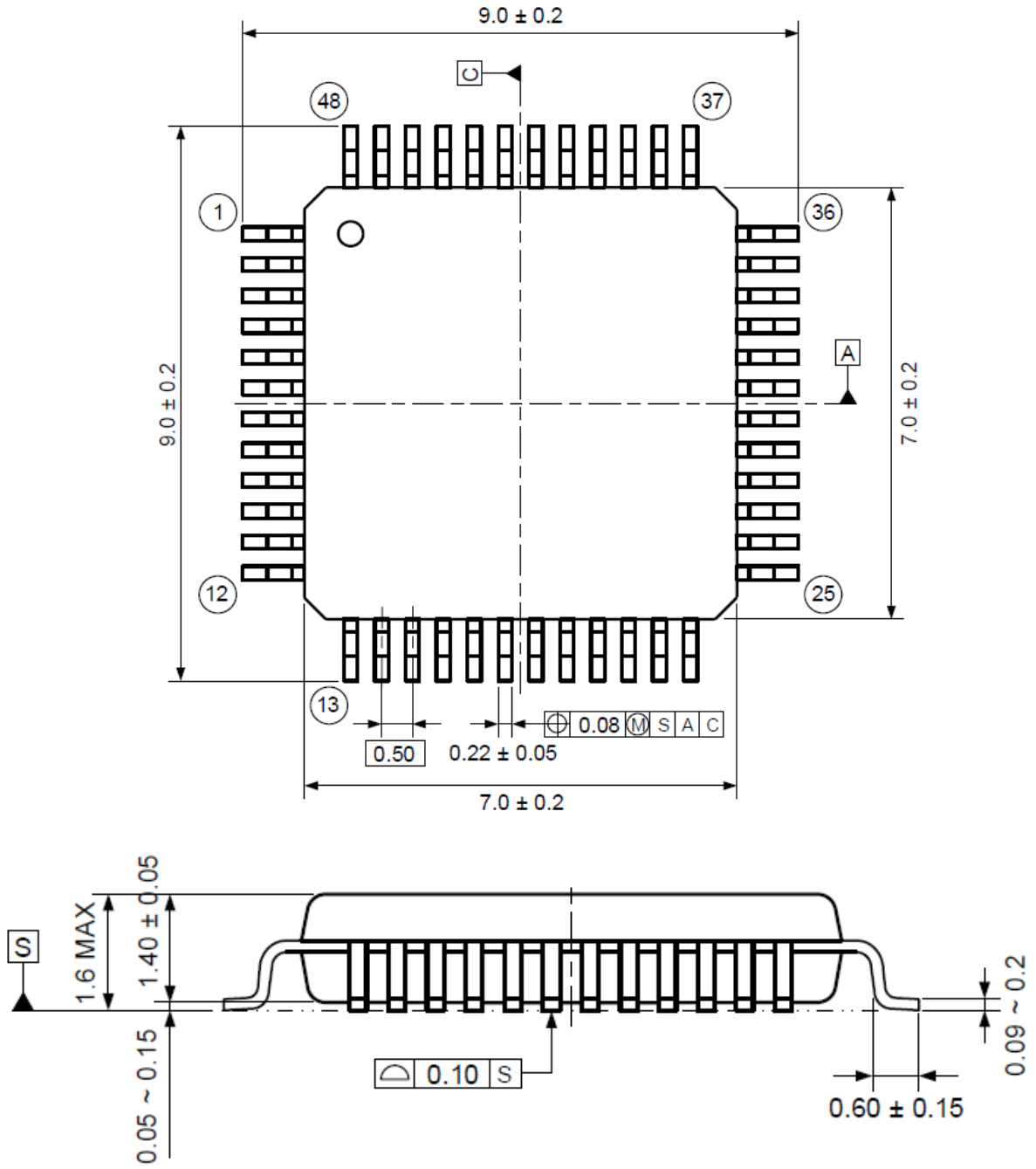


Figure 84. Electric Equivalent Circuit of Crystal Oscillator

14. Package

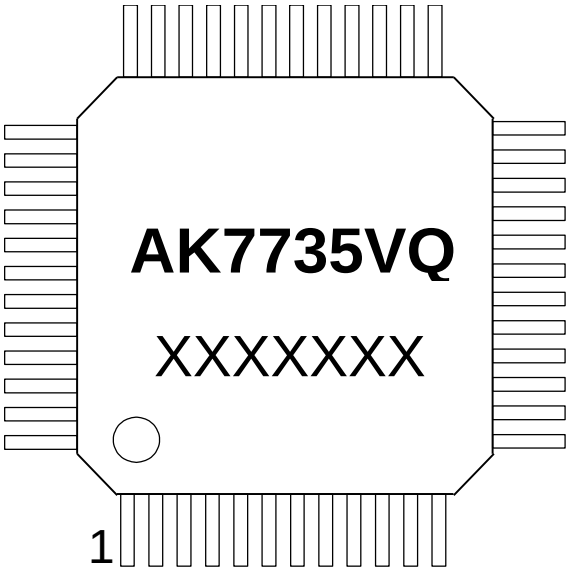
■ Outline Dimensions



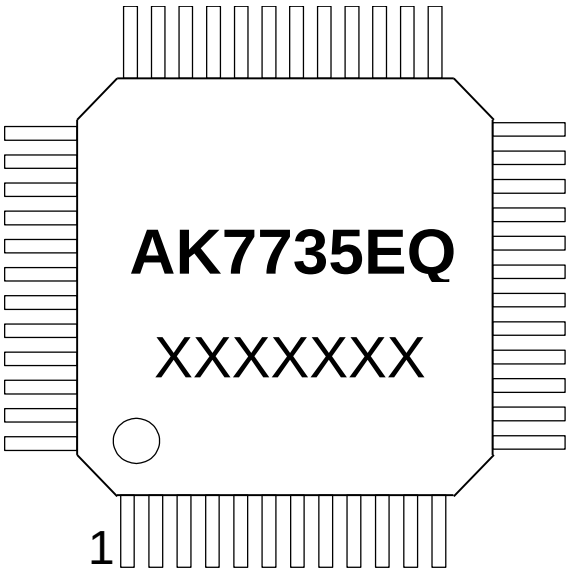
■ Material and Lead Finish

Package: Epoxy, Halogen (Br and Cl) free
Lead frame: Copper
Lead-finish: Soldering (Pb free) plate

■ **Marking**



1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK7735VQ



1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK7735EQ

15. Ordering Guide

AK7735VQ	-40 ~ +85°C	48-pin LQFP (0.5mm pitch)
AK7735EQ	-20 ~ +85°C	48-pin LQFP (0.5mm pitch)
AKD7735	Evaluation Board for AK7735	

16. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
16/12/01	00	First Edition		

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