PRELIMINARY

MX27C1610

16M-BIT [2M x 8/1M x 16] CMOS OTP ROM

FEATURES

- 2M x 8 or 1M x 16 organization
- 5V Vcc for Read operation
- 10V Vpp Programming operation
- Fast access time: 100/120 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100uA
- Package type:
  - 42 pin plastic DIP

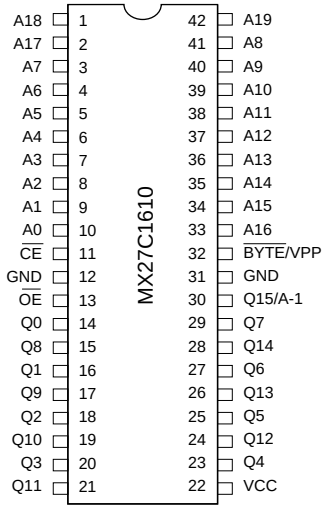
GENERAL DESCRIPTION

The MX27C1610 is a 16M-bit, One Time Programmable Read Only Memory. It is organized as 2M x 8 or 1M x 16 and has a static standby mode, and features fast programming. For programming outside from the system, existing EPROM programmers may be used. The MX27C1610 supports a intelligent fast programming algorithm which can result in programming time of less than two minutes.

This One Time Programmable Read Only Memory is packaged in industry standard 42 pin dual-in-line plastic package.

PIN CONFIGURATIONS

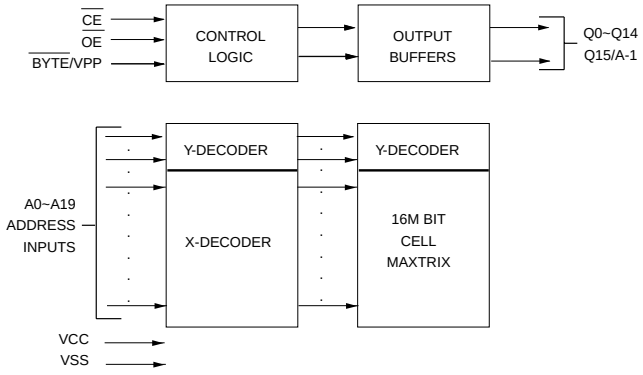
PDIP



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A19	Address Input
Q0~Q14	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$/VPP	Word/Byte Selection /Program Supply Voltage
Q15/A-1	Q15(Word mode)/LSB addr. (Byte mode)
VCC	Power Supply Pin (+5V)
GND	Ground Pin

BLOCK DIAGRAM



TRUTH TABLE OF $\overline{BYTE}$ FUNCTION

BYTE MODE($\overline{BYTE}$ = GND)

$\overline{CE}$	$\overline{OE}$	Q15/A-1	MODE	Q0-Q7	SUPPLY CURRENT
H	X	X	Non selected	High Z	Standby(ICC2)
L	H	X	Non selected	High Z	Operating(ICC1)
L	L	A-1 input	Selected	DOUT	Operating(ICC1)

WORD MODE($\overline{BYTE}$ = VCC)

$\overline{CE}$	$\overline{OE}$	Q15/A-1	MODE	Q0-Q7	SUPPLY CURRENT
H	X	High Z	Non selected	High Z	Standby(ICC2)
L	H	High Z	Non selected	High Z	Operating(ICC1)
L	L	DOUT	Selected	DOUT	Operating(ICC1)

NOTE : X = H or L

FUNCTIONAL DESCRIPTION

READ MODE

The MX27C1610 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$'s, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - t $\overline{OE}$.

WORD-WIDE MODE

With $\overline{BYTE}$/VPP at VCC ± 0.2V outputs Q0-7 present data Q0-7 and outputs Q8-15 present data Q8-15, after CE and $\overline{OE}$ are appropriately enabled.

BYTE-WIDE MODE

With $\overline{BYTE}$/VPP at GND ± 0.2V, outputs Q8-15 are tri-stated. If Q15/A-1 = VIH, outputs Q0-7 present data bits Q8-15. If Q15/A-1 = VIL, outputs Q0-7 present data bits Q0-7.

STANDBY MODE

The MX27C1610 has a CMOS standby mode which reduces the maximum VCC current to 100 uA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.2V. The MX27C1610 also has a TTL-standby mode which reduces the maximum VCC current to 4 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 uF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between Vcc and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on One Time Programmable Read Only Memory arrays, a 4.7 uF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

WRITE OPERATIONS

Commands are written to the COMMAND INTERFACE REGISTER (CIR) using standard microprocessor write timings. The CIR serves as the interface between the microprocessor and the internal chip operation. The CIR can decipher Read Array, Read Silicon ID and Program command. In the event of a read command, the CIR simply points the read path at either the array or the silicon ID, depending on the specific read command given. For a program cycle, the CIR informs the write state machine, and the write state machine and the write state machine will control the program sequences and the CIR will only respond to status reads. After the write state machine has completed its task, it will allow the CIR to respond to its full command set. The CIR stays at read status register mode until the microprocessor issues another valid command sequence.

Device operations are selected by writing commands into the CIR. See command definition table below.

MODE SELECT TABLE

MODE	$\overline{CE}$	$\overline{OE}$	A9	A0	Q15/A-1	$\overline{BYTE}$/VPP(5)	Q8-14	Q0-7
Read (Word) (2)	VIL	VIL	X	X	Q15 Out	VIH	Q8-14 Out	Q0-7 Out
Read (Upper Byte) (2)	VIL	VIL	X	X	VIH	VIL	High Z	Q8-15 Out
Read (Lower Byte) (2)	VIL	VIL	X	X	VIL	VIL	High Z	Q0-7 Out
Output Disable (2)	VIL	VIH	X	X	High Z	X	High Z	High Z
Standby (2)	VIH	X	X	X	High Z	X	High Z	High Z
Write Operation (2)	VIL	VIH	X	X	Q15 In	VPP	Q8-14 In	Q0-7 In
ManufacturerID(3)(1)	VIL	VIL	VH	VIL	0B	VIH	00H	C2H
Device ID(3)(1)	VIL	VIL	VH	VIH	0B	VIH	00H	6AH

NOTES:
1. VH = 10V ± 0.5V
2. X Either VIL or VIH.
3. A1= VIL, other address lines not specified are at "X" states
4. See DC Programming Characteristics for VPP voltages.
5. $\overline{BYTE}$/VPP is intended for operation under DC Voltage conditions only. VPP=10V± 0.5V for write operation

COMMAND DEFINITIONS OF WRITE OPERATION TABLE

Command Sequence		Read/ Reset	Silicon ID Read	Page/Byte Program	Read Status Reg.	Clear Status Reg.
Bus Write Cycles Req'd		4	4	4	4	3
First Bus Write Cycle	Addr	5555H	5555H	5555H	5555H	5555H
	Data	AAH	AAH	AAH	AAH	AAH
Second Bus Write Cycle	Addr	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH
	Data	55H	55H	55H	55H	55H
Third Bus Write Cycle	Addr	5555H	5555H	5555H	5555H	5555H
	Data	F0H	90H	A0H	70H	50H
Fourth Bus Read/Write Cycle	Addr	RA	00H/01H	PA	X	
	Data	RD	C2H/6AH	PD	SRD	

NOTES:
1. In the write operation mode, $\overline{BYTE}$/VPP should be set to 10V±0.5V.
2. 5555H and 2AAAH address command codes stand for Hex number starting from A0 to A14.
3. RA=Address of the memory location to be read.
   RD=Data read from location RA during read operation.
   PA=Address of the memory location to be programmed.
   PO=Data to be programmed at location PA.

DEVICE OPERATION

SILICON ID READ

The Silicon ID Read mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force VID (10V±o.5V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from VIL to VIH. All addresses are don't cares except A0 and A1.

The manufacturer and device codes may also be read via the command register, for instances when the MX27C1610 is programmed in a system without access to high voltage on the A9 pin.

MX27C1610 Silion ID Codes

Type	A_{19}	A_{18}	A_{17}	A_{16}	A_1	A_0	Code(HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code**	X	X	X	X	VIL	VIL	C2H*	1	1	0	0	0	0	1	0
Device Code**	X	X	X	X	VIL	VIH	6AH*	0	1	1	0	1	0	1	0

* The high byte of the code will be 00H and low byte of the code will be C2H for Manufacturer code and 6AH of Device code.
** All other address lines not specified are also at "X" state. X=VIH or VIL.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the CIR contents are altered by a valid command sequence.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

The MX27C1610 is accessed when $\overline{CE}$ and $\overline{OE}$ are low the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

Note that the read/reset command is not valid when program is in progress.

PAGE PROGRAM

The device is set up in the programming mode when the programming Voltage Vpp=10V is applied with Vcc=5V, and $\overline{OE}$=VIH.

Any attempt to write to the device without the three-cycle command sequence will not start the internal Write State Machine(WSM), no data will be written to the device.

After three-cycle command (see command table) sequence is given, a word load is performed by applying a low pulse on the $\overline{CE}$ input with $\overline{CE}$ low and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ The data is latched by the rising edge of $\overline{CE}$. Maximum of 128 bytes of data may be loaded into each page by the same procedure as outlined in the page program section below.

WORD-WIDE LOAD

Word loads are used to enter the 128 bytes(64 words) of a page to be programmed or the software codes for data protection. A word load is performed by applying a low pulse on the $\overline{CE}$ input with $\overline{CE}$ and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$. The data is latched by the rising edge of $\overline{CE}$.

PROGRAM

The device is programmed on a page basis. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data word has been loaded into the device, successive words are entered in the same manner. The time between word loads must be less than 30us otherwise the load period could be teminated. A6 to A19 specify the page address, i.e., the device is page-aligned on 128 bytes(64 words)boundary. The page address must be valid during each high to low transition of $\overline{CE}$. A0 to A5 specify the word address withih the page. The word may be loaded in any order; sequential loading is not required. If a high to low transition of $\overline{CE}$ is not detected whithin 100us of the last low to high transition, the load period will end and the internal programming period will start. The Auto page program terminates when status on Q7 is "1" at which time the device stays at read status register mode until the CIR contents are altered by a valid command sequence.

READ STATUS REGISTER

The MXIC's16 Mbit OTP ROM contains a status register which may be read to determine when a program operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the Read Status command to the CIR. After writing this command, all subsequent read operations output data from the status register until another valid command sequence is written to the CIR. A Read Array command must be written to the CIR to return to the Read Array mode.

It should be noted that the contents of the status register are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$ whichever occurs last in the read cycle. This prevents possible bus errors which might occur if the contents of the status register change while reading the status register. $\overline{CE}$ or $\overline{OE}$ must be toggled with each subsequent status read, or the completion of a program operation will not be evident.

The Status Register is the interface between the microprocessor and the Write State Machine (WSM). When the WSM is active, this register will indicate the status of the WSM, and will also hold the bits indicating whether or not the WSM was successful in performing the desired operation. The WSM can set status bit4 and bit7. However, the WSM can only clear bit 7 but can not clear bit 4. If Program fail status bit is detected, the Status Register is not cleared until the "Clear Status Register command" is issued. The MX27C1610 automatically outputs Status Register data when read after Page Program or Read Status Command write cycle. The internal state machine is set for reading array data upon device power-up.

CLEAR STATUS REGISTER

The Program fail status bit (Q4) are set by the write state machine, and can only be reset by the system software. These bits can indicate various failure conditions(see Table below). By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several pages . The status register may then be read to determine if an error occurred during that programming series. This adds flexibility to the way the device may be programmed. Additionally, once the program fail bit happens, the program operation can not be performed further. The program fail bit must be reset by system software before further page program are attempted. To clear the status register, the Clear Status Register command is written to the CIR. Then, any other command may be issued to the CIR. Note again that before a read cycle can be initiated, a Read command must be written to the CIR to specify whether the read data is to come from the Array, Status Register or Silicon ID.

STATUS REGISTER TABLE

	STATUS	NOTES	Q7	Q4	Q3
IN PROGRESS	PROGRAM	1,2	0	0	0
COMPLETE	PROGRAM	1,2	1	0	0
FAIL	PROGRAM	1,3	1	1	0
AFTER CLEARING STATUS REGISTER			1	0	0

NOTES:
1. Q7 : WRITE STATE MACHINE STATUS
   1 = READY, 0 = BUSY
   Q4 : PROGRAM FAIL STATUS
   1 = FAIL IN PROGRAM, 0 = SUCCESSFUL PROGRAM
   Q3=0 = RESERVED FOR FUTURE ENHANCEMENTS.
   These bits are reserved for future use ; mask them out when polling the Status Register.
2. PROGRAM STATUS is for the status during Page Programming.
3. FAIL STATUS bit(Q4) is provied during Page Program mode.

LOW VCC WRITE INHIBIT

To avoid initiation of a write cycle during VCC power-up and power-down, a write cycle is locked out for VCC less than VLKO(= 3.2V , typically 3.5V). If VCC < VLKO, the command register is disabled and all internal program circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the VCC level is greater than VLKO. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional write when VCC is above VLKO.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 10ns (typical) on $\overline{CE}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH. To initiate a write cycle $\overline{CE}$ must be a logical zero while $\overline{OE}$ is a logical one, and $\overline{BYTE}$/VPP=10V.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0℃ to 70℃
Storage Temperature	-65℃ to 125℃
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
A9	-0.5V to 13.5V
$\overline{BYTE}$/VPP	-0.5V to 12.0V

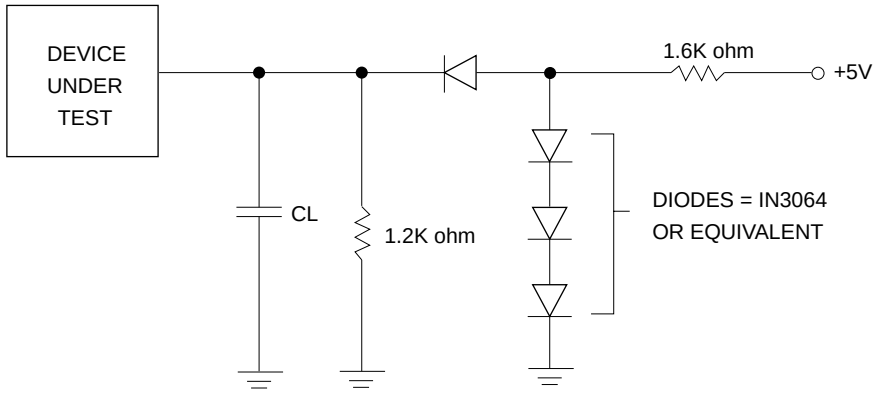
NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

CAPACITANCE TA = 25℃, f = 1.0 MHz

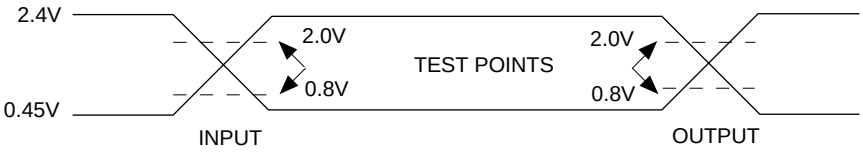
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			14	pF	VIN = 0V
CVPP	VPP Capacitance			20	pF	VPP=0V
COUT	Output Capacitance			16	pF	VOUT = 0V

SWITCHING TEST CIRCUITS



CL = 100 pF Including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are < 10ns.

DC CHARACTERISTICS TA = 0℃ to 70℃, VCC = 5V±10%

SYMBOL	PARAMETER	NOTES	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
ILI	Input Leakage Current	1			±10	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current	1			±10	uA	VCC = VCC Max VIN = VCC or GND
ISB1	VCC Standby Current(CMOS)	1		1	100	uA	VCC = VCC Max $\overline{CE}$ = VCC±0.2V
ISB2	VCC Standby Current(TTL)			2	4	mA	VCC = VCC Max $\overline{CE}$ = VIH
ICC1	VCC Read Current	1		50	60	mA	VCC = VCC Max CMOS: $\overline{CE}$ = GND± 0.2V $\overline{BYTE}$/VPP = GND±0.2V or VCC± 0.2V Inputs = GND±0.2V or VCC± 0.2V TTL : $\overline{CE}$ = VIL, $\overline{BYTE}$/VPP = VIL or VIH Inputs = VIL or VIH, f = 10MHz, IOUT = 0 mA
ICC2	VCC Read Current	1		30	35	mA	VCC = VCC Max, CMOS: $\overline{CE}$ = GND± 0.2V $\overline{BYTE}$/VPP = VCC±0.2V or GND± 0.2V Inputs = GND±0.2V or VCC±0.2V TTL: $\overline{CE}$= VIL, $\overline{BYTE}$/VPP = VIH or VIL Inputs = VIL or VIH, f = 5MHz, IOUT = 0mA
ICC4	VCC Program Current	1		30	50	mA	Program in Progress
VIL	Input Low Voltage	2	-0.3		0.8	V	
VIH	Input High Voltage	3	2.4		VCC+0.3	V	
VOL	Output Low Voltage				0.45	V	IOL = 2.1mA
VOH	Output High Voltage		2.4			V	IOH = -2mA

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at VCC = 5.0V, T = 25℃. These currents are valid for all product versions (package and speeds).
2. VIL min. = -1.0V for pulse width £ 50ns.
   VIL min. = -2.0V for pulse width £ 20ns.
3. VIH max. = VCC + 1.5V for pulse width £ 20ns. If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC CHARACTERISTICS --- READ OPERATIONS

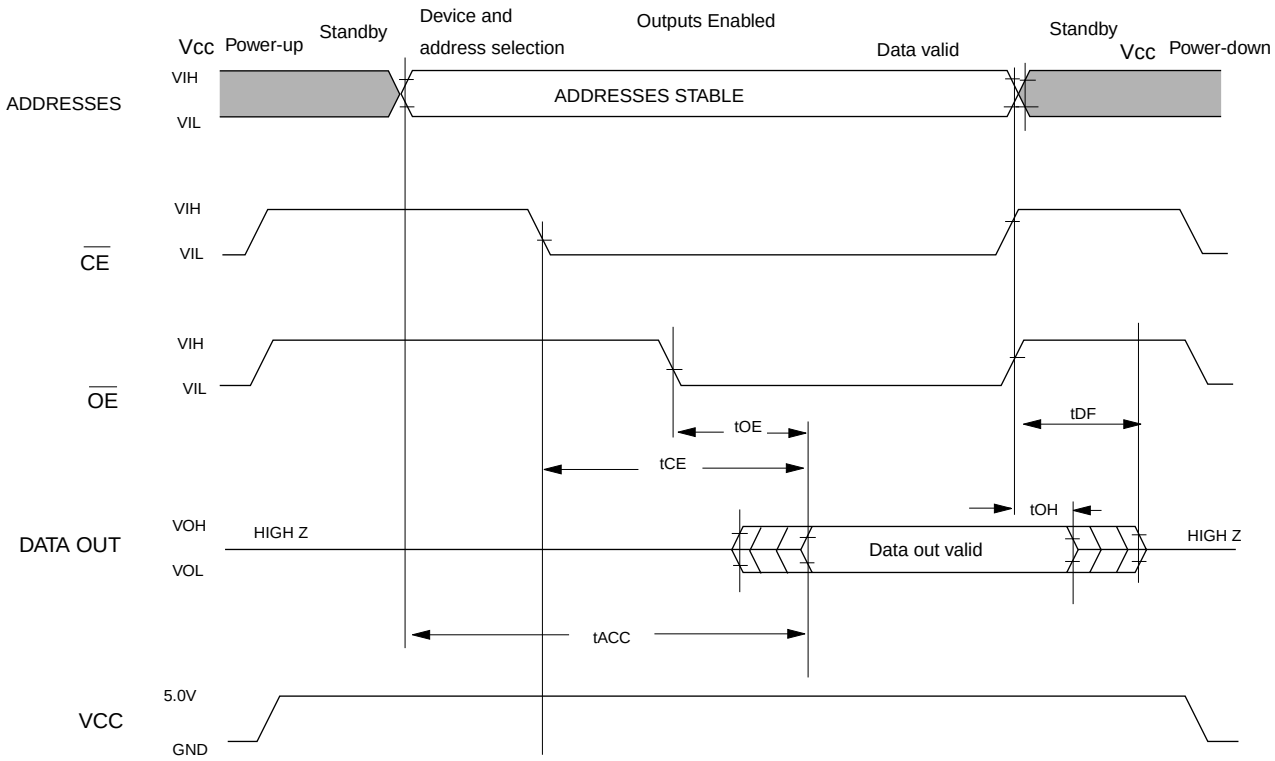
		27C1610-10		27C1610-12			
SYMBOL	DESCRIPTIONS	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		100		120	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		100		120	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		50		50	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output in High Z	0	35	0	35	ns	$\overline{CE}$=VIL
tOH	Address to Output hold	0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL
tBACC	$\overline{BYTE}$/VPP to Output Delay		100		120	ns	$\overline{CE}$= $\overline{OE}$=VIL
tBHZ	$\overline{BYTE}$/VPP Low to Output in High Z		50		50	ns	$\overline{CE}$=VIL

NOTE:
1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V
- Input rise and fall times: 10ns
- Output load: 1TTL gate+100pF(Including scope and jig)
- Reference levels for measuring timing: 0.8V, 2.0V

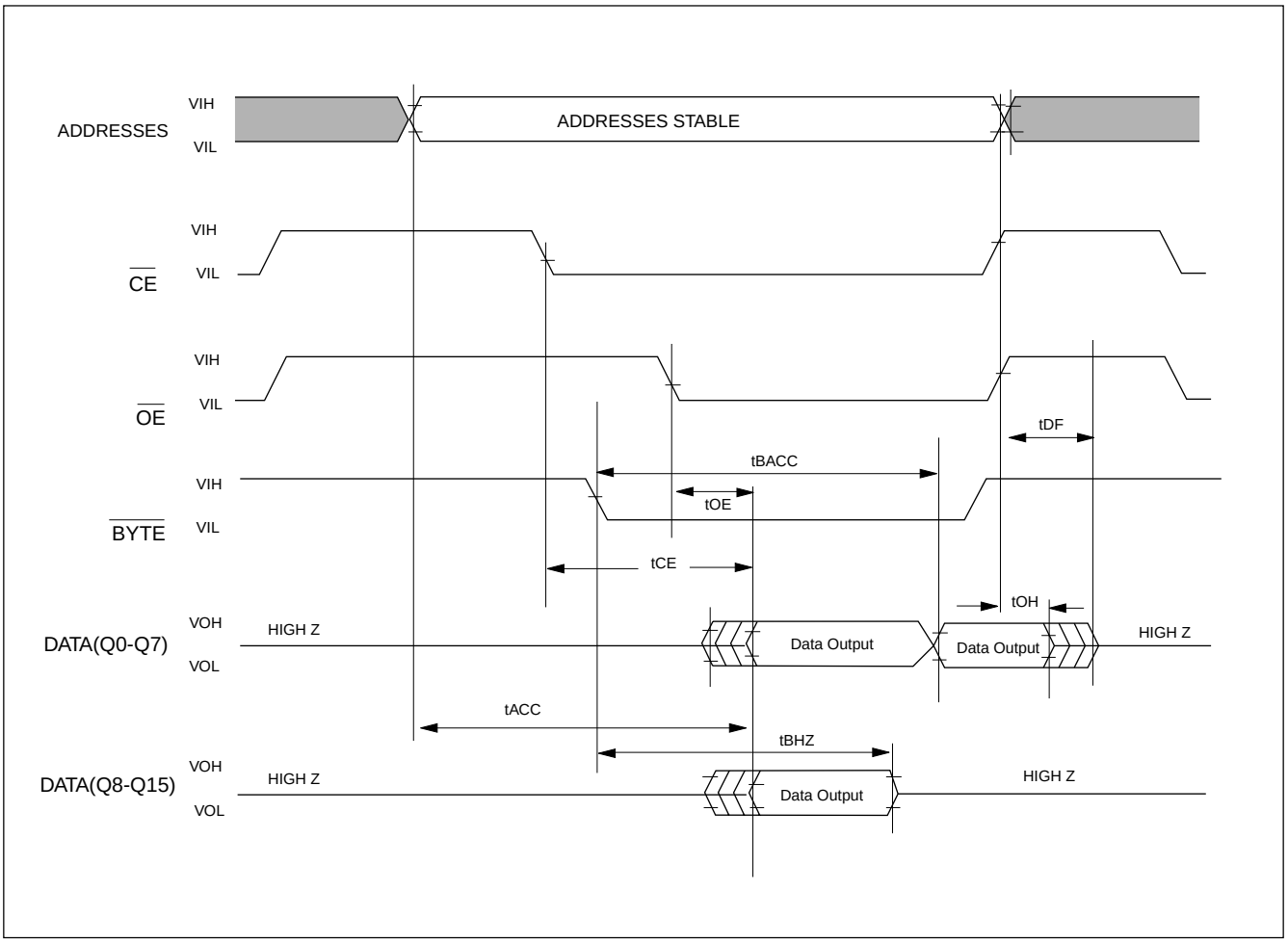
Figure 1. READ TIMING WAVEFORMS



NOTE:

1.For real world application, $\overline{\text{BYTE}}$/VPP pin should be either static high(word mode) or static low(byte mode); dynamic switching of $\overline{\text{BYTE}}$/VPP pin is not recommended.

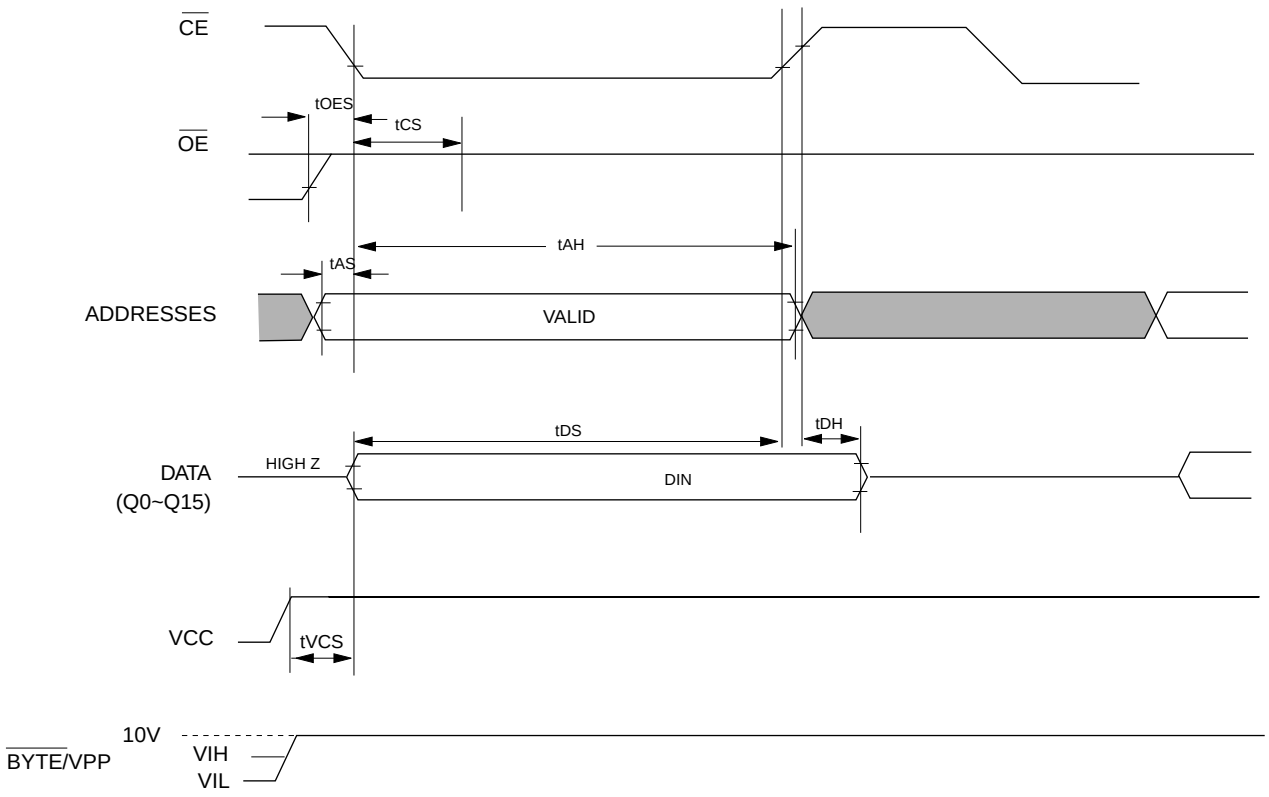
Figure 2. $\overline{\text{BYTE}}$/VPP TIMING WAVEFORMS



AC CHARACTERISTICS --- PROGRAM OPERATIONS

		27C1610-10		27C1610-12		
SYMBOL	DESCRIPTION	MIN.	MAX.	MIN.	MAX.	UNIT
tWC	Write Cycle Time	100		120		ns
tAS	Address Setup Time	0		0		ns
tAH	Address Hold Time	50		60		ns
tDS	Data Setup Time	50		60		ns
tDH	Data Hold Time	0		0		ns
tOES	Output Enable Setup Time	0		0		ns
tCES	$\overline{CE}$ Setup Time	0		0		ns
tCS	$\overline{CE}$ Setup Time	0		0		ns
tCH	$\overline{CE}$ Hold Time	0		0		ns
tWP	Write Pulse Width	50		60		ns
tWPH	Write Pulse Width High	30		50		ns
tBALC	Word Address Load Cycle	0.3	30	0.3	30	us
tBAL	Word Address Load Time	100		100		us
tSRA	Status Register Access Time	70		90		ns
tCESR	$\overline{CE}$ Setup before S.R. Read	70		70		ns
tVCS	VCC Setup Time	50		50		us
tRAW	Read Operation Set Up Time After Write		20		20	us

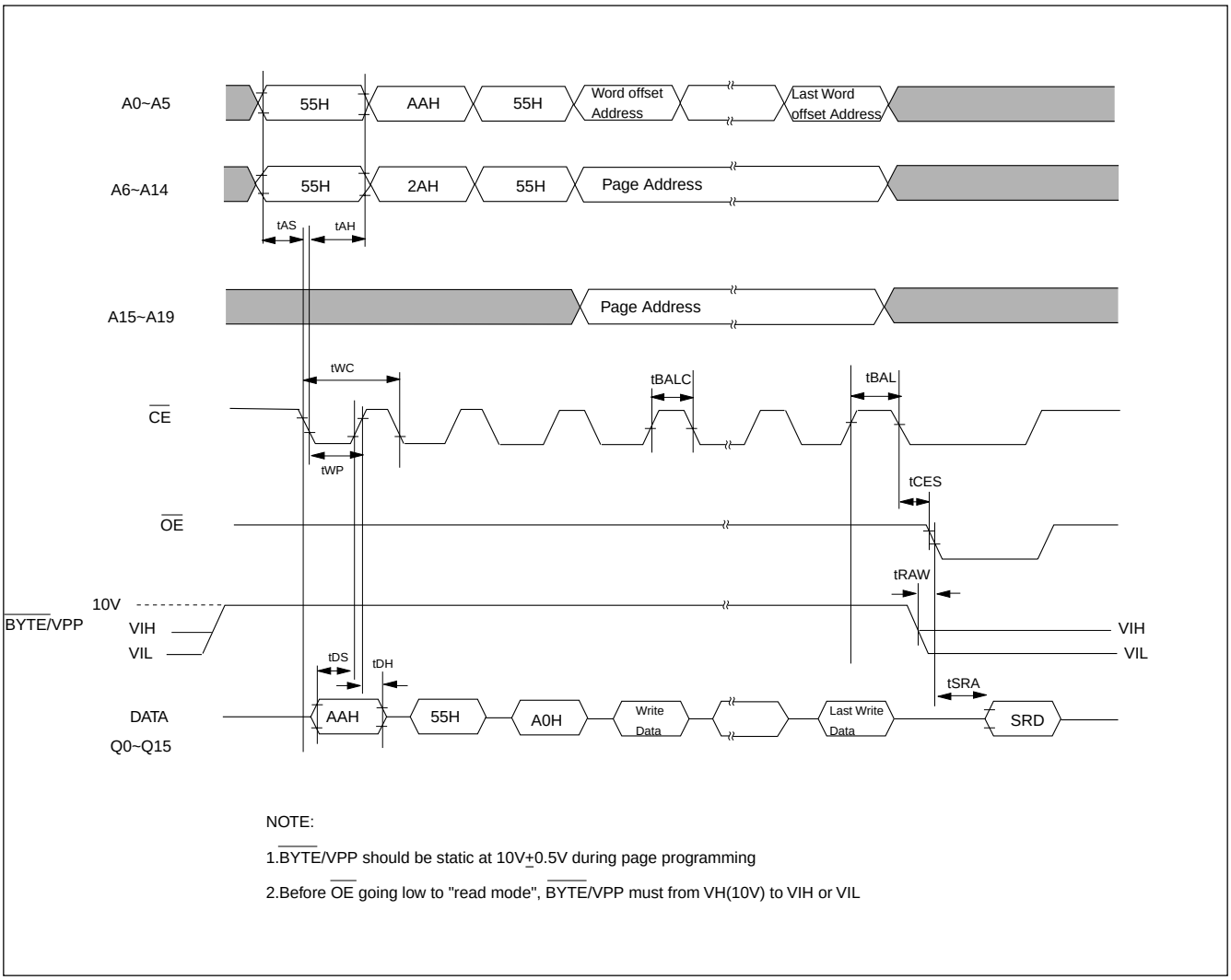
Figure 3. COMMAND WRITE TIMING WAVEFORMS



NOTE:

1. BYTE/VPP pin should be static at 10V±0.5V during Write operation.
2. BYTE/VPP pin should be static at TTL, or CMOS level, during Read operation.

Figure 4. AUTOMATIC PAGE PROGRAM TIMING WAVEFORMS



NOTE:

1.BYTE/VPP should be static at 10V±0.5V during page programming

2.Before OE going low to "read mode", BYTE/VPP must from VH(10V) to VIH or VIL

PROGRAMMING PERFORMANCE

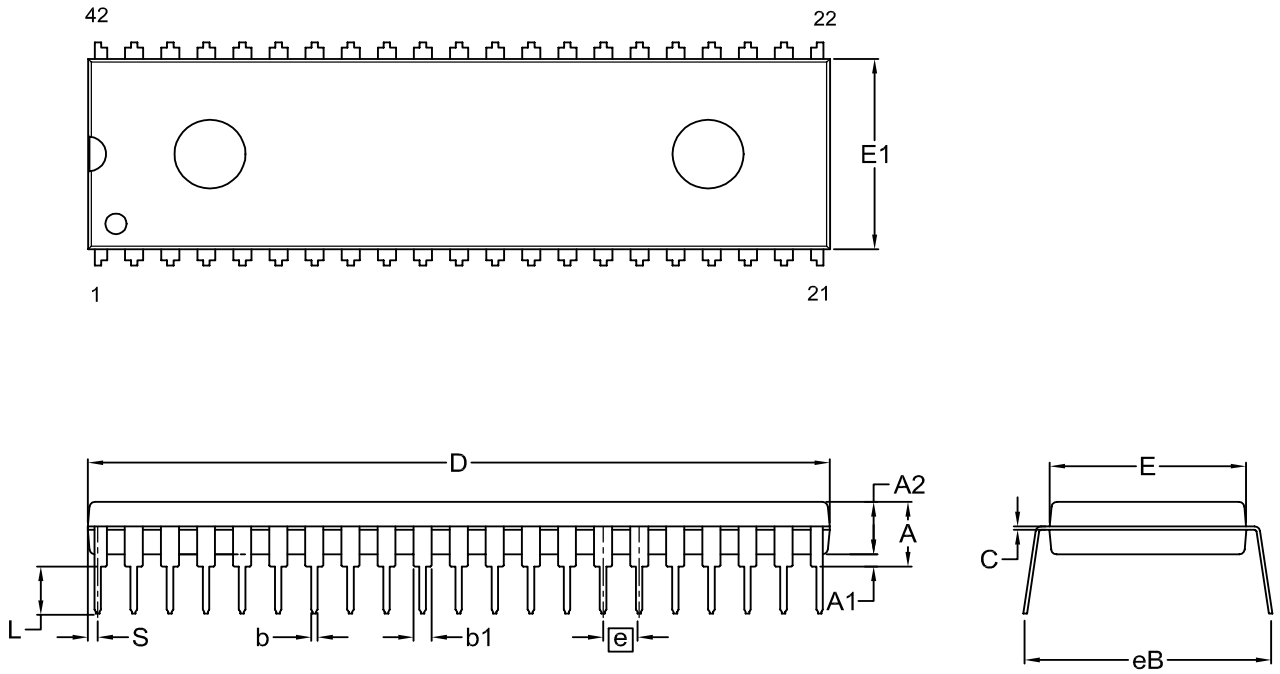
	LIMITS			
PARAMETER	MIN.	TYP.	MAX.	UNITS
Page Programming Time		0.9	27	ms
Chip Programming Time		14	150	sec
Byte Program Time		7		us

LATCHUP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.		

PACKAGE INFORMATION

Title: Package Outline for PDIP 42L (600MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	---	0.51	3.73	0.38	1.14	0.20	51.94	15.11	13.84		15.75	2.92	0.38
	Nom.	---	0.64	3.94	0.46	1.27	0.25	52.07	15.24	13.97	2.54	16.51	3.30	0.64
	Max.	4.90	0.76	4.14	0.53	1.40	0.30	52.20	15.37	14.10		17.27	3.68	0.89
Inch	Min.	---	0.020	0.147	0.015	0.045	0.008	2.045	0.595	0.545		0.620	0.115	0.015
	Nom.	---	0.025	0.155	0.018	0.050	0.010	2.050	0.600	0.550	0.100	0.650	0.130	0.025
	Max.	0.193	0.030	0.163	0.021	0.055	0.012	2.055	0.605	0.555		0.680	0.145	0.035

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0202.5	5				07-04-'02

Revision History

Revision No.	Description	Page	Date
1.3	Changed title from "Advanced Information" to "Preliminary"	P1	APR/26/2000
1.4	To modify package information	P17	NOV/19/2002

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