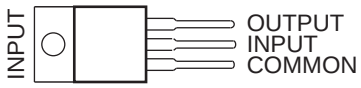
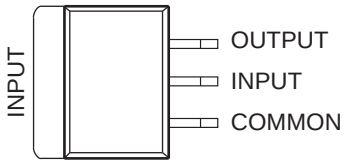
FEATURES

- 3-Terminal Regulators
- Output Current up to 1.5 A
- No External Components
- Internal Thermal-Overload Protection
- High Power-Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

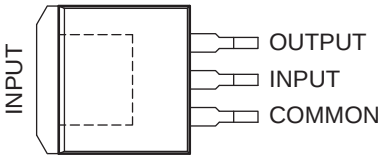
KCS (TO-220) PACKAGE
(TOP VIEW)



KTE (PowerFLEX™) PACKAGE
(TOP VIEW)



KTT (TO-263) PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This series of fixed-negative-voltage integrated-circuit voltage regulators is designed to complement Series μA7900 in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 A of output current. The internal current limiting and thermal shutdown features of these regulators essentially make them immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power-pass element in precision regulators.

ORDERING INFORMATION(1)

T_J	$V_{O(NOM)}$	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	–12 V	TO-220, short shoulder – KCS	Tube of 50	UA7912CKCS	UA7912C
	–8 V	PowerFLEX™ – KTE	Reel of 2000	UA7908CKTER	UA7908C
		TO-220, short shoulder – KCS	Tube of 50	UA7908CKCS	UA7908C
	–5 V	PowerFLEX – KTE	Reel of 2000	UA7905CKTER	UA7905C
		TO-220, short shoulder – KCS	Tube of 50	UA7905CKCS	UA7905C
		TO-263 – KTT	Reel of 500	UA7905CKTTR	UA7905C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

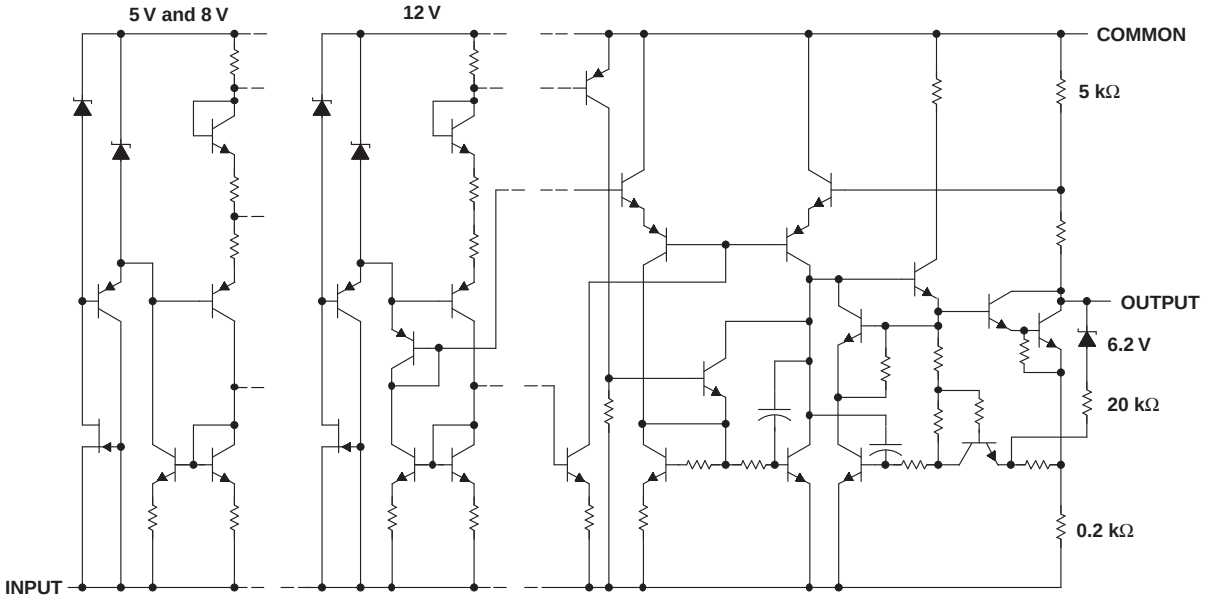
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerFLEX, PowerPAD are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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SCHEMATIC



All component values are nominal.

Absolute Maximum Ratings(1)

over virtual junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage		–35	V
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Package Thermal Data(1)

PACKAGE	BOARD	θ_{JA}	θ_{JC}	θ_{JP}(2)
PowerFLEX (KTE)	High K, JESD 51-5	23°C/W	3°C/W	2.7°C/W
TO-220 (KCS)	High K, JESD 51-5	19°C/W	17°C/W	3°C/W
TO-263 (KTT)	High K, JESD 51-5	25.3°C/W	18°C/W	1.94°C/W

(1) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(2) For packages with exposed thermal pads, such as QFN, PowerPAD™, or PowerFLEX, θ_{JP} is defined as the thermal resistance between the die junction and the bottom of the exposed pad.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_I	Input voltage	μA7905	–7	–25	V
		μA7908	–10.5	–25	
		μA7912	–14.5	–30	
I_O	Output current			1.5	A
T_J	Operating virtual junction temperature		0	125	°C

uA7905 Electrical Characteristics

at specified virtual junction temperature, V_I = –10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J(1)	μA7905C			UNIT
			MIN	TYP	MAX	
Output voltage(2)	I_O = 5 mA to 1 A, V_I = –7 V to –20 V, $P_D \le 15$ W	25°C	–4.8	–5	–5.2	V
		0°C to 125°C	–4.75		–5.25	
Input regulation	V_I = –7 V to –25 V			12.5	50	mV
	V_I = –8 V to –12 V			4	15	
Ripple rejection	V_I = –8 V to –12 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A			15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		–0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		125		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = –7 V to –25 V			0.15	0.5	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.
(2) This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA7908 Electrical Characteristics

at specified virtual junction temperature, V_I = –14 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J(1)	μA7908C			UNIT
			MIN	TYP	MAX	
Output voltage(2)	I_O = 5 mA to 1 A, V_I = –10.5 V to –23 V, $P_D \le 15$ W	25°C	–7.7	–8	–8.3	V
		0°C to 125°C	–7.6		–8.4	
Input regulation	V_I = –10.5 V to –25 V			12.5	160	mV
	V_I = –11 V to –17 V			4	80	
Ripple rejection	V_I = –11.5 V to –21.5 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A			15	160	mV
	I_O = 250 mA to 750 mA			5	80	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		–0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		200		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = –10.5 V to –25 V			0.15	1	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.
(2) This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA7912 Electrical Characteristics

at specified virtual junction temperature, V_I = –19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J(1)	μA7912C			UNIT
			MIN	TYP	MAX	
Output voltage(2)	I_O = 5 mA to 1 A, V_I = –14.5 V to –27 V, $P_D \le$ 15 W	25°C	–11.5	–12	–12.5	V
		0°C to 125°C	–11.4		–12.6	
Input regulation	V_I = –14.5 V to –25 V			5	80	mV
	V_I = –16 V to –22 V			3	30	
Ripple rejection	V_I = –15 V to –25 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A			15	200	mV
	I_O = 250 mA to 750 mA			5	75	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		–0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		300		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = –14.5 V to –25 V			0.04	0.5	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.
(2) This specification applies only for dc power dissipation permitted by absolute maximum ratings.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA7905CKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	0 to 125		
UA7905CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7905C	Samples
UA7905CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7905C	Samples
UA7905CKTER	OBSOLETE	PFM	KTE	3		TBD	Call TI	Call TI	0 to 125	UA7905C	
UA7905CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7905C	Samples
UA7908CKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	0 to 125		
UA7908CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7908C	Samples
UA7908CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7908C	Samples
UA7908CKTER	OBSOLETE	PFM	KTE	3		TBD	Call TI	Call TI	0 to 125	UA7908C	
UA7912CKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	0 to 125		
UA7912CKCS	OBSOLETE	TO-220	KCS	3		TBD	Call TI	Call TI	0 to 125	UA7912C	
UA7912CKTER	OBSOLETE	PFM	KTE	3		TBD	Call TI	Call TI	0 to 125	UA7912C	
UA7915CKTER	OBSOLETE	PFM	KTE	3		TBD	Call TI	Call TI	0 to 125	UA7915C	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

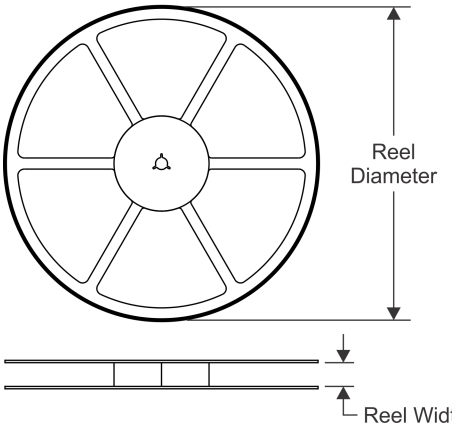
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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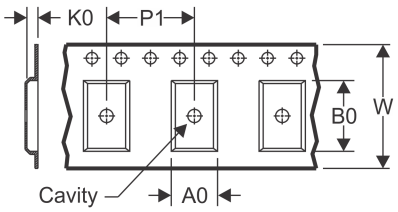
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

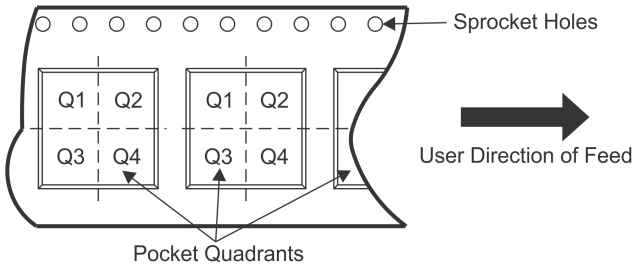


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

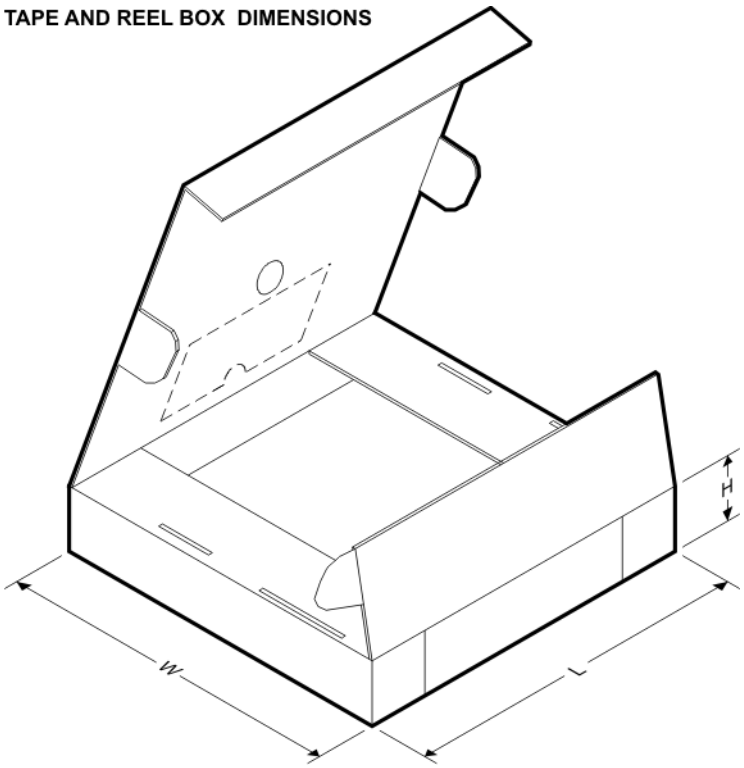
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA7905CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

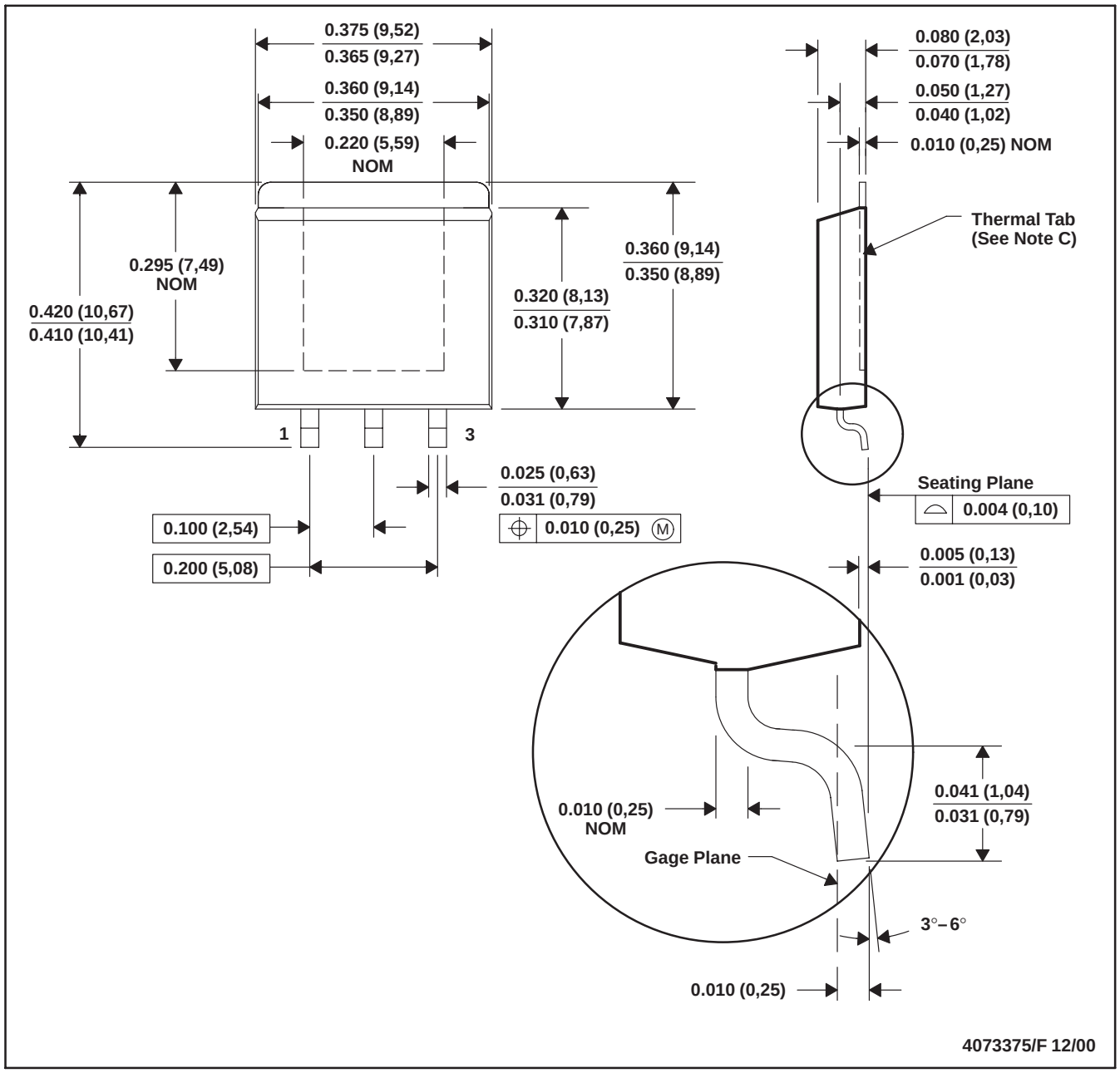


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA7905CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0

MPFM001E – OCTOBER 1994 – REVISED JANUARY 2001

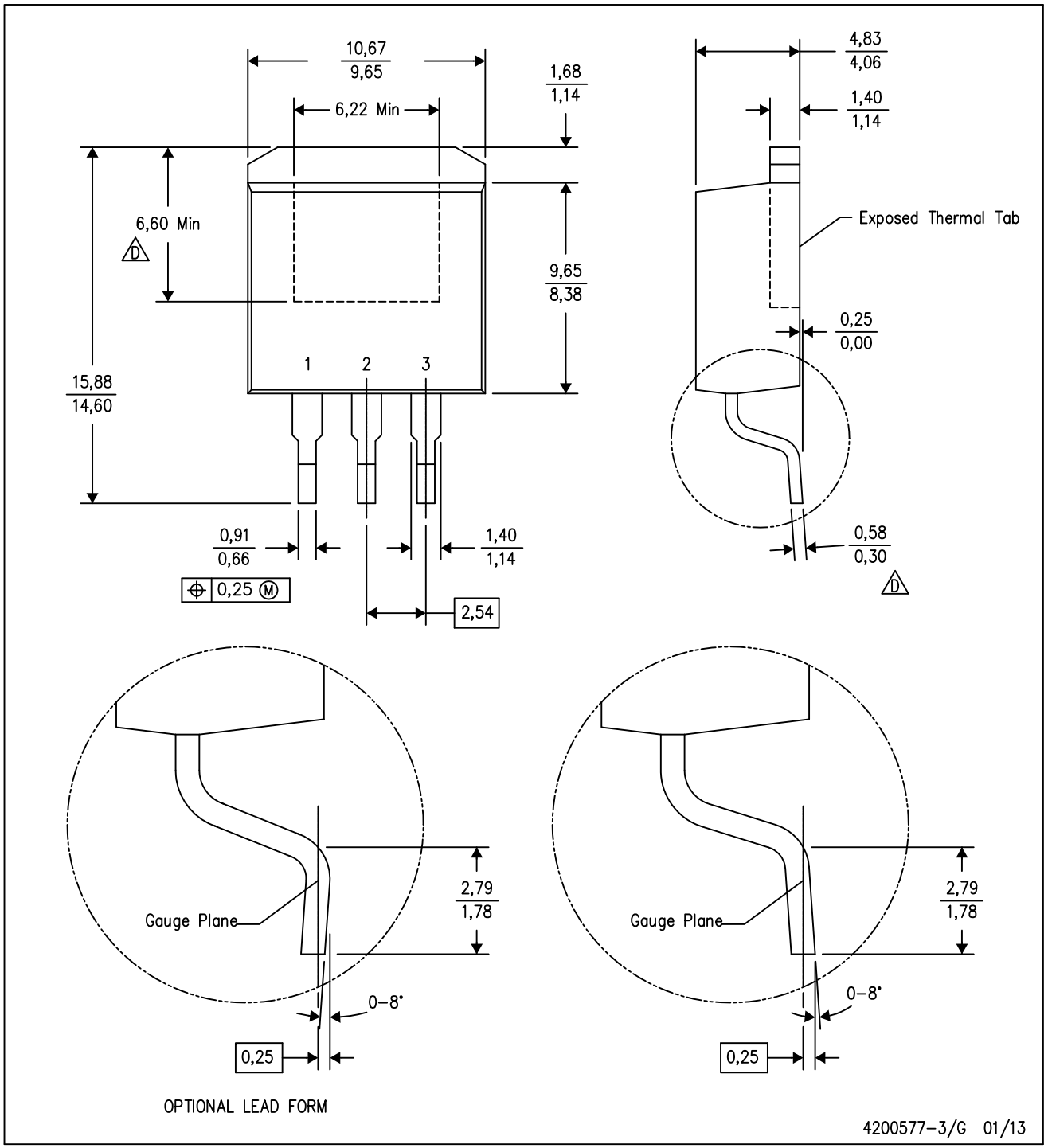
KTE (R-PSFM-G3) **PowerFLEX™ PLASTIC FLANGE-MOUNT**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the thermal tab.
D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
E. Falls within JEDEC MO-169

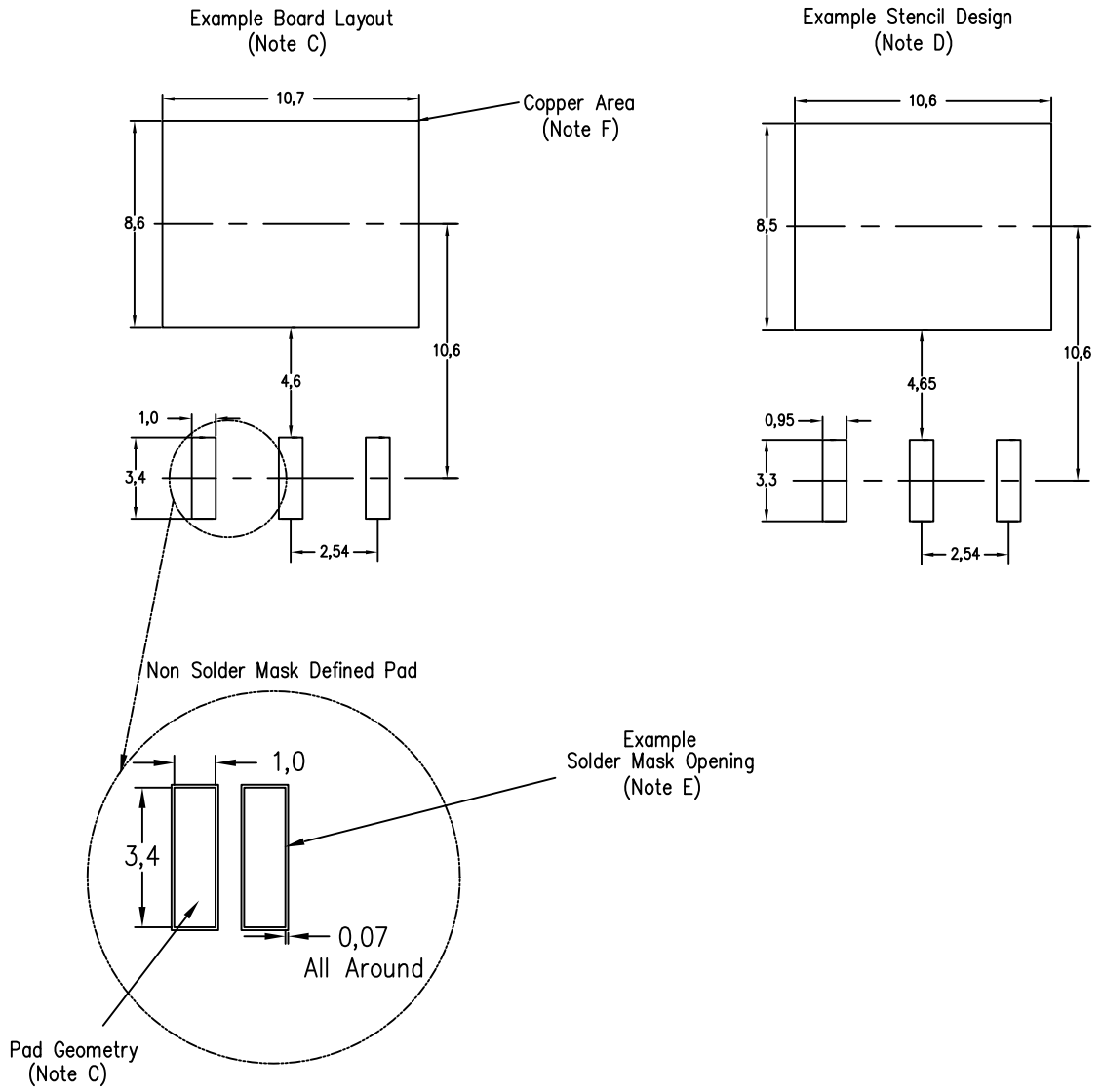
PowerFLEX is a trademark of Texas Instruments.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE

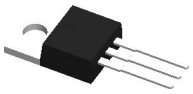


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

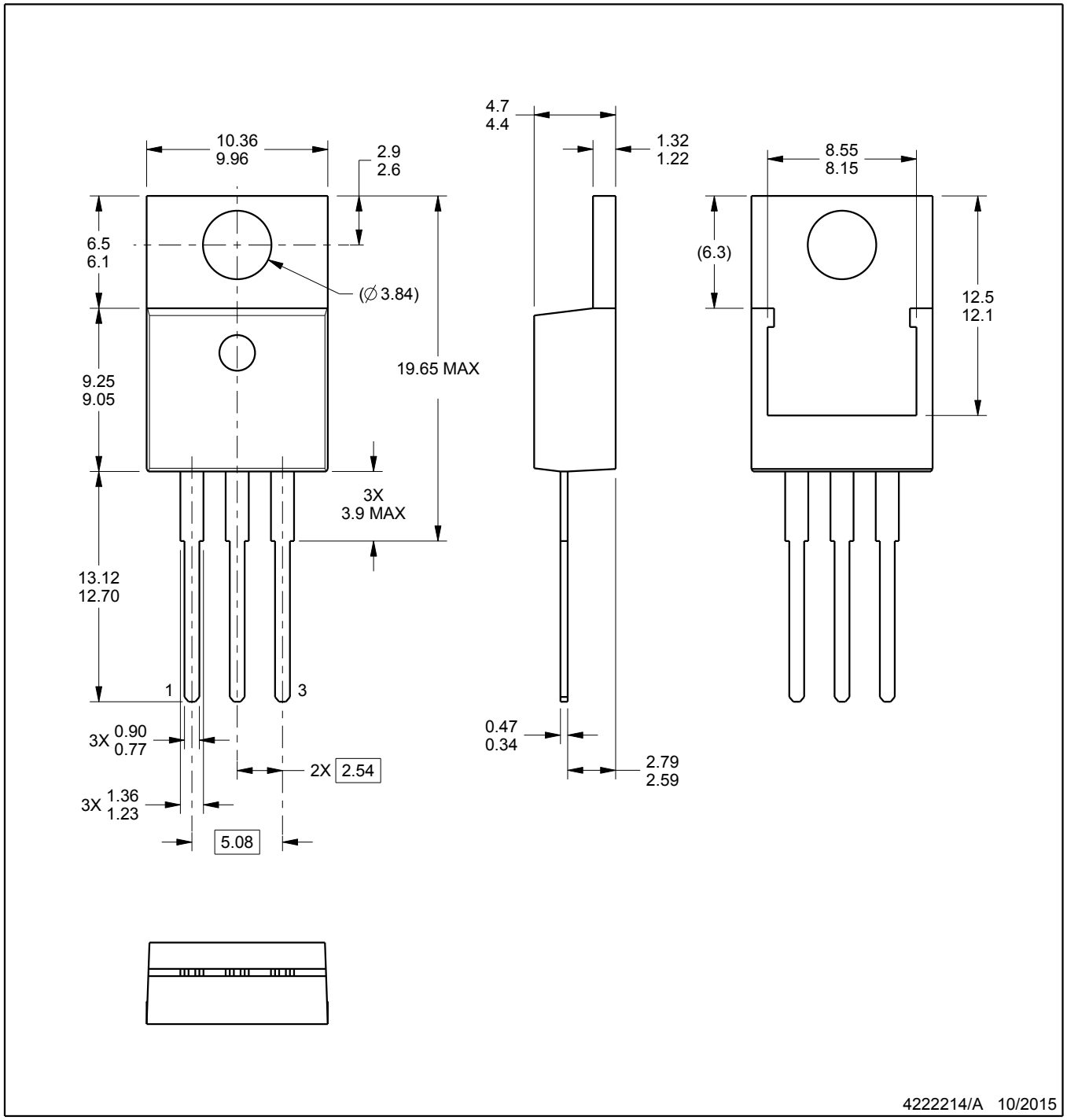


PACKAGE OUTLINE

KCS0003B

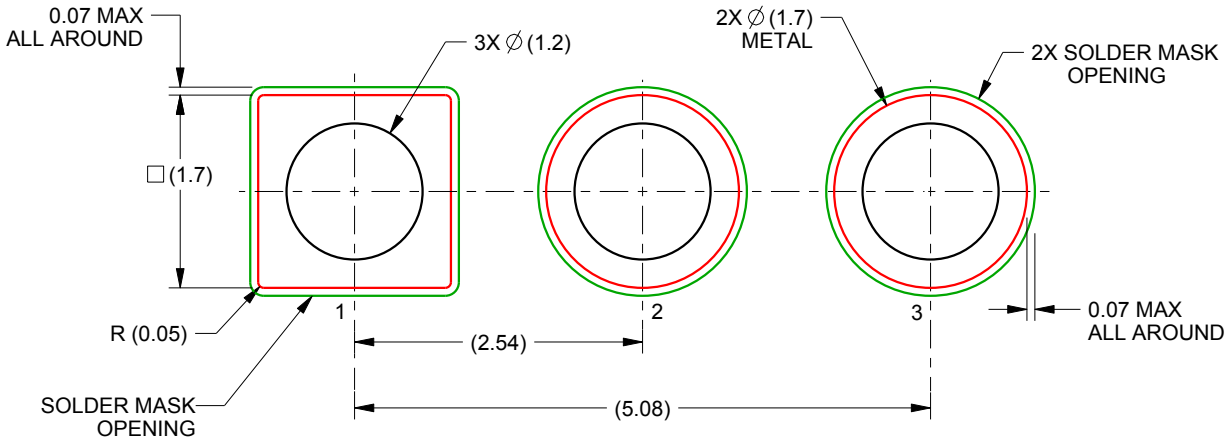
TO-220 - 19.65 mm max height

TO-220



NOTES:

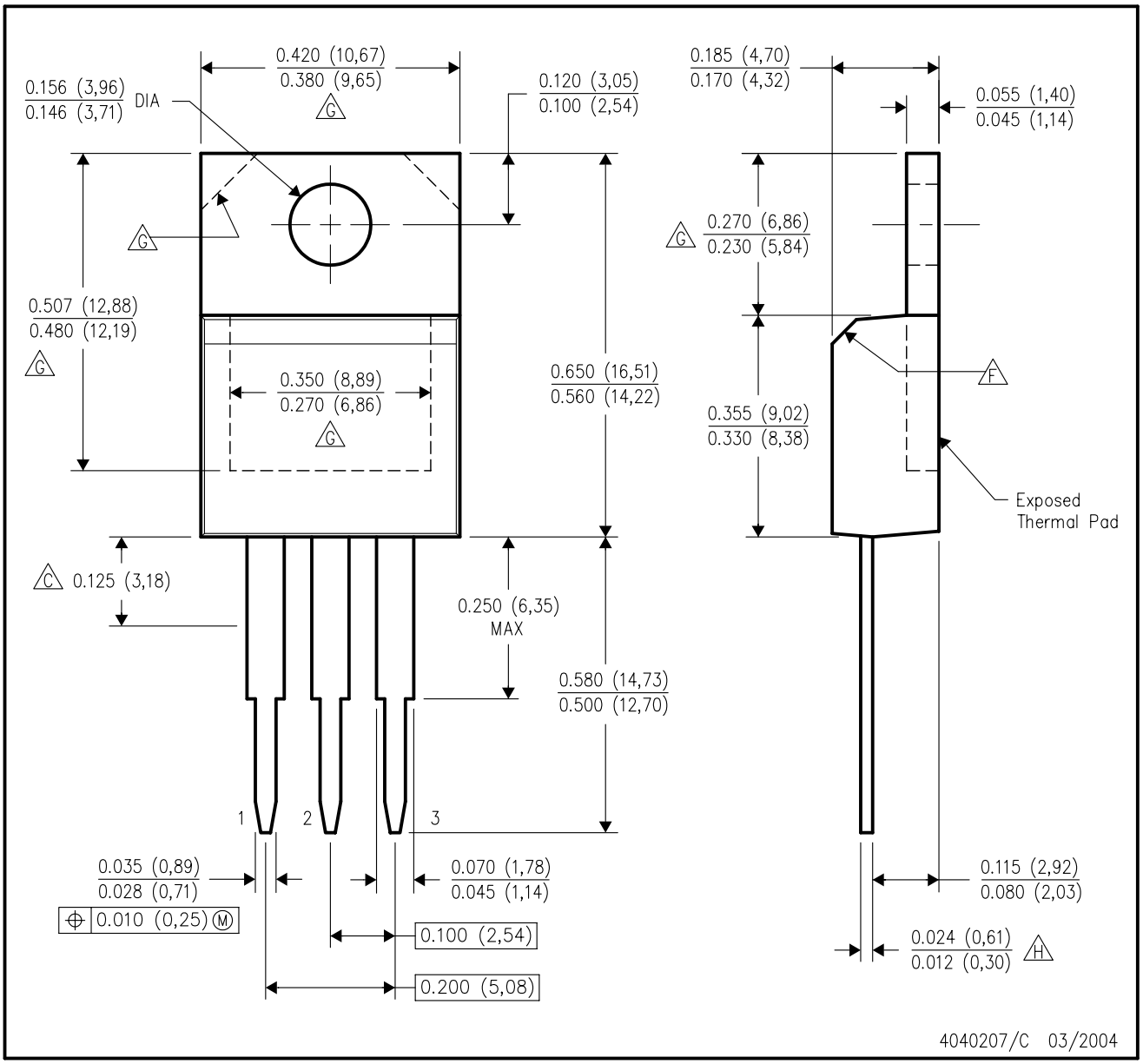
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/A 10/2015

KC (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Thermal pad contour optional within these dimensions.
- H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness.

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