MH4V724AWXJ -5, -6

FAST PAGE MODE 301989888 - BIT (4194304 - WORD BY 72 - BIT) DYNAMIC RAM

DESCRIPTION

The MH4V724AWXJ is 4194304-word x 72-bit dynamic ram module. This consist of four industry standard 4M x 16 dynamic RAMs in SOJ and two industry standard 4Mx 4 dynamic RAMs in SOJ and one industry EEPROM in TSSOP.

The mounting of SOJs and TSSOP on a card edge dual in-line package provides any application where high densities and large of quantities memory are required.

This is a socket-type memory module ,suitable for easy interchange or addition of module.

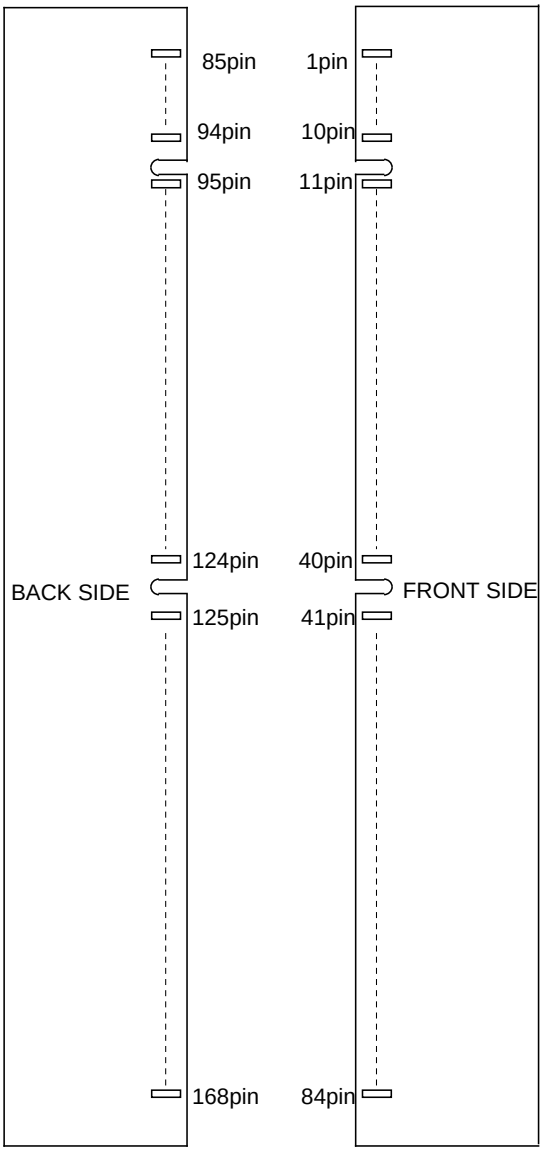
FEATURES

Type name	/RAS access time (max.ns)	/CAS access time (max.ns)	Address access time (max.ns)	/OE access time (max.ns)	Cycle time (min.ns)
MH4V724AWXJ-5	50	13	25	13	90
MH4V724AWXJ-6	60	15	30	15	110

- Utilizes industry standard 4M x 16 RAMs in SOJ and industry standard 4M x 4 RAMs in SOJ and industry standard EEPROM in TSSOP
- 168-pin (84-pin dual dual in-line package)
- Single +3.3V(±0.3V) supply operation
- Low stand-by power dissipation
  10.8mW(Max) . . . . . LVCMOS input level
- Low operation power dissipation
  MH4V724AWXJ -5 . . . . . 2.82W(Max)
  MH4V724AWXJ -6 . . . . . 2.53W(Max)
- All input are directly LVTTL compatible
- All output are three-state and directly LVTTL compatible
- Includes(0.22uF x 8) decoupling capacitors
- 4096 refresh cycle every 64ms
- Fast-page mode,Read-modify-write, /CAS before /RAS refresh,Hidden refresh capabilities
- JEDEC standard pin configuration and SPD
- Gold plating contact pads

Row Address	A0 ~ A11
Column Address	A0 ~ A9

PIN CONFIGURATION



APPLICATION

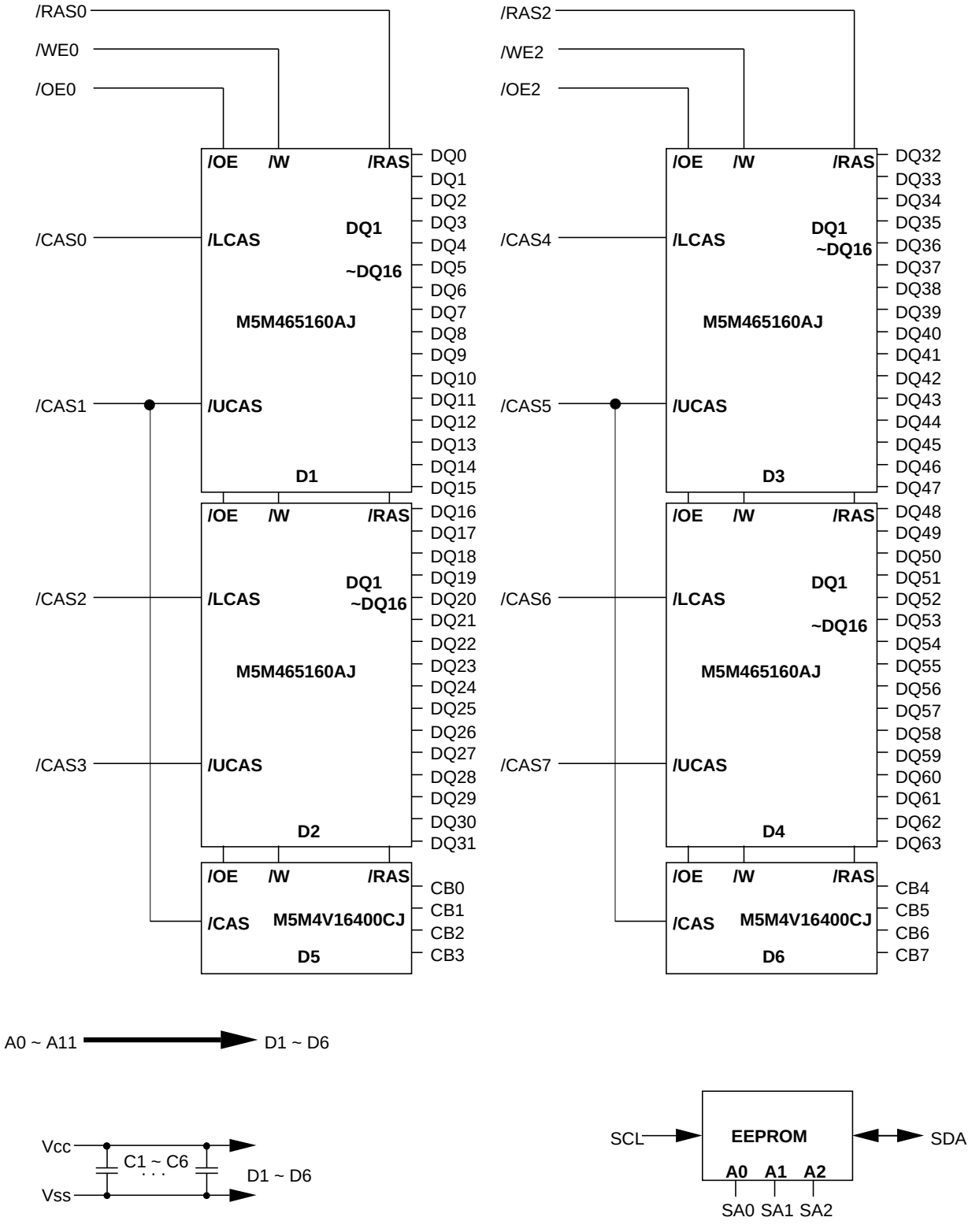
Main memory unit for computers , Microcomputer memory

PIN CONFIGURATION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	/OE2	86	DQ32	128	DU
3	DQ1	45	/RAS2	87	DQ33	129	NC
4	DQ2	46	/CAS2	88	DQ34	130	/CAS6
5	DQ3	47	/CAS3	89	DQ35	131	/CAS7
6	Vcc	48	/WE2	90	Vcc	132	DU
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	DU	104	DQ47	146	DU
21	NC	63	NC	105	NC	147	NC
22	NC	64	Vss	106	NC	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE0	69	DQ24	111	DU	153	DQ56
28	/CAS0	70	DQ25	112	/CAS4	154	DQ57
29	/CAS1	71	DQ26	113	/CAS5	155	DQ58
30	/RAS0	72	DQ27	114	NC	156	DQ59
31	/OE0	73	Vcc	115	DU	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	A11	164	NC
39	NC	81	NC	123	NC	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	DU	167	SA2
42	DU	84	Vcc	126	DU	168	Vcc

NC: No Connect
DU: Don't Use

BLOCK DIAGRAM



Serial Presence Detect TABLE

Bytes	Function described		SPD entry data	SPD DATA entry(Hex)
0	Defines # bytes written into serial memory at module mfgr		128	80
1	Total # bytes of SPD memory device		256 Bytes	08
2	Fundamental memory type		FPM DRAM	01
3	# Row Addresses on this assembly		A0-A11	0C
4	# Column Addresses on this assembly		A0-A9	0A
5	# Module Banks on this assembly		1bank	01
6	Data Width of this assembly...		x72	48
7	... Data Width continuation		0	00
8	Voltage interface standard of this assembly		3.3V LVTTL	02
9	RAS# access time of this assembly	-5	50ns	32
		-6	60ns	3C
10	CAS# access time of this assembly	-5	13ns	0D
		-6	15ns	0F
11	DIMM Configuration type (Non-parity,Parity,ECC)		ECC	02
12	Refresh Rate/Type		normal refresh(15.625uS)	00
13	DRAM width,Primary DRAM		x16	10
14	Error Checking DRAM data width		x4	04
15-31	Reserved for future offerings		open	00
32-61	Superset Memory type(may be used in future)		open	00
62	SPD Data Revision Code		Rev 1	01
63	Checksum for bytes 0-62		Check sum for -5	40
			Check sum for -6	4C
64-71	Manufacturers JEDEC ID code per JEP-106		MITSUBISHI	1CFFFFFFFFFFFFFF
72	Manufacturing location		Miyoshi,Japan	01
			Tajima,Japan	02
			NC,USA	03
			Germany	04
73-90	Manufacturer's Part Number		MH4V724AWXJ-5	4D4834563732344157584A2D352D352020202020
			MH4V724AWXJ-6	4D4834563732344157584A2D362D362020202020
91-92	Revision Code		PCB revision	rrrr
93-94	Manufacturing date		year/week code	yy/ww
95-98	Assembly Serial Number		serial number	ssssssss
99-125	Manufacturer Specific Data		open	00
126-127	Reserved		open	00
128-255	Open User Free-Form area not defined		open	00

FUNCTION

The MH4V724AWXJ provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., Fast page mode, /RAS-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	/RAS	/CAS	/W	/OE	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
/CAS before /RAS refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5~ 4.6	V
VI	Input Voltage		-0.5~ 4.6	V
VO	Output Voltage		-0.5~ 4.6	V
IO	Output current		50	mA
Pd	Power dissipation	Ta=25°C	6	W
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		-40~125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
VIH	High-level input voltage, all inputs	2.0		Vcc+0.3	V
VIL	Low-level input voltage	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
VOH	High-level output voltage		IOH=-2.0mA	2.4		Vcc	V
VOL	Low-level output voltage		IOL=2.0mA	0		0.4	V
IOZ	Off-state output current		Q floating 0V ≤VOUT≤ Vcc	-10		10	uA
I I	Input current (except /CAS)		0V≤VIN≤Vcc+0.3, Other input pins=0V	-60		60	uA
I I (CAS)	Input current (/CAS)		0V≤VIN≤Vcc+0.3, Other input pins=0V	-20		20	uA
ICC1 (AV)	Average supply current from Vcc operating (Note 3,4,5)	- 5	/RAS, /CAS cycling tRC=tWC=min. output open			780	mA
		- 6				700	
ICC2	Supply current from Vcc , stand-by		/RAS=/CAS =VIH, output open			8	mA
			/RAS=/CAS=WE≥Vcc -0.2, output open			3	
ICC4(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4,5)	- 5	/RAS=VIL,/CAS cycling tPC=min. output open			580	mA
		- 6				520	
ICC6(AV)	Average supply current from Vcc /CAS before /RAS refresh mode (Note 3,5)	- 5	/CAS before /RAS refresh cycling tRC=min. output open			780	mA
		- 6				700	

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc3 (AV), Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Under condition of column address being changed once or less while /RAS=VIL and /CAS=VIH

CAPACITANCE (Ta = 0~70°C, Vcc = 3.3V±0.3V, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI (/CAS)	Input capacitance, /CAS input	VI=Vss f=1MHZ Vi=25mVrms			22	pF
CI	Input capacitance, except /CAS input				75	pF
C(DQ)	Input/Output capacitance,DATA				22	pF
C(SCL)	Input capacitance, SPD clock				7	pF
C(SDA)	Input/Output capacitance,SPD DATA				7	pF
C(SA0~3)	Input capacitance, SPD address				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted , see notes 6,13,14)

Symbol	Parameter		Limits				Unit
			- 5		- 6		
			Min	Max	Min	Max	
tCAC	Access time from /CAS	(Note 7,8)		13		15	ns
tRAC	Access time from /RAS	(Note 7,9)		50		60	ns
tAA	Column address access time	(Note 7,10)		25		30	ns
tCPA	Access time from /CAS precharge	(Note 7,11)		30		35	ns
tOEA	Access time from /OE	(Note 7)		13		15	ns
tCLZ	Output low impedance time /CAS low	(Note 7)	5		5		ns
tOFF	Output disable time after /CAS high	(Note 12)	0	13	0	15	ns
tOEZ	Output disable time after /OE high	(Note 12)	0	13	0	15	ns

Note 6: An initial pause of 500us is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing /CAS before /RAS refresh).
Note the /RAS may be cycled during the initial pause . And any 8 /RAS or /RAS /CAS cycles are required after prolonged periods (greater than 64 ms) of /RAS inactivity before proper device operation is achieved.
7: Measured with a load circuit equivalent to 1 TTL load and 100pF.The reference levels for measuring of output signals are 2.0V(VOH)and 0.8V(VOL).
8: Assumes that tRCD ≥ tRCD(max), tASC ≥ tASC(max).
9: Assumes that tRCD ≤ tRCD(max) and tRAD ≤ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
10: Assumes that tRAD ≥ tRAD(max) and tASC ≤ tASC(max).
11: Assumes that tCP ≤ tCP(max) and tASC ≥ tASC(max).
12: tOFF (max) and tOEZ(max) defines the time at which the output achieves the high impedance state (IOUT ≤ I ± 10uA I) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)
(Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted ,see notes 13,14)

Symbol	Parameter		Limits				Unit
			-5		-6		
			Min	Max	Min	Max	
tREF	Refresh cycle time			64		64	ms
tRP	/RAS high pulse width		30		40		ns
tRCD	Delay time, /RAS low to /CAS low	(Note15)	18	37	20	45	ns
tCRP	Delay time, /CAS high to /RAS low		10		10		ns
tRPC	Delay time, /RAS high to /CAS low		0		0		ns
tCPN	/CAS high pulse width		10		10		ns
tRAD	Column address delay time from /RAS low	(Note16)	13	25	15	30	ns
tASR	Row address setup time before /RAS low		0		0		ns
tASC	Column address setup time before /CAS low	(Note17)	0	5	0	10	ns
tRAH	Row address hold time after /RAS low		8		10		ns
tCAH	Column address hold time after /CAS low		13		15		ns
tDZC	Delay time, data to /CAS low	(Note18)	0		0		ns
tDZO	Delay time, data to /OE low	(Note18)	0		0		ns
tCDD	Delay time, /CAS high to data	(Note19)	13		15		ns
tODD	Delay time, /OE high to data	(Note19)	13		15		ns
tT	Transition time	(Note20)	1	50	1	50	ns

Note 13: The timing requirements are assumed tT =5ns.
14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.V_{IH}(min) and V_{IL}(max) of the switching characteristics are 2.0V and 0.8V respectively
15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.tRCD(min) is specified as tRCD(min) = tRAH(min) + 2tT + tASC(min) .
16: tRAD(max) is specified as a reference point only. If tRAD≥tRAD(max) and tASC≤tASC(max), access time is controlled exclusively by tAA.
17: tASC(max) is specified as a reference point only. If tRCD≥tRCD(max) and tASC≥tASC(max), access time is controlled exclusively by tCAC.
18: Either tDZC or tDZO must be satisfied.
19: Either tCDD or tODD must be satisfied.
20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		-5		-6		
		Min	Max	Min	Max	
tRC	Read cycle time	90		110		ns
tRAS	/RAS low pulse width	50	10000	60	10000	ns
tCAS	/CAS low pulse width	13	10000	15	10000	ns
tCSH	/CAS hold time after /RAS low	50		60		ns
tRSH	/RAS hold time after /CAS low	13		15		ns
tRCS	Read Setup time after /CAS high	0		0		ns
tRCH	Read hold time after /CAS low (Note 21)	0		0		ns
tRRH	Read hold time after /RAS low (Note 21)	10		10		ns
tRAL	Column address to /RAS hold time	25		30		ns
tOCH	/CAS hold time after /OE low	13		15		ns
tORH	/RAS hold time after /OE low	13		15		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		-5		-6		
		Min	Max	Min	Max	
tWC	Write cycle time	90		110		ns
tRAS	/RAS low pulse width	50	10000	60	10000	ns
tCAS	/CAS low pulse width	13	10000	15	10000	ns
tCSH	/CAS hold time after /RAS low	50		60		ns
tRSH	/RAS hold time after /CAS low	13		15		ns
tWCS	Write setup time before /CAS low (Note 23)	0		0		ns
tWCH	Write hold time after /CAS low	10		10		ns
tCWL	/CAS hold time after /W low	13		15		ns
tRWL	/RAS hold time after W low	13		15		ns
tWP	Write pulse width	10		10		ns
tDS	Data setup time before /CAS low or W low	0		0		ns
tDH	Data hold time after /CAS low or W low	10		10		ns
tOEH	/OE hold time after /W low	13		15		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		-5		-6		
		Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note22)	131		155		ns
tRAS	/RAS low pulse width	91	10000	105	10000	ns
tCAS	/CAS low pulse width	54	10000	60	10000	ns
tCSH	/CAS hold time after /RAS low	91		105		ns
tRSH	/RAS hold time after /CAS low	54		60		ns
tRCS	Read setup time before /CAS low	0		0		ns
tCWD	Delay time, /CAS low to /W low (Note23)	36		40		ns
tRWD	Delay time, /RAS low to /W low (Note23)	73		85		ns
tAWD	Delay time, address to /W low (Note23)	48		55		ns
tCWL	/CAS hole time after /W low	15		15		ns
tRWL	/RAS hold time after /W low	15		15		ns
tWP	Write pulse width	10		10		ns
tDS	Data setup time before /W loe	0		0		ns
tDH	Data hold time after /W low	10		10		ns
tOEH	/OE hold time after /W low	13		15		ns

Note 22: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+5tT.
23:tWCS, tCWD,tRWD ,tAWD and,tCPWD are specified as reference points only. If tWCS≥tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≥tCWD(min), tRWD≥tRWD (min), tAWD≥tAWD(min) and tCPWD ≥tCPWD(min) (for Fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) is satisfied,the DQ (at access time and until /CAS or /OE goes back to VIH) is indeterminate.

Fast Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits				Unit
		-5		-6		
		Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	35		40		ns
tPRWC	Fast page mode read write/read modify write cycle time	76		85		ns
tRAS	/RAS low pulse width for read write cycle (Note25)	85	51200	100	51200	ns
tCP	/CAS high pulse width (Note26)	8	10	10	15	ns
tCPRH	/RAS hold time after /CAS precharge	30		35		ns
tCPWD	Delay time, /CAS precharge to W low (Note23)	53		60		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective Fast page mode cycle.
25: tRAS(min) is specified as two cycles of /CAS input are performed.
26: tCP(max) is specified as a reference point only. If tCP ≥ tCP(max),access time is controlled exclusively by tCAC.

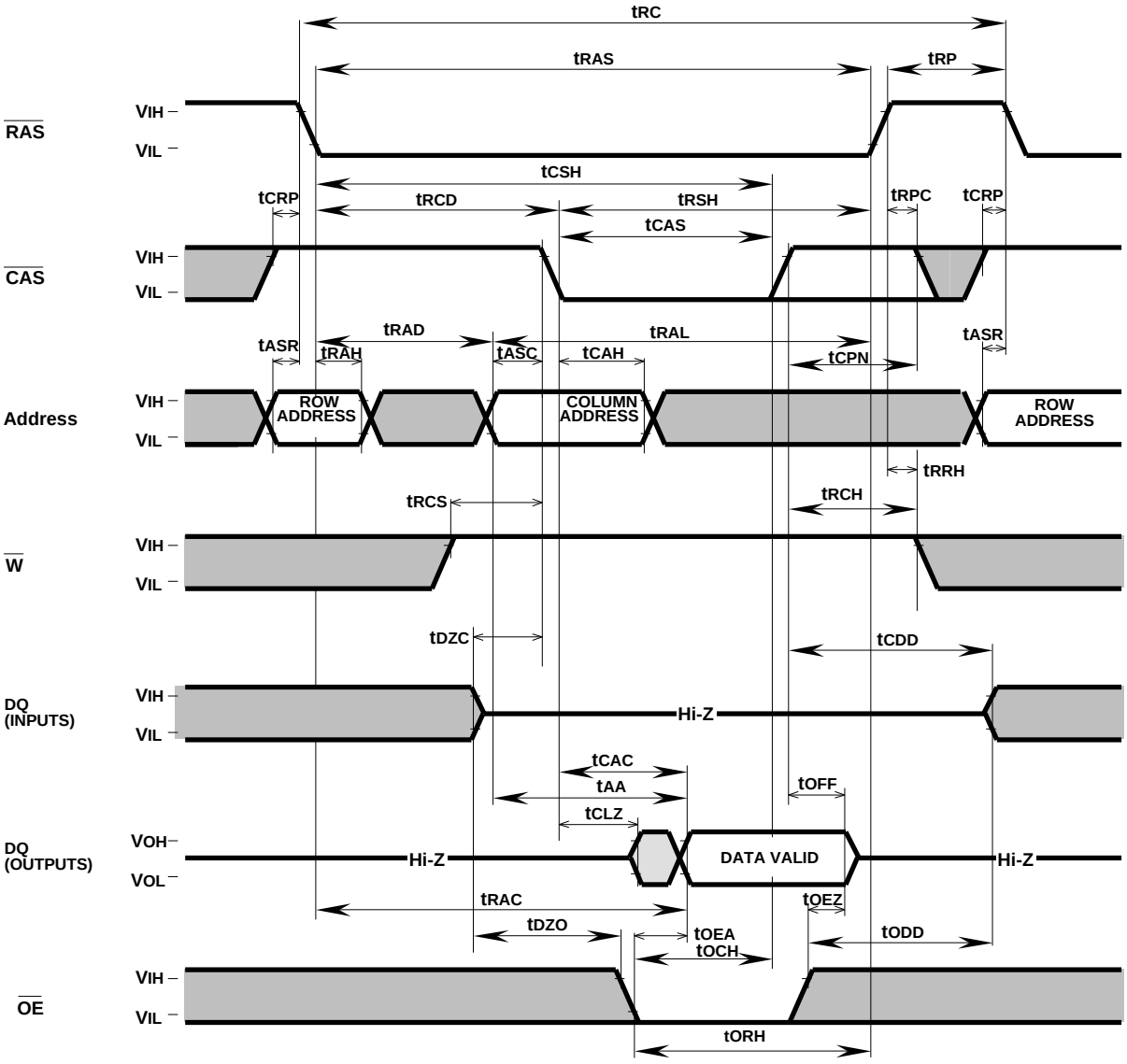
/CAS before /RAS Refresh Cycle (Note 27)

Symbol	Parameter	Limits				Unit
		-5		-6		
		Min	Max	Min	Max	
tCSR	/CAS setup time before /RAS low	10		10		ns
tCHR	/CAS hold time after /RAS low	10		10		ns
tRSR	Read setup time before /RAS low	10		10		ns
tRHR	Read hold time after /RAS low	10		10		ns

Note 27: Eight or more /CAS before /RAS cycles instead of eight /RAS cycles are necessary for proper operation of /CAS before /RAS refresh mode.

Timing Diagrams (Note 28)

Read Cycle

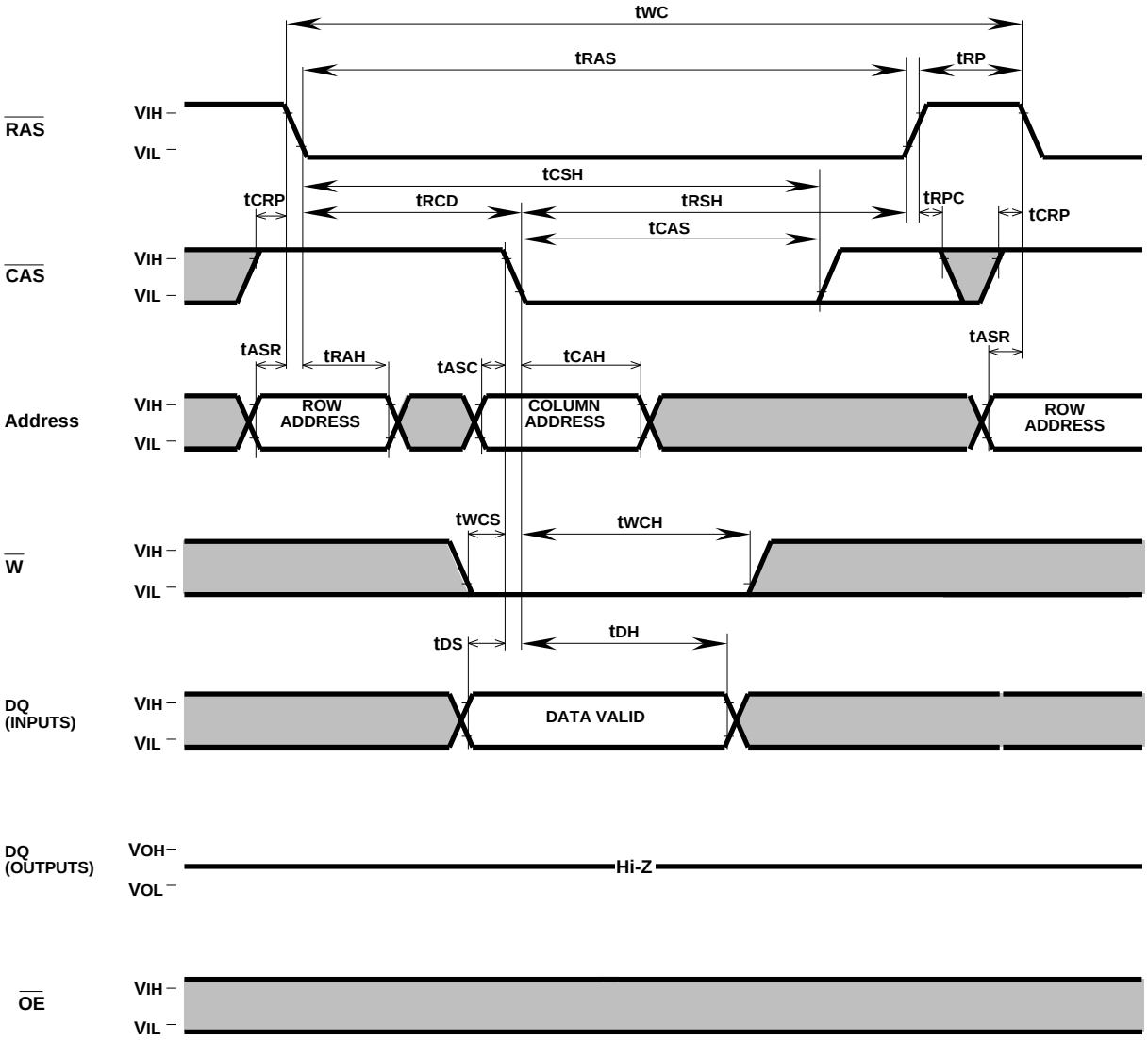


Note 28

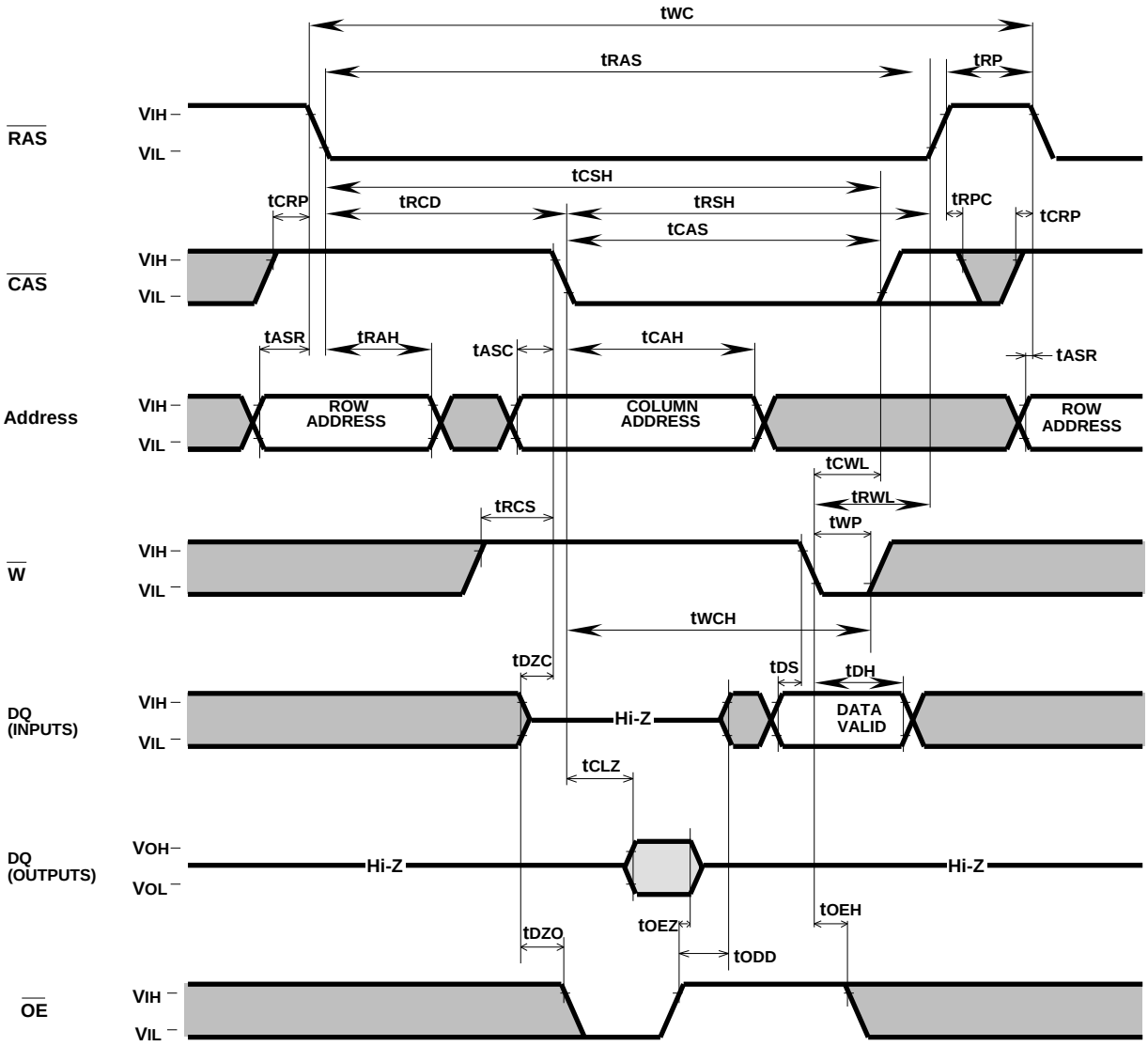
Indicates the don't care input.
VIH(min)≤VIN≤VIH(max) or VIL(min)≤VIN≤VIL(max)

Indicates the invalid output.

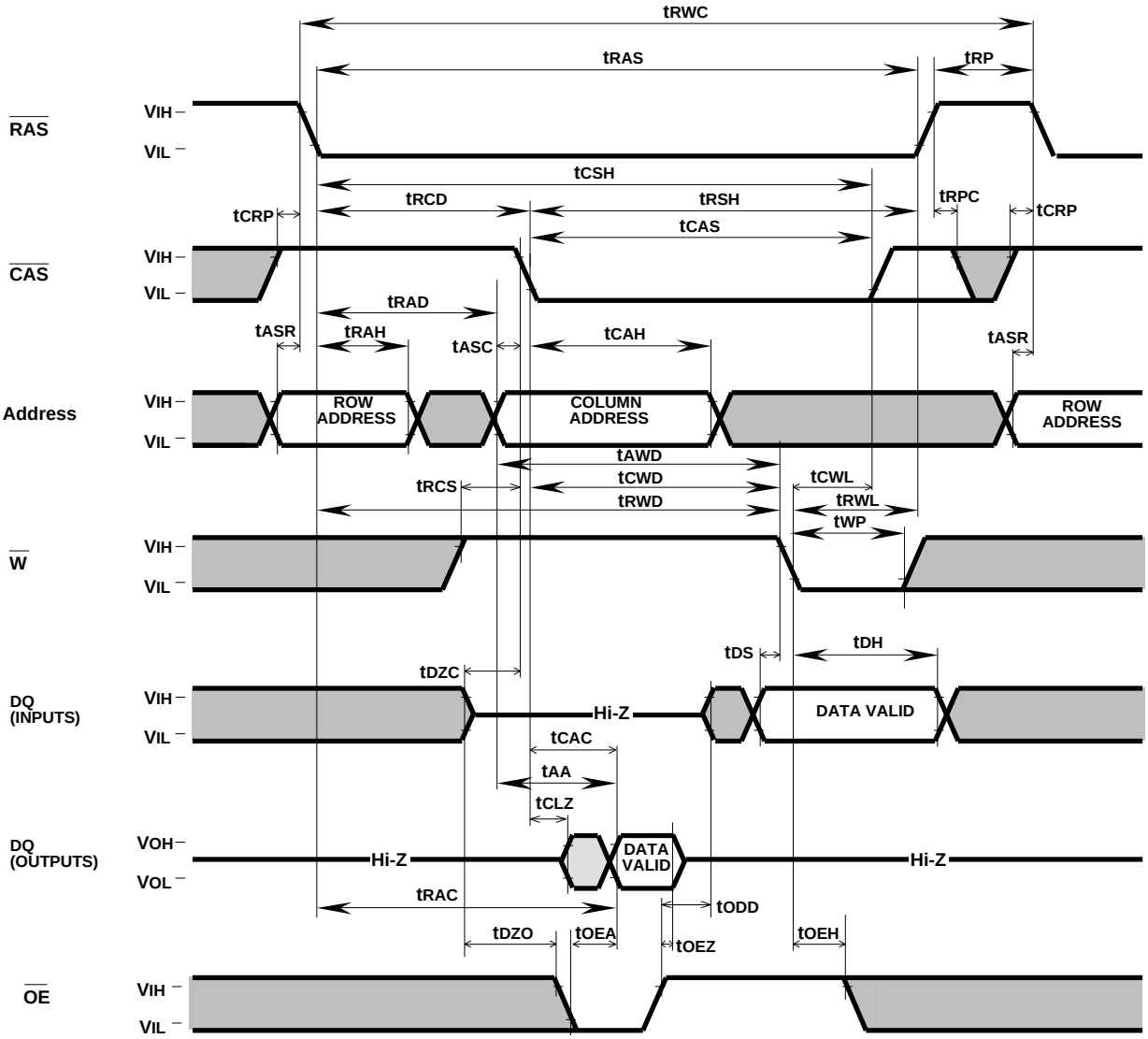
Write Cycle (Early write)



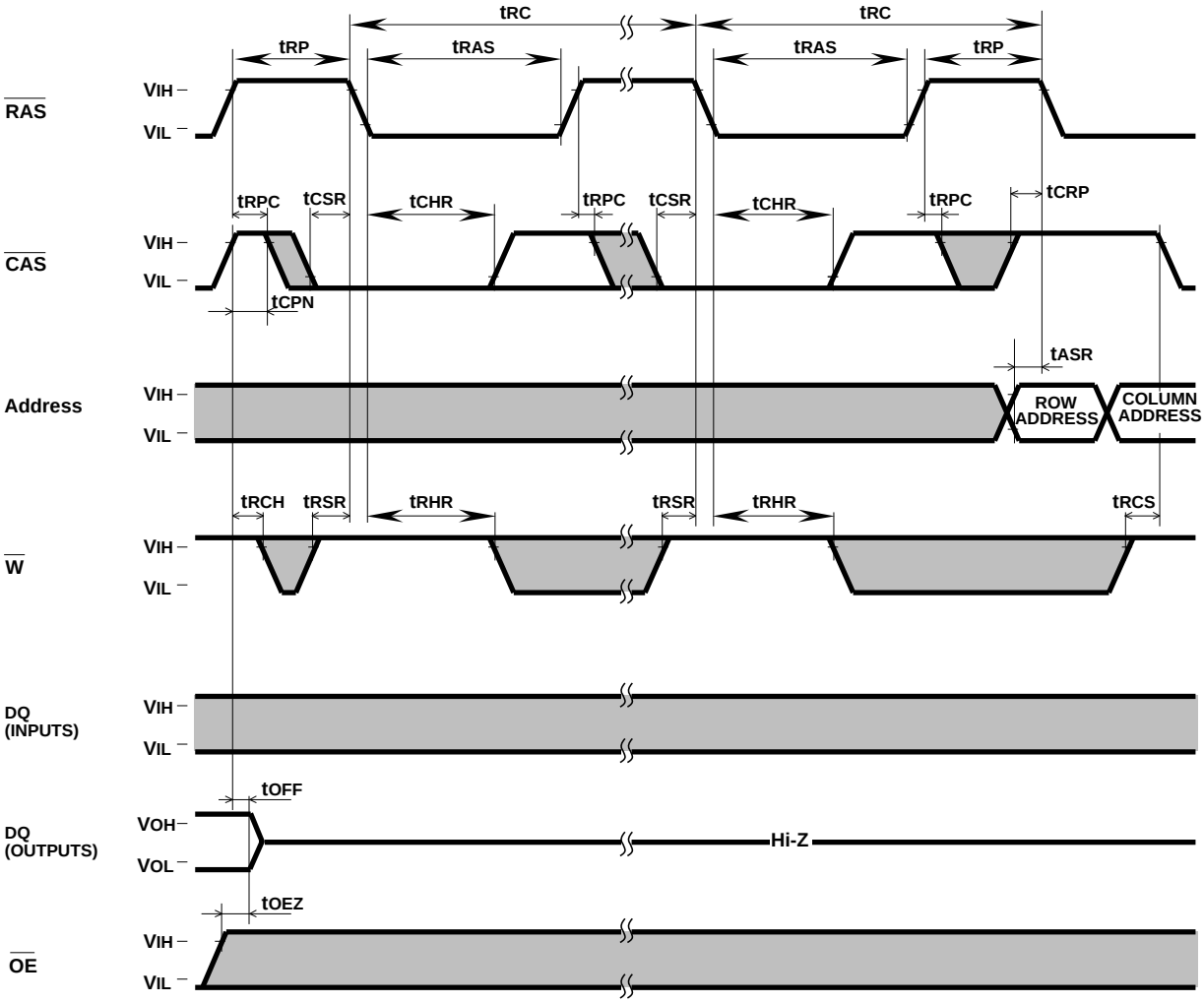
Write Cycle (Delayed write)



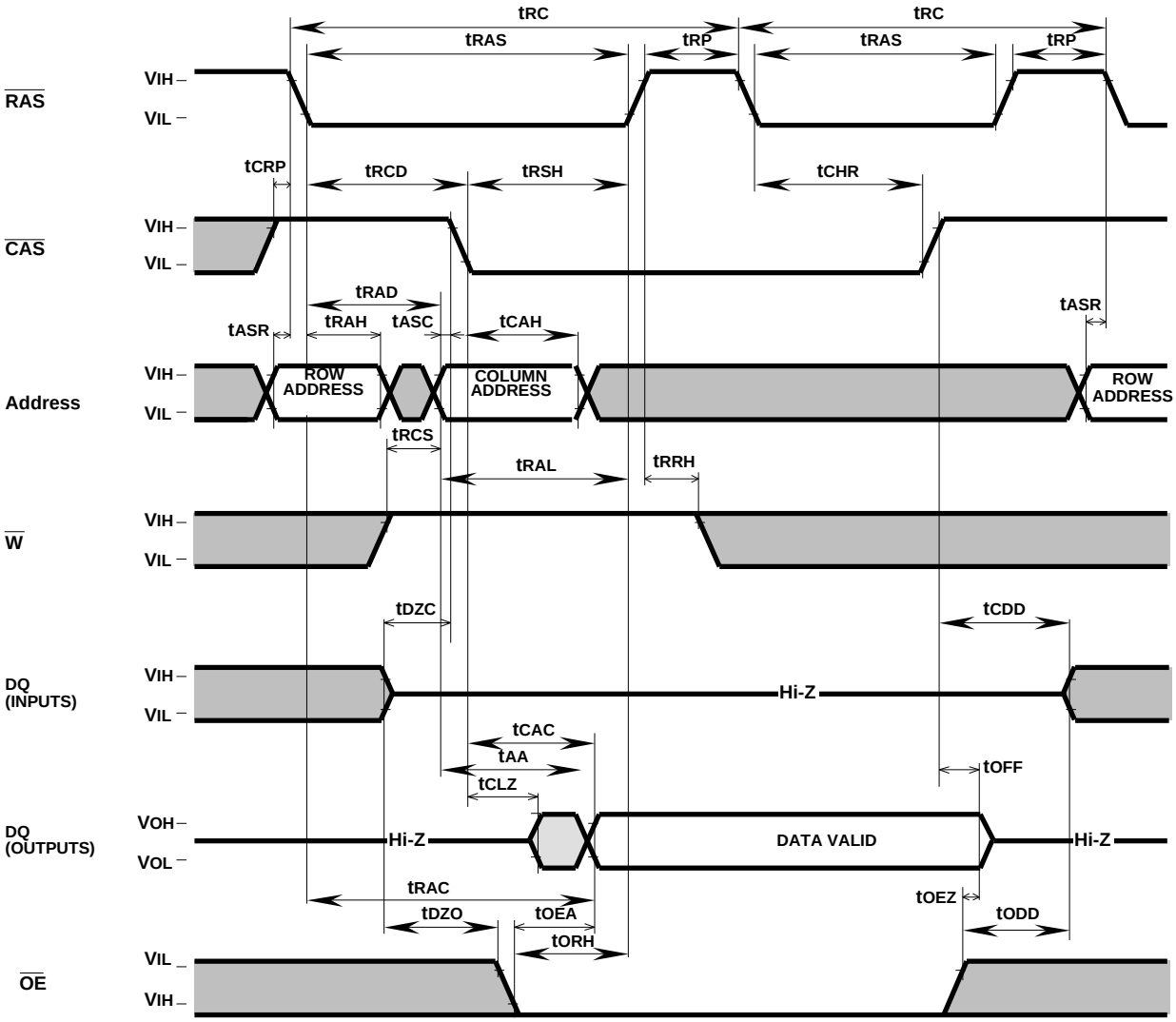
Read-Write, Read-Modify-Write Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

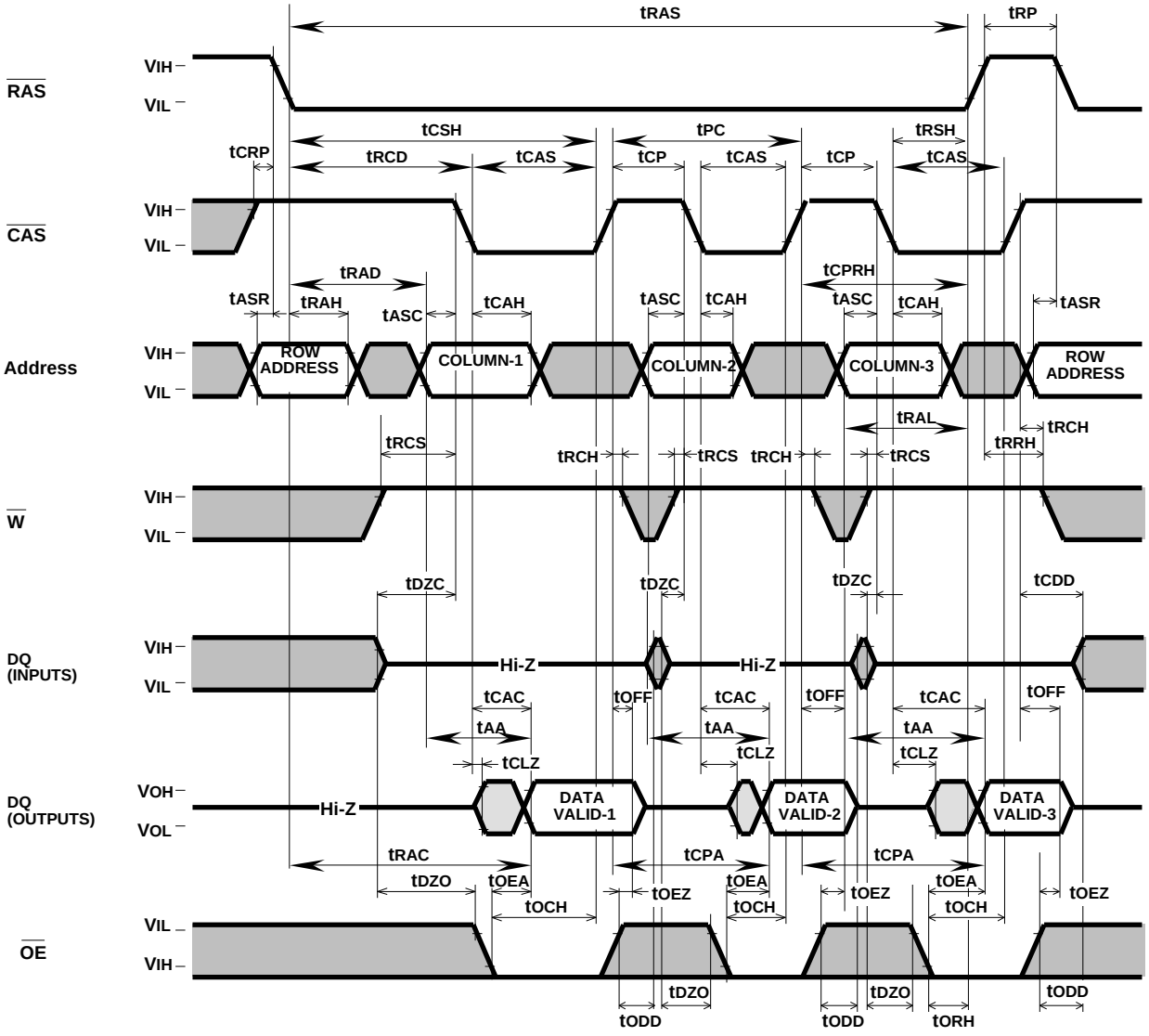


Hidden Refresh Cycle (Read) (Note 29)

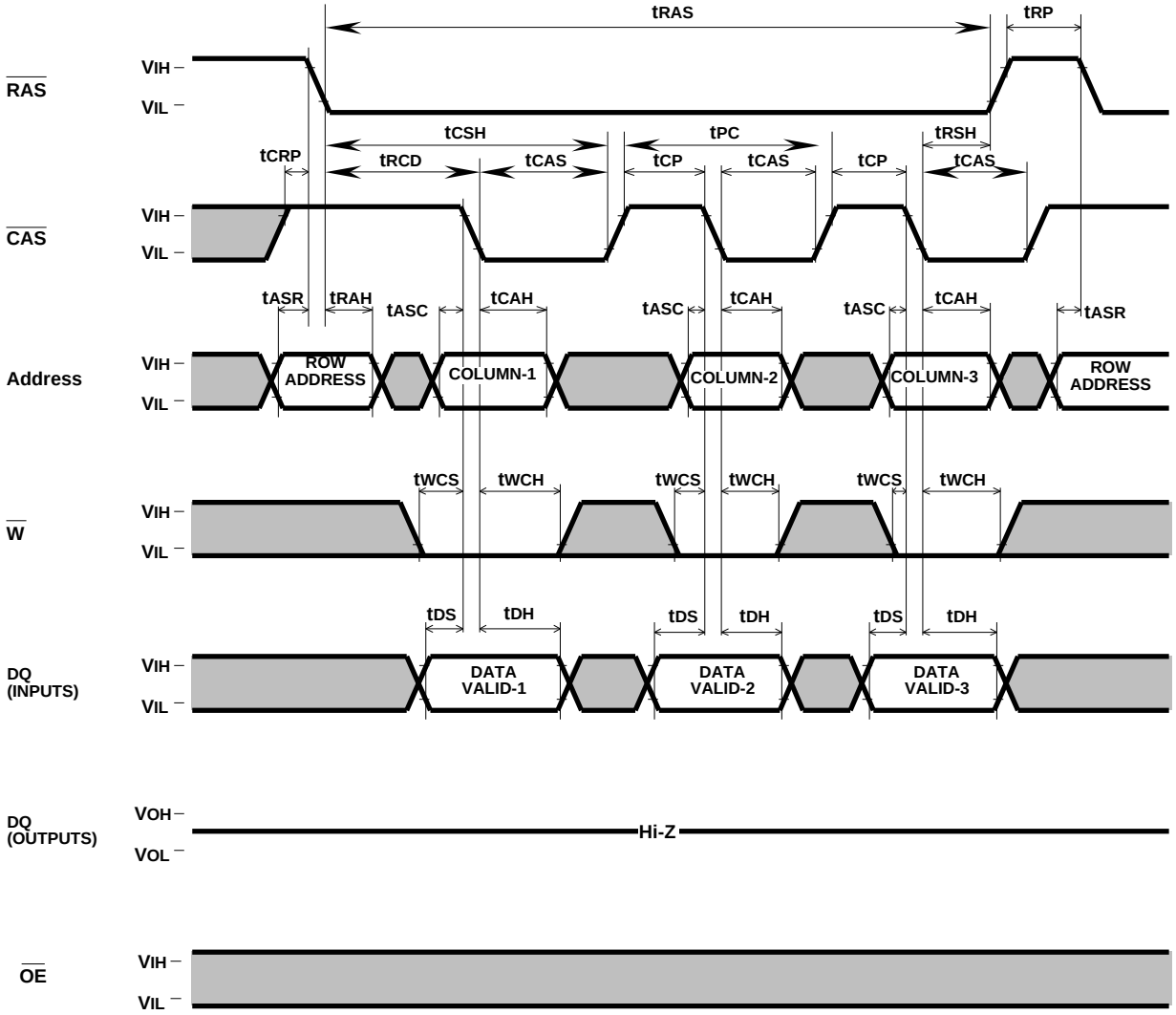


Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

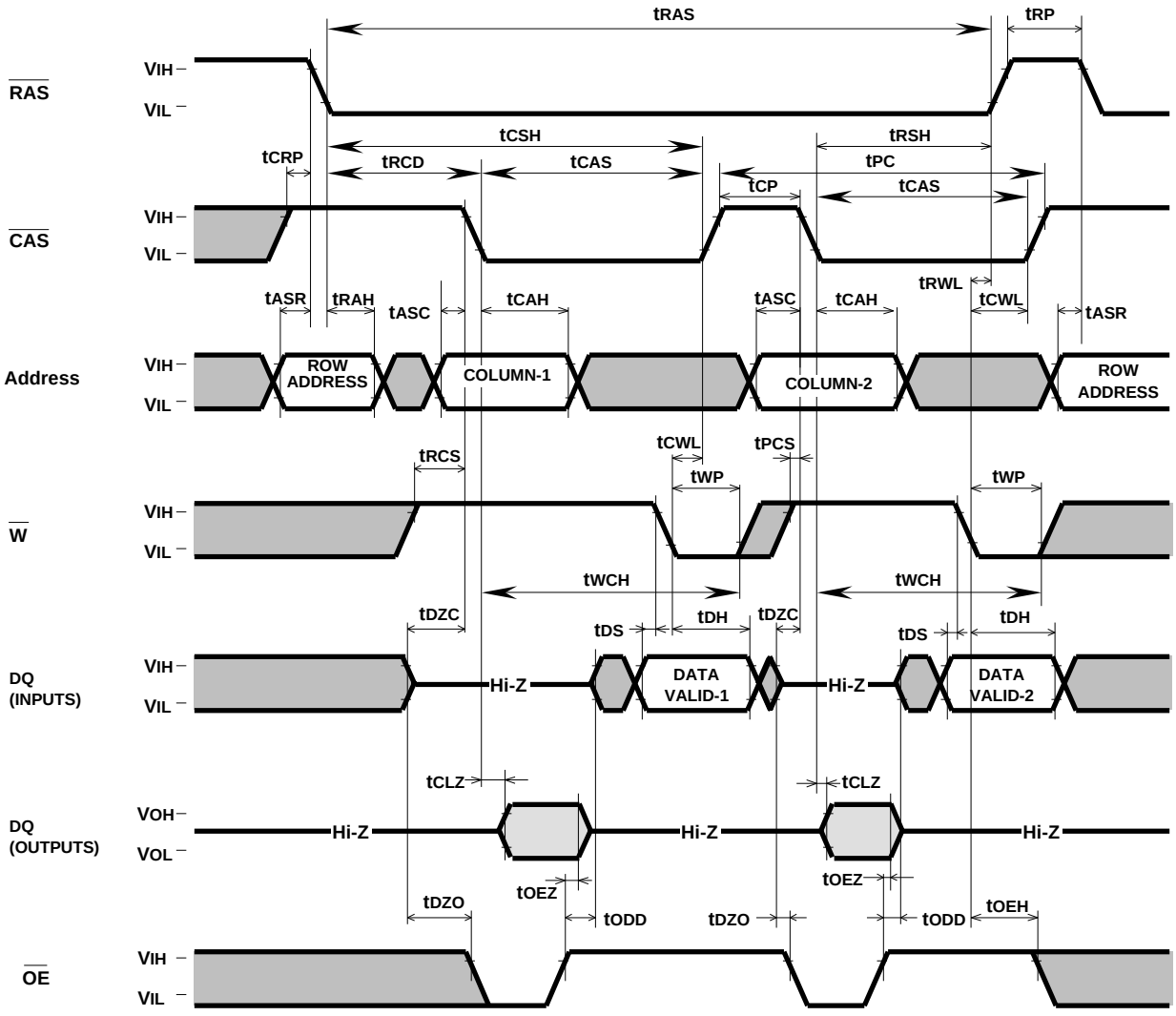
Fast Page Mode Read Cycle



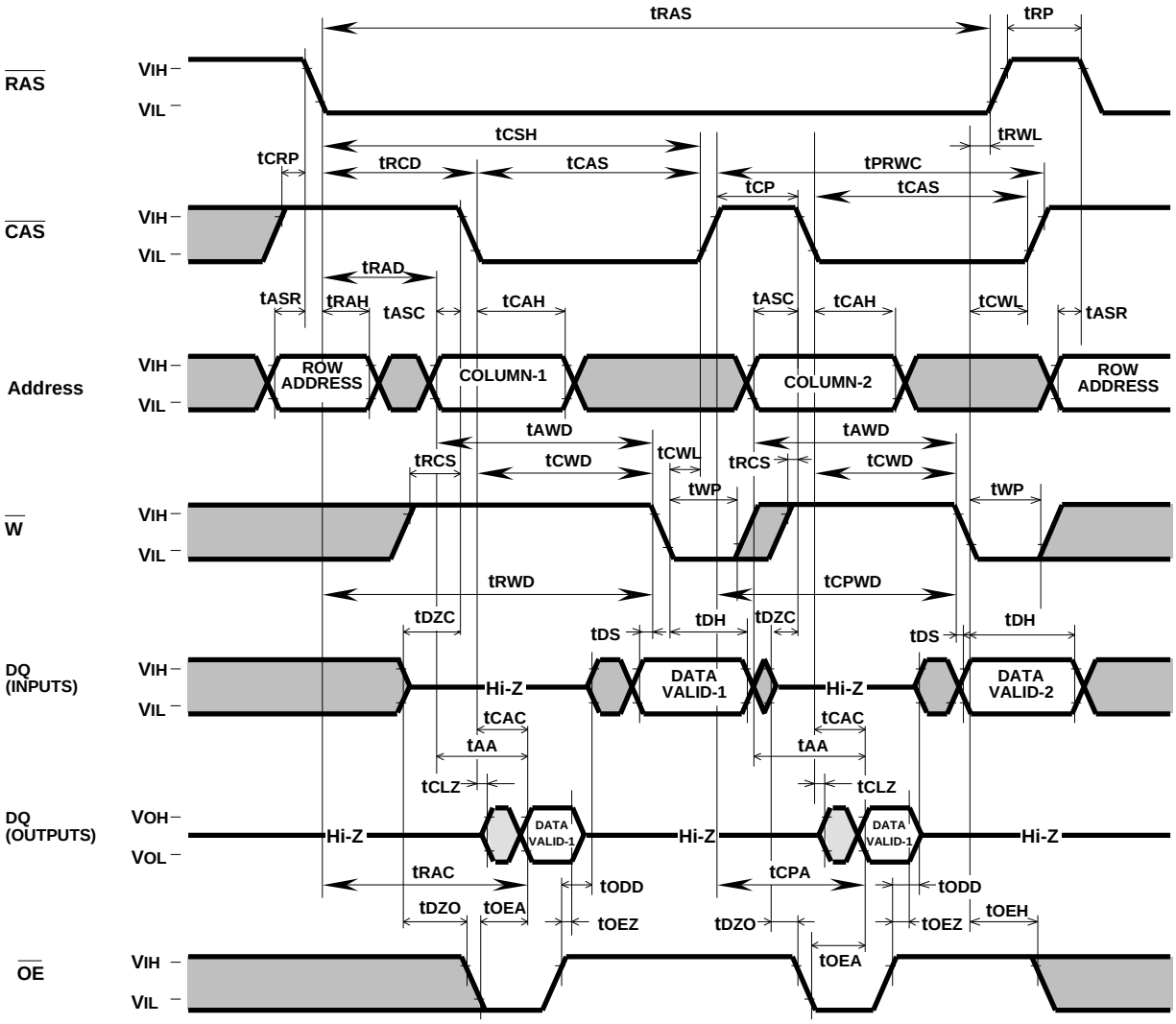
Fast Page Mode Write Cycle (Early Write)



Fast-Page Mode Write Cycle (Delayed Write)



Fast Page Mode Read-Write,Read-Modify-Write Cycle



MH4V724AWXJ -5, -6

Unit:mm

Package outline

