NIPPON PRECISION CIRCUITS INC.

SM5816AF

6-channel DSD-PCM Converter

Preliminary Product Bulletin

OVERVIEW

The SM5816AF is a 6-channel DSD data to 6-channel 8fs or 2fs PCM data converter IC. During conversion, decimation filtering is performed using a filter with selectable fixed coefficients (4 sets) or optional filter coefficients that are written to the built-in RAM. Also, DSD input/outputs and PCM outputs are available for use in master/slave mode operation, in a wide range of system configurations, making it easy to construct a multi-channel DSD/PCM reproduction system.

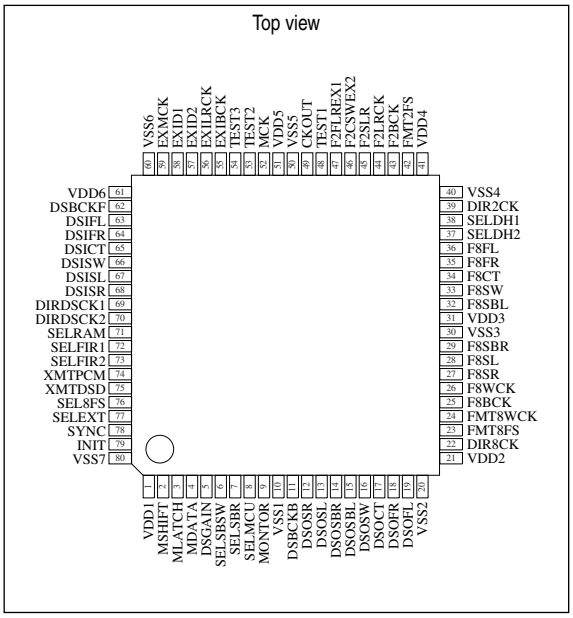
FEATURES

- 512fs master clock (22.5792MHz, fs = 44.1kHz)
- DSD inputs connected directly to outputs in through mode
- Clock master/slave switching for DSD input/outputs and PCM outputs
- 2-system external data inputs (3-wire), with 2fs output data BCK and LRCK pins switchable between external inputs and internal filter outputs
- Decimation filter characteristics
  - Fixed coefficients: 4 sets (8fs), 1 set (2fs)
  - Writable coefficients: 1 set
- Dither rounding function in 8fs/24-bit output mode only, with switchable ON/OFF and summing position
- Mute operation
- 8fs output format: [MSB-first left-justified 32-bit] or [MSB-first right-justified 24-bit]
- 2fs output format: [MSB-first left-justified 32-bit] or [IIS 32-bit]
- +6dB DSD gain switching function
- System clock output switchable between external system clock and internal system clock
- 3.3V ± 10% supply voltage
- 5V tolerant inputs for direct connection to 5V logic inputs
- −20 to 70°C operating temperature range
- 80-pin QFP package

APPLICATIONS

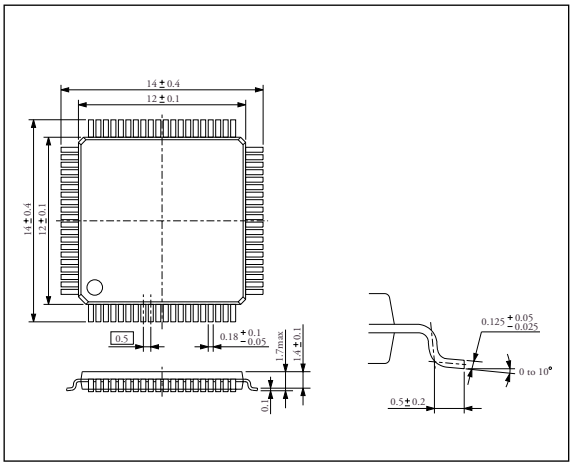
- Multi-channel SACD players
- SACD-compatible AV amplifiers

PINOUT



PACKAGE DIMENSIONS

(Unit: mm)

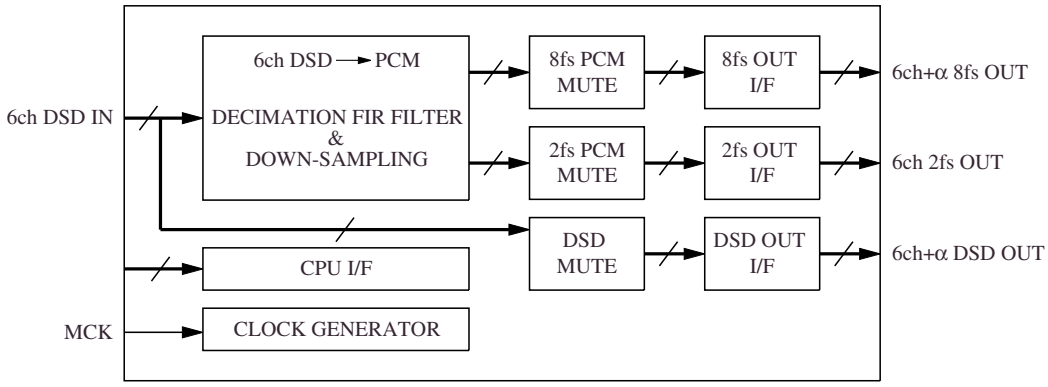


PIN DESCRIPTION

No.	Name	I/O	Description
1	VDD1	–	Supply pin 1
2	MSHIFT	I	Serial control shift clock
3	MLATCH	I	Serial control latch clock
4	MDATA	I	Serial control command data
5	DSGAIN	I	DSD signal gain set
6	SELSBSW	I	DSD-SW input to DSD 8fs-SW/(SBL, SBR) output select
7	SELSBR	I	DSD 8fs-(SBL, SBR) output select
8	SELMCU	I	Control method select
9	MONTOR	O	Parameter change monitor output
10	VSS1	–	Ground pin 1
11	DSBCKB	I/O	DSD through-mode data output: bit clock
12	DSOSR	O	DSD through-mode data output: surround right-channel
13	DSOSL	O	DSD through-mode data output: surround left-channel
14	DSOSBR	O	DSD through-mode data output: surround back right-channel
15	DSOSBL	O	DSD through-mode data output: surround back left-channel
16	DSOSW	O	DSD through-mode data output: subwoofer-channel
17	DSOCT	O	DSD through-mode data output: center-channel
18	DSOFR	O	DSD through-mode data output: front right-channel
19	DSOFL	O	DSD through-mode data output: front left-channel
20	VSS2	–	Ground pin 2
21	VDD2	–	Supply pin 2
22	DIR8CK	I	8fs output F8BCK, F8WCK I/O select
23	FMT8FS	I	8fs PCM format (MSB first)
24	FMT8WCK	I	8fs PCM WCK format
25	F8BCK	I/O	8fs PCM BCK (bit clock)
26	F8WCK	I/O	8fs PCM WCK (word clock)
27	F8SR	O	8fs PCM data output: surround right-channel
28	F8SL	O	8fs PCM data output: surround left-channel
29	F8SBR	O	8fs PCM data output: surround back right-channel
30	VSS3	–	Ground pin 3
31	VDD3	–	Supply pin 3
32	F8SBL	O	8fs PCM data output: surround back left-channel
33	F8SW	O	8fs PCM data output: subwoofer-channel
34	F8CT	O	8fs PCM data output: center-channel
35	F8FR	O	8fs PCM data output: front right-channel
36	F8FL	O	8fs PCM data output: front left-channel
37	SELDH2	I	Output dither rounding ON/OFF and summing position select
38	SELDH1	I	

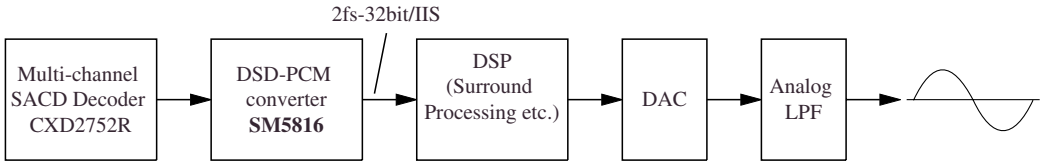
No.	Name	I/O	Description
39	DIR2CK	I	2fs output F2BCK, F2LRCK I/O select
40	VSS4	–	Ground pin 4
41	VDD4	–	Supply pin 4
42	FMT2FS	I	2fs PCM format
43	F2BCK	I/O	2fs or external data BCK
44	F2LRCK	I/O	2fs or external data LRCK
45	F2SLR	O	2fs PCM data output: surround left/right-channel
46	F2CSWEX2	O	2fs PCM data output: center/subwoofer-channel or external data 2 output
47	F2FLREX1	O	2fs PCM data output: front left/right-channel or external data 1 output
48	TEST1	I	Test pin 1
49	CKOUT	O	System clock output
50	VSS5	–	Ground pin 5
51	VDD5	–	Supply pin 5
52	MCK	I	Master clock input: 512fs
53	TEST2	I	Test pin 2
54	TEST3	I	Test pin 3
55	EXIBCK	I	External PCM data BCK input
56	EXILRCK	I	External PCM data LRCK input
57	EXID2	I	External PCM data input 2
58	EXID1	I	External PCM data input 1
59	EXMCK	I	External system clock input
60	VSS6	–	Ground pin 6
61	VDD6	–	Supply pin 6
62	DSBCKF	I/O	DSD data input bit clock
63	DSIFL	I	DSD data input: front left-channel
64	DSIFR	I	DSD data input: front right-channel
65	DSICT	I	DSD data input: center-channel
66	DSISW	I	DSD data input: subwoofer-channel
67	DSISL	I	DSD data input: surround left-channel
68	DSISR	I	DSD data input: surround right-channel
69	DIRDSCK1	I	DSBCKF I/O select
70	DIRDSCK2	I	DSBCKB I/O select
71	SELRAM	I	FIR coefficient ROM/RAM select
72	SELFIR1	I	FIR coefficient (ROM) select
73	SELFIR2	I	
74	XMTPCM	I	PCM output mute control input
75	XMTDSD	I	DSD output mute control input
76	SEL8FS	I	PCM output rate select
77	SELEXT	I	2fs output/external data output select
78	SYNC	I	Forced sync pint
79	INIT	I	Initialization control pin
80	VSS7	–	Ground pin 7

BLOCK DIAGRAM

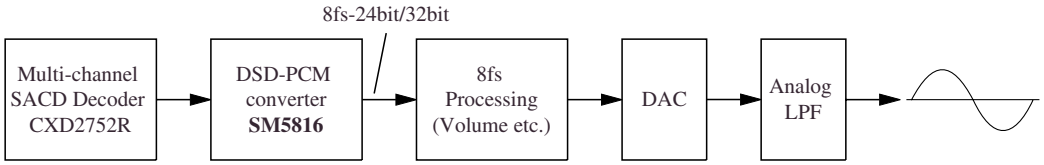


TYPICAL APPLICATION CIRCUITS

Surround Processor



DSD-to-PCM Conversion Reproduction



NPC DSD-Related Products

- SM5866AS: DSD/PCM-compatible multi-level D/A converter

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