AN-6024 — FMS6xxx Product Series

Understanding Analog Video Signal Clamps, Bias, DC-Restore, and AC or DC Coupling Methods

Description

The video filter, driver, and switch matrix products offered by Fairchild Semiconductor have various input coupling and clamping configurations. Choices include input AC or DC coupling, output AC or DC coupling, and various input clamping and bias configurations. An example would be the classic sync strip and pulse-DC-restore circuit or, alternatively, the continuous time clamp/bias circuit. Each type of coupling/clamping implementation has specific advantages and disadvantages for a specific application.

Most designs incorporate a single supply running from 5V down to 2.7V. Designers must be concerned about whether or not the video signal will be clipped at 2.7V V_{CC} and ensure that proper DC biasing is established at the input. Users of these video products should understand the specifics of the input and output analog video signal. If the input is a 140-IRE $1V_{pp}$ with 75% saturation CVBS signal, care must be taken to bias the signal within the input common mode range of the amplifier. The systems designer must not forget that the CVBS signal can have 100% saturation, which increases the input signal amplitude to $1.23V_{pp}$ and requires a system design that accommodates this signal without causing signal clipping.

Analog component video essentially maintains the same luma (Y) as CVBS, but keeps the color information separated. Pb is the blue color difference signal and Pr is the red color difference signal. Component analog video (Y, Pb, Pr) includes several different formats: standard definition (SD), enhanced definition (ED or PS), and high definition (HD). Special attention must be given to setting the optimal bias conditions of these inputs; whether they are AC or DC coupled from the driving device.

Figure 1 shows the various video formats with appropriate signal amplitude and bias levels.

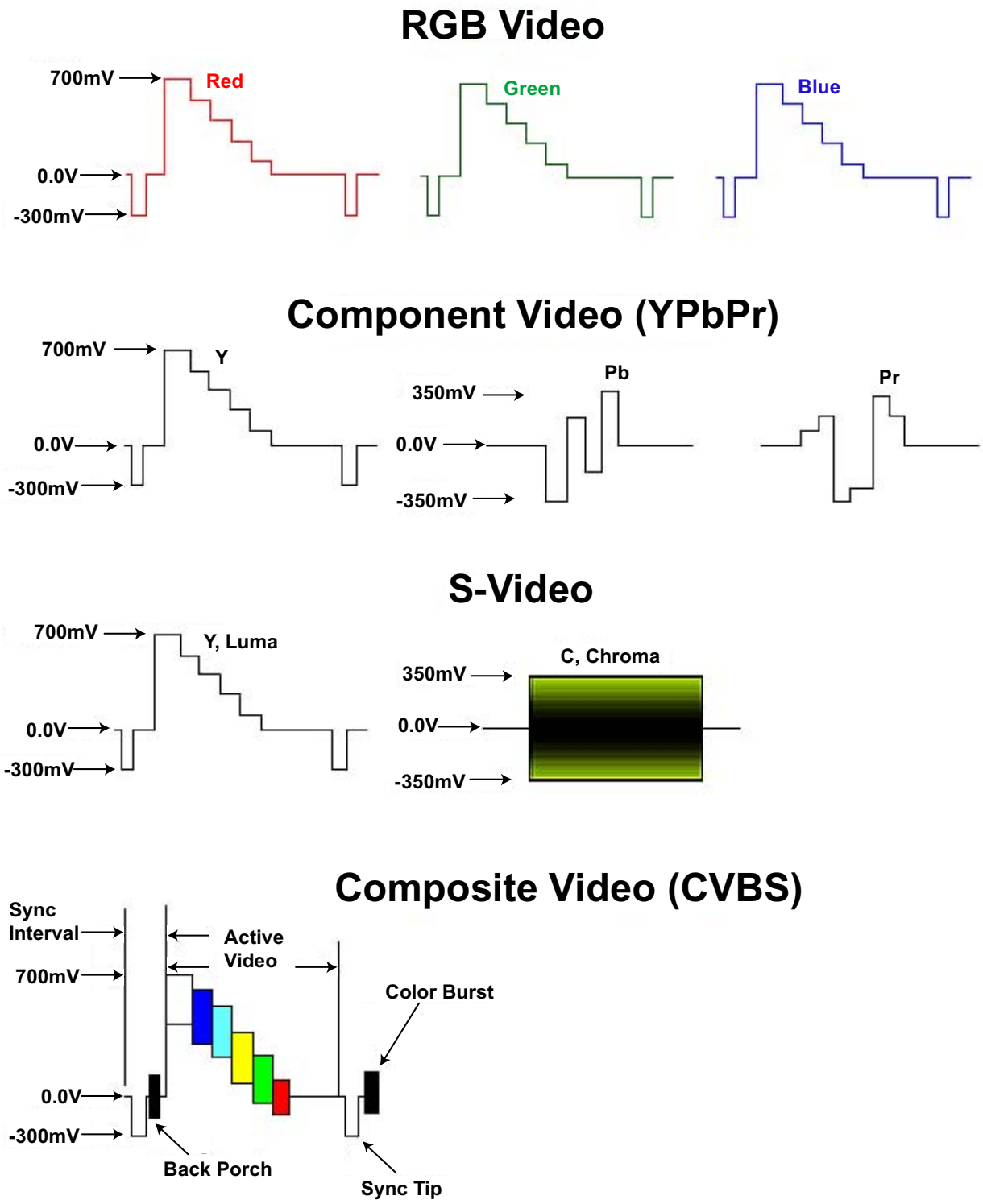

Figure 1. Video formats and their appropriate signal levels

AC coupled Video Input

It is very common in video and graphics systems to AC couple the analog video input signals into a given device. This allows the receiving device to set its own optimum DC bias level on the device side of the capacitor independently of the driving signal's DC bias level. For example, a receiving device of an analog-to-digital converter may set the clamping level or blanking level of the video signal equal to the internal ADC code zero voltage, regardless of the driving signal's absolute DC level. Another example would be in a purely analog system where the receiving device may set the analog signal's common mode level around $V_{CC}/2$ to optimize its headroom in processing the signal. The receiving device can also match the "clamped" level to a predetermined DC reference voltage, allowing for a consistent and stable DC output voltage. Also, by blocking DC, the receiving device protects itself from potentially damaging DC current flow.

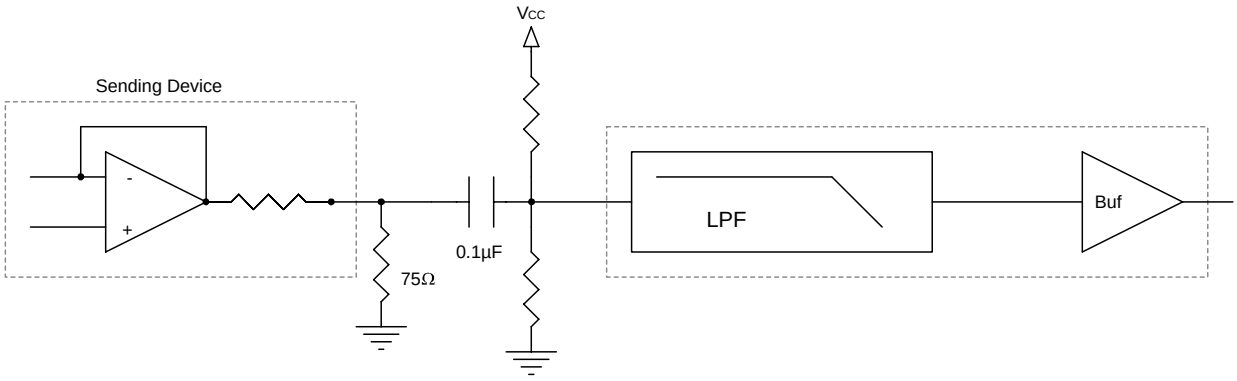

Figure 2. AC Coupled Input

Sync Strip and Pulsed DC Restore

A classic way to implement DC restore for any AC-coupled video input signal is by stripping off the embedded sync portion of the video signal and creating a digital pulse. This pulse can be used to trigger a charge pump circuit. Each time a sync signal is detected, the charge pump circuit is enabled, charging or discharging the input capacitor proportional to an on-chip error voltage in a closed-loop system. The system converges on the bias voltage over the first several lines and thereafter maintains or corrects for small errors on each successive line. Several Fairchild devices, such as the FMS6407, FMS6403, FMS6406, and FMS6408, use this type of clamping DC restore system.

The circuit is triggered from the channel that includes the embedded sync, usually a Y, G, or CV channel. The chrominance channels (Pb, Pr, or C) are also pumped to the appropriate DC levels during the triggered event. This implementation has several advantages and also some inherent disadvantages. One advantage of this type of clamping is that it can be triggered by the horizontal sync event. This allows updates and corrections in the bias level for every line, even during a non-active portion of the video. Since the DC reference level can be generated from an on-chip band gap voltage, the system can lock to a known DC level. This allows the DC output levels of the device to be accurately controlled and remain very flat over the temperature and voltage variations of the system, which is a great advantage when using the DC output coupling option. In addition, the FMS6403 and FMS6407 implement an architectural feature that allows an external digital separated sync input, which triggers the clamping event. As in RGB graphics, with a digital separated sync, the device can be put into external sync mode with the digital HSYNC used as the sync input to trigger the clamp event. This allows a proper DC restore of graphics formats that may not be compatible with the internal sync stripper and clamp generator.

The DC restore approach can also be implemented with back-porch clamping, as in the FMS6403 and FMS6407 programmed to HD mode, which keeps a constant blanking level, even with large variations in the absolute sync amplitude. The first disadvantage with this approach is the necessity for an input capacitor (although this capacitor can be relatively small in value, typically 0.1uF). Second, there is a die area cost associated with having this function in the device. Third, the internal sync stripper must be designed with a range of pre-determined formats to accurately process the sync signal and successfully generate the internal clamp pulse. Input formats outside this predetermined range may not DC restore properly unless an external sync pulse is applied. Fourth, due to the closed-loop DC restore system on chip and the fact that the input circuits are part of that loop, the input impedance of the driving source can affect the ability of the DC restore circuit to function properly. Most input video signals originate from relatively low drive impedance sources, with 75Ω being standard (doubly terminated 75Ω = 37.5Ω). Some

applications may require higher drive impedances, such as a 300Ω loaded DAC.
In this case, the drive impedance can have an adverse impact on the DC restore performance. The FMS6403, FMS6407, FMS6406, and FMS6408 can all tolerate impedances up to 150Ω. Higher drive impedances are not recommended
and may cause stability problems with the on-chip DC restore loop.

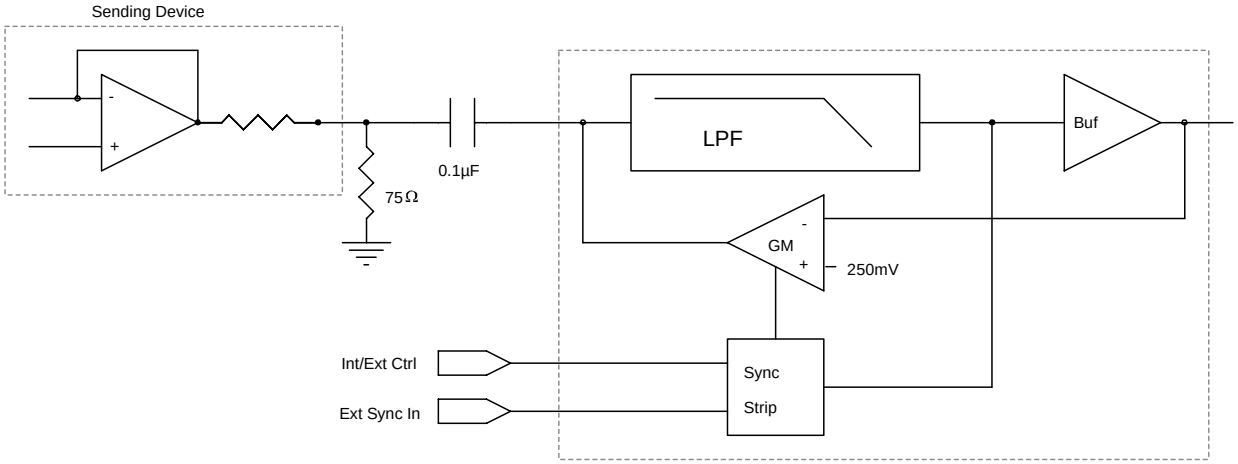

Figure 3. Sync Stripper with DC Restore

Clamp/Bias Input Circuitry

Several of Fairchild's recently released video/driver/switch products, such as the FMS6501, the FMS6143/45/46 family, and the FMS6363, offer clamp/bias circuitry on the input of the chip to set the DC bias for AC coupled applications. The circuit default is set to the clamp mode and, by using a 7.5MΩ–resistor to $V_{CC,}$ the device can be set to the bias mode. In clamp mode, the circuit clamps the lowest level (usually the bottom of the sync tip) of the incoming video signal to a predetermined on-chip reference voltage level. The clamp circuit is not triggered by a sync tip event, but rather by a continuous time circuit that clamps the lowest level of the input at a predetermined DC level and prevents the signal from falling below this level. In bias mode, the input is biased to the mid-scale reference voltage level through an on-chip high-impedance source.

The clamp referred to in this section operates differently than the pulsed DC restore circuit described previously. There is no internal sync stripper and pulsed charge pump circuit and there is no closed-loop system monitoring the output level. This has the advantage of reducing on-chip circuitry, which translates to less die area and a lower-cost device. It also has the advantage of being independent of predetermined timing and formats since no sync stripper and pulse generator are necessary. This allows compatibility with more unsupported video and/or graphics formats.

These devices can also be driven with a DC-coupled input that may be advantageous in certain applications, such as a known DC input drive. Limitations, when compared to the closed-loop pulsed DC restore approach, include the fact that output DC voltages may vary with system temperature and supply voltage variations. There is not a closed-loop system controlling the absolute output level and the device output level is dependent on the amplitude of the sync. If the sync amplitude varies with respect to the active video amplitude, the DC level of the output momentarily shifts as the clamp adjusts.

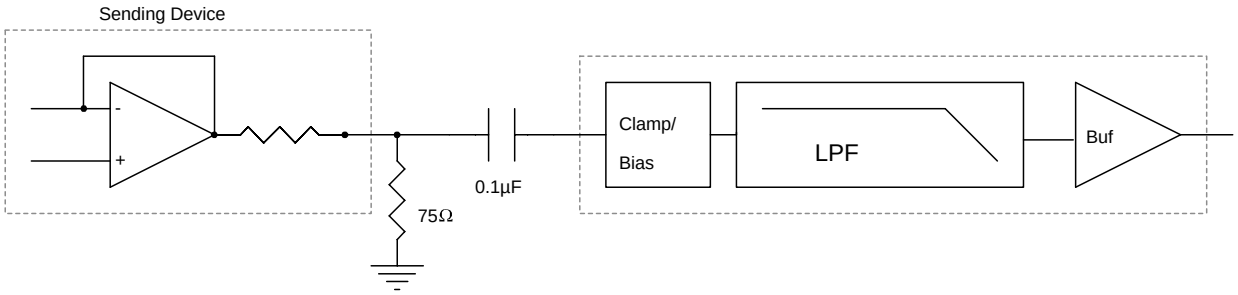

Figure 4. AC Coupled Input with Clamp/Bias

DC Coupled Input

Several Fairchild filter/driver devices; such as the FMS6417A, FMS6418B, and FMS6419, are designed specifically for DC-coupled input applications. The intent is for these devices to be driven by an input that is single ended, ground referenced, and DC coupled. An example would be a standard current mode output of a video/graphics DAC. These common DAC devices, such as the FMS3818, use the doubly terminated 75Ω load (37.5Ω) as the load for the current stirring DAC to develop the output voltage. Therefore, the DAC output in this type of system has a known DC level that is ground referenced.

Devices in this family are intended to work seamlessly with a video DAC output, with the following advantages: (1) no need for a input coupling cap; (2) no potential settling time for the clamp; (3) no tilt from the input cap discharge; (4) no potential glitch pulse; (5) no input impedance limitation as with the pulsed DC restore loop; and (6) no need for the on-chip sync stripper, charge pump circuitry, and servo loop. The limitations are that the input signal must be at a known DC level and biased with a voltage swing in the range of 0 to 1.3V DC. There is no feedback control on the absolute DC level of the output voltage and may vary with system temperature and supply voltage.

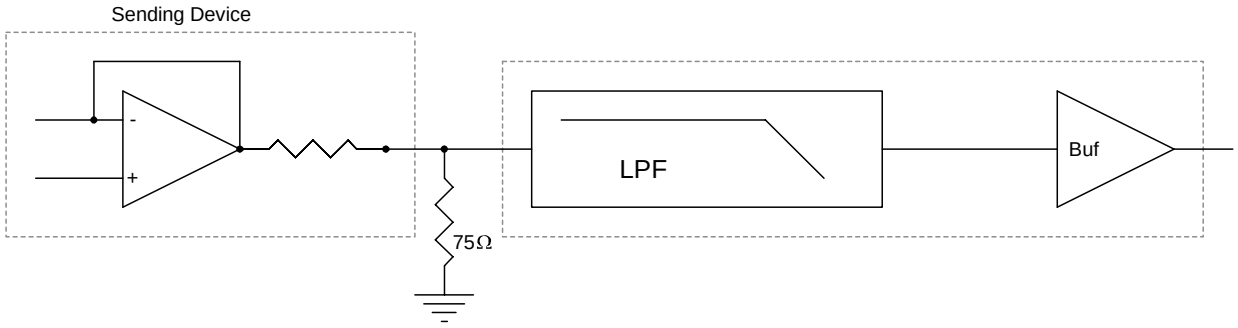

Figure 5. DC Coupled Input

AC Coupled Output

The most common approach used to feed a video signal to a visual media device is to AC couple the signal. This allows the receiving device to set the common mode level on its input, independent of the incoming video signal DC level. A 75Ω–series resistor should be placed as close to the device output as possible. This helps isolate the downstream parasitics from the output of the device and provides for optimal signal conditions. The AC coupling capacitor should be a 200µF, minimum. This is the smallest coupling capacitor that can be utilized and still achieve acceptable field tilt. Most applications have more stringent field tilt requirements and use a 470µF or 1000µF as coupling capacitors.

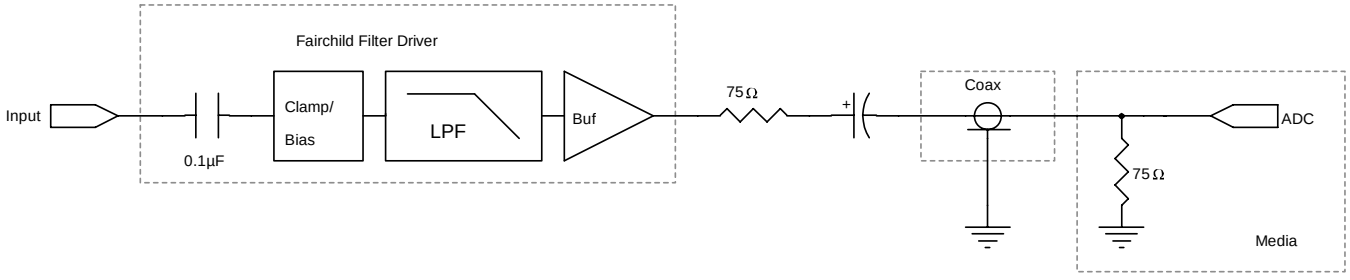

Figure 6. AC Coupled Output

DC Coupled Output

The most direct approach used to feed a video signal to a visual media device is to DC couple the signal. This eliminates the need for a coupling capacitor and allows for a tilt-free signal to be sent to the media device. One disadvantage to this approach is that the receiving device needs to know the incoming DC levels to process the video signal properly. This works for a system designed to handle known DC levels, but may cause a problem with systems which expect the common mode level at a different reference point.

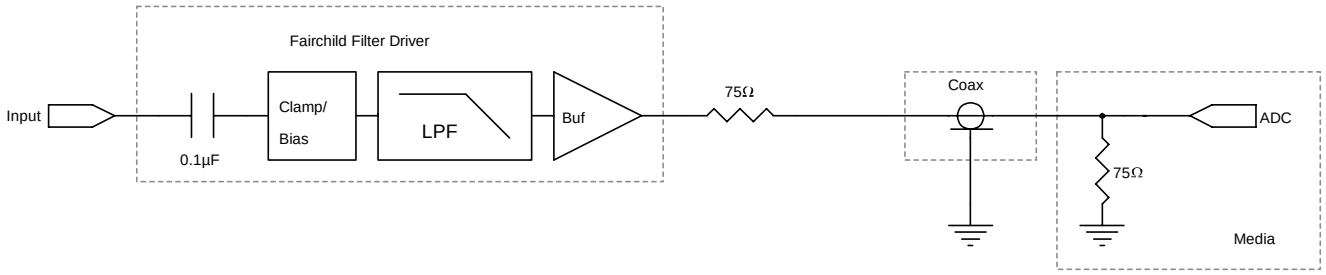

Figure 7. DC Coupled Output

Summary

The video filter/driver and switch matrix products offered by Fairchild Semiconductor have a variety of possible input/output signal coupling and clamping configurations. System designers have the choice of input/output AC or DC coupling. The choices for clamping options include the classic sync strip and pulsed DC restore circuit, the continuous time clamped/bias circuit, or DC coupling. Each type of implementation has specific advantages and limitations for a given application, which need to be taken into consideration by the system designer. For AC-coupled inputs, the FMS6403, FMS6407, FMS6406, and FMS6408 offer sync triggered pulse clamp circuits. These devices include an internal sync stripper and pulse generator. The FMS6403 and FMS6407 offer an external sync mode, where a digital-separated sync can be used to pulse the DC restore circuit on each sync pulse. These devices have a maximum input impedance specification of 150Ω. The FMS6501, FMS6143/45/46 family, and FMS6363 devices all use the continuous time clamp/bias circuit. These devices can be input AC or DC coupled and offer the most flexibility. There is no sync stripping and pulse generating circuitry in these devices. The FMS6417/18/19 are designed and intended for DC-coupled inputs. These devices are designed for a ground-referenced DC-coupled input, require an input signal with a voltage swing of 0 to 1.3V, and function best when directly coupled to the output of a video and/or a graphics DAC.