HB56SW3272ESK-5/6

256MB Buffered EDO DRAM DIMM
32-Mword × 72-bit, 4k Refresh, 2 Bank Module
(36 pcs of 16M × 4 components)

HITACHI

ADE-203-872B (Z)
Rev. 1.0
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Description

The HB56SW3272ESK belong to 8-byte DIMM (Dual in-line Memory Module) family , and have been developed an optimized main memory solution for 4 and 8-byte processor applications. The HB56SW3272ESK is 32 M × 72 Dynamic RAM Module, mounted 36 pieces of 64-Mbit DRAM (HM5165405) sealed in TCP package and 2 pieces of 16-bit BiCMOS line driver sealed in TSSOP package. The HB56SW3272ESK offer Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56SW3272ESK are 168-pin socket type package (dual lead out). Therefore, the HB56SW3272ESK make high density mounting possible without surface mount technology. The HB56SW3272ESK provide common data inputs and outputs. Decoupling capacitors are mounted beside each TCP on its module board.

Note: Do not push the cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

Features

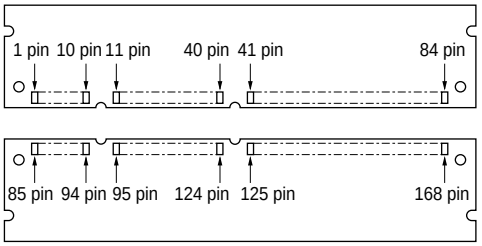
- 168-pin socket type package (Dual lead out)
  - Lead pitch : 1.27 mm
- Single 3.3 V supply (±0.3 V)
- High speed
  - Access time: t_{RAC} = 50 ns/60 ns (max)
  - Access time: t_{CAC} = 18 ns/20 ns (max)
- Low power dissipation
  - Active mode: 8.78 W/7.49 W (max)
  - Standby mode (TTL): 295.2 mW (max)
- JEDEC standard outline buffered 8-byte DIMM
- Buffered input except $\overline{RAS}$ and DQ

- 4-byte interleave enabled, dual address input (A0/B0)
- EDO page mode capability
- 4096 refresh cycles: 64 ms
- 2 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh

Ordering Information

Type No.	Access time	Package	Contact pad
HB56SW3272ESK-5 HB56SW3272ESK-6	50 ns 60 ns	168-pin dual lead out socket type	Gold

Pin Arrangement



Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	$\overline{OE}2$	86	DQ36	128	NC
3	DQ1	45	$\overline{RE}2$	87	DQ37	129	$\overline{RE}3$
4	DQ2	46	$\overline{CE}4$	88	DQ38	130	$\overline{CE}5$
5	DQ3	47	NC	89	DQ39	131	NC
6	V_{CC}	48	$\overline{WE}2$	90	V_{CC}	132	$\overline{PDE}$
7	DQ4	49	V_{CC}	91	DQ40	133	V_{CC}
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	V_{CC}	101	DQ49	143	V_{CC}
18	V_{CC}	60	DQ24	102	V_{CC}	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	NC	106	DQ53	148	NC
23	V_{SS}	65	DQ25	107	V_{SS}	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	V_{CC}	68	V_{SS}	110	V_{CC}	152	V_{SS}
27	$\overline{WE}0$	69	DQ28	111	NC	153	DQ64
28	$\overline{CE}0$	70	DQ29	112	$\overline{CE}1$	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ66
30	$\overline{RE}0$	72	DQ31	114	$\overline{RE}1$	156	DQ67
31	$\overline{OE}0$	73	V_{CC}	115	NC	157	V_{CC}
32	V_{SS}	74	DQ32	116	V_{SS}	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71

Pin Arrangement (cont)

Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	V_{CC}	82	PD7	124	V_{CC}	166	PD8
41	NC	83	ID0 (V_{SS})	125	NC	167	ID1 (V_{SS})
42	NC	84	V_{CC}	126	B0	168	V_{CC}

Pin Description

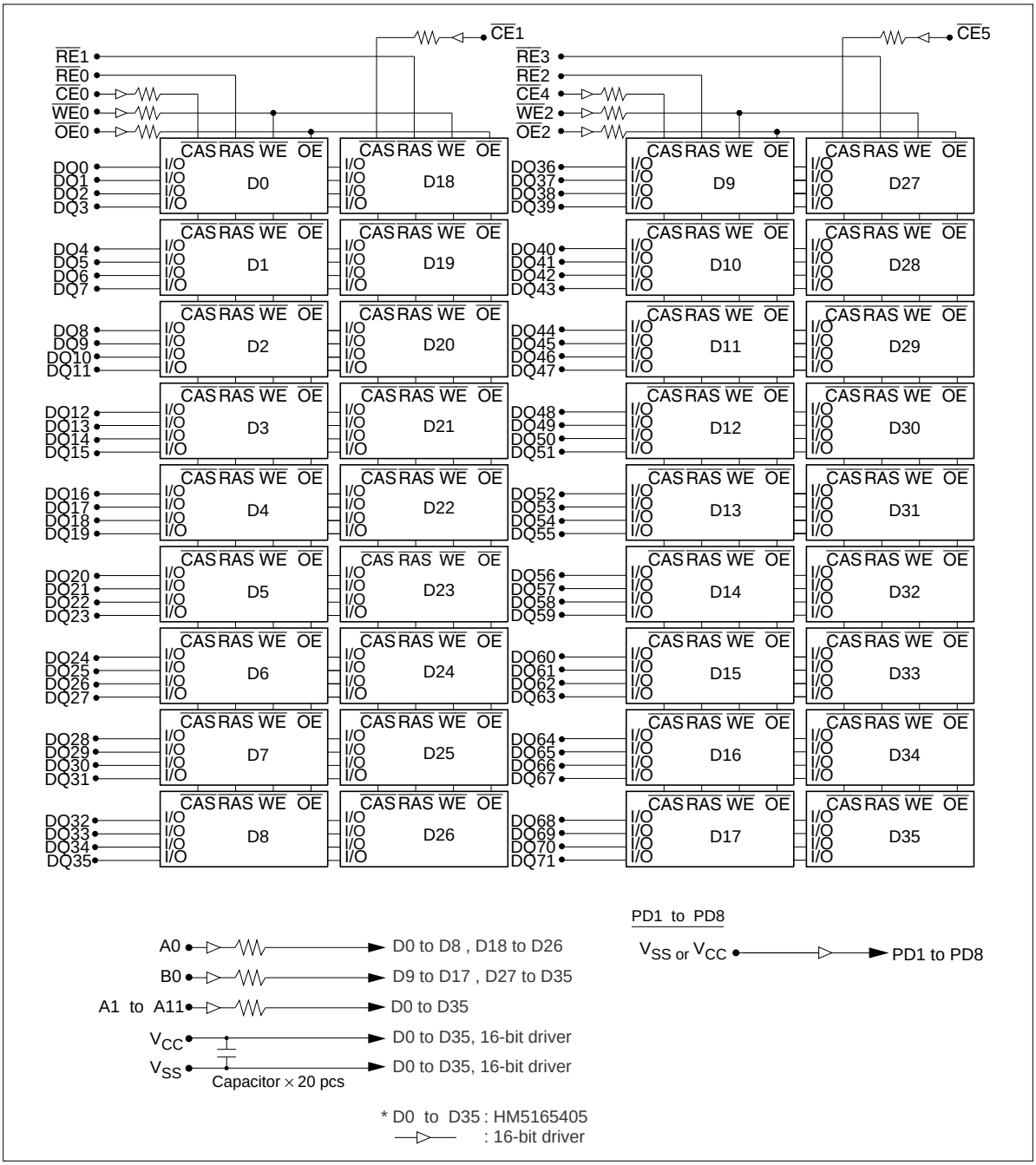
Pin name	Function	
A0 to A11, B0	Address input	
	Row address (D0 to D35)	A0 to A11, B0
	Column address (D0 to D35)	A0 to A11, B0
	Refresh address (D0 to D35)	A0 to A11, B0
DQ0 to DQ71	Data input/output	
$\overline{RE}$0 to $\overline{RE}$3	Row address strobe ($\overline{RAS}$)	
$\overline{CE}$0, $\overline{CE}$1, $\overline{CE}$4, $\overline{CE}$5	Column address strobe ($\overline{CAS}$)	
$\overline{WE}$0, $\overline{WE}$2	Read/Write enable	
$\overline{OE}$0, $\overline{OE}$2	Output enable	
PD1 to PD8	Presence detect	
ID0 , ID1	ID bit	
$\overline{PDE}$	Presence detect enable	
V_{CC}	Power supply	
V_{SS}	Ground	
NC	No connection	

Presence Detect Pin Assignment (Controlled by $\overline{\text{PDE}}$ pin)

		$\overline{\text{PDE}}$ = Low		**$\overline{\text{PDE}}$ = High**
Pin name	**Pin No.**	**50 ns**	**60ns**	**All**
PD1	79	1	1	High-Z
PD2	163	0	0	High-Z
PD3	80	0	0	High-Z
PD4	164	0	0	High-Z
PD5	81	1	1	High-Z
PD6	165	0	1	High-Z
PD7	82	0	1	High-Z
PD8	166	0	0	High-Z

Note: 1: High level (driver output). 0: Low level (driver output)

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	19	W
Storage temperature range	Tstg	–55 to +125	°C

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1, 2
	V_{SS}	0	0	0	V	2
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1
Ambient temperature range	Ta	0	—	70	°C	
Ambient illuminance	—	—	—	100	lx	

Notes: 1. All voltage referred to V_{SS}.
2. The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current*1, *2	I_{CC1}	—	2440	—	2080	mA	t_{RC} = min
Standby current	I_{CC2}	—	82	—	82	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z
		—	28	—	28	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*2	I_{CC3}	—	2440	—	2080	mA	t_{RC} = min
Standby current*1	I_{CC5}	—	190	—	190	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	2440	—	2080	mA	t_{RC} = min
EDO page mode current*1, *3	I_{CC7}	—	2080	—	1900	mA	$\overline{RAS}$ = V_{IL} , $\overline{CAS}$ cycle, t_{HPC} = t_{HPC} min
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ V_{CC} + 0.3 V
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ V_{CC} Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Measured with one sequential address change per EDO cycle, t_{HPC}.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ±0.3 V)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	20	pF	1
Input capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	—	20	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	78	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	27	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V) *[1], *[2], *[19]

Test Conditions

- Input rise and fall time: 2 ns
- Input levels: V_{IL} = 0 V, V_{IH} = 3 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)
- Ambient illuminance: Under 100 lx

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	84	—	104	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10000	10	10000	ns	
Row address setup time	t_{ASR}	5	—	5	—	ns	
Row address hold time	t_{RAH}	8	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	8	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	12	32	14	40	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	10	20	12	25	ns	4
$\overline{RAS}$ hold time	t_{RSH}	18	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	35	—	40	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	18	—	20	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	ns	7

Read Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	50	—	60	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	18	—	20	ns	9, 10, 17
Access time from address	t_{AA}	—	30	—	35	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	18	—	20	ns	9
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time from $\overline{RAS}$	t_{RCHR}	50	—	60	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	15	—	18	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	2	—	2	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	21
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	18	—	20	ns	13, 21
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	18	—	20	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	18	—	20	—	ns	5
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	3	—	ns	21
Output buffer turn-off to $\overline{RAS}$	t_{OFR}	—	13	—	15	ns	13, 21
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	18	—	20	ns	13
$\overline{WE}$ to Din delay time	t_{WED}	18	—	20	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	13	—	15	—	ns	

Write Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	ns	14
Write command hold time	t_{WCH}	8	—	10	—	ns	
Write command pulse width	t_{WP}	8	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8	—	10	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	15
Data-in hold time	t_{DH}	13	—	15	—	ns	15

Read-Modify-Write Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	116	—	140	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	72	—	84	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	30	—	34	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	42	—	49	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	13	—	15	—	ns	

Refresh Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	8	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	5	—	5	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	ns	

EDO Page Mode Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode cycle time	t_{HPC}	20	—	25	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	33	—	40	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	33	—	40	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	ns	9, 22
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	8	—	10	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	28	—	35	—	ns	
Write pulse width during $\overline{CAS}$ precharge	t_{WPE}	8	—	10	—	ns	
$\overline{OE}$ precharge time	t_{OEP}	8	—	10	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode read- modify-write cycle time	t_{HPRWC}	57	—	68	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	45	—	54	—	ns	14

Refresh

Parameter	**Symbol**	**Max**	**Unit**	**Notes**
Refresh period	t_{REF}	64	ms	4096 cycles

Notes:
1. AC measurements assume t_T = 2 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh).
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, than the access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max), t_{OEZ} (max), t_{WEZ} (max) and t_{OFR} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. t_{DS} and t_{DH} are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.

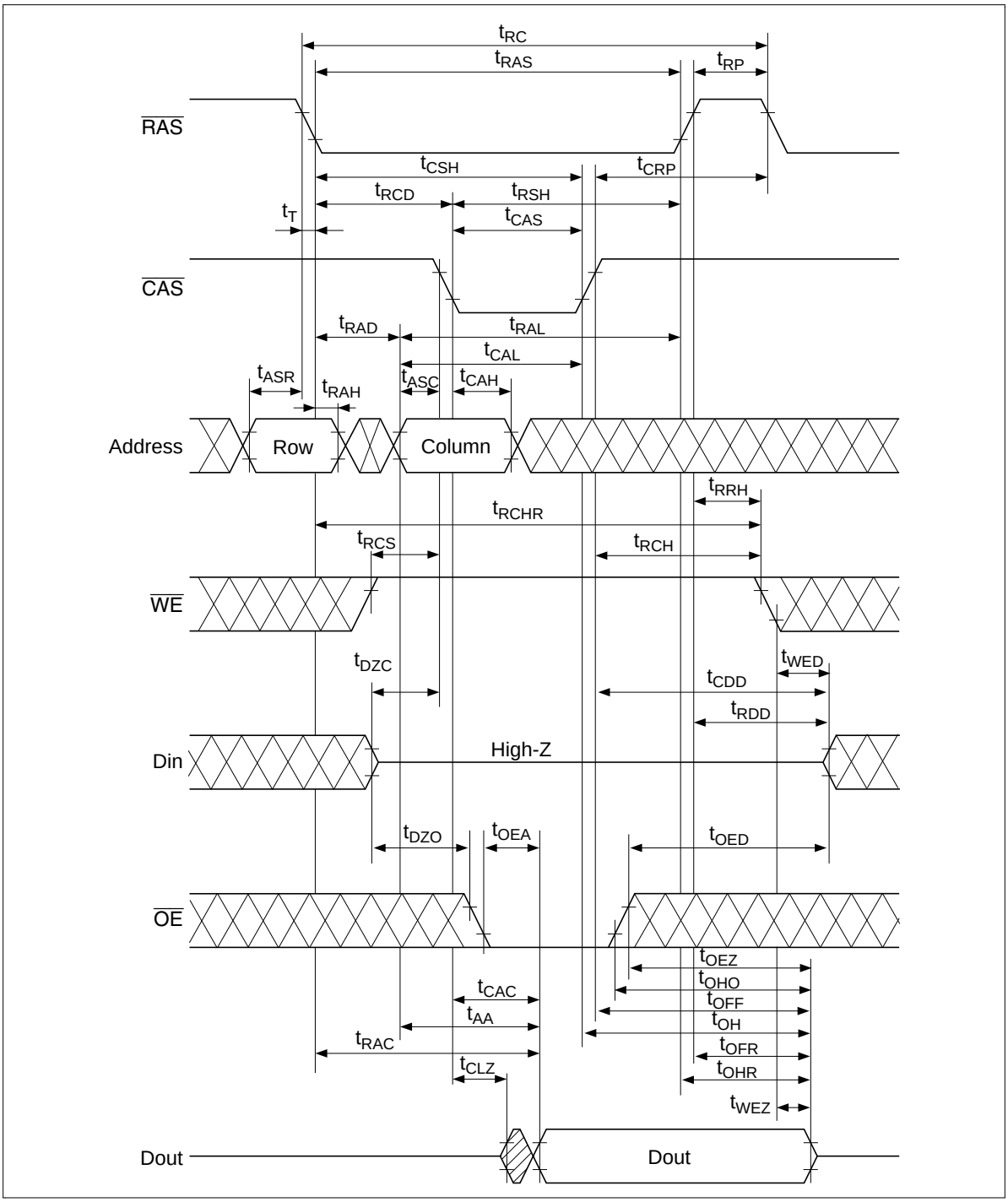
19. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.
20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2\ t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH} and between t_{OFR} and t_{OFF}.
22. t_{DOH} defines the time at which the output level go cross. V_{OL} = 0.8 V, V_{OH} = 2.0 V of output timing reference level.
23. XXX: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

    ///////: Invalid Dout

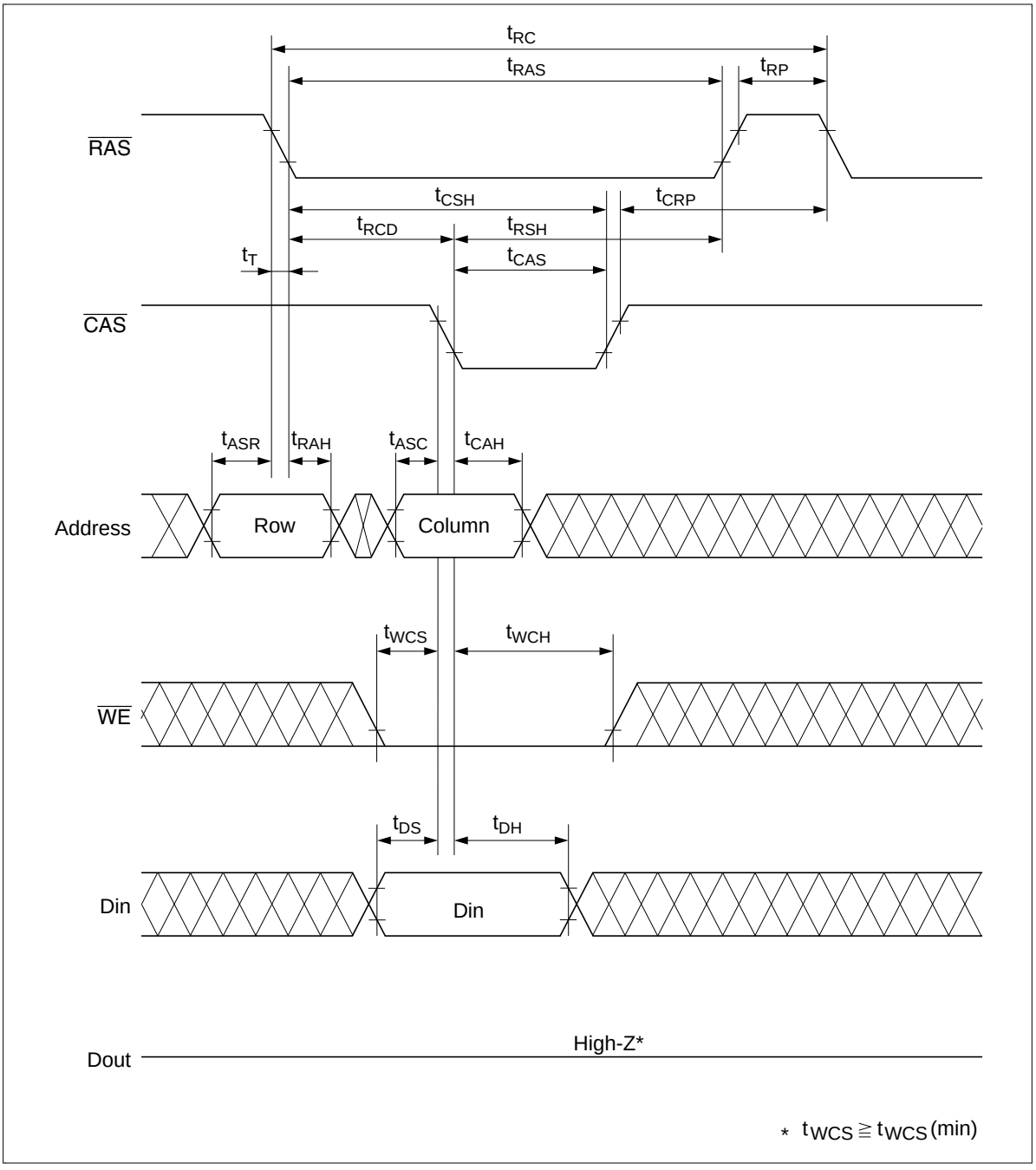
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms*[23]

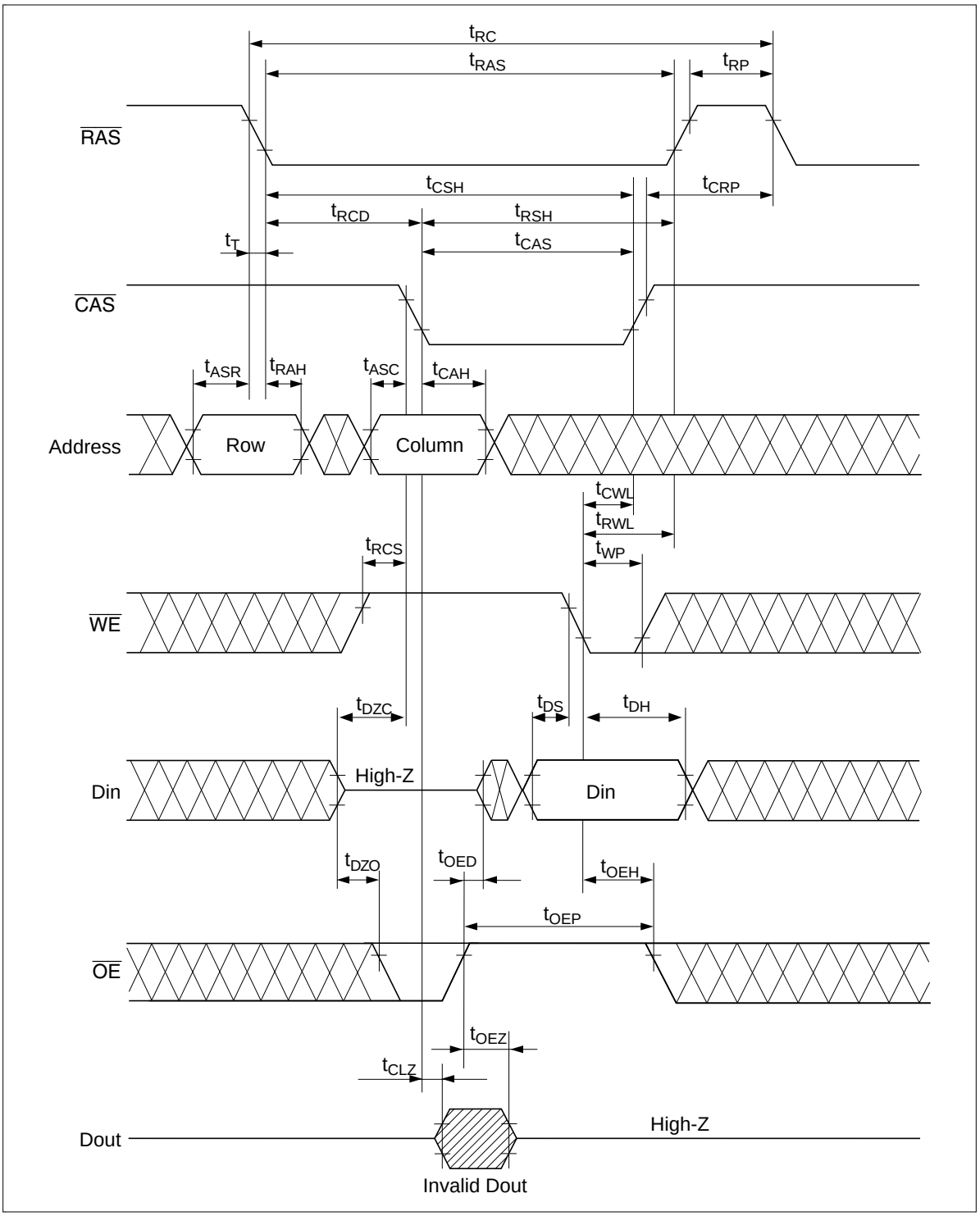
Read Cycle



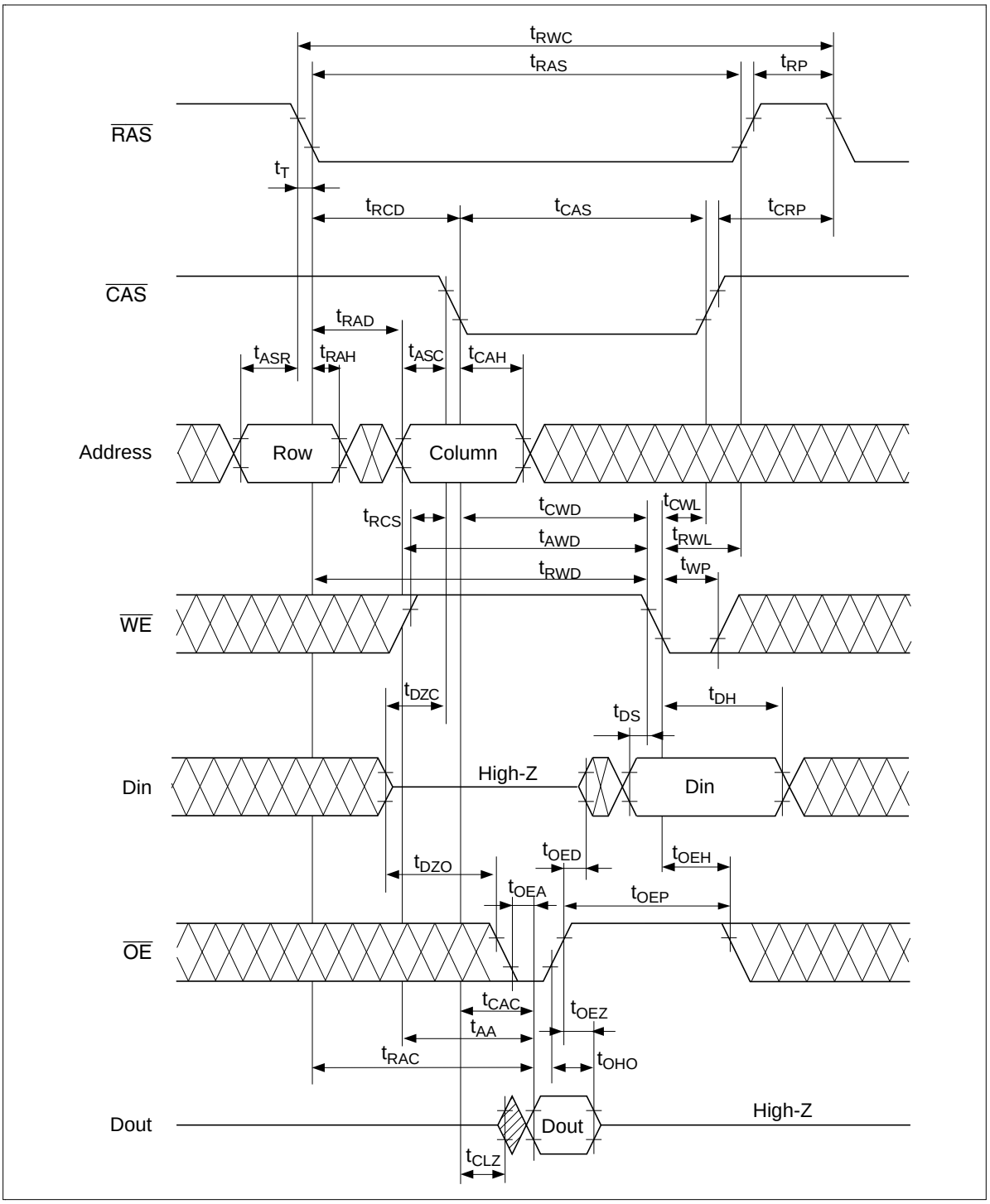
Early Write Cycle



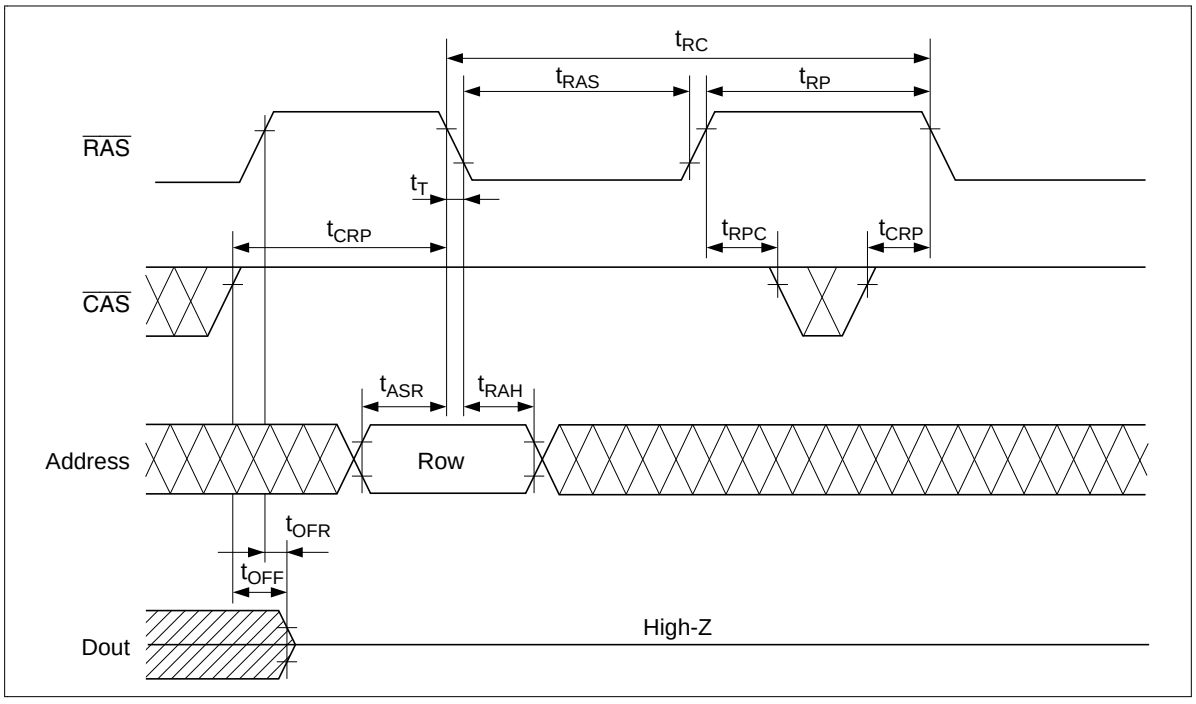
Delayed Write Cycle*[18]



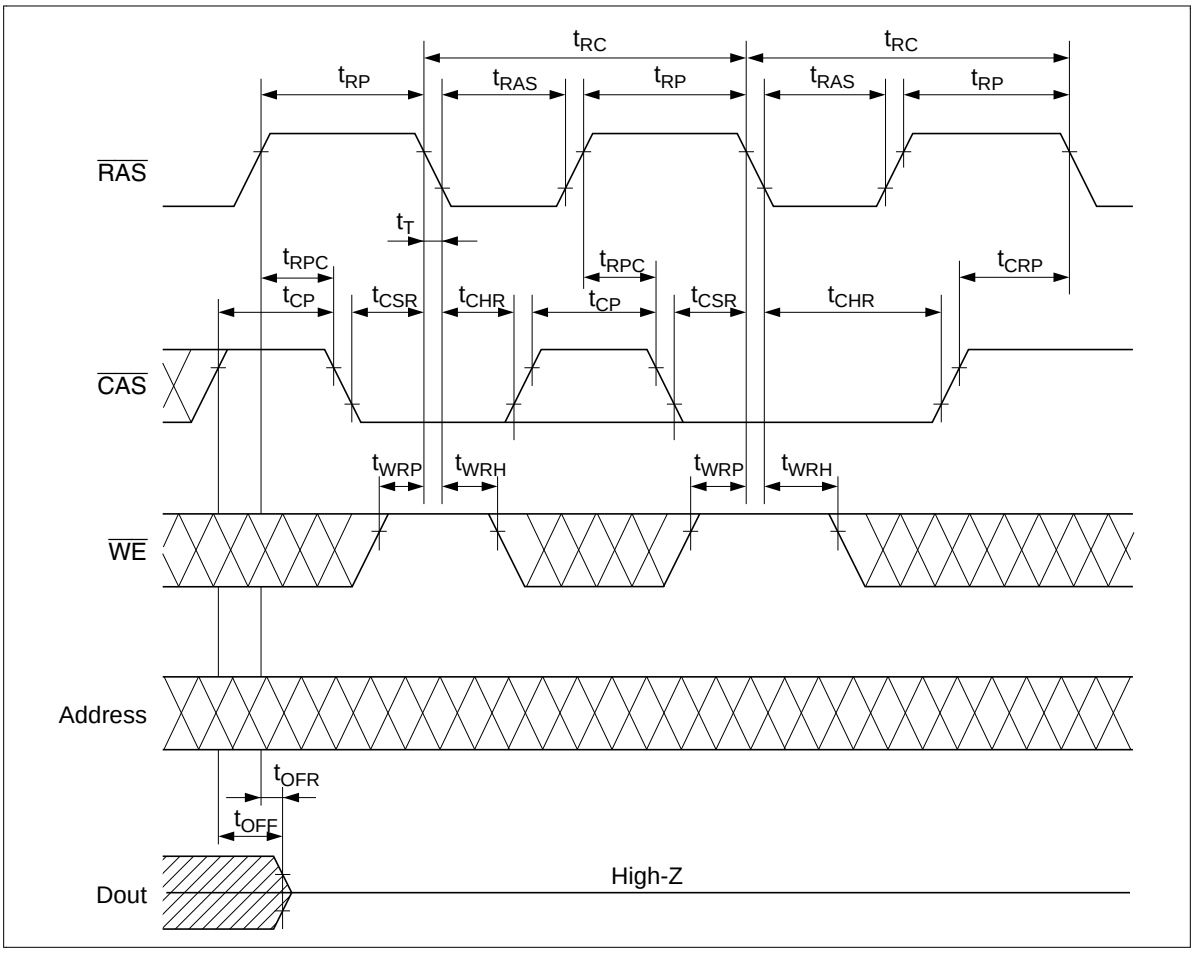
Read-Modify-Write Cycle*[18]



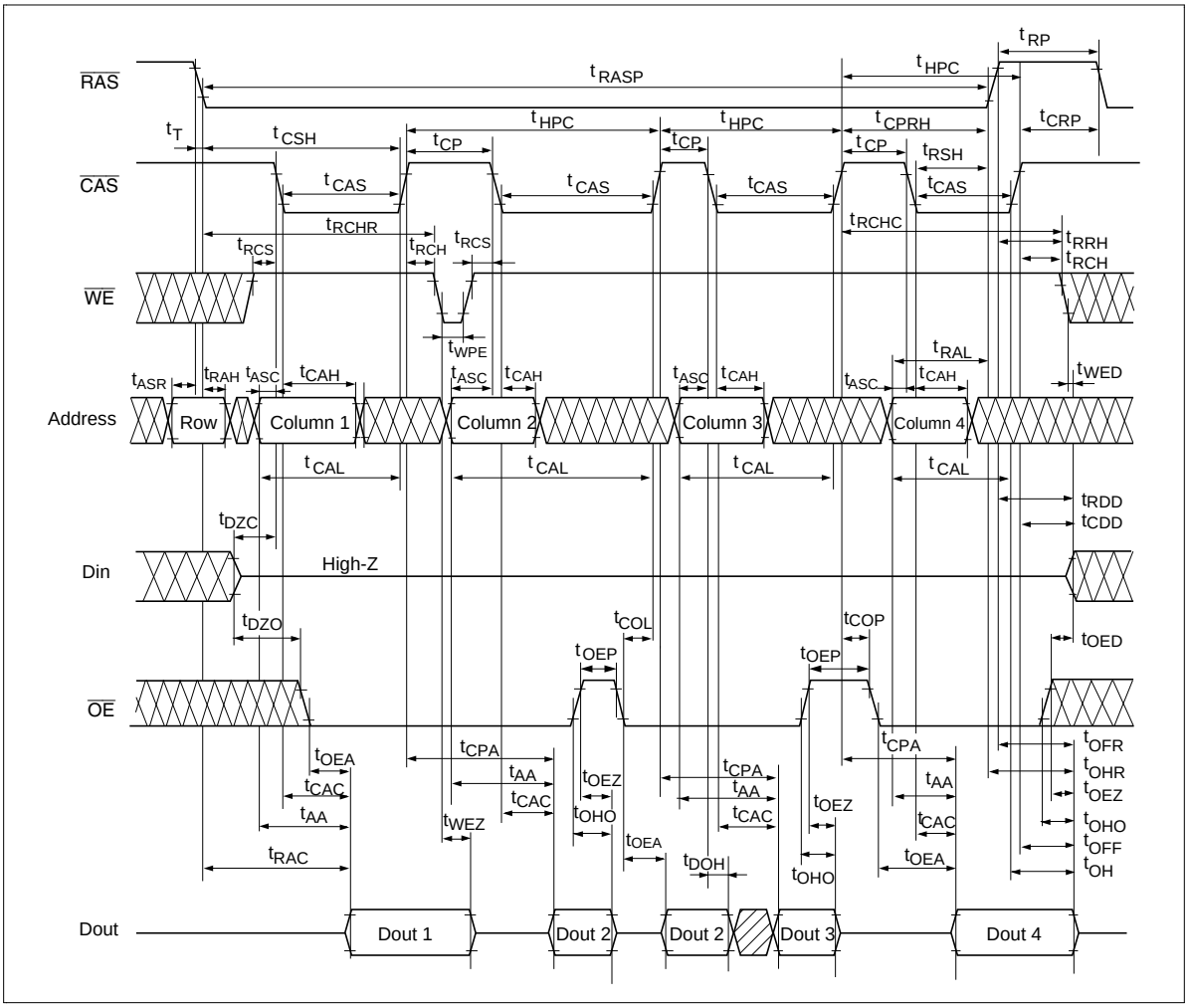
$\overline{\text{RAS}}$-Only Refresh Cycle



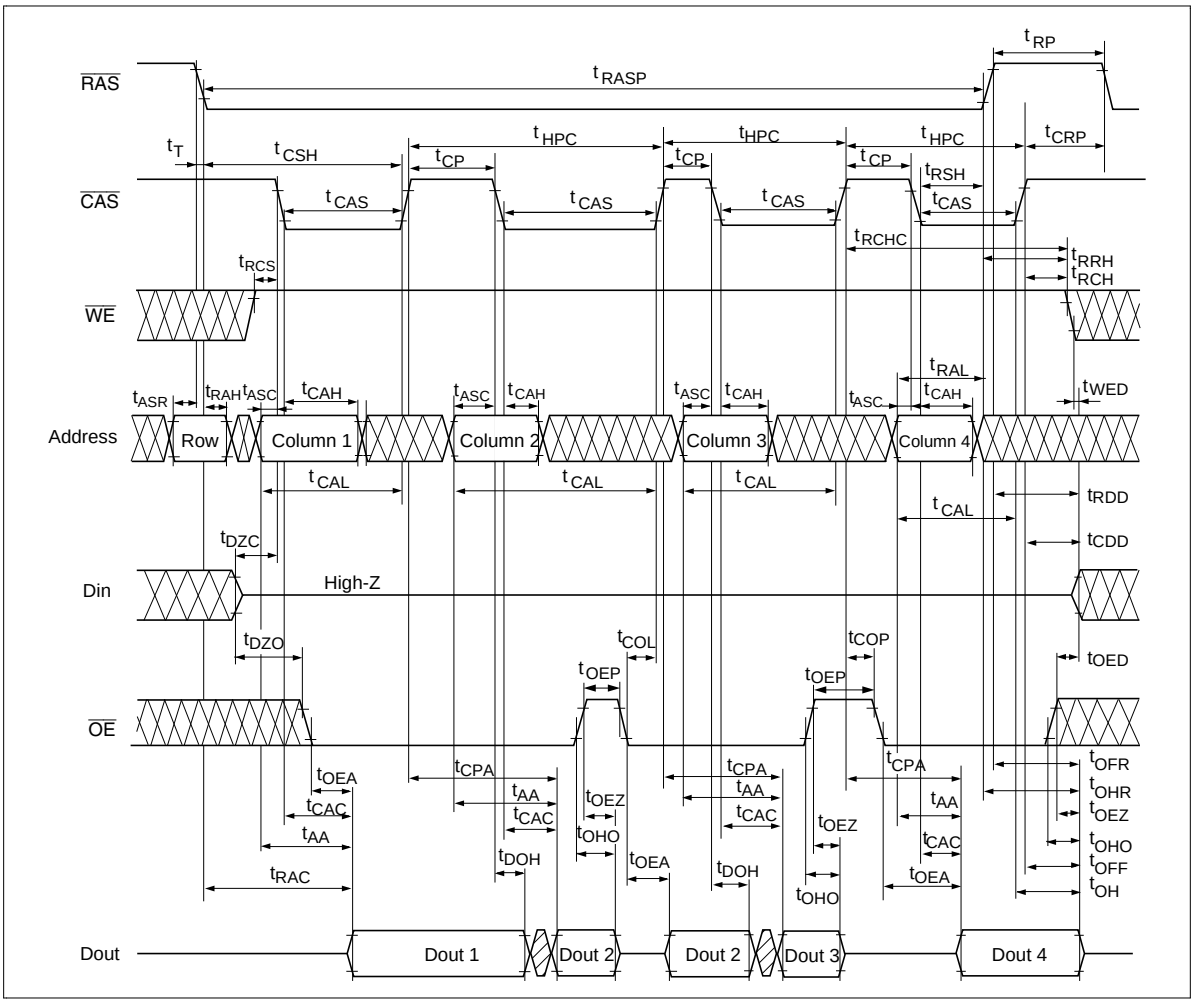
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



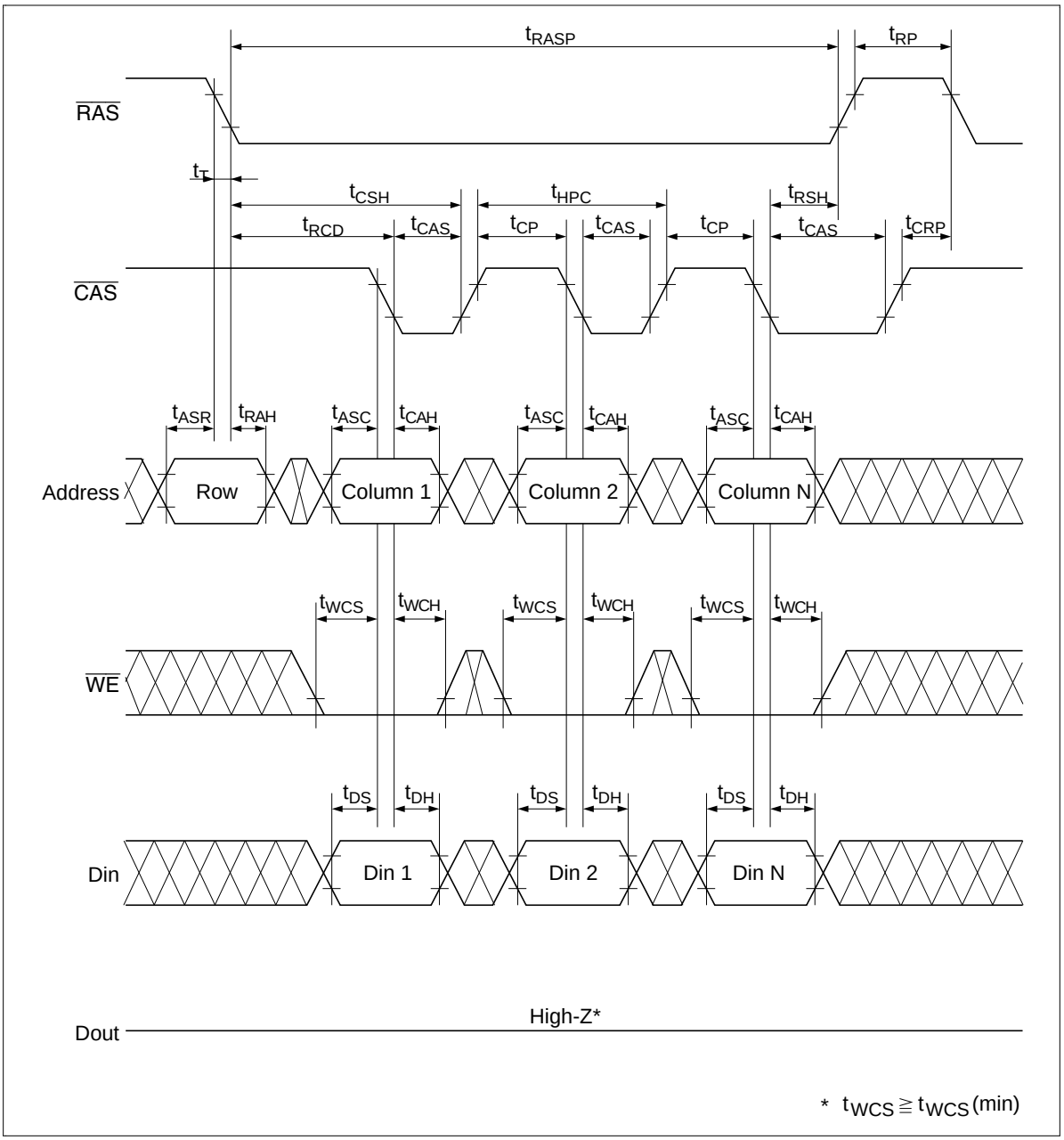
EDO Page Mode Read Cycle (1)



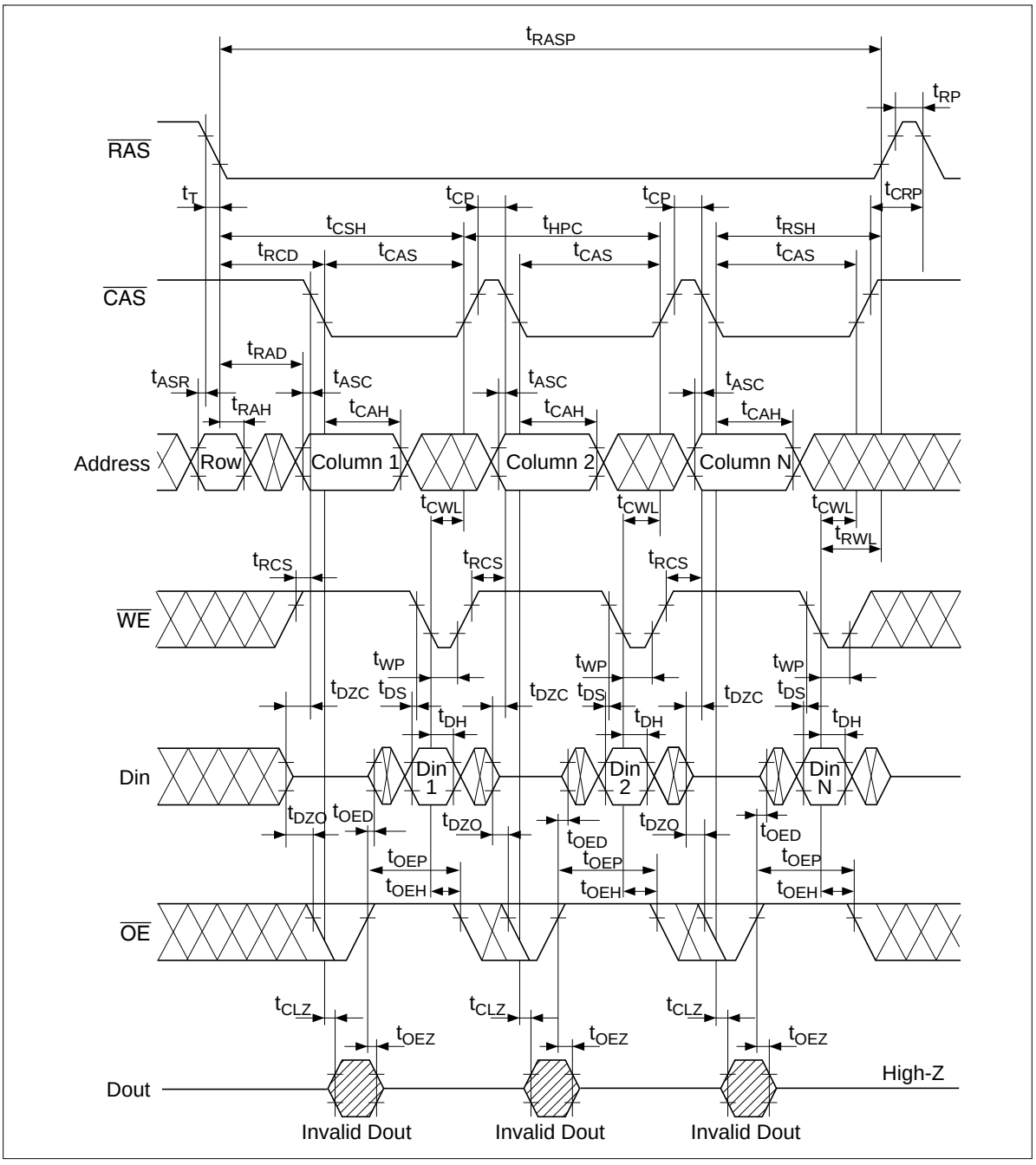
EDO Page Mode Read Cycle (2)



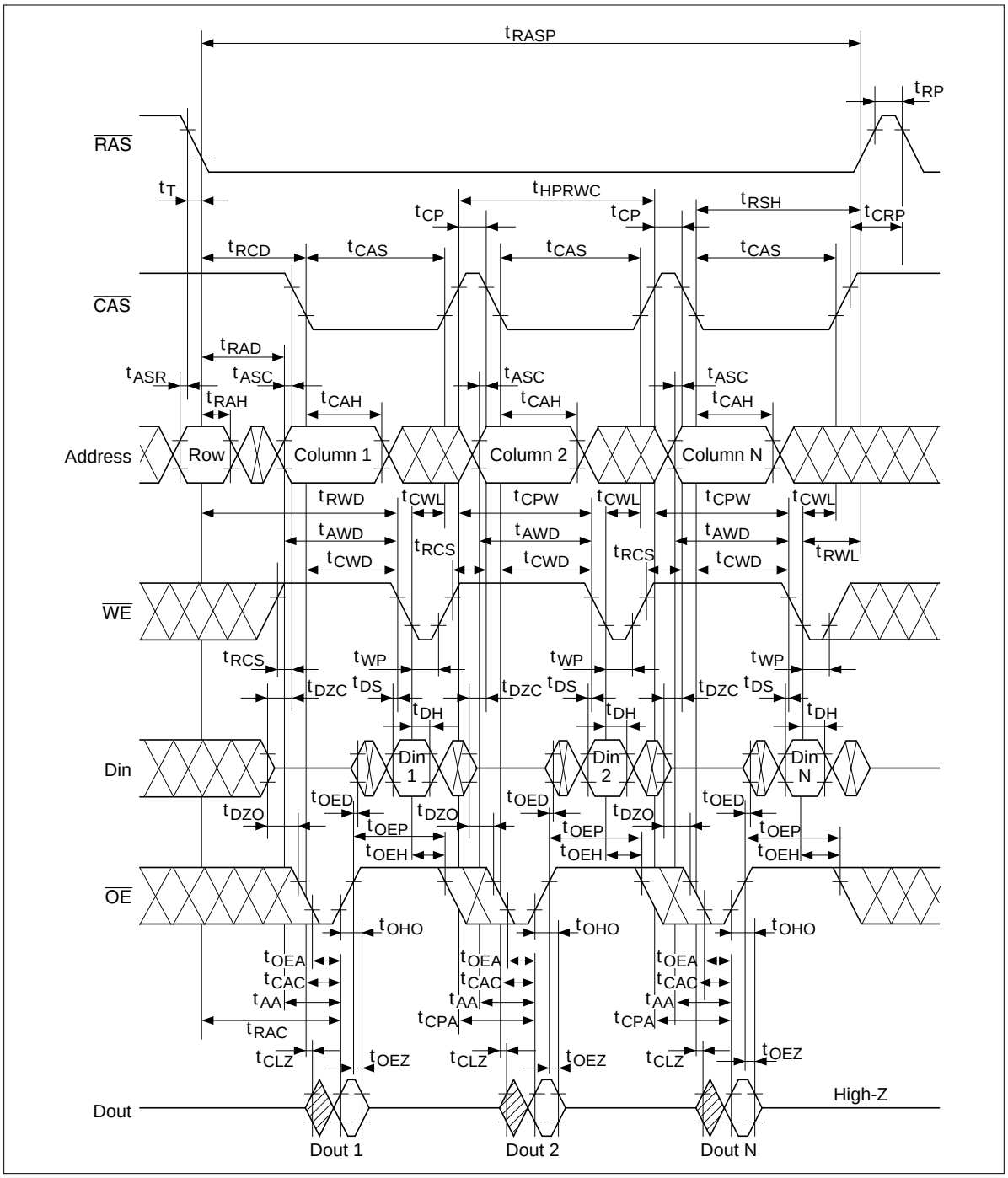
EDO Page Mode Early Write Cycle



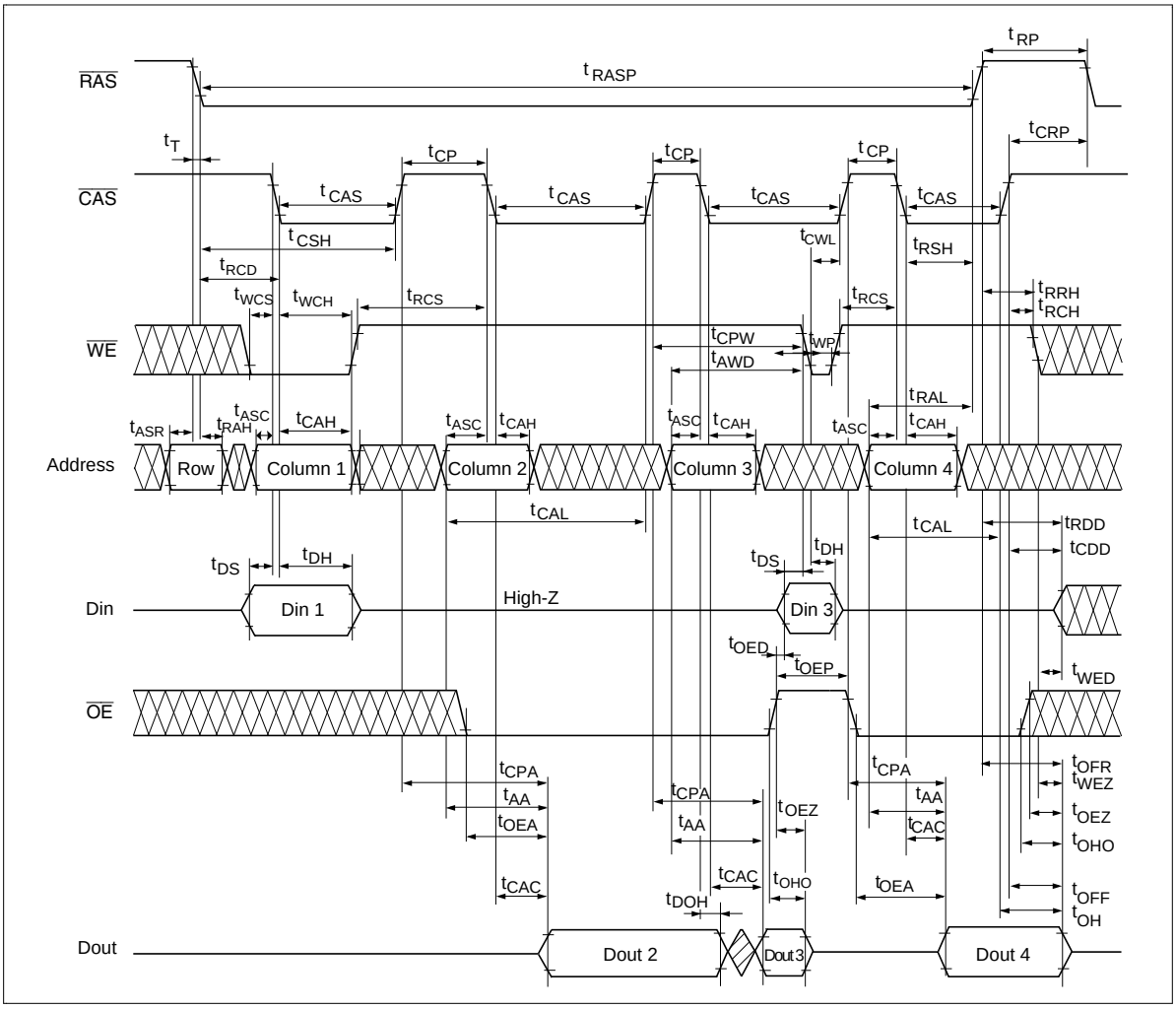
EDO Page Mode Delayed Write Cycle*[18]



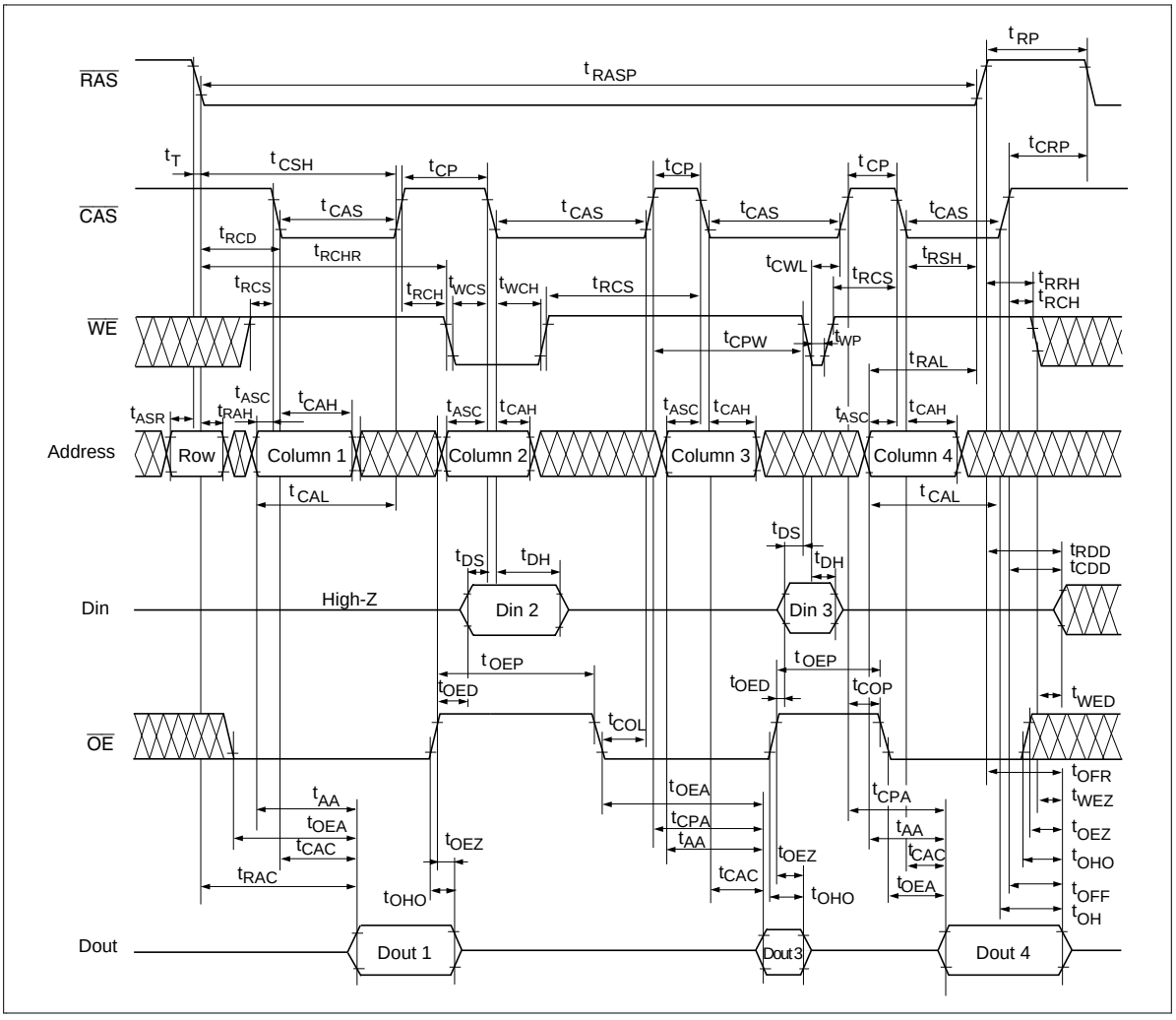
EDO Page Mode Read-Modify-Write Cycle*[18]



EDO Page Mode Mix Cycle (1)*[20]

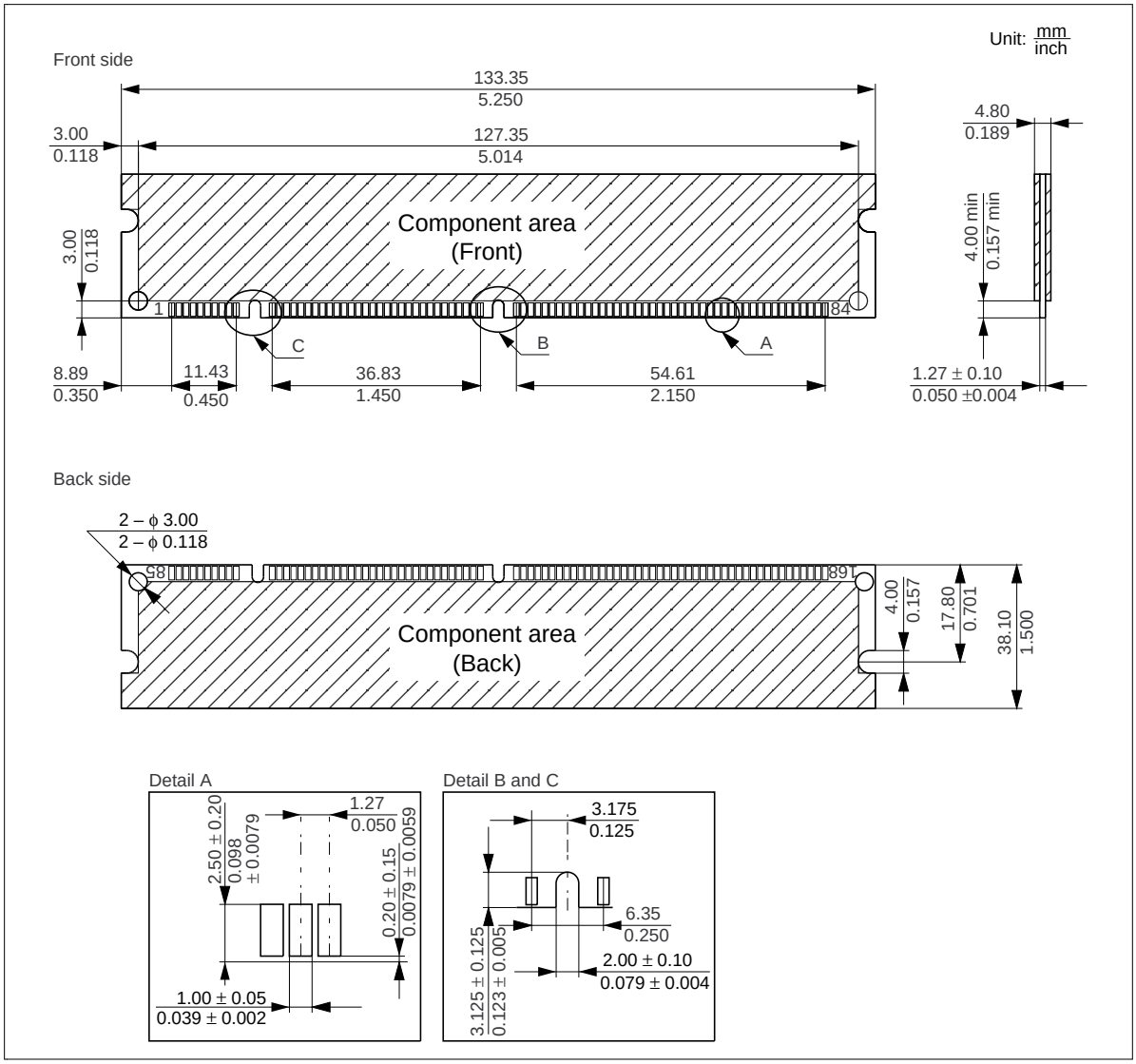


EDO Page Mode Mix Cycle (2) *[20]



Physical Outline

HB56SW3272ESK Series



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jan. 30, 1998	Initial issue (referred to HM5164405/HM5165405 Series Rev. 0.1)	S. Tsukui	K. Tsuneda
0.1	Mar. 16, 1998	Change of Block Diagram Change of Physical Outline	S. Tsukui	K. Tsuneda
1.0	Jun. 23, 1998	(referred to HM5164405/HM5165405 Series rev. 1.0) General Description Addition of Notes about protection from mechanical defects AC Test condition Addition of Ambient illuminance		