



## U3525

## LINEAR INTEGRATED CIRCUIT

### REGULATING PWM IC

#### DESCRIPTION

The UTC **U3525** is a pulse width modulator IC and designed for switching power supplies application to improve performance and reduce external parts usage.

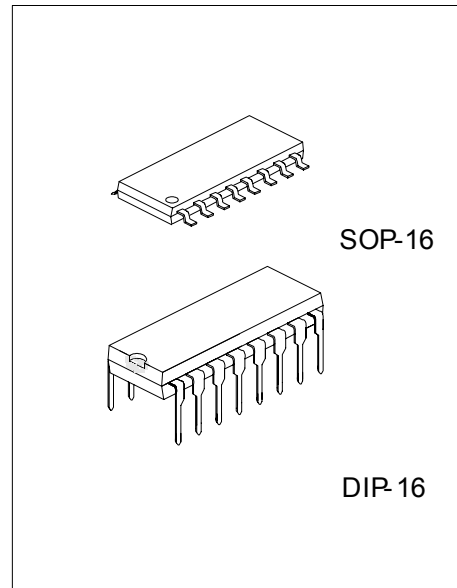
A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. The output stage features NOR logic, giving a LOW output for an OFF state. An under-voltage lockout circuitry, which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages, includes approximately 500 mV of hysteresis for jitter free operation. The PWM circuits also feature a latch following the comparator. When a PWM pulses has been terminated, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA.

#### FEATURES

- \* Input Voltage: 8~35V
- \* On-chip +5.1V reference is trimmed to ±1%
- \* 100HZ ~ 500KHZ oscillator range
- \* Separate oscillator sync terminal
- \* Adjustable dead time control
- \* Internal soft-start
- \* Pulse-by-pulse shutdown
- \* Input under-voltage lockout with hysteresis
- \* Latching PWM to prevent multiple pulses
- \* Dual source/sink output drivers

#### ORDERING INFORMATION

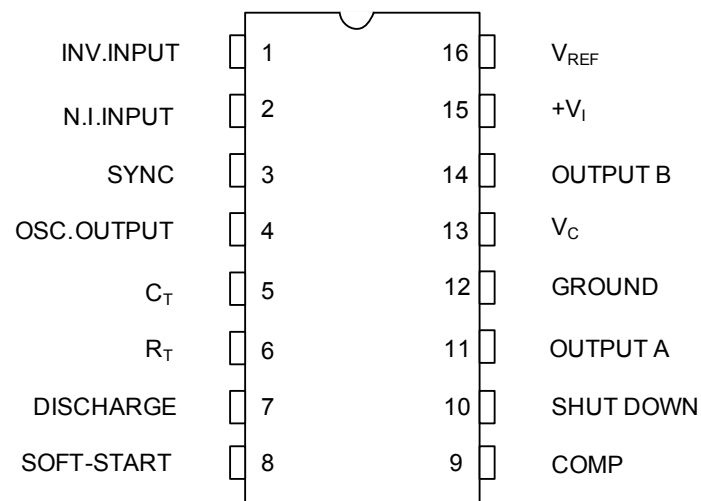
Order Number		Package	Packing
Normal	Lead Free Plating		
U3525-D16-T	U3525L-D16-T	DIP-16	Tube
U3525-S16-R	U3525L-S16-R	SOP-16	Tape Reel
U3525-S16-T	U3525L-S16-T	SOP-16	Tube



\*Pb-free plating product number: U3525L

<p>U3525L-D16-T</p>	<p>(1) Packing Type (2) Package Type (3) Lead Plating</p>	<p>(1) R: Tape Reel, T: Tube (2) D16: DIP-16, S16: SOP-16 (3) L: Lead Free Plating Blank: Pb/Sn</p>
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### ■ PIN CONNECTIONS (top view)

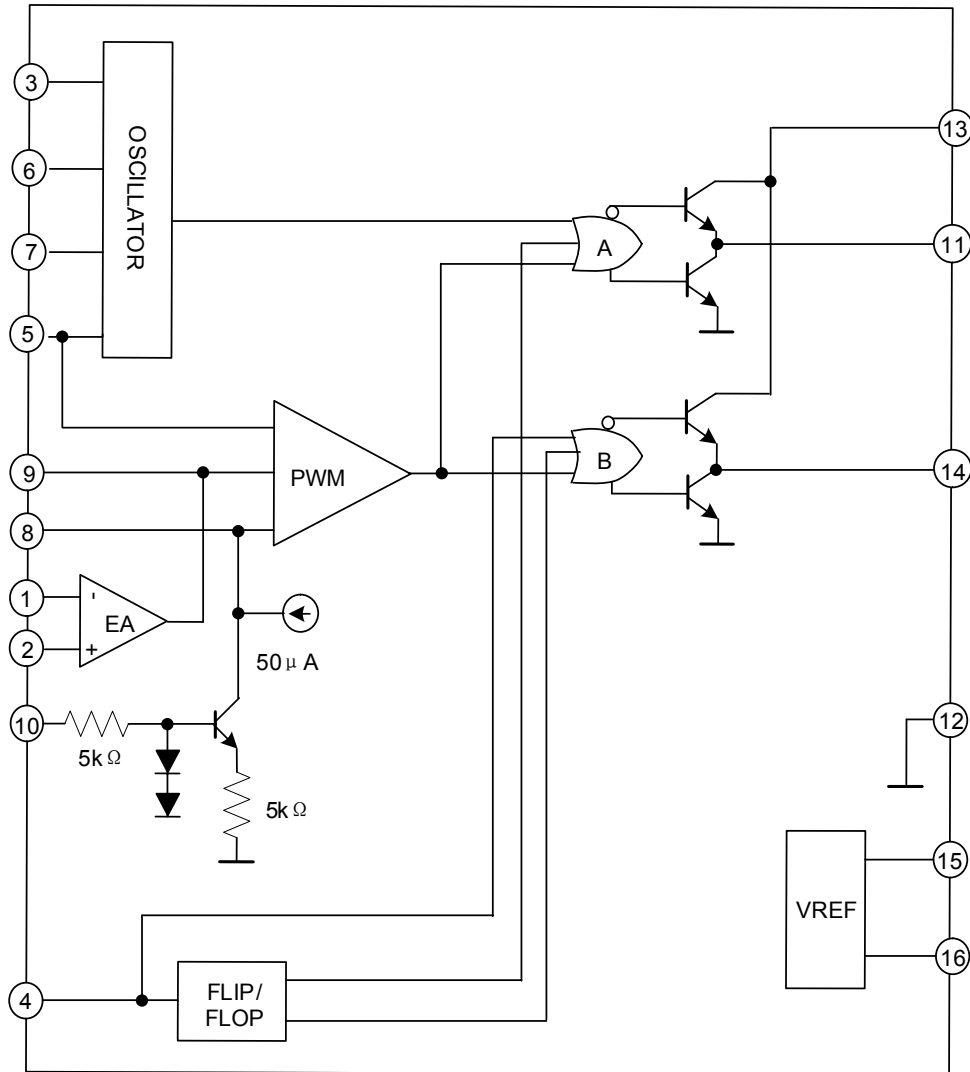


### ■ THERMAL DATA

PARAMETER		SYMBOL	RATING	UNIT
Thermal Resistance Junction-ambient	DIP16	$\theta_{JA}$	80	°C/W
	SOP-16	$\theta_{JA}$	50	°C/W

Note: Thermal resistance junction-alumina with the device soldered on the middle of an alumina supporting substrate measuring 15×20 mm; 0.65 mm thickness with infinite heat sink.

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{IN}$	40	V
Collector Supply Voltage	$V_C$	40	V
Oscillator Charging Current	$I_{OSC}$	5	mA
Output Current, Source or Sink	$I_O$	500	mA
Reference Output Current	$I_R$	50	mA
Current through $C_T$ Terminal		5	mA
Logic Inputs	$I_T$	-0.3 ~ +5.5	V
Analog Inputs		-0.3 ~ $V_i$	V
Total Power Dissipation at $T_a=70^\circ\text{C}$	$P_D$	1000	mW
Junction Temperature	$T_J$	-55 ~ +125	$^\circ\text{C}$
Operating Ambient Temperature	$T_{ORP}$	0 ~ +70	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-65 ~ +150	$^\circ\text{C}$

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ RECOMMENDED OPERATING CONDITIONS (Note)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	$V_{IN}$	8 ~ 35	V
Collector Supply Voltage	$V_C$	4.5 ~ 35	V
Sink/Source Load Current (steady state)	$I_{STEAD}$	0 ~ 100	mA
Sink/Source Load Current (peak)	$I_{PEAK}$	0 ~ 400	mA
Reference Load Current	$I_{LOAD}$	0 ~ 20	mA
Oscillator Frequency Range	$F_O$	100 ~ 400K	Hz
Oscillator Timing Resistor	$R_O$	2 ~ 150	K $\Omega$
Oscillator Timing Capacitor	$C_O$	0.001 ~ 0.1	$\mu\text{F}$
Dead Time Resistor Range	$R_T$	0 ~ 500	$\Omega$

Note: Range over which the device is functional and parameter limits are guaranteed.

## ■ ELECTRICAL CHARACTERISTICS ( $V_{IN}=25\text{V}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>REFERENCE SECTION</b>						
Output Voltage	$V_{REF}$	$T_J=25^\circ\text{C}$	5	5.1	5.2	V
Total Output Variation (Note 1)		Line, Load and Temperature	4.95		5.25	V
Long Term Stability (Note 1)	$\Delta V_{REF}$	$T_J=125^\circ\text{C}$ , 1000 hrs		20	50	mV
Line Regulation	$\Delta V_{REF}$	$V_{IN}=8\sim 35\text{V}$		10	20	mV
Load Regulation	$\Delta V_{REF}$	$I_L=0\sim 20\text{mA}$		20	50	mV
Temp. Stability (Note 1)	$\Delta V_{REF}/\Delta T$	Over Operating Range		20	50	mV
Output Noise Voltage (Note 1)		10 Hz $\leq f \leq$ 10 kHz, $T_J=25^\circ\text{C}$		40	200	$\mu\text{Vrms}$
Short Circuit Current		$V_{REF}=0$ , $T_J=25^\circ\text{C}$		80	100	mA
<b>OSCILLATOR SECTION</b>						
Clock Amplitude (Note 1, 2)			3	3.5		V
Sync Threshold			1.2	2	2.8	V
Sync Input Current		Sync Voltage = 3.5 V		1	2.5	mA
Current Mirror		$I_{RT}=2\text{mA}$	1.7	2	2.2	mA
Maximum Frequency	$f_{MAX}$	$R_T=2\text{K}\Omega$ , $C_T=470\text{pF}$	400			KHz
Minimum Frequency	$f_{MIN}$	$R_T=200\text{K}\Omega$ , $C_T=0.1\mu\text{F}$			120	Hz
Clock Width (Note 1, 2)		$T_J=25^\circ\text{C}$	0.3	0.5	1	$\mu\text{s}$
Initial Accuracy (Note 1, 2)		$T_J=25^\circ\text{C}$		$\pm 2$	$\pm 6$	%
Voltage Stability (Note 1, 2)		$V_{IN}=8\sim 35\text{V}$		$\pm 1$	$\pm 2$	%
Temperature Stability (Note 1)	$\Delta f/\Delta T$	Over Operating Range		$\pm 3$	$\pm 6$	%

### ■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ERROR AMPLIFIER SECTION (V<sub>CM</sub> = 5.1 V)</b>						
Output Low Level				0.2	0.5	V
Output High Level			3.8	5.6		V
Input Offset Voltage	V <sub>OS</sub>			2	10	mV
Input Bias Current	I <sub>b</sub>			1	10	μA
Input Offset Current	I <sub>os</sub>				1	μA
Comm. Mode Reject.	CMR	V <sub>CM</sub> = 1.5 ~ 5.2 V	60	75		dB
Supply Voltage Rejection	PSR	V <sub>IN</sub> = 8 ~ 35 V	50	60		dB
DC Open Loop Gain		R <sub>L</sub> ≥ 10 MΩ	60	75		dB
DC Transconduct. (Note 1, 3)		30 KΩ ≤ R <sub>L</sub> ≤ 1 MΩ, T <sub>J</sub> = 25°C	1.1	1.5		ms
Gain Bandwidth Product (Note 1)		G <sub>v</sub> = 0 dB, T <sub>J</sub> = 25°C	1	2		MHz
<b>PWM COMPARATOR</b>						
Input Threshold (Note 2)		Zero Duty-cycle	0.7	0.9		V
		Maximum Duty-cycle		3.3	3.6	V
Input Bias Current (Note 1)				0.05	1	μA
Minimum Duty-cycle					0	%
Maximum Duty-cycle (Note 2)			45	49		%
<b>SHUTDOWN SECTION</b>						
Soft Start Low Level		V <sub>SD</sub> = 2.5 V		0.4	0.7	V
Shutdown Threshold		To outputs, V <sub>SS</sub> = 5.1 V, T <sub>J</sub> = 25°C	0.6	0.8	1	V
Shutdown Input Current		V <sub>SD</sub> = 2.5 V		0.4	1	mA
Soft Start Current		V <sub>SD</sub> = 0 V, V <sub>SS</sub> = 0 V	25	50	80	μA
Shutdown Delay (Note 1)		V <sub>SD</sub> = 2.5 V, T <sub>J</sub> = 25°C		0.2	0.5	μs
<b>OUTPUT DRIVERS (each output) (V<sub>C</sub> = 20 V)</b>						
Output Low Level		I <sub>SINK</sub> = 20 mA		0.2	0.4	V
		I <sub>SINK</sub> = 100 mA		1	2	V
Output High Level		I <sub>SOURCE</sub> = 20 mA	18	19		V
		I <sub>SOURCE</sub> = 100 mA	17	18		V
Under-Voltage Lockout		V <sub>COMP</sub> and V <sub>SS</sub> = High	6	7	8	V
Collector Leakage	I <sub>C</sub>	V <sub>C</sub> = 35 V			200	μA
Rise Time (Note 1)	t <sub>R</sub>	C <sub>L</sub> = 1 nF, T <sub>J</sub> = 25 °C		100	600	ns
Fall Time (Note 1)	t <sub>F</sub>	C <sub>L</sub> = 1 nF, T <sub>J</sub> = 25 °C		50	300	ns
<b>TOTAL STANDBY CURRENT</b>						
Supply Current	I <sub>S</sub>	V <sub>IN</sub> = 35 V		14	20	mA

Note:1.The parameters are not 100% tested in production.

2.Tested at fosc=40 KHz (R<sub>T</sub>=3.6 KΩ, C<sub>T</sub>=10nF, R<sub>D</sub>=0 Ω). Approximate oscillator frequency is defined by :

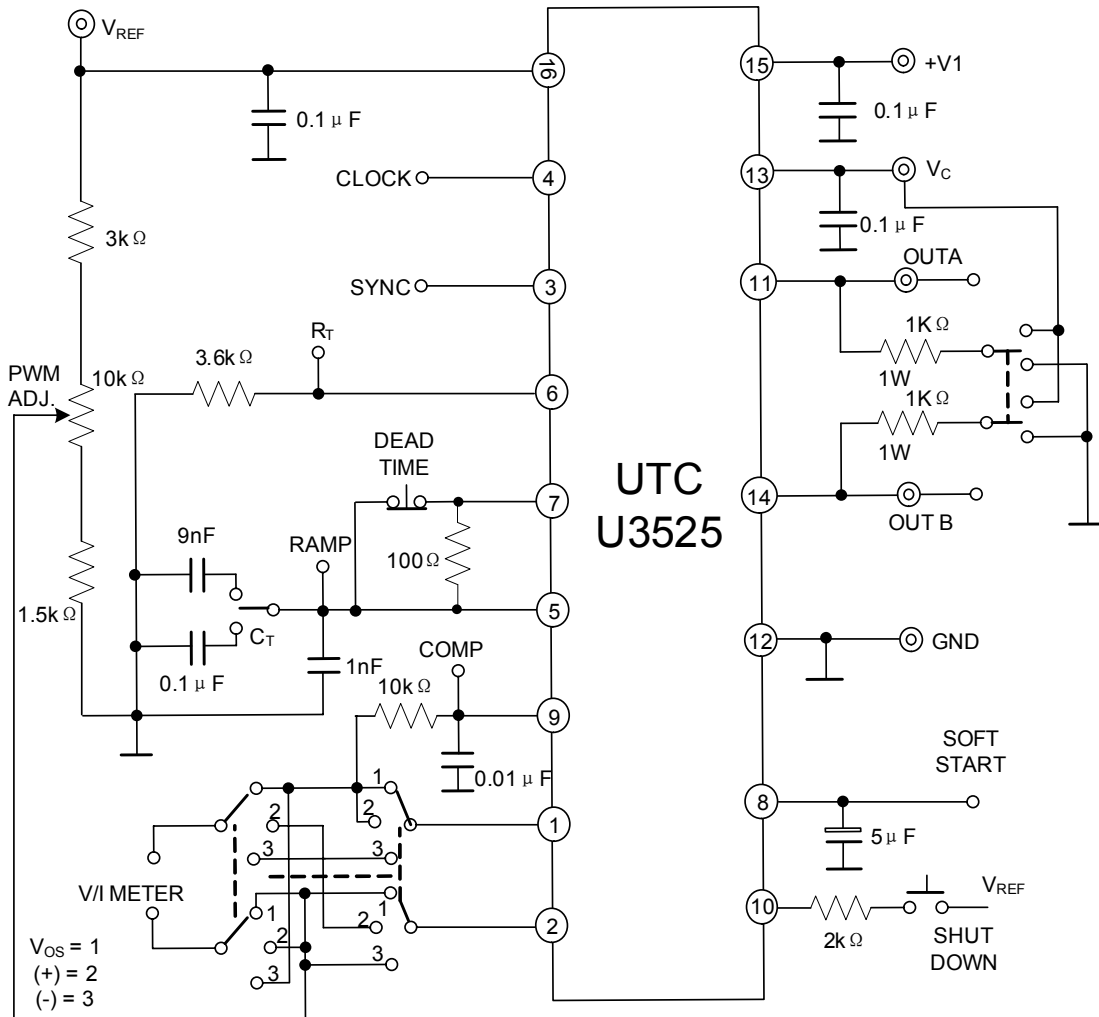
$$f = \frac{1}{C_T(0.7R_T + 3R_D)}$$

3.DC transconductance (g<sub>M</sub>) relates to DC open-loop voltage gain (G<sub>V</sub>) according to the following equation:  
G<sub>V</sub>=g<sub>M</sub>R<sub>L</sub> where R<sub>L</sub> is the resistance from pin 9 to ground. The minimum g<sub>M</sub> specification is used to calculate minimum G<sub>V</sub> when the error amplifier output is loaded.

# U3525

## LINEAR INTEGRATED CIRCUIT

### TEST CIRCUIT



## APPLICATION INFORMATION AND CIRCUIT

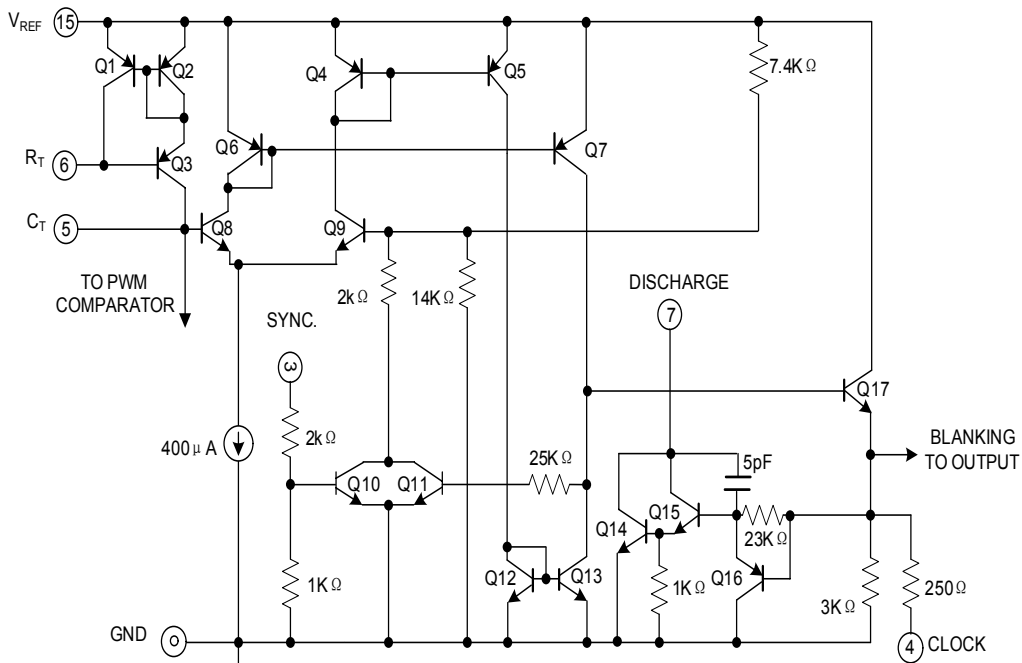
### SHUTDOWN OPTIONS (see Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 $\mu$ A to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150 $\mu$ A current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

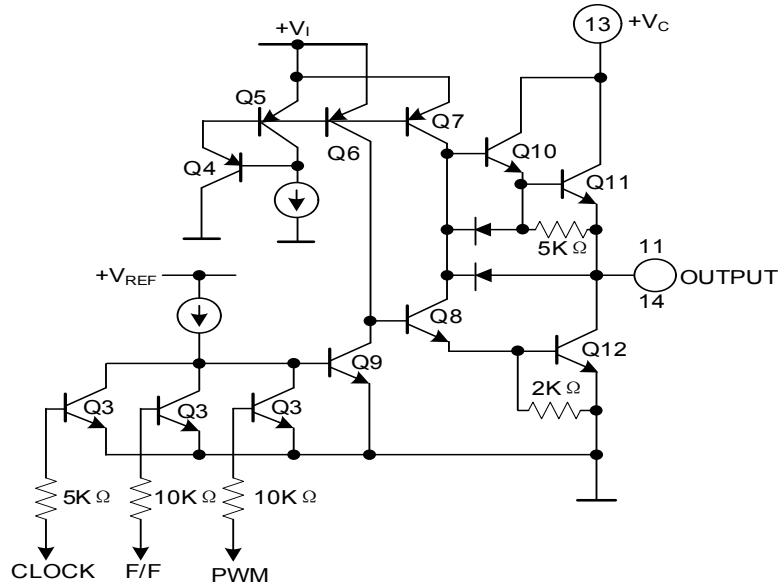
Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

### OSCILLATOR SCHEMATIC

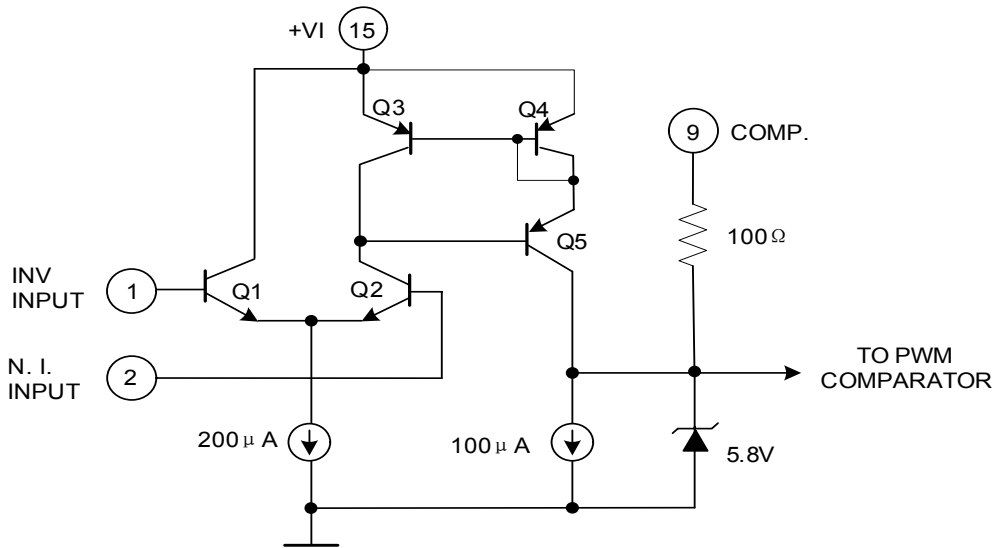


## APPLICATION INFORMATION AND CIRCUIT(Cont.)

### OUTPUT CIRCUIT (1/2 CIRCUIT SHOWN)



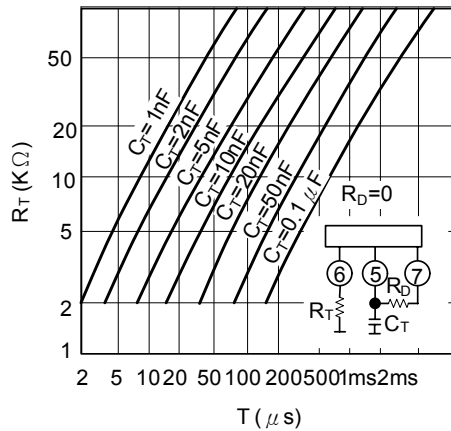
### ERROR AMPLIFIER



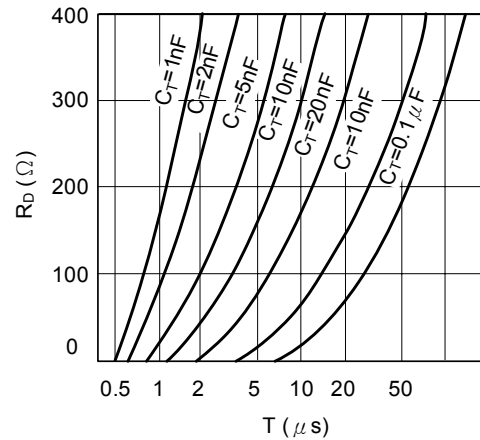


## ■ TYPICAL CHARACTERISTICS

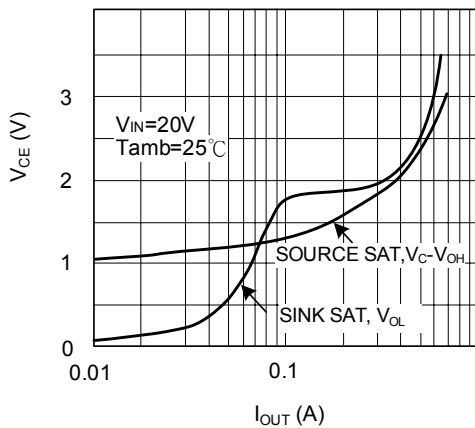
Oscillator Charge Time vs.  $R_T$  and  $C_T$



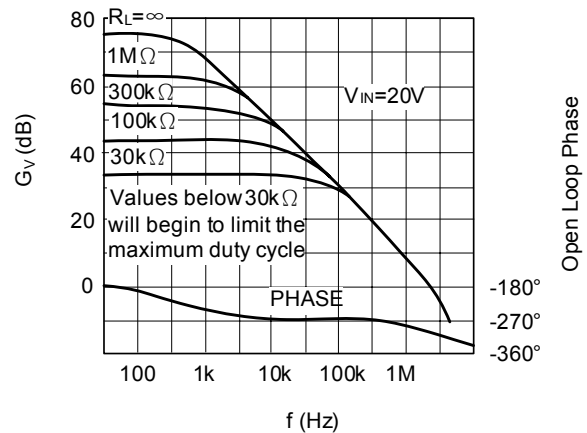
Oscillator DisCharge Time vs.  $R_D$  and  $C_T$



Output Saturation Characteristics



Error Amplifier Voltage Gain and Phase vs Frequency



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