

PIC18F14K22LIN Data Sheet

20-Pin Flash Microcontrollers with Integrated LIN Transceiver and Voltage Regulator

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PIC18F14K22LIN

20-Pin Flash Microcontrollers with Integrated LIN Transceiver and Voltage Regulator

Cross-referenced Material:

This data sheet refers heavily to the following Microchip data sheets:

- PIC18F1XK22/LF1XK22 Data Sheet (DS41365)
- MCP2021/2, LIN Tranceiver with Voltage Regulator Data Sheet (DS22018)

Please have these documents available when reading this device specification. Only deviations from the data sheets listed above will be noted.

Devices Included In This Data Sheet:

- PIC18F14K22LIN

High-Performance RISC CPU:

- C Compiler Optimized Architecture/Instruction Set
- 256 Bytes Data EEPROM
- Linear Program Memory Addressing to 16 Kbytes
- Linear Data Memory Addressing to 512 Bytes
- Up to 16 MIPS Operation
- 16-bit Wide Instructions, 8-bit Wide Data Path
- Priority Levels for Interrupts
- 31-Level, Software Accessible Hardware Stack
- 8 x 8 Single-Cycle Hardware Multiplier

Flexible Oscillator Structure:

- Precision 16 MHz Internal Oscillator Block:
  - Factory calibrated to ±1%
  - Software selectable frequencies range of 31 kHz to 16 MHz
  - 64 MHz performance available using PLL – no external components required
- Four Crystal modes up to 64 MHz
- Two External Clock modes up to 64 MHz
- 4X Phase-Lock Loop (PLL)
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops
- Two-Speed Oscillator Start-up

Special Microcontroller Features:

- Full 5.5V Operation
- Self-Reprogrammable under Software Control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Programmable Brown-out Reset (BOR)
- Extended Watchdog Timer (WDT) with On-Chip Oscillator and Software Enable
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug via Two Pins

Power Managed Modes:

- RUN – CPU on, Peripherals on
- IDLE – CPU off, Peripherals on
- Sleep – CPU off, Peripherals off

Analog Features:

- Analog-to-Digital (A/D) Converter module:
  - 10-bit resolution
  - 9 analog input channels
  - Auto acquisition capability
  - Conversion available during Sleep
- Analog Comparator module with:
  - Two rail-to-rail analog comparators
  - Comparator inputs and outputs externally accessible and configurable
- Voltage Reference module with:
  - Programmable on-chip voltage reference (CV_{REF}) module (% of V_{DD})
  - Fixed Voltage Reference (FVR) with multiple reference voltages

Peripheral Features:

- 12 I/O pins and 1 Input Only Pin:
  - High current sink/source 25 mA/25 mA
  - Individually programmable weak pull-ups
  - Individually programmable interrupt-on-pin change
- Three External Interrupt Pins
- Four Timer modules:
  - 3 16-bit timers/counters with prescaler
  - 1 8-bit timer/counter with 8-bit period register, prescaler and postscaler
  - Dedicated, low-power Timer1 oscillator

- Enhanced Capture/Compare/PWM (ECCP) module with:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and Auto-restart
  - PWM output steering control
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter module (EUSART):
  - Supports RS-232, RS-485 and LIN 2.0
  - Auto-Baud Detect
  - Auto Wake-up on Start bit
- SR Latch (555 Timer) module with:
  - Configurable inputs and outputs
  - Supports mTouch™ capacitive sensing applications
- On-board Voltage Regulator:
  - Output voltage of 5.0V with tolerances of ±3% over temperature range
  - Maximum continuous input voltage of 30V
  - Internal thermal overload protection
  - Internal short circuit current limit
  - External components limited to filter capacitor only and load capacitor
  - Automatic thermal shutdown
- Internal Bus Transceiver Compliant with LIN Bus Specifications 1.3, 2.0 and 2.1 and are Compliant to SAE J2602:
  - Support Baud Rates up to 20 Kbaud
  - 43V load dump protected
  - Very low EMI meets stringent OEM requirements
  - Wide supply voltage, 6.0V-18.0V continuous:
  - Internal pull-up resistor and diode
  - Protected against ground shorts
  - Protected against loss of ground
  - High current drive
  - Automatic thermal shutdown
- Extended Temperature Range: -40 to +125°C



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TABLE 1: DEVICE OVERVIEW

Device	Program Memory		Data Memory		Pins	I/O	10-bit A/D Channels	Comparators	Timers 8-bit/16-bit	ECCP	EUSART(1)	SR Latch	Other Features
	Bytes	Words	SRAM (bytes)	Data EEPROM (bytes)									
PIC18F14K22LIN	16K	8K	512	256	20	13	9-ch	2	1/3	1	1	Yes	LIN Transceiver, Voltage Regulator

Note 1: EUSART dedicated to LIN communications.

Pin Diagrams

20-PIN SSOP

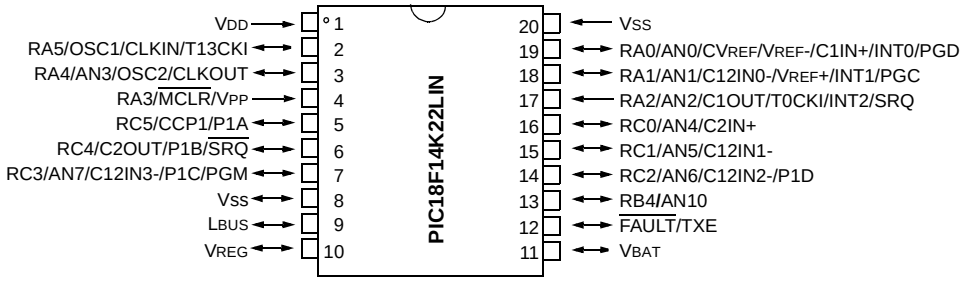
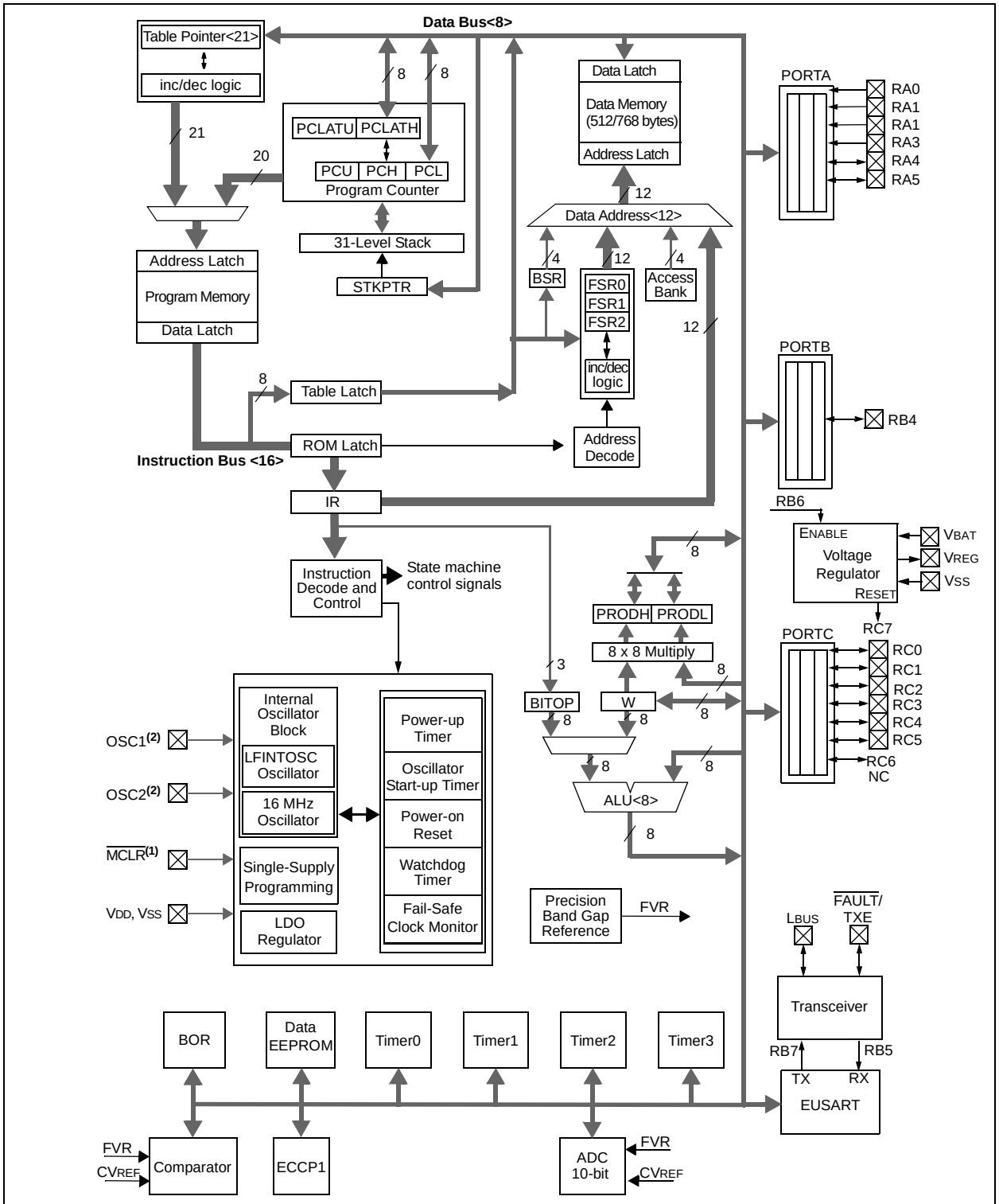


FIGURE 1: PIC18F14K22LIN BLOCK DIAGRAM



Note 1: RA3 is only available when $\overline{\text{MCLR}}$ functionality is disabled.

2: OSC1/CLKIN and OSC2/CLKOUT are only available in select Oscillator modes and when these pins are not being used as digital I/O. Refer to DS41365, "*PIC18(L)F1XK22 Data Sheet*", Section 2.0 "Oscillator Module" for additional information.

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TABLE 2: PIC18F14K22LIN PIN SUMMARY

20-PiN SSOP	I/O	Analog	Comparator	Reference	ECCP	EUSART	SR Latch	Timers	Interrupts	Pull-up	Basic
19	RA0	AN0	C1IN+	VREF-/CVREF	—	—	—	—	IOC/INT0	Y	PGD
18	RA1	AN1	C12IN0-	VREF+	—	—	—	—	IOC/INT1	Y	PGC
17	RA2	AN2	C1OUT	—	—	—	SRQ	T0CKI	IOC/INT2	Y	—
4	RA3	—	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$/VPP
3	RA4	AN3	—	—	—	—	—	—	IOC	Y	OSC2/CLKOUT
2	RA5	—	—	—	—	—	—	T13CKI	IOC	Y	OSC1/CLKIN
13	RB4	AN10	—	—	—	—	—	—	IOC	Y	—
Note	RB5	—	—	—	—	RXD	—	—	—	—	—
Note	RB6	—	—	—	—	—	—	—	—	—	CS/LWAKE
Note	RB7	—	—	—	—	TXD	—	—	—	—	—
16	RC0	AN4	C2IN+	—	—	—	—	—	—	—	—
15	RC1	AN5	C12IN1-	—	—	—	—	—	—	—	—
14	RC2	AN6	C12IN2-	—	P1D	—	—	—	—	—	—
7	RC3	AN7	C12IN3-	—	P1C	—	—	—	—	—	PGM
6	RC4		C2OUT	—	P1B	—	$\overline{\text{SRQ}}$	—	—	—	—
5	RC5	—	—	—	CCP1/P1A	—	—	—	—	—	—
Note	RC6	—	—	—	—	—	—	—	—	—	no connection
Note	RC7	—	—	—	—	—	—	—	—	—	RESET input from Voltage Regulator
12	$\overline{\text{FAULT}}$/ TXE	—	—	—	—	—	—	—	—	—	
11	VBAT	—	—	—	—	—	—	—	—	—	
10	VREG	—	—	—	—	—	—	—	—	—	
9	LBUS	—	—	—	—	—	—	—	—	—	
8	—	—	—	—	—	—	—	—	—	—	VSS
1	—	—	—	—	—	—	—	—	—	—	VDD
20	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Internal connection. No associated external pin.

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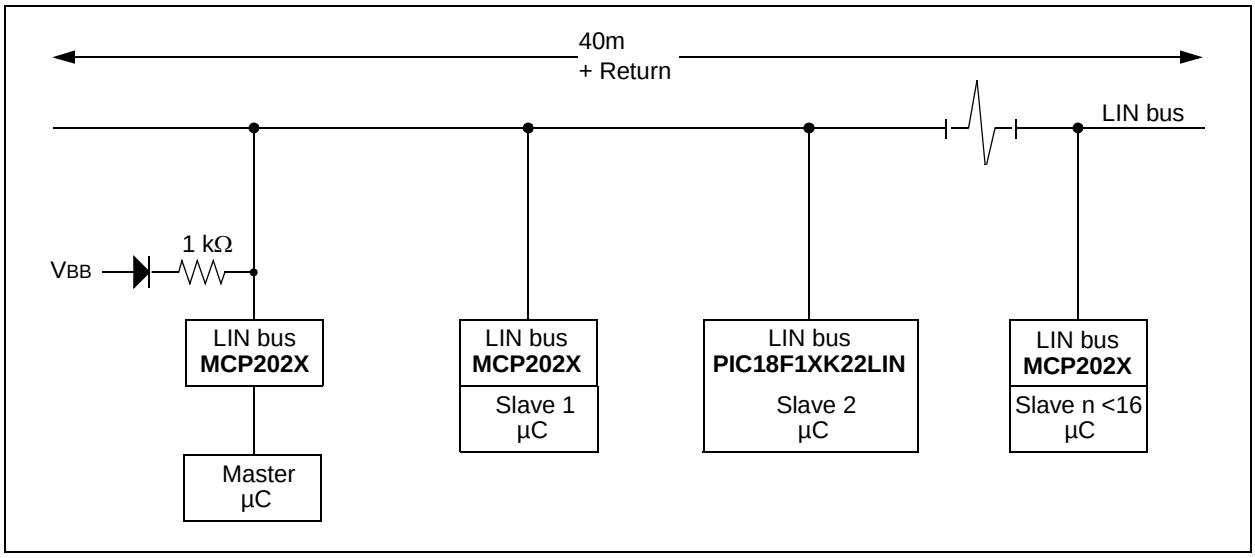
1.0 USING THE MCP200X IN LIN BUS APPLICATIONS

Note:	Failure to follow the recommended setup and initialization may result in improper or unknown LIN operation.

1.1 Hardware

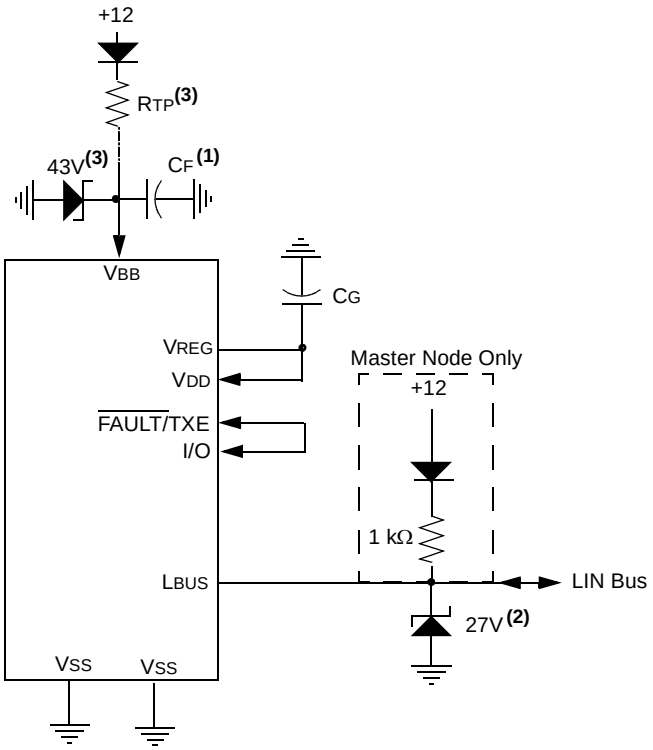
The MCP200X internal connections are optimized to reduce the number of components in a typical LIN/J2602 node in a LIN bus system. Some features and modules of the stand-alone PIC18F14K22 are no longer available or their functionality has changed.

FIGURE 1-1: TYPICAL LIN NETWORK CONFIGURATION



For this reason, the following (Example 1-1) is a recommended block diagram. Note the microcontroller is powered by the internal voltage regulator and an external connection must be made between V_{REG} and V_{BB} along with a load capacitor. $\overline{FAULT}$/TXE can be monitored or controlled by any I/O pin.

EXAMPLE 1-1: TYPICAL PIC18F14K22LIN APPLICATION



Note 1: C_F is the filter capacitor for the external voltage supply.

2: Transient suppressor diode. V_{CLAMP} L = 27V.

3: These components are required for additional load dump protection above 43V.

1.2 Software

Please refer to the sections of this data sheet to determine what facilities have changed and what register values need to be properly initialized. Failure to follow these guidelines may result in improper operation.

1.2.1 TYPICAL INITIALIZATION CODE

```
InitialiseIOports
       MOVLB   0xF             ;point the F bank
       MOVLW   0x04            ;disable AN8:9,11
       ANDWF   ANSELH,f
       MOVLW   0xC0            ;PORTB7:6 must be inputs
       IORWF   TRISB,f
       MOVLW   0xCF            ;PORTB5:4 must be outputs
       ANDWF   TRISB,f
       BSF     LINCS           ;Chip Select Transceiver
       MOVLW   0x80
       IORWF   TRISC,f         ;PORTC7 is an input
       RETURN

SetupLINUSART
       MOVLB   0x0F            ;Register Bank 0xF
       MOVLW   B'10010000'     ;UART enabled,8-bit,continuous receive
       MOVWF   RCSTA
       MOVLW   B'00000100'     ;8-bit, asynchronous, high-baudrate
       MOVWF   TXSTA
```

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```
        MOVLW   B'00001000'    ;16-bit Baud Rate Generator
        MOVWF   BAUDCON
        CLRF    SPBRGH
        MOVLW   0x31           ;setup initially for 20KBaud @ 4.0MHz, BRGH=1, BRG16=1
        MOVWF   SPBRG
        BSF     LINCS          ;to enable transceiver
        RETURN
```

1.3 Sample Transmit Software

This routine is called when PIR1<TXIF> = 1:

```
PutDATAbyte
        MOVF    INDF0,w               ; copy data byte into w-register
        MOVWF   TXREG
        INCF    FSR0, f               ; point to next location
        DECFSZ  MESSAGE_COUNTER, f    ; decrement Message Counter by one
        RETURN
```

1.4 Sample Receive Software

The following routines are called when PIR1<RCIF> = 1:

```
GetBREAK
        BTFSS   RCSTA,FERR     ; was BREAK character longer than 8 bits?
        GOTO    BadBREAKchar   ; no, not a valid BREAK, too short
        MOVF    RCREG,w        ; dump break character, reset RCIF and FERR
        BTFSS   STATUS,Z
        GOTO    BadBREAKchar   ; no, not a valid BREAK, not zero
        DECF    MESSAGE_COUNTER
        BTFSS   LINRX
        GOTO    $-2
        BSF     BAUDCTL,ABDEN  ; enable AutoBaud
        RETURN
BadBREAKchar
        MOVF    RCREG,w        ; dump break character, reset RCIF and FERR
        RETURN

GetSYNC
        BTFSC   BAUDCTL,ABDOVF; did baud rate generator overflow?
        GOTO    BadSYNCchar; yes, bad sync character
        BTFSC   RCSTA,FERR; was there a Framing Error?
        GOTO    BadSYNCchar; yes, bad sync character
        DECF    SPBRG
        MOVF    RCREG,w        ; dump sync character, reset RCIF
        DECF    MESSAGE_COUNTER
        RETURN
BadSYNCchar
        BCF     BAUDCTL,ABDOVF; clear the overflow condition
        MOVLW   .12            ; reset the state machine
        MOVWF   MESSAGE_COUNTER
        RETURN

GetDATAbyte
        MOVF    RCREG,w        ; get character, reset RCIF and FERR
        MOVWF   RXTX_REG       ; copy data into w-register
        MOVWF   INDF0          ; copy data into data area
        INCF    FSR0, f        ; point to next location
        DECF    MESSAGE_COUNTER, f ; decrement number of bytes to receive by one
        RETURN
```

NOTES:

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2.0 MEMORY ORGANIZATION

See DS41365, “PIC18F1XK22/LF1XK22 Data Sheet” for descriptions of program memory, Data RAM and Data EEPROM.

TABLE 2-1: SPECIAL FUNCTION REGISTER MAP FOR PIC18F14K22LIN DEVICES

Address	Name	Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FD7h	TMR0H	FAFh	SPBRG	F87h	—(2)	F5Fh	—(2)
FFEh	TOSH	FD6h	TMR0L	FAEh	RCREG	F86h	—(2)	F5Eh	—(2)
FFDh	TOSL	FD5h	T0CON	FADh	TXREG	F85h	—(2)	F5Dh	—(2)
FFCh	STKPTR	FD4h	—(2)	FACh	**TXSTA**(3)	F84h	—(2)	F5Ch	—(2)
FFBh	PCLATU	FD3h	OSCCON	FABh	**RCSTA**(3)	F83h	—(2)	F5Bh	—(2)
FFAh	PCLATH	FD2h	OSCCON2	FAAh	EEADRH	F82h	**PORTC**(3)	F5Ah	—(2)
FF9h	PCL	FD1h	WDTCON	FA9h	EEADR	F81h	**PORTB**(3)	F59h	—(2)
FF8h	TBLPTRU	FD0h	RCON	FA8h	EEDATA	F80h	PORTA	F58h	—(2)
FF7h	TBLPTRH	FCFh	TMR1H	FA7h	EECON2(1)	F7Fh	**ANSELH**(3)	F57h	—(2)
FF6h	TBLPTRL	FCEh	TMR1L	FA6h	EECON1	F7Eh	ANSEL	F56h	—(2)
FF5h	TABLAT	FCDh	T1CON	FA5h	—(2)	F7Dh	—(2)	F55h	—(2)
FF4h	PRODH	FCCh	TMR2	FA4h	—(2)	F7Ch	—(2)	F54h	—(2)
FF3h	PRODL	FCBh	PR2	FA3h	—(2)	F7Bh	—(2)	F53h	—(2)
FF2h	INTCON	FCAh	T2CON	FA2h	IPR2	F7Ah	IOCB		
FF1h	INTCON2	FC9h	**SSPBUF**(3)	FA1h	PIR2	F79h	IOCA		
FF0h	INTCON3	FC8h	**SSPADD**(3)	FA0h	PIE2	F78h	WPUB		
FEFh	INDF0(1)	FC7h	**SSPSTAT**(3)	F9Fh	**IPR1**(3)	F77h	WPUA		
FEEh	POSTINC0(1)	FC6h	**SSPCON1**(3)	F9Eh	**PIR1**(3)	F76h	SLRCON		
FEDh	POSTDEC0(1)	FC5h	**SSPCON2**(3)	F9Dh	**PIE1**(3)	F75h	—(2)		
FECh	PREINC0(1)	FC4h	ADRESH	F9Ch	—(2)	F74h	—(2)		
FEBh	PLUSW0(1)	FC3h	ADRESL	F9Bh	OSCTUNE	F73h	—(2)		
FEAh	FSR0H	FC2h	ADCON0	F9Ah	—(2)	F72h	—(2)		
FE9h	FSR0L	FC1h	ADCON1	F99h	—(2)	F71h	—(2)		
FE8h	WREG	FC0h	ADCON2	F98h	—(2)	F70h	—(2)		
FE7h	INDF1(1)	FBFh	CCPR1H	F97h	—(2)	F6Fh	**SSPMASK**(3)		
FE6h	POSTINC1(1)	FBEh	CCPR1L	F96h	—(2)	F6Eh	—(2)		
FE5h	POSTDEC1(1)	FBDh	CCP1CON	F95h	—(2)	F6Dh	CM1CON0		
FE4h	PREINC1(1)	FBCh	VREFCON2	F94h	**TRISC**(3)	F6Ch	CM2CON1		
FE3h	PLUSW1(1)	FBBh	VREFCON1	F93h	**TRISB**(3)	F6Bh	CM2CON0		
FE2h	FSR1H	FBAh	VREFCON0	F92h	TRISA	F6Ah	—(2)		
FE1h	FSR1L	FB9h	PSTRCON	F91h	—(2)	F69h	SRCON1		
FE0h	BSR	FB8h	**BAUDCON**(3)	F90h	—(2)	F68h	SRCON0		
FDFh	INDF2(1)	FB7h	PWM1CON	F8Fh	—(2)	F67h	—(2)		
FDEh	POSTINC2(1)	FB6h	ECCP1AS	F8Eh	—(2)	F66h	—(2)		
FDDh	POSTDEC2(1)	FB5h	—(2)	F8Dh	—(2)	F65h	—(2)		
FDCh	PREINC2(1)	FB4h	—(2)	F8Ch	—(2)	F64h	—(2)		
FDBh	PLUSW2(1)	FB3h	TMR3H	F8Bh	**LATC**(3)	F63h	—(2)		
FDAh	FSR2H	FB2h	TMR3L	F8Ah	**LATB**(3)	F62h	—(2)		
FD9h	FSR2L	FB1h	T3CON	F89h	LATA	F61h	—(2)		
FD8h	STATUS	FB0h	SPBRGH	F88h	—(2)	F60h	—(2)		

Legend: = Unimplemented data memory locations, read as '0',

Note 1: This is not a physical register.

2: Unimplemented registers are read as '0'.

3: Registers in **BOLD** have functional differences. Please refer to appropriate chapters for details.

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TABLE 2-2: REGISTER FILE SUMMARY (PIC18F14K22LIN)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
TOSU	—	—	—	Top-of-Stack Upper Byte (TOS<20:16>)					---0 0000
TOSH	Top-of-Stack, High Byte (TOS<15:8>)								0000 0000
TOSL	Top-of-Stack, Low Byte (TOS<7:0>)								0000 0000
STKPTR	STKOVF	STKUNF	—	SP4	SP3	SP2	SP1	SP0	00-0 0000
PCLATU	—	—	—	Holding Register for PC<20:16>					---0 0000
PCLATH	Holding Register for PC<15:8>								0000 0000
PCL	PC, Low Byte (PC<7:0>)								0000 0000
TBLPTRU	—	—	—	Program Memory Table Pointer Upper Byte (TBLPTR<20:16>)					---0 0000
TBLPTRH	Program Memory Table Pointer, High Byte (TBLPTR<15:8>)								0000 0000
TBLPTRL	Program Memory Table Pointer, Low Byte (TBLPTR<7:0>)								0000 0000
TABLAT	Program Memory Table Latch								0000 0000
PRODH	Product Register, High Byte								xxxx xxxx
PRODL	Product Register, Low Byte								xxxx xxxx
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RABIE	TMR0IF	INT0IF	RABIF	0000 000x
INTCON2	$\overline{\text{RABPU}}$	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RABIP	1111 -1-1
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF	11-0 0-00
INDF0	Uses contents of FSR0 to address data memory – value of FSR0 not changed (not a physical register)								N/A
POSTINC0	Uses contents of FSR0 to address data memory – value of FSR0 post-incremented (not a physical register)								N/A
POSTDEC0	Uses contents of FSR0 to address data memory – value of FSR0 post-decremented (not a physical register)								N/A
PREINC0	Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented (not a physical register)								N/A
PLUSW0	Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented (not a physical register) – value of FSR0 offset by W								N/A
FSR0H	—	—	—	—	Indirect Data Memory Address Pointer 0, High Byte				---- 0000
FSR0L	Indirect Data Memory Address Pointer 0, Low Byte								xxxx xxxx
WREG	Working Register								xxxx xxxx
INDF1	Uses contents of FSR1 to address data memory – value of FSR1 not changed (not a physical register)								N/A
POSTINC1	Uses contents of FSR1 to address data memory – value of FSR1 post-incremented (not a physical register)								N/A
POSTDEC1	Uses contents of FSR1 to address data memory – value of FSR1 post-decremented (not a physical register)								N/A
PREINC1	Uses contents of FSR1 to address data memory – value of FSR1 pre-incremented (not a physical register)								N/A
PLUSW1	Uses contents of FSR1 to address data memory – value of FSR1 pre-incremented (not a physical register) – value of FSR1 offset by W								N/A
FSR1H	—	—	—	—	Indirect Data Memory Address Pointer 1, High Byte				---- 0000
FSR1L	Indirect Data Memory Address Pointer 1, Low Byte								xxxx xxxx
BSR	—	—	—	—	Bank Select Register				---- 0000
INDF2	Uses contents of FSR2 to address data memory – value of FSR2 not changed (not a physical register)								N/A
POSTINC2	Uses contents of FSR2 to address data memory – value of FSR2 post-incremented (not a physical register)								N/A
POSTDEC2	Uses contents of FSR2 to address data memory – value of FSR2 post-decremented (not a physical register)								N/A
PREINC2	Uses contents of FSR2 to address data memory – value of FSR2 pre-incremented (not a physical register)								N/A
PLUSW2	Uses contents of FSR2 to address data memory – value of FSR2 pre-incremented (not a physical register) – value of FSR2 offset by W								N/A
FSR2H	—	—	—	—	Indirect Data Memory Address Pointer 2, High Byte				---- 0000
FSR2L	Indirect Data Memory Address Pointer 2, Low Byte								xxxx xxxx
STATUS	—	—	—	N	OV	Z	DC	C	---x xxxx

Legend: x = unknown, u = unchanged, – = unimplemented, q = value depends on condition

Note 1: The SBOREN bit is only available when the BOREN<1:0> Configuration bits = 01; otherwise it is disabled and reads as '0'. Refer to DS41365, "*PIC18(L)F1XK22 Data Sheet*", Section 21.4 "Brown-out Reset (BOR)" for additional information

2: The RA3 bit is only available when Master Clear Reset is disabled (MCLRE Configuration bit = 0). Otherwise, RA3 reads as '0'. This bit is read-only.

3: Rows highlighted in black show required values for normal LIN protocol applications.

TABLE 2-2: REGISTER FILE SUMMARY (PIC18F14K22LIN) (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
TMR0H	Timer0 Register, High Byte								0000 0000
TMR0L	Timer0 Register, Low Byte								xxxx xxxx
T0CON	TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0	1111 1111
OSCCON	IDLEN	IRCF2	IRCF1	IRCF0	OSTS	HFIOFS	SCS1	SCS0	0011 qq00
OSCCON2	—	—	—	—	—	PRI_SD	HFIOFL	LFIOFS	---- -10x
WDTCON	—	—	—	—	—	—	—	SWDTEN	--- ---0
RCON	IPEN	SBOREN(1)	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$	0q-1 11q0
TMR1H	Timer1 Register, High Byte								xxxx xxxx
TMR1L	Timer1 Register, Low Bytes								xxxx xxxx
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000
TMR2	Timer2 Register								0000 0000
PR2	Timer2 Period Register								1111 1111
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000
SSPBUF(3)	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**xxxx xxxx**
SSPADD(3)	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0000 0000**
SSPSTAT(3)	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0000 0000**
SSPCON1(3)	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0000 0000**
SSPCON2(3)	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0000 0000**
ADRESH	A/D Result Register, High Byte								xxxx xxxx
ADRESL	A/D Result Register, Low Byte								xxxx xxxx
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	ADON	--00 0000
ADCON1	—	—	—	—	PVCFG1	PVCFG0	NVCFG1	NVCFG0	---- 0000
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	0-00 0000
CCPR1H	Capture/Compare/PWM Register 1, High Byte								xxxx xxxx
CCPR1L	Capture/Compare/PWM Register 1, Low Byte								xxxx xxxx
CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000
VREFCON2	—	—	—	DAC1R4	DAC1R3	DAC1R2	DAC1R1	DAC1R0	---0 0000
VREFCON1	D1EN	D1LPS	DAC1OE	---	D1PSS1	D1PSS0	—	D1NSS	000- 00-0
VREFCON0	FVR1EN	FVR1ST	FVR1S1	FVR1S0	—	—	—	—	0001 ----
PSTRCON	—	—	—	STRSYNC	STRD	STRC	STRB	STRA	---0 0001
BAUDCON(3)	**ABDOVF**	**RCIDL**	**0**	**0**	**BRG16**	**—**	**WUE**	**ABDEN**	**0100 0-00**
PWM1CON	PRSEN	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0	0000 0000
ECCP1AS	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0	0000 0000
TMR3H	Timer3 Register, High Byte								xxxx xxxx
TMR3L	Timer3 Register, Low Byte								xxxx xxxx
T3CON	RD16	—	T3CKPS1	T3CKPS0	T3CCP1	$\overline{T3SYNC}$	TMR3CS	TMR3ON	0-00 0000

Legend: x = unknown, u = unchanged, – = unimplemented, q = value depends on condition

Note 1: The SBOREN bit is only available when the BOREN<1:0> Configuration bits = 01; otherwise it is disabled and reads as '0'. Refer to DS41365, "*PIC18(L)F1XK22 Data Sheet*", Section 21.4 "Brown-out Reset (BOR)" for additional information

2: The RA3 bit is only available when Master Clear Reset is disabled (MCLRE Configuration bit = 0). Otherwise, RA3 reads as '0'. This bit is read-only.

3: Rows highlighted in black show required values for normal LIN protocol applications.

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TABLE 2-2: REGISTER FILE SUMMARY (PIC18F14K22LIN) (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
SPBRGH	EUSART Baud Rate Generator Register, High Byte								0000 0000
SPBRG	EUSART Baud Rate Generator Register, Low Byte								0000 0000
RCREG	EUSART Receive Register								0000 0000
TXREG	EUSART Transmit Register								0000 0000
TXSTA(3)	**0**	**0**	**TXEN**	**0**	**SENDB**	**BRGH**	**TRMT**	**0**	**0000 0010**
RCSTA(3)	**SPEN**	**0**	**0**	**CREN**	**0**	**FERR**	**OERR**	**0**	**0000 000x**
EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000
EEADRH	—	—	—	—	—	—	EEADR9	EEADR8	---- --00
EEDATA	EEPROM Data Register								0000 0000
EECON2	EEPROM Control Register 2 (not a physical register)								0000 0000
EECON1	EEPGD	CFGS	—	FREE	WRERR	WREN	WR	RD	xx-0 x000
IPR2	OSCFIP	C1IP	C2IP	EEIP	BCLIP	—	TMR3IP	—	1111 111-
PIR2	OSCFIF	C1IF	C2IF	EEIF	BCLIF	—	TMR3IF	—	0000 000-
PIE2	OSCFIE	C1IE	C2IE	EEIE	BCLIE	—	TMR3IE	—	0000 000-
IPR1(3)	**—**	**ADIP**	**RCIP**	**TXIP**	**1**	**CCP1IP**	**TMR2IP**	**TMR1IP**	**-111 1111**
PIR1(3)	**—**	**ADIF**	**RCIF**	**TXIF**	**0**	**CCP1IF**	**TMR2IF**	**TMR1IF**	**-000 0000**
PIE1(3)	**—**	**ADIE**	**RCIE**	**TXIE**	**0**	**CCP1IE**	**TMR2IE**	**TMR1IE**	**-000 0000**
OSCTUNE	INTSRC	PLLEN	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	0000 0000
TRISC(3)	**TRISC7**	**—**	**TRISC5**	**TRISC4**	**TRISC3**	**TRISC2**	**TRISC1**	**TRISC0**	**1111 1111**
TRISB(3)	**TRISB7**	**TRISB6**	**TRISB5**	**TRISB4**	**—**	**—**	**—**	**—**	**1111 ----**
TRISA	—	—	TRISA5	TRISA4	—	TRISA2	TRISA1	TRISA0	--11 -111
LATC(3)	**$\overline{\text{LINRESET}}$**	**—**	**LATC5**	**LATC4**	**LATC3**	**LATC2**	**LATC1**	**LATC0**	**xxxx xxxx**
LATB(3)	LATB7	LATB6	LATB5	LATB4	—	—	—	—	xxxx ----
LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	--xx -xxx
PORTC(3)	**$\overline{\text{LINRESET}}$**	**—**	**RC5**	**RC4**	**RC3**	**RC2**	**RC1**	**RC0**	**xxxx xxxx**
PORTB(3)	**LINTX**	**LINCS**	**LINRX**	**RB4**	**—**	**—**	**—**	**—**	**xxxx ----**
PORTA	—	—	RA5	RA4	RA3(2)	RA2	RA1	RA0	--xx xxxx
ANSELH(3)	**—**	**—**	**—**	**—**	**0**	**ANS10**	**0**	**0**	**---- 1111**
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111
IOCB	IOCB7	IOCB6	IOCB5	IOCB4	—	—	—	—	0000 ----
IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	—	—	—	—	1111 ----
WPUA	—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	--11 1111
SLRCON	—	—	—	—	—	Reserved	Reserved	Reserved	---- -111
SSPMSK(3)	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1111 1111**
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 1000
CM2CON1	MC1OUT	MC2OUT	C1RSEL	C2RSEL	C1HYS	C2HYS	C1SYNC	C2SYNC	0000 0000
CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 1000
SRCON1	SRSPE	SRSCKE	SRSC2E	SRSC1E	SRRPE	SRRCKE	SRRC2E	SRRC1E	0000 0000
SRCON0	SRLEN	SRCLK2	SRCLK1	SRCLK0	SRQEN	SRNQEN	SRPS	SRPR	0000 0000

Legend: x = unknown, u = unchanged, – = unimplemented, q = value depends on condition

Note 1: The SBOREN bit is only available when the BOREN<1:0> Configuration bits = 01; otherwise it is disabled and reads as '0'. Refer to DS41365, "*PIC18(L)F1XK22 Data Sheet*", Section 21.4 "Brown-out Reset (BOR)" for additional information

2: The RA3 bit is only available when Master Clear Reset is disabled (MCLRE Configuration bit = 0). Otherwise, RA3 reads as '0'. This bit is read-only.

3: Rows highlighted in black show required values for normal LIN protocol applications.

NOTES:

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3.0 I/O PORTS

3.1 PORTB, TRISB and LATB Registers

PORTB is a 4-bit wide, bidirectional port. It functions the same as described in the "PIC18F1XK22/LF1XK22 Data Sheet" (DS41365) with the following differences.

Three bits are dedicated to the LIN transceiver. No pins are associated with this function. Only RB4 is available on a pin. The corresponding data direction register is TRISB. The TRISB bits must be set as '001x 0000'.

The PORTB Data Latch register (LATB) is also memory mapped. Read-modify-write operations on the LATB register read and write the latched output value for PORTB.

EXAMPLE 3-1: INITIALIZING PORTB

```
MOVLW   0C0h    ; set RB6 and RB7
                ; high
MOVWF   PORTB   ; Initialize PORTB by
                ; clearing output
                ; data latches
CLRF    LATB    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   030h    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISB   ; Set RB<7:6> as outputs
                ; and RB<5:4> as inputs
```

.

Note:	On a Power-on Reset, RB<5:4> are configured as analog inputs by default and read as '0'.

REGISTER 3-1: PORTB: PORTB REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	U-0	U-0	U-0	U-0
LINTX	LINCS	LINRX	RB4	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **LINTX**: Dedicated to the LIN Transceiver Transmit Function

bit 6 **LINCS**: Dedicated to the LIN Transceiver Chip Select Function

bit 5 **LINRX**: Dedicated to the LIN Transceiver Receive Function

bit 4 **RB4**: PORTB I/O Pin bit
1 = Port pin is >V_{IH}
0 = Port pin is <V_{IL}

bit 3-0 **Unimplemented**: Read as '0'

REGISTER 3-2: TRISB: PORTB TRI-STATE REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	U-0	U-0	U-0	U-0
TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **TRISB<7:6>:** PORTB Tri-State Control bits
Initialize as 0 = PORTB pin configured as an output

bit 5-4 **TRISB<5:4>:** PORTB Tri-State Control bits
Initialize as 1 = PORTB pin configured as an input (tri-stated)

bit 3-0 **Unimplemented**: Read as ‘0’

REGISTER 3-3: LATB: PORTB DATA LATCH REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	U-0	U-0	U-0	U-0
LATB7	LATB6	LATB5	LATB4	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **LATB7**: Dedicated to the LIN Transceiver Transmit Function

bit 6 **LATB6**: Dedicated to the LIN Transceiver Chip Select Function

bit 5 **LATB5**: Dedicated to the LIN Transceiver Receive Function

bit 4 **LATB4**: RB<7:4> Port I/O Output Latch Register bits

bit 3-0 **Unimplemented**: Read as ‘0’

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REGISTER 3-4: WPUB: WEAK PULL-UP PORTB REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	U-0	U-0	U-0	U-0
WPUB7	WPUB6	WPUB5	WPUB4	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **WPUB<7:4>:** Weak Pull-up Enable bit
1 = Pull-up enabled
0 = Pull-up disabled

bit 3-0 **Unimplemented**: Read as ‘0’

REGISTER 3-5: IOCB: INTERRUPT-ON-CHANGE PORTB REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
IOCB7	IOCB6	IOCB5	IOCB4	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **IOCB<7:4>**: Interrupt-on-Change bits
1 = Interrupt-on-change enabled
0 = Interrupt-on-change disabled

bit 3-0 **Unimplemented**: Read as ‘0’

TABLE 3-1: PORTB I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RB4/AN10/SDI/SDA	RB4	0	O	DIG	LATB<4> data output.
		1	I	TTL	PORTB<4> data input; Programmable weak pull-up.
	AN10	1	I	ANA	ADC input channel 10.
RB5/AN11/RX/DT	RB5	0	O	DIG	LATB<5> data output.
		1	I	TTL	PORTB<5> data input; Programmable weak pull-up.
	RX	1	I	ST	Asynchronous serial receive data input (USART module).
RB6/SCK/SCL	RB6	0	O	DIG	LATB<6> data output.
		1	I	TTL	PORTB<6> data input; Programmable weak pull-up.
RB7/TX/CK	RB7	0	O	DIG	LATB<7> data output.
		1	I	TTL	PORTB<7> data input; Programmable weak pull-up.
	TX	1	O	DIG	Asynchronous serial transmit data output (USART module).

Legend: DIG = Digital level output; TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; x = Don’t care (TRIS bit does not affect port direction or is overridden for this option).

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
ANSELH	—	—	—	—	0	ANS10	0	0	30
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RABIE	TMR0IF	INT0IF	RABIF	—(1)
INTCON2	$\overline{\text{RABPU}}$	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RABIP	—(1)
IOCB	IOCB7	IOCB6	IOCB5	IOCB4					25
LATB	LATB7	LATB6	LATB5	LATB4	—	—	—	—	24
PORTB	LINTX	LINCS	LINRX	RB4	—	—	—	—	23
RCSTA	SPEN	0	0	CREN	0	FERR	OERR	0	38
SLRCON	Reserved								—(1)
SSPCON1	Reserved								—(1)
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	24
TXSTA	0	0	TXEN	0	SENDB	BRGH	TRMT	0	37
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	—	—	—	—	25

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTB.
0 = must always be written as '0' to avoid undefined LIN operation.

Note 1: Information about these registers can be found in the "*PIC18(L)F1XK22 Data Sheet*" (DS41365).

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3.2 PORTC, TRISC and LATC Registers

PORTC is an 8-bit wide, bidirectional port. It functions the same as described in the "PIC18F1XK22/LF1XK22 Data Sheet" (DS41365) with the following differences.

One bit is dedicated to the LIN transceiver and one bit is not available. No pins are associated with this function. Only RC<5:0> are available on pins. The corresponding data direction register is TRISC. The TRISC bits must be set as '1xxx xxxx'.

The PORTC Data Latch register (LATC) is also memory mapped. Read-modify-write operations on the LATC register read and write the latched output value for PORTC.

Note:	On a Power-on Reset, RC<7:6> and RC<3:0> are configured as analog inputs and read as '0'.

EXAMPLE 3-2: INITIALIZING PORTC

```
CLRF    PORTC   ; Initialize PORTC by
                ; clearing output
                ; data latches
CLRF    LATC    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0FFh    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISC   ; Set RC<3:0> as inputs
                ; RC<5:4> as outputs
                ; RC<7:6> as inputs
```

REGISTER 3-6: PORTC: PORTC REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
$\overline{\text{LINRESET}}$	—	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{LINRESET}}$**: LIN Reset Input bit
1 = LIN Reset not asserted
0 = LIN Reset asserted

bit 6 **RC6**: No function

bit 5-0 **RC<5:0>**: PORTC I/O Pin bits
1 = Port pin is > V_{IH}
0 = Port pin is < V_{IL}

REGISTER 3-7: TRISC: PORTC TRI-STATE REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISC7	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **TRISC7:** PORTC Tri-State Control bits
1 = PORTC pin configured as LIN Reset input (tri-stated)
0 = Do not use to avoid internal contention

bit 6 **TRISC6:** Don’t care

bit 5-0 **TRISC<5:0>:** PORTC Tri-State Control bits
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

REGISTER 3-8: LATC: PORTC DATA LATCH REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
$\overline{\text{LINRESET}}$	—	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{LINRESET}}$**: LIN Reset Input bit
1 = LIN Reset not asserted
0 = LIN Reset asserted

bit 6 **LATC6**: No function

bit 5-0 **LATC<5:0>**: RB<7:0> Port I/O Output Latch Register bits

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TABLE 3-3: PORTC I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RC0/AN4/C2IN+	RC0	0	O	DIG	LATC<0> data output.
		1	I	ST	PORTC<0> data input.
	AN4	1	I	ANA	A/D input channel 4.
	C2IN+	1	I	ANA	Comparators C2 non-inverting input.
RC1/AN5/ C12IN1-	RC1	0	O	DIG	LATC<1> data output.
		1	I	ST	PORTC<1> data input.
	AN5	1	I	ANA	A/D input channel 5.
	C12IN1-	1	I	ANA	Comparators C1 and C2 inverting input, channel 1.
RC2/AN6/ C12IN2-/P1D	RC2	0	O	DIG	LATC<2> data output.
		1	I	ST	PORTC<2> data input.
	AN6	1	I	ANA	A/D input channel 6.
	C12IN2-	1	I	ANA	Comparators C1 and C2 inverting input, channel 2.
	P1D	0	O	DIG	ECCP1 Enhanced PWM output, channel D.
RC3/AN7/ C12IN3-/P1C/ PGM	RC3	0	O	DIG	LATC<3> data output.
		1	I	ST	PORTC<3> data input.
	AN7	1	I	ANA	A/D input channel 7.
	C12IN3-	1	I	ANA	Comparators C1 and C2 inverting input, channel 3.
	P1C	0	O	DIG	ECCP1 Enhanced PWM output, channel C.
	PGM	x	I	ST	Single-Supply Programming mode entry (ICSP™). Enabled by LVP Configuration bit; all other pin functions disabled.
RC4/C2OUT/P1B	RC4	0	O	DIG	LATC<4> data output.
		1	I	ST	PORTC<4> data input.
	C2OUT	0	O	DIG	Comparator 2 output.
	P1B	0	O	DIG	ECCP1 Enhanced PWM output, channel B.
RC5/CCP1/P1A	RC5	0	O	DIG	LATC<5> data output.
		1	I	ST	PORTC<5> data input.
	CCP1	0	O	DIG	ECCP1 compare or PWM output.
		1	I	ST	ECCP1 capture input.
	P1A	0	0	DIG	ECCP1 Enhanced PWM output, channel A.
RC6	RC6	unavailable			
RC7	RC7	1	I	ST	PORTC<7> data input.

Legend: DIG = Digital level output; TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

TABLE 3-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	—(1)
ANSELH	—	—	—	—	0	ANS10	0	0	30
CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	—(1)
ECCP1AS	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0	—(1)
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RABIE	TMR0IF	INT0IF	RABIF	—(1)
INTCON2	$\overline{\text{RABPU}}$	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RABIP	—(1)
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF	—(1)
LATC	$\overline{\text{LINRESET}}$	—	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	28
PORTC	$\overline{\text{LINRESET}}$	—	RC5	RC4	RC3	RC2	RC1	RC0	27
PSTRCON	—	—	—	STRSYNC	STRD	STRC	STRB	STRA	—(1)
VREFCON1	D1EN	D1LPS	DAC1OE	---	D1PSS1	D1PSS0	---	D1NSS	—(1)
SLRCON	—	—	—	—	—	Reserved	Reserved	Reserved	—(1)
SSPCON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	—(1)
TRISC	TRISC7	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	28
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	—(1)
T3CON	RD16	—	T3CKPS1	T3CKPS0	T3CCP1	$\overline{\text{T3SYNC}}$	TMR3CS	TMR3ON	—(1)

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTB.

0 = must always be written as '0' to avoid undefined LIN operation.

Note 1: Information about these registers can be found in the "*PIC18(L)F1XK22 Data Sheet" (*DS41365).

3.3 Port Analog Control

REGISTER 3-9: ANSELH: ANALOG SELECT HIGH REGISTER

U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	—	0	ANS10	0	0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **Must be '0'**

bit 2 **ANS10:** RB4 Analog Select Control bit

1 = Digital input buffer of RB4 is disabled
0 = Digital input buffer of RB4 is enabled

bit 1-0 **Must be '0'**

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4.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

4.1 Master SSP (MSSP) Module Overview

The Master Synchronous Serial Port (MSSP) module is not to be used as its operation conflicts with LIN pin functions.

TABLE 4-1: REGISTERS ASSOCIATED WITH MSSP OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
IPR1	—	ADIP	RCIP	TXIP	1	CCP1IP	TMR2IP	TMR1IP	—(1)
PIE1	—	ADIE	RCIE	TXIE	0	CCP1IE	TMR2IE	TMR1IE	—(1)
PIR1	—	ADIF	RCIF	TXIF	0	CCP1IF	TMR2IF	TMR1IF	—(1)
TRISC	TRISC7	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	28
SSPADD	0	0	0	0	0	0	0	0	—(1)
SSPBUF	Don't care								—(1)
SSPCON1	0	0	0	0	0	0	0	0	—(1)
SSPCON2	0	0	0	0	0	0	0	0	—(1)
SSPMSK	1	1	1	1	1	1	1	1	—(1)
SSPSTAT	0	0	0	0	0	0	0	0	—(1)

Legend: Shaded cells are not used by the MSSP in SPI mode.

Register bits shown above must not be changed from their initial values and read as shown.

Note 1: Information about these registers can be found in the "*PIC18(L)F1XK22 Data Sheet*" (DS41365).

NOTES:

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5.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. It functions the same as described in the “PIC18F1XK22/LF1XK22 Data Sheet” (DS41365) with the following differences.

FIGURE 5-1: ADC BLOCK DIAGRAM

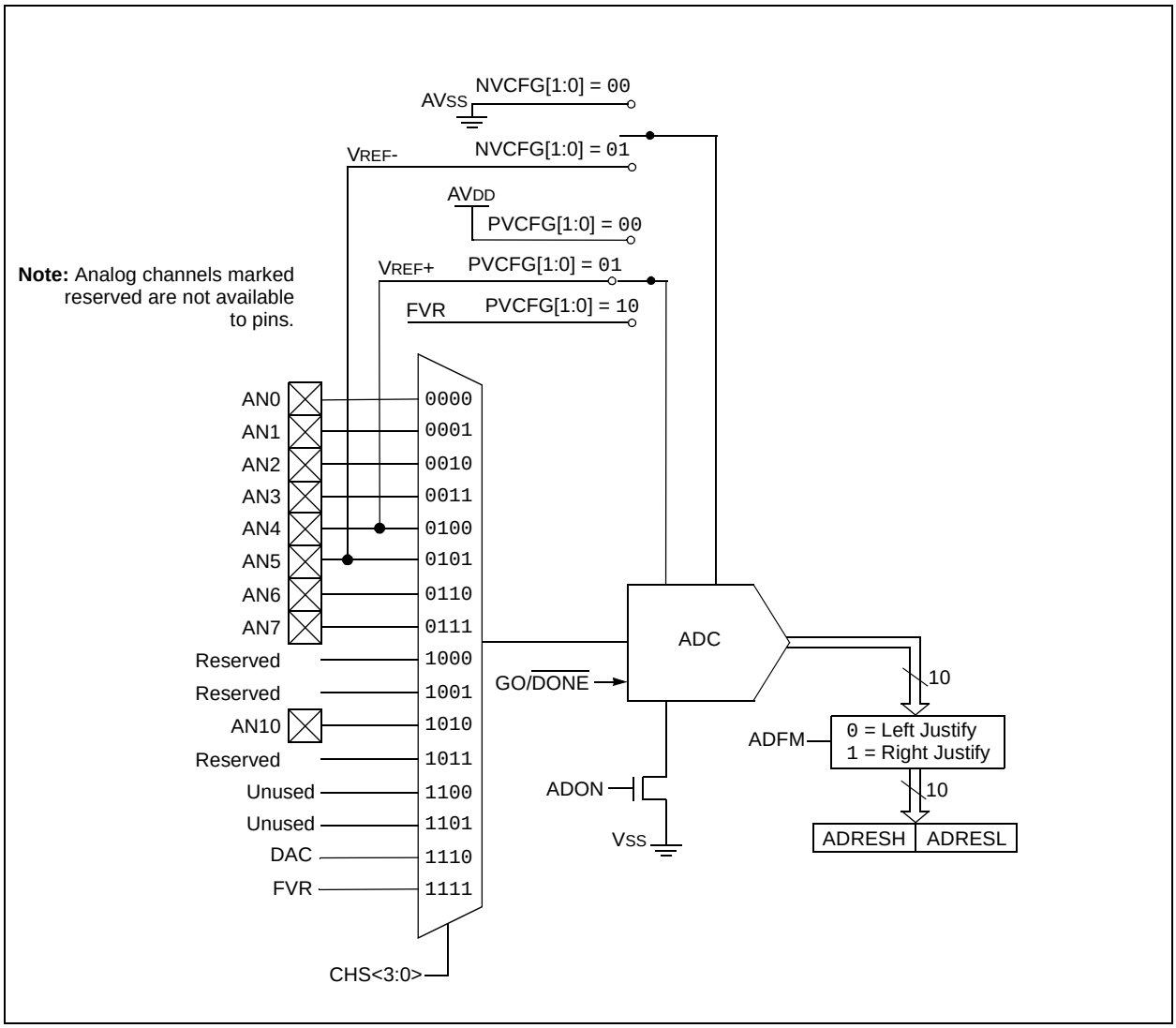


TABLE 5-1: REGISTERS ASSOCIATED WITH A/D OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
ADRESH	A/D Result Register, High Byte								—(1)
ADRESL	A/D Result Register, Low Byte								—(1)
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	—(1)
ADCON1	—	—	—	—	PVCFG1	PVCFG0	NVCFG1	NVCFG0	—(1)
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	—(1)
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	—(1)
ANSELH	—	—	—	—	0	ANS10	0	0	30
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RABIE	TMR0IF	INT0IF	RABIF	—(1)
IPR1	—	ADIP	RCIP	TXIP	1	CCP1IP	TMR2IP	TMR1IP	—(1)
PIE1	—	ADIE	RCIE	TXIE	0	CCP1IE	TMR2IE	TMR1IE	—(1)
PIR1	—	ADIF	RCIF	TXIF	0	CCP1IF	TMR2IF	TMR1IF	—(1)
TRISA	–	–	TRISA5	TRISA4	–	TRISA2	TRISA1	TRISA0	—(1)
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	–	–	–	–	24
TRISC	TRISC7	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	28

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion

0 = must always be written as '0' to avoid undefined LIN operation.

Note 1: Information about these registers can be found in the "*PIC18(L)F1XK22 Data Sheet*" (DS41365).

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6.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It is the same as contained in the standard PIC18F1XK22 (See "PIC18F1XK22/LF1XK22 Data Sheet" (DS41365) with the following exceptions:

- The 9-bit character length and address detection should never be selected
- Synchronous Master or Slave modes are not supported.
- Programmable clock and data polarity should not be used.

6.1 EUSART Asynchronous LIN Transmitter

6.1.1 ASYNCHRONOUS LIN TRANSMISSION SETUP:

1. Initialize the SPBRGH:SPBRG register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Register 6-3).
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. Enable the transmission by setting the TXEN control bit. This will cause the TXIF interrupt bit to be set.
4. If interrupts are desired, set the TXIE interrupt enable bit. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
5. Load 8-bit data into the TXREG register. This will start the transmission.

TABLE 6-1: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
BAUDCON	ABDOVF	RCIDL	0	0	BRG16	—	WUE	ABDEN	39
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RABIE	TMR0IF	INT0IF	RABIF	—(1)
IPR1	—	ADIP	RCIP	TXIP	1	CCP1IP	TMR2IP	TMR1IP	—(1)
PIE1	—	ADIE	RCIE	TXIE	0	CCP1IE	TMR2IE	TMR1IE	—(1)
PIR1	—	ADIF	RCIF	TXIF	0	CCP1IF	TMR2IF	TMR1IF	—(1)
RCSTA	SPEN	0	0	CREN	0	FERR	OERR	0	38
SPBRG	EUSART Baud Rate Generator Register, Low Byte								—(1)
SPBRGH	EUSART Baud Rate Generator Register, High Byte								—(1)
TXREG	EUSART Transmit Register								—(1)
TXSTA	0	0	TXEN	0	SENDB	BRGH	TRMT	0	37

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.
0 = must always be written as '0' to avoid undefined LIN operation.

Note 1: Information about these registers can be found in the "*PIC18(L)F1XK22 Data Sheet*" (DS41365).

6.1.2 EUSART ASYNCHRONOUS LIN RECEIVER

6.1.2.1 Asynchronous Reception Setup:

1. Initialize the SPBRGH:SPBRG register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Register 6-3).
2. Enable the serial port by setting the SPEN bit and the RX/DT pin TRIS bit. The SYNC bit must be clear for asynchronous operation.
3. If interrupts are desired, set the RCIE interrupt enable bit and set the GIE and PEIE bits of the INTCON register.
4. Enable reception by setting the CREN bit.
5. The RCIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
6. Read the RCSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
7. Get the received 8 Least Significant data bits from the receive buffer by reading the RCREG register.
8. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

TABLE 6-2: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
BAUDCON	ABDOVF	RCIDL	0	0	BRG16	—	WUE	ABDEN	39
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RABIE	TMR0IF	INT0IF	RABIF	__(1)
IPR1	—	ADIP	RCIP	TXIP	1	CCP1IP	TMR2IP	TMR1IP	__(1)
PIE1	—	ADIE	RCIE	TXIE	0	CCP1IE	TMR2IE	TMR1IE	__(1)
PIR1	—	ADIF	RCIF	TXIF	0	CCP1IF	TMR2IF	TMR1IF	__(1)
RCREG	EUSART Receive Register								__(1)
RCSTA	SPEN	0	0	CREN	0	FERR	OERR	0	38
SPBRG	EUSART Baud Rate Generator Register, Low Byte								__(1)
SPBRGH	EUSART Baud Rate Generator Register, High Byte								__(1)
TRISC	TRISC7	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	__(1)
TXSTA	0	0	TXEN	0	SENDB	BRGH	TRMT	0	37

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

Note 1: Information about these registers can be found in "*PIC18(L)F1XK22 Data Sheet*" (DS41365).

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REGISTER 6-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0
0	0	TXEN(1)	0	SENDB	BRGH	TRMT	0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Must be '0'**

bit 6 **Must be '0'**

bit 5 **TXEN:** Transmit Enable bit(1)
1 = Transmit enabled
0 = Transmit disabled

bit 4 **Must be '0'**

bit 3 **SENDB:** Send Break Character bit
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed

bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0 **Must be '0'**

Note 1: SREN/CREN overrides TXEN in Sync mode.

REGISTER 6-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	0	0	CREN	0	FERR	OERR	0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **SPEN:** Serial Port Enable bit
1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)
0 = Serial port disabled (held in Reset)

bit 6 **Must be ‘0’**

bit 5 **Don’t care**

bit 4 **CREN:** Continuous Receive Enable bit
1 = Enables receiver
0 = Disables receiver

bit 3 **Must be ‘0’**

bit 2 **FERR:** Framing Error bit
1 = Framing error (can be updated by reading RCREG register and receive next valid byte)
0 = No framing error

bit 1 **OERR:** Overrun Error bit
1 = Overrun error (can be cleared by clearing bit CREN)
0 = No overrun error

bit 0 **Don’t care**

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REGISTER 6-3: BAUDCON: BAUD RATE CONTROL REGISTER

R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	0	0	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **ABDOVF:** Auto-Baud Detect Overflow bit
Asynchronous mode:
1 = Auto-baud timer overflowed
0 = Auto-baud timer did not overflow
Synchronous mode:
Don’t care

bit 6 **RCIDL**: Receive Idle Flag bit
Asynchronous mode:
1 = Receiver is Idle
0 = Start bit has been detected and the receiver is active
Synchronous mode:
Don’t care

bit 5 **Must be ‘0’**

bit 4 **Must be ‘0’**

bit 3 **BRG16:** 16-bit Baud Rate Generator bit
1 = 16-bit Baud Rate Generator is used (SPBRGH:SPBRG)
0 = 8-bit Baud Rate Generator is used (SPBRG)

bit 2 **Unimplemented:** Read as ‘0’

bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
1 = Receiver is waiting for a falling edge. No character will be received but RCIF will be set on the falling edge. WUE will automatically clear on the rising edge.
0 = Receiver is operating normally
Synchronous mode:
Don’t care

bit 0 **ABDEN**: Auto-Baud Detect Enable bit
Asynchronous mode:
1 = Auto-Baud Detect mode is enabled (clears when auto-baud is complete)
0 = Auto-Baud Detect mode is disabled
Synchronous mode:
Don’t care

NOTES:

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7.0 LIN/J2602 TRANSCEIVER AND VOLTAGE REGULATOR

Please refer to “MCP2021/2, LIN Transceiver with Voltage Regulator Data Sheet” (DS22018). Only differences in the PIC18F14K22LIN are noted here.

The LIN/J2602 Transceiver provides a physical interface to a LIN half-duplex bus. It is intended for automotive and industrial applications with serial bus speeds up to 20 Kbaud.

The PIC18F14K22LIN provides a +5V 50 mA regulated power output.

7.1 Pin Descriptions

7.1.1 POWER OUTPUT (V_{REG})

Positive Supply Voltage Regulator Output pin.

7.1.2 GROUND (V_{SS})

Ground pin.

7.1.3 BATTERY (V_{BB})

Battery Positive Supply Voltage pin. This pin is also the input for the Internal Voltage Regulator.

7.1.4 LIN BUS

The bidirectional LIN bus Interface pin is the driver unit for the LIN pin.

7.1.5 $\overline{\text{FAULT}}$/TXE

Fault Detect output and Transmitter Enable input bidirectional pin.

7.2 Internal Connections

7.2.1 TRANSMIT DATA INPUT (TXD)

The Transmit Data Input pin has an internal pull-up to V_{REG}. The LIN pin is low (dominant) when TXD is low. Internally connected to PORTB<7>.

7.2.2 RECEIVE DATA OUTPUT (RXD)

The Receive Data Output pin is a standard CMOS output and follows the state of the LIN pin. It is internally connected to PORTB<5>.

7.2.3 CS/LWAKE

Chip Select Input pin. It is internally connected to PORTB<6>.

7.2.4 $\overline{\text{RESET}}$

$\overline{\text{RESET}}$ is an open-drain output. It is internally connected to PORTC<7>.

NOTES:

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8.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

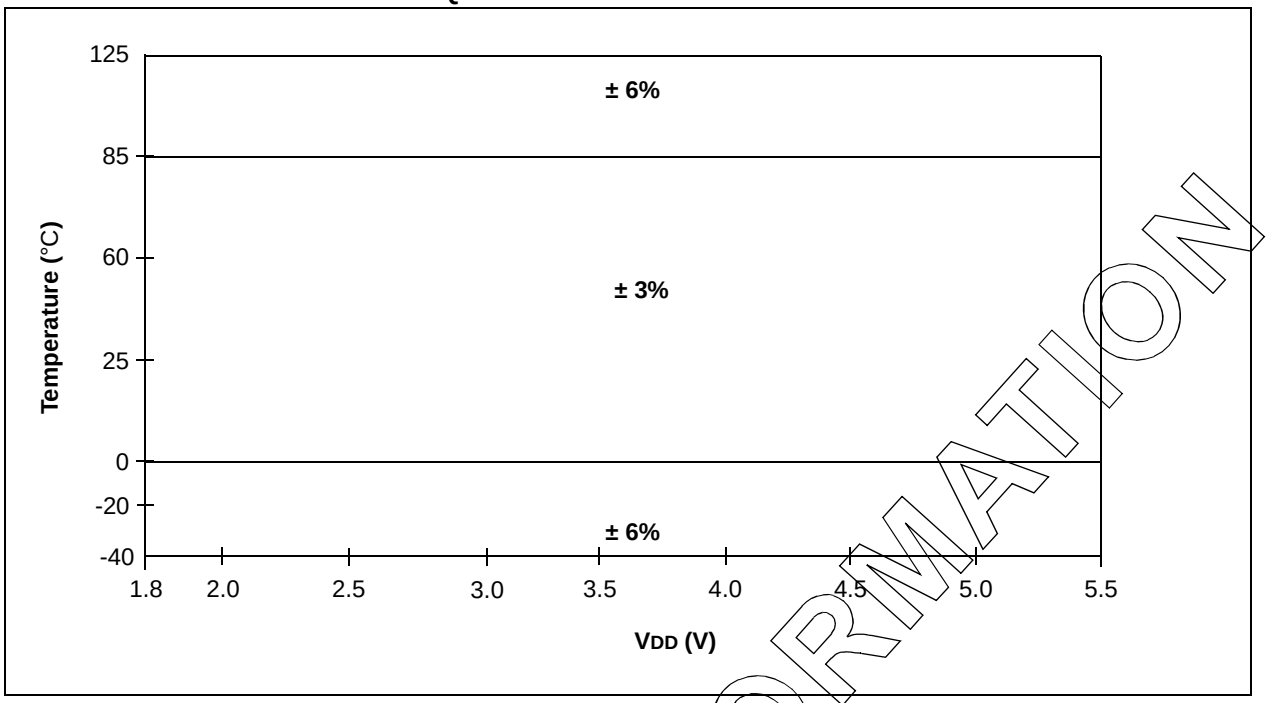
Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS}, PIC18F1XK22 ..... -0.3V to +6.0V
Voltage on V_{DD} with respect to V_{SS}, PIC18LF1XK22 ..... -0.3V to +4.0V
Voltage on $\overline{MCLR}$ with respect to V_{SS} ..... -0.3V to +9.0V
Voltage on all other pins with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V
Total power dissipation(1) ..... 800 mW
Maximum current out of V_{SS} pin ..... 95 mA
Maximum current into V_{DD} pin ..... 95 mA
Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD}) ..... ± 20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by all ports ..... 90 mA
Maximum current sourced by all ports ..... 90 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

ADVANCE INFORMATION

FIGURE 8-1: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



8.1 DC Characteristics: RC Run Supply Current, PIC18F14K22LIN

PIC18F14K22LIN		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device Characteristics**	**Typ.**	**Max.**	**Units**	**Conditions**		
D008		15.5	19.5	µA	-40°C	VDD = 5.0V	FOSC = 31 kHz(4) (**RC_RUN** mode, LFINTOSC source)
		16.5	20.5	µA	+25°C		
		20.5	29.5	µA	+85°C		
		30.5	35.5	µA	+125°C		
D009		0.98	0.98	mA	-40°C TO +125°C	VDD = 5.0V	FOSC = 1 MHz (**RC_RUN** mode, HFINTOSC source)
D010		4.0	4.7	mA	-40°C TO +125°C	VDD = 5.0V	FOSC = 16 MHz (**RC_RUN** mode, HF-INTOSC source)

* These parameters are characterized but not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

4: FVR and BOR are disabled.

5: When a single temperature range is provided for a parameter, the specification applies to both industrial and extended temperature devices.

ADVANCE INFORMATION

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8.2 DC Characteristics: RC Idle Supply Current, PIC18F14K22LIN

PIC18F14K22LIN		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
D011		8.5	12.5	µA	-40°C	VDD = 5.0V	FOSC = 31 kHz(4) (**RC_IDLE** mode, LFINTOSC source)
		9.5	14.5	µA	+25°C		
		13.5	24.5	µA	+85°C		
		24.5	30.5	µA	+125°C		
D012		630	780	µA	-40°C to +125°C	VDD = 5.0V	FOSC = 1 MHz (**RC_IDLE** mode, HF-INTOSC source)
D013		1.8	2.2	mA	-40°C to +125°C	VDD = 5.0V	FOSC = 16 MHz (**RC_IDLE** mode, HF-INTOSC source)

* These parameters are characterized but not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

4: FVR and BOR are disabled.

5: When a single temperature range is provided for a parameter, the specification applies to both industrial and extended temperature devices.

ADVANCE INFORMATION

8.3 DC Characteristics: Primary Run Supply Current, PIC18F14K22LIN

PIC18F14K22LIN		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device Characteristics**	**Typ.**	**Max.**	**Units**	**Conditions**		
D014		.30	.42	mA	-40°C to +125°C	VDD = 5.0V	FOSC = 1 MHz (**PRI_RUN**, EC Med Osc)
D015		3.9	4.4	mA	-40°C to +125°C	VDD = 5.0V	FOSC = 16 MHz (**PRI_RUN**, EC High Osc)
D016		12.1	14.6	mA	-40°C to +125°C	VDD = 5.0V	FOSC = 64 MHz (**PRI_RUN**, EC High Osc)
D017		3.8	4.8	mA	-40°C to +125°C	VDD = 5.0V	FOSC = 4 MHz 16 MHz Internal (**PRI_RUN HS+PLL**)
D018		12.6	15.6	mA	-40°C to +125°C	VDD = 5.0V	FOSC = 16 MHz 64 MHz Internal (**PRI_RUN HS+PLL**)

* These parameters are characterized but not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

4: FVR and BOR are disabled.

5: When a single temperature range is provided for a parameter, the specification applies to both industrial and extended temperature devices.

ADVANCE INFORMATION

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8.4 DC Characteristics: Primary Idle Supply Current, PIC18F14K22LIN

PIC18F14K22LIN		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device Characteristics**	**Typ.**	**Max.**	**Units**	**Conditions**		
D019		420	455	μA	-40°C to +125°C	VDD = 5.0V	FOSC = 1 MHz (**PRI_IDLE** mode, EC Med Osc)
D020		4.0	4.2	mA	-40°C to +125°C	VDD = 5.0V	FOSC = 16 MHz (**PRI_IDLE**mode, EC High Osc)
D021		5.3	6.3	mA	-40°C to +125°C	VDD = 5.0V	FOSC = 64 MHz (**PRI_IDLE**mode, EC High Osc)

* These parameters are characterized but not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

4: FVR and BOR are disabled.

5: When a single temperature range is provided for a parameter, the specification applies to both industrial and extended temperature devices.

8.5 DC Characteristics: Secondary Run Supply Current, PIC18F14K22LIN

PIC18F14K22LIN		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device Characteristics**	**Typ.**	**Max.**	**Units**	**Conditions**		
D022		15.5	19.5	μA	-40°C	VDD = 5.0V	FOSC = 32 kHz(3) (**SEC_RUN** mode, Timer1 as clock)
		16.5	20.5	μA	+25°C		
		20.5	29.5	μA	+85°C		
		30.5	35.5	μA	+125°C		

* These parameters are characterized but not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

4: FVR and BOR are disabled.

ADVANCE INFORMATION

8.6 DC Characteristics: Secondary Idle Supply Current, PIC18F14K22LIN

PIC18F14K22LIN		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device Characteristics**	**Typ.**	**Max.**	**Units**	**Conditions**		
D023		8.5	12.5	µA	-40°C	VDD = 5.0V	FOSC = 32 kHz(3) (**SEC_IDLE** mode, Timer1 as clock)
		9.5	14.5	µA	+25°C		
		13.5	24.5	µA	+85°C		
		24.5	30.5	µA	+125°C		

* These parameters are characterized but not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

4: FVR and BOR are disabled.

8.7 Thermal Considerations

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C					
Param No.	**Sym.**	**Characteristic**	**Typ.**	**Units**	**Conditions**
TH01	θJA	Thermal Resistance Junction to Ambient	108.1	°C/W	20-pin SSOP package
TH02	θJC	Thermal Resistance Junction to Case	24	°C/W	20-pin SSOP package
TH03	TJMAX	Maximum Junction Temperature	150	°C	
TH04	PD	Power Dissipation	—	W	PD = PINTERNAL + PI/O
TH05	PINTERNAL	Internal Power Dissipation	—	W	PINTERNAL = IDD x VDD(1)
TH06	PI/O	I/O Power Dissipation	—	W	PI/O = Σ (IOL * VOL) + Σ (IOH * (VDD - VOH))
TH07	PDER	Derated Power	—	W	PDER = PDMAX (TJ - TA)/θJA(2)

Legend: TBD = To Be Determined

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature.

3: TJ = Junction Temperature.

ADVANCE INFORMATION

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9.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Graphs and tables are not available at this time.

NOTES:

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10.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C for Various Device Families
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICkit™ 3 Debug Express
- Device Programmers
  - PICkit™ 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

10.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

10.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

10.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

10.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

10.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

10.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

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10.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

10.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

10.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

10.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

10.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

10.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

10.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

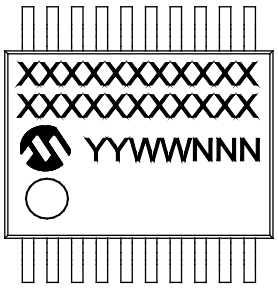
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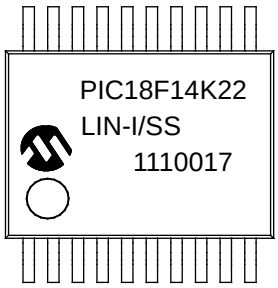
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

20-Lead SSOP (5.30 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

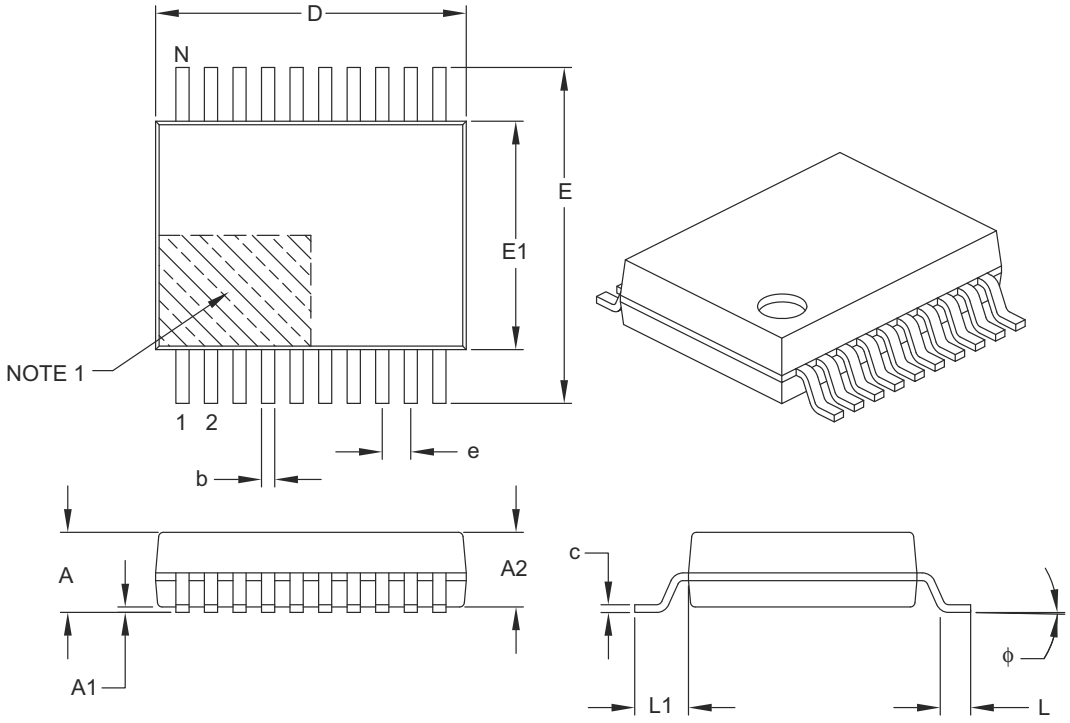
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

11.2 Package Details

The following section give the technical details of the package.

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

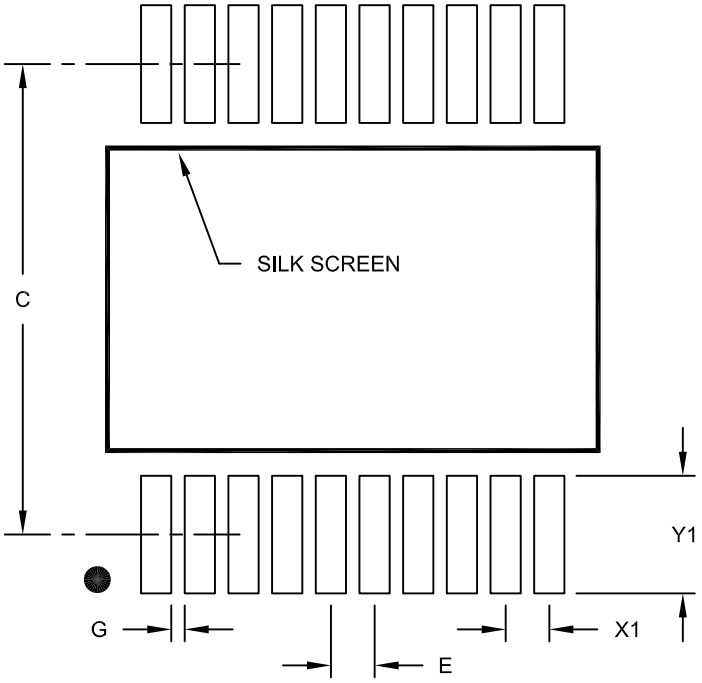
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

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20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (April 2011)

Initial release of this document.

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Device: PIC18F14K22LIN Literature Number: DS41580A

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC18F14K22LIN[(1)]
Temperature Range:	E = -40°C to +125°C (Extended)
Package:	SS = SSOP
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC18F14K22LIN-500E/SS 301 = 5.0V Voltage Regulator, Extended temp., SSOP package, Extended V_{DD} limits, QTP pattern #301.

Note 1: T = in tape and reel SSOP Package only.

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