NCP1215A

Low Cost Variable OFF Time Switched Mode Power Supply Controller

The NCP1215A is a controller for low power off−line flyback Switched Mode Power Supplies (SMPS) featuring low size, weight and cost constraints together with a good low standby power performance. The operating principle uses switching frequency reduction at light load by increasing the OFF Time. Also, when OFF Time expands, the peak current is gradually reduced down to approximately 1/4 of the maximum peak current to prevent from exciting the transformer mechanical resonances. The risk of acoustic noise is thus greatly diminished while keeping good standby power performance.

A low power internal supply block also ensures very low current consumption at startup without hampering the standby power performance.

A special primary current sensing technique minimizes the impact of SMPS switching on control IC operation. The choice of peak voltage across the current sense resistor allows dissipation to be further reduced. The negative current sensing technique offers advantages over a traditional approach by avoiding the voltage drop incurred by traditional MOSFET source sensing. Thus, the IC drive capability is greatly improved.

Finally, the bulk input ripple ensures a natural frequency dithering which smooths the EMI signature.

Features

- Variable OFF Time Control Method
- Very Low Current Consumption at Startup
- Natural Frequency Dithering for Improved EMI Signature
- Current Mode Control Operation
- Peak Current Compression Reduces Transformer Noise
- Programmable Current Sense Resistor Peak Voltage
- Undervoltage Lockout
- Pb−Free Packages are Available

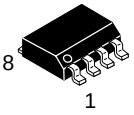
Typical Applications

- Auxiliary Power Supply
- Standby Power Supply
- AC−DC Adapter
- Off−line Battery Charger

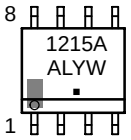
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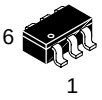
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MARKING DIAGRAM

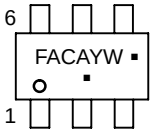


SOIC−8
D SUFFIX
CASE 751





TSOP−6
(SOT23−6, SC59−6)
SN SUFFIX
CASE 318G

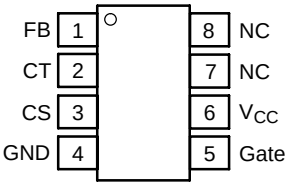


FAC	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

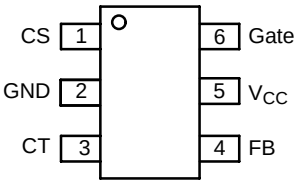
PIN CONNECTIONS

SOIC−8



(Top View)

TSOP−6

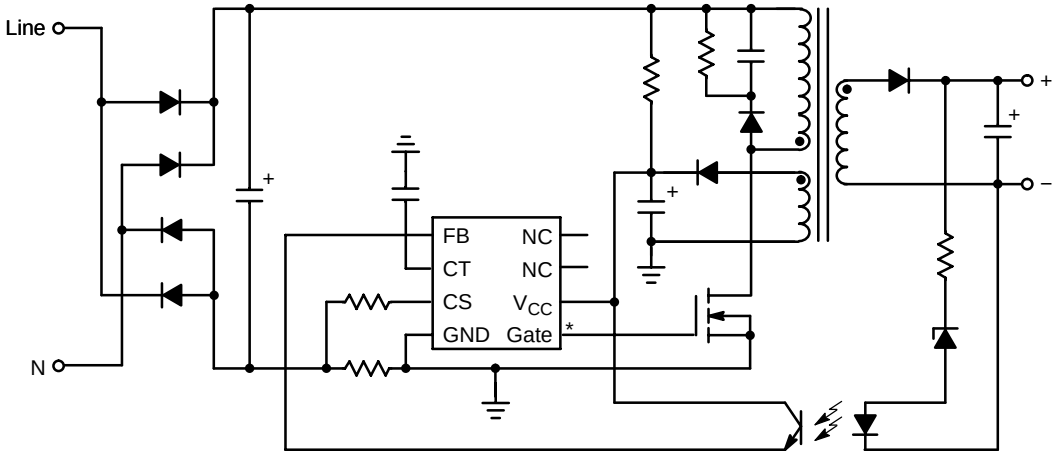


(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

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*If your application requires a gate−source resistor, please refer to design guidelines in this document.

Figure 1. Typical Application

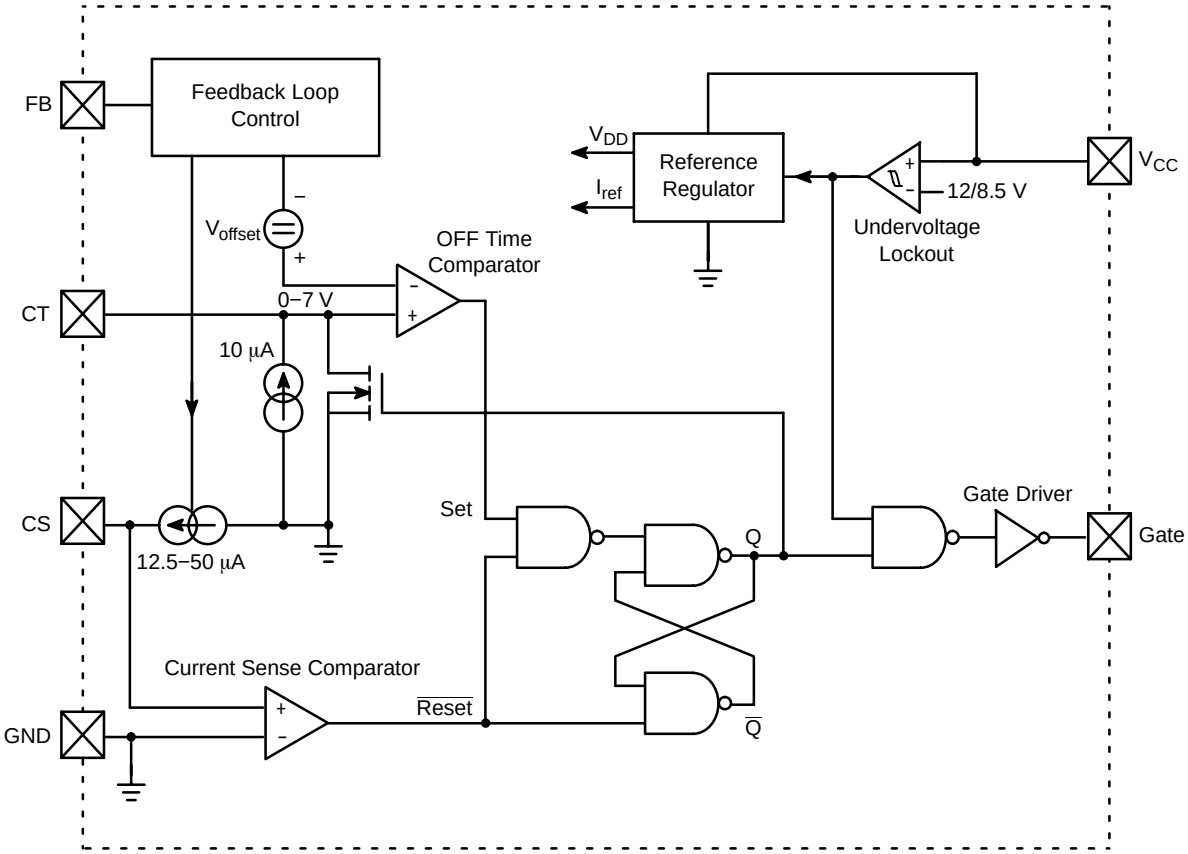


Figure 2. Representative Block Diagram

PIN FUNCTION DESCRIPTION

TSOP−6	SO−8	Symbol	Description
4	1	FB	The FB pin provides voltage feedback loop. The current injected into the pin determines the primary switch OFF time interval. It also influences the peak value of the primary current.
3	2	CT	Connection for an external timing programming capacitor.
1	3	CS	The CS pin senses the power switch current.
2	4	GND	Primary and internal ground.
6	5	Gate	Output drive for an external power MOSFET.
5	6	V_{CC}	Power supply voltage and Undervoltage Lockout.
7	7	NC	Unconnected pin.
8	8	NC	Unconnected pin.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
FB Pins Voltage Range	V_{FB}	−0.3 to 18	V
CS and CT Pin Voltage Range	V_{in}	−0.3 to 10	V
Thermal Resistance, Junction−to−Air (SOIC−8 Version)	$R_{\theta JA}$	178	°C/W
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
ESD Voltage Protection, Human Body Model (HBM)	$V_{ESD-HBM}$	2.0	kV
ESD Voltage Protection, Machine Model (MM)	V_{ESD-MM}	200	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
NCP1215ADR2	SOIC−8	2500 Units / Reel
NCP1215ADR2G	SOIC−8 (Pb−Free)	2500 Units / Reel
NCP1215ASNT1	TSOP−6	3000 Units / Reel
NCP1215ASNT1G	TSOP−6 (Pb−Free)	3000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_J = 25°C, for min/max values T_J = 0°C to +105°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE FEEDBACK					
Offset Voltage	V_{offset}	1.05	1.19	1.34	V
Maximum CT Pin Voltage at FB Current = 25 μA (Including V_{offset})	$V_{CT-25\mu A}$	2.4	3.1	4.3	V
Maximum CT Pin Voltage at FB Current = 50 μA (Including V_{offset})	$V_{CT-50\mu A}$	3.6	4.6	6.2	V
CT PIN − OFF TIME CONTROL					
Source Current (CT Pin Grounded)	I_{CT}	8.0	9.8	11.5	μA
Source Current Maximum Voltage Capability	V_{CT-max}	−	6.5	−	V
Minimum CT Pin Voltage (Pin Unloaded, Discharge Switch Turned On)	V_{CT-min}	−	−	20	mV
CURRENT SENSE					
Minimum Source Current (I_{FB} = 180 μA, CT Pin Grounded)	I_{CS-min}	8.0	12.5	16	μA
Maximum Source Current (I_{FB} = 0 μA, CT Pin Grounded)	I_{CS-max}	40	49	58	μA
Comparator Threshold Voltage	V_{th}	15	42	80	mV
Propagation Delay (CS Falling Edge to Gate Output)	t_{delay}	−	215	310	ns
GATE DRIVE					
Sink Resistance (I_{sink} = 30 mA)	R_{OL}	25	40	90	Ω
Source Resistance (I_{source} = 30 mA)	R_{OH}	55	80	130	Ω
POWER SUPPLY					
V_{CC} Startup Voltage	$V_{startup}$	−	12.5	14.2	V
Undervoltage Lockout Threshold Voltage	V_{UVLO}	7.2	9.0	−	V
Hysteresis ($V_{startup}$ − V_{UVLO})	V_{hys}	2.2	3.5	−	V
V_{CC} Startup Current Consumption (V_{CC} = 8.0 V)	$I_{CC-start}$	−	2.8	6.5	μA
V_{CC} Steady State Current Consumption (C_{GATE} = 1.0 nF, f_{SW} = 100 kHz, FB open)	I_{CC-SW}	0.55	0.9	1.75	mA

TYPICAL CHARACTERISTICS

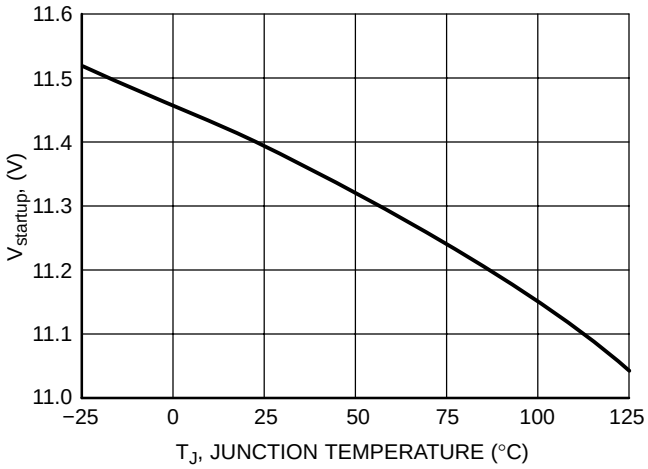


Figure 3. $V_{startup}$ Threshold vs. Junction Temperature

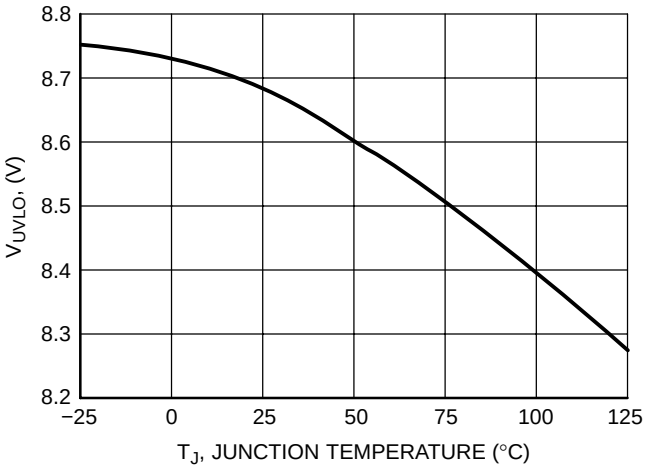


Figure 4. V_{UVLO} Threshold vs. Junction Temperature

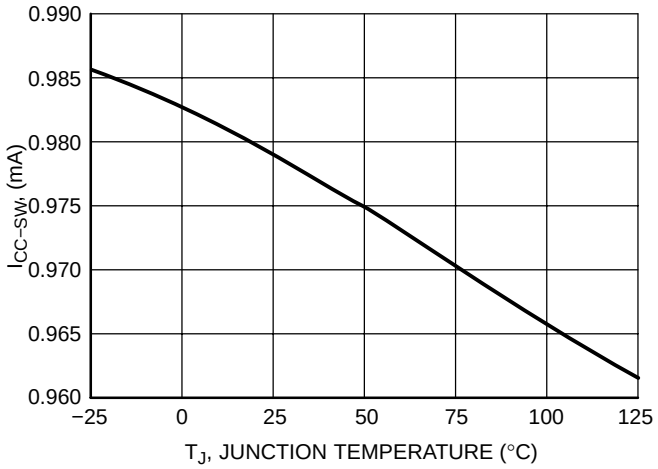


Figure 5. Operating Current Consumption vs. Junction Temperature

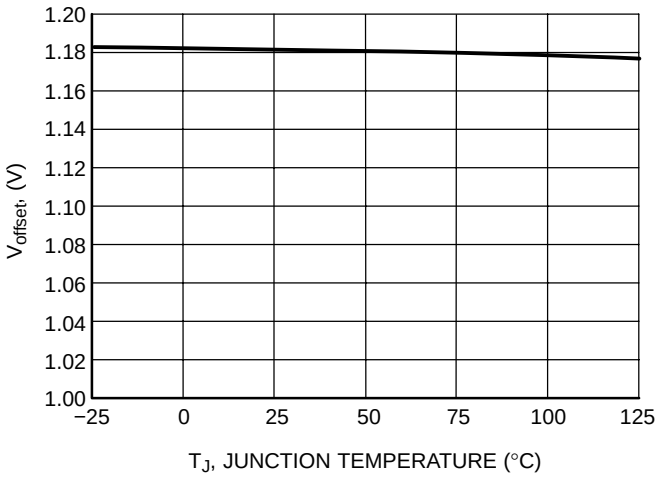


Figure 6. Offset Voltage vs. Junction Temperature

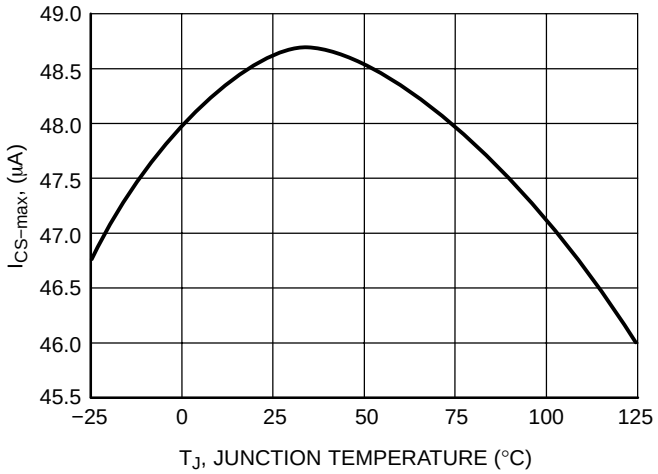


Figure 7. Current Sense Source Current vs. Junction Temperature

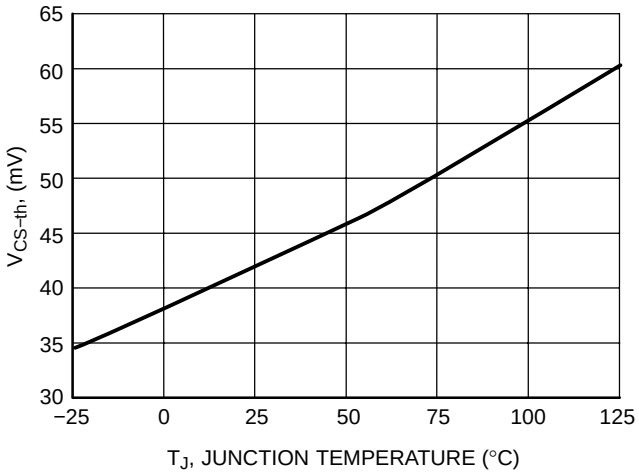


Figure 8. Current Sense Threshold vs. Junction Temperature

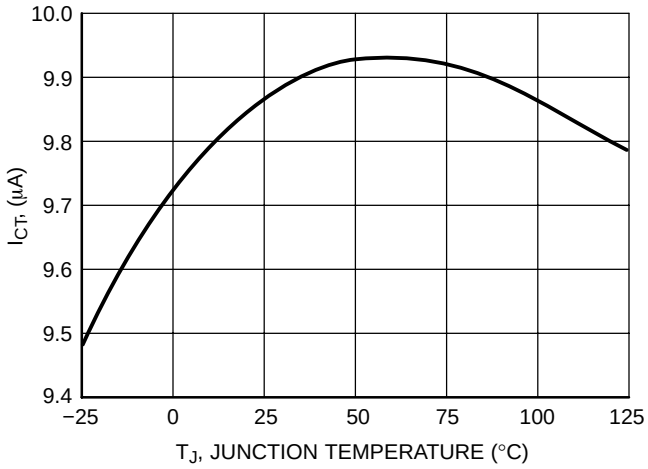


Figure 9. CT Pin Source Current vs. Junction Temperature

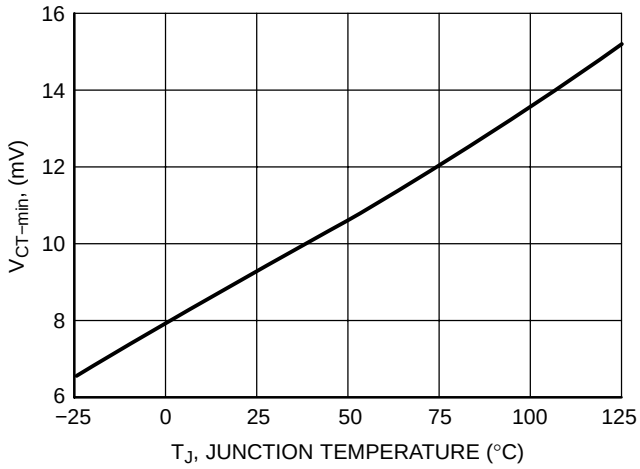


Figure 10. CT Pin Threshold vs. Junction Temperature

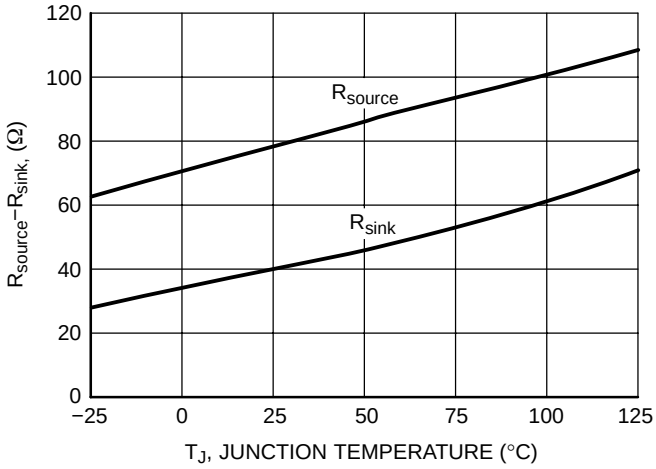


Figure 11. Drive Sink and Source Resistance vs. Junction Temperature

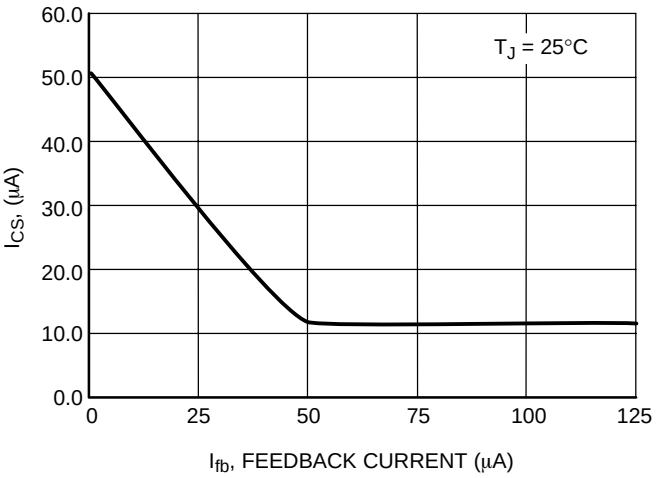


Figure 12. Current Sense Source Current vs. Feedback Current

APPLICATION INFORMATION

The NCP1215A implements a current mode SMPS with a variable OFF time dependant upon output power demand. It can be seen from the typical application that NCP1215A is designed to operate with a minimum number of external component. The NCP1215A incorporates the following features:

- **Frequency Foldback:** Since the switch−off time increases when power demand decreases, the switching frequency naturally diminishes in light load conditions. This helps to minimize switching losses and offers excellent standby power performance.
- **Very Low Startup Current:** The patented internal supply block is specially designed to offer a very low current consumption during startup. It allows the use of a very high value external startup resistor, greatly reducing dissipation, improving efficiency and minimizing standby power consumption.
- **Natural Frequency Dithering:** The quasi−fixed t_{on} mode of operation improves the EMI signature since the switching frequency varies with the natural bulk ripple voltage.
- **Peak Current Compression:** As the load becomes lighter, the frequency decreases and can enter the audible range. To avoid exciting transformer mechanical resonances, hence generating acoustic noise, the NCP1215A includes a patented technique, which reduces the peak current as power goes down. As such, inexpensive transformer can be used without having noise problems.
- **Negative Primary Current Sensing:** By sensing the total current, this technique does not modify the MOSFET driving voltage (Vgs) while switching. Furthermore, the programming resistor together with the pin capacitance, forms a residual noise filter which blanks spurious spikes. Also fixing primary current level to a maximum value sets the maximum power limit.
- **Programmable Primary Current Sense:** It offers a second peak current adjustment variable which improves the design flexibility.
- **Secondary or Primary Regulation:** The feedback loop arrangement allows simple secondary or primary side regulation without significant additional external components.

A detailed description of each internal block within the IC is given in the following text.

Feedback Loop Control

The main task of the Feedback Loop Block is to control the SMPS output voltage through the change of primary switch OFF time interval. It sets the peak voltage of the timing capacitor, which varies upon the output power demand. Figure 13 shows the simplified internal schematic:

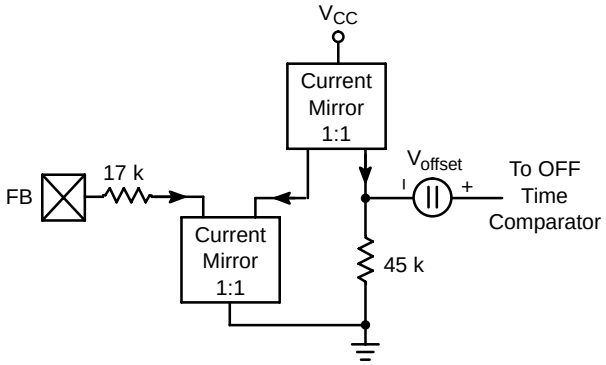


Figure 13. Feedback Loop − OFF Time Control

The voltage feedback signal is sensed as a current injected through the FB pin.

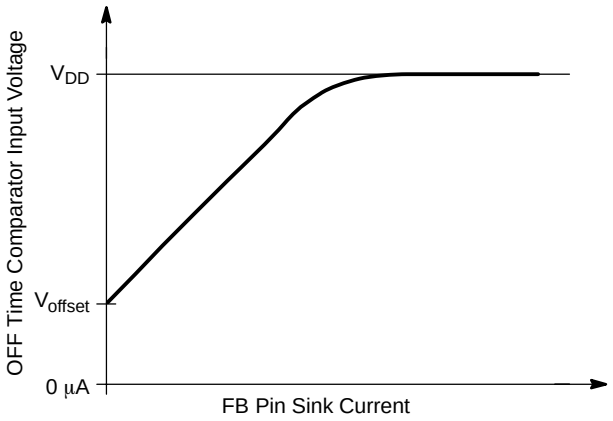


Figure 14. FB Loop Transfer Characteristic

The transfer characteristic (output voltage to input current) of the feedback loop control block can be seen in Figure 14. V_{DD} refers to the internal stabilized supply whereas the offset value sets the maximum switching frequency in lack of optocoupler current (e.g. an output short−circuit).

To keep the switching frequency above the audio range in light load condition the FB pin also regulates in certain range the peak primary current. The corresponding block diagram can be seen from Figure 15.

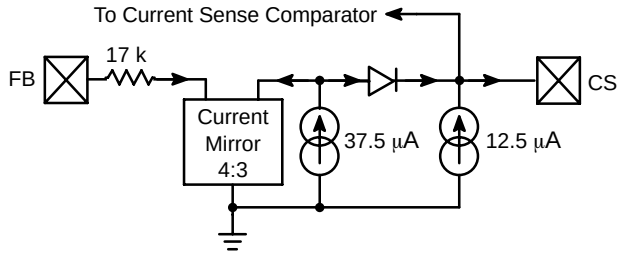


Figure 15. Feedback Loop − Current Sense Control

The resulting current sense regulation characteristic can be seen from Figure 16.

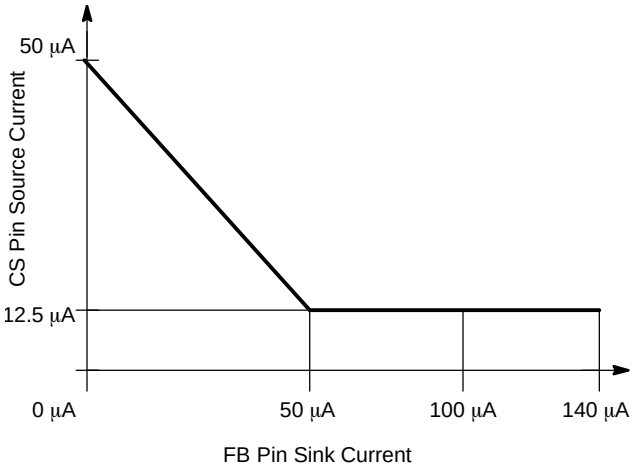


Figure 16. Current Sense Regulation Characteristic

When the load goes light, the compression circuitry decreases the peak current. This has the effect of slightly increasing the switching frequency but the compression ratio is selected to not hamper the standby power.

OFF Time Control

The loop signal together with the internal current source, via an external capacitor, controls the switch−off time. This is portrayed in Figure 17.

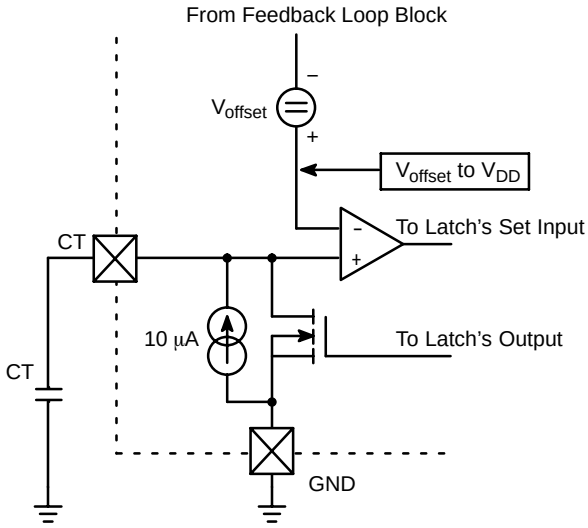


Figure 17. OFF Time Control

During the switch−ON time, the CT capacitor is kept discharged by a MOSFET switch. As soon as the latch output changes to a low state, the voltage across CT created by the internal current source, starts to ramp−up until its value reaches the threshold given by the feedback loop demand.

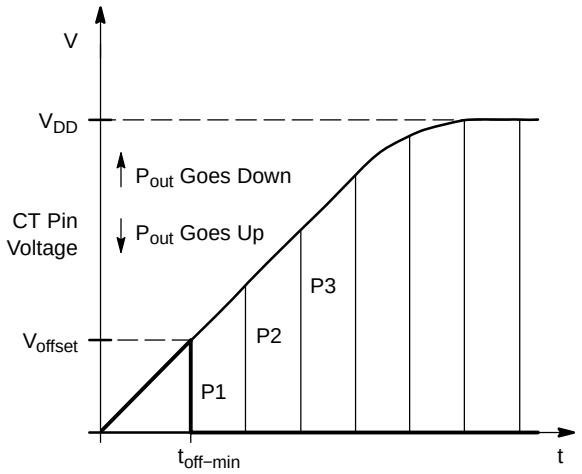


Figure 18. CT Pin Voltage ($P_{out1} > P_{out2} > P_{out3}$)

The voltage that can be observed on CT pin is shown in Figure 18. The **bold** waveform shows the maximum output power when the OFF time is at its minimum. The IC allows an OFF time of several seconds.

Primary Current Sensing

The primary current sensing circuit is shown in Figure 19.

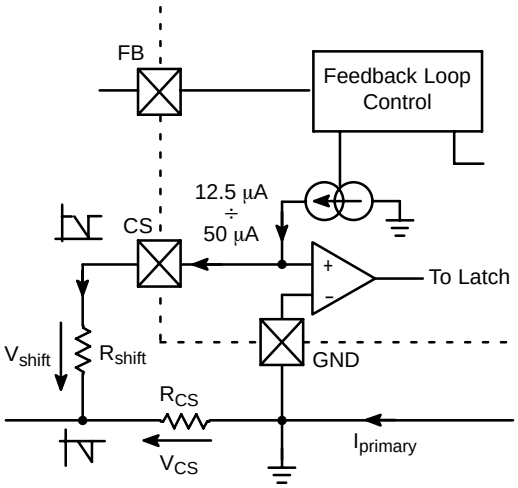


Figure 19. Primary Current Sensing

When the primary switch is ON, the transformer current flows through the sense resistor R_{cs}. The current creates a voltage, V_{cs} which is negative with respect to GND. Since the comparator connected to CS pin requires a positive voltage, the voltage V_{shift} is developed across the resistor R_{shift} by a current source which level−shifts the negative voltage V_{cs}. The level−shift current is in range from 12.5 to 50 μA depending on the Feedback Loop Control block signal (see more details in the Feedback Loop Control section).

The peak primary current is thus equal to:

$$I_{pk} = \frac{R_{shift}}{R_{CS}} \cdot I_{CS} \qquad \text{(eq. 1)}$$

A typical CS pin voltage waveform is shown in Figure 20.

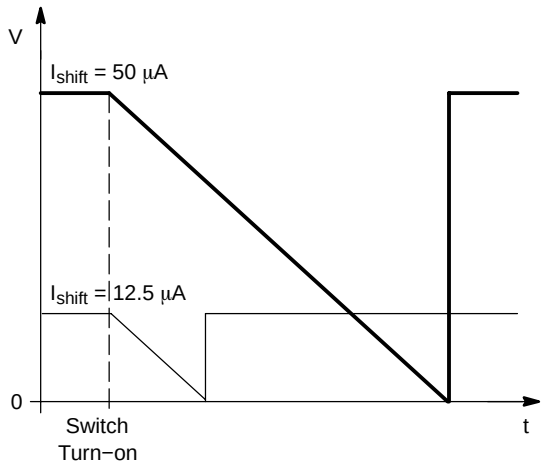


Figure 20. CS Pin Voltage

Figure 20 also shows the effect of the inductor current of differing output power demand.

The primary current sensing method we described, brings the following benefits compared to the traditional approach:

- Maximum peak voltage across the current sense resistor is determined and can be optimized by the value of the shift resistor.
- CS pin is not exposed to negative voltage, which could induce a parasitic substrate current within the IC and distort the surrounding internal circuitry.
- The gate drive capability is improved because the current sense resistor is located out of the gate driver loop and does not deteriorate the turn−on and also turn−off gate drive amplitude.

Gate Driver

The Gate Driver consists of a CMOS buffer designed to directly drive a power MOSFET.

It features an unbalanced source and sink capabilities to optimize turn ON and OFF performance without additional external components. Since the power MOSFET turns off at high drain current, to minimize its turn−off losses the sink capability of the gate driver is increased for a faster turn−off. To the opposite, the source capability is lower to slow−down power MOSFET at turn−on in order to reduce the EMI noise.

Whenever the IC supply voltage is lower than the undervoltage threshold, the Gate Driver is low, pulling down the gate to ground. It eliminates the need for an external resistor.

Startup Circuit

An external startup resistor is connected between high voltage potential of the input bulk capacitor and V_{CC} supply capacitor. The value of the resistor can be calculated as follows:

$$R_{startup} = \frac{V_{bulk} - V_{startup}}{I_{startup}} \qquad \text{(eq. 2)}$$

Where:

$V_{startup}$	V_{CC} voltage at which IC starts operation (see spec.)
$I_{startup}$	Startup current
V_{bulk}	Input bulk capacitor's voltage

Since the V_{bulk} voltage has obviously much higher value than $V_{startup}$ the equation can be simplified in the following way:

$$R_{startup} = \frac{V_{bulk}}{I_{startup}} \qquad \text{(eq. 3)}$$

The startup current can be calculated as follows:

$$I_{startup} = C_{Vcc} \frac{V_{startup}}{t_{startup}} + I_{CC-start} \qquad \text{(eq. 4)}$$

Where:

C_{Vcc}	V_{CC} capacitor value
$t_{startup}$	Startup time
$I_{CC-start}$	IC current consumption (see spec.)

If the IC current consumption is assumed constant during the startup phase, one can obtain resulting equation for startup resistor calculation:

$$R_{startup} = \frac{V_{bulk}}{C_{Vcc}\frac{V_{startup}}{t_{startup}} + I_{CC-start}} \quad \text{(eq. 5)}$$

Switching Frequency

The switching frequency varies with the output load and input voltage. The highest frequency appears at highest input voltage and maximum output power.

Since the peak primary current is fixed, the on time portion of the switching period can be calculated:

$$t_{on} = L_p \frac{I_{pk}}{V_{bulk}} \quad \text{(eq. 6)}$$

Where:

L_p Transformer primary inductance

I_{pk} Peak primary current

Using equation for peak primary current estimation the switch−on time is:

$$t_{on} = L_p \frac{R_{shift}}{R_{cs} \cdot V_{bulk}} 50 \cdot 10^{-6} \quad \text{(eq. 7)}$$

Minimum switch−on time occurs at maximum input voltage:

$$t_{on-min} = L_p \frac{R_{shift}}{R_{cs} \cdot V_{bulk-max}} 50 \cdot 10^{-6} \quad \text{(eq. 8)}$$

As it can be seen from the above equation, the switch−on time linearly depends on the input bulk capacitor voltage. Since this voltage has ripple due to AC input voltage and input rectifier, it allows natural frequency dithering to improve EMI signature of the SMPS.

The switch−off time is determined by the charge of an external capacitor connected to the CT pin. The minimum t_{off} value can be computed by:

$$t_{off-min} = C_T \frac{V_{offset}}{I_{CT}} = C_T \frac{1.2}{10^{-5}} = 0.12 \cdot 10^6 C_T \quad \text{(eq. 9)}$$

Where:

V_{offset} Offset voltage (see spec.)

I_{CT} CT pin source current (see spec.)

The maximum switching frequency then can be evaluated by:

$$f_{sw-max} = \frac{1}{t_{on-min} + t_{off-min}} = \frac{1}{\frac{L_p \cdot R_{shift}}{V_{bulk} \cdot R_{cs}} \cdot 50 \cdot 10^{-6} + 0.12 \cdot 10^6 \cdot C_T} \quad \text{(eq. 10)}$$

As output power diminishes, the switching frequency decreases because the switch−off time prolongs upon feedback loop. The range of the frequency change is sufficient to keep output voltage regulation in any light load condition.

Application Design Example

An example of the typical wall adapter application is described hereafter.

As a wall adapter it should be able to operate properly with wide range of the input voltage from 90 VAC up to 265 VAC. The bulk capacitor voltage then can be calculated:

$$V_{bulk-min} = V_{AC-min}\sqrt{2} = 90 \cdot \sqrt{2} = 127 \text{ VDC} \quad \text{(eq. 11)}$$

$$V_{bulk-max} = V_{AC-max}\sqrt{2} = 265 \cdot \sqrt{2} = 375 \text{ VDC} \quad \text{(eq. 12)}$$

The requested output power is 5.2 Watts.

Assuming 80% efficiency the input power is equal to:

$$P_{in} = \frac{P_{out}}{\eta} = \frac{5.2}{0.8} = 6.5 \text{ W} \quad \text{(eq. 13)}$$

The average value of input current at minimum input voltage is:

$$I_{in-avg} = \frac{P_{in}}{V_{bulk-min}} = \frac{6.5}{127} = 51.2 \text{ mA} \quad \text{(eq. 14)}$$

The suitable reflected primary winding voltage for 600 V rated MOSFET switch is:

$$V_{flbk} = 600 \text{ V} - V_{bulk-max} - V_{spike} = 600 - 375 - 100 = 125 \text{ V} \quad \text{(eq. 15)}$$

Using calculated flyback voltage the maximum duty cycle can be calculated:

$$\delta_{max} = \frac{V_{flbk}}{V_{flbk} + V_{bulk-min}} = \frac{125}{125 + 127} = 0.496 = 0.5 \quad \text{(eq. 16)}$$

Following equation determines peak primary current:

$$I_{ppk} = \frac{2 \cdot I_{in-avg}}{\delta_{max}} = \frac{2 \cdot 51.2 \cdot 10^{-3}}{0.5} = 204.7 \text{ mA} \quad \text{(eq. 17)}$$

The desired maximum switching frequency at minimum input voltage is 75 kHz.

The highest switching frequency occurs at the highest input voltage and its value can be estimated as follows:

$$f_{max-high} = f_{max-low} \frac{V_{bulk-max}}{V_{bulk-min}} \delta_{max} = 75 \cdot 10^3 \frac{375}{127} 0.5 = 110.7 \text{ kHz} \quad \text{(eq. 18)}$$

This frequency is much below 150 kHz, so that the desired operating frequency can be exploited for further calculation of the primary inductance:

$$L_p = \frac{V_{bulk-min} \cdot \delta_{max}}{I_{ppk} \cdot f_{sw-max}} = \frac{127 \cdot 0.5}{0.2047 \cdot 75 \cdot 10^3} = 4.14 \text{ mH} \quad \text{(eq. 19)}$$

The EF16 core for transformer was selected. It has cross−section area A_e = 20.1 mm^2. The N67 magnetic allows to use maximum operating flux density B_{max} = 0.28 Tesla.

The number of turns of the primary winding is:

$$n_p = \frac{L_p \cdot I_{ppk}}{B_{max} \cdot A_e} = \frac{4.14 \cdot 10^{-3} \cdot 0.2047}{0.28 \cdot 20.1 \cdot 10^{-6}} = 150 \text{ turns} \quad \text{(eq. 20)}$$

The A_L factor of the transformer's core can be calculated:

$$A_L = \frac{L_p}{(n_p)^2} = \frac{4.14 \cdot 10^{-3} \cdot}{(150)^2} = 184 \text{ nH} \quad \text{(eq. 21)}$$

For an adapter output voltage of 6.5 V, the number of turns of the secondary winding can be calculated accounting Schottky diode for output rectifier as follows:

$$n_S = \frac{(V_S + V_{fwd})(1 - \delta_{max})n_p}{\delta_{max} \cdot V_{bulk-min}} = \frac{(6.5 + 0.7)(1 - 0.5)150}{0.5 \cdot 127} = 8.5 = 9 \text{ turns} \quad \text{(eq. 22)}$$

The number of turns for auxiliary winding can be calculated similarly:

$$n_S = \frac{(V_S + V_{fwd})(1 - \delta_{max})n_p}{\delta_{max} \cdot V_{bulk-min}} = \frac{(12 + 1)(1 - 0.5)150}{0.5 \cdot 127} = 15.35 = 15 \text{ turns} \quad \text{(eq. 23)}$$

The peak primary current is known from initial calculations. The current sense method allows choosing the voltage drop across the current sense resistor. Let's use a value of 0.5 V. The value of the current sense resistor can then be evaluated as follows:

$$R_{CS} = \frac{V_{CS}}{I_{ppk}} = \frac{0.5}{0.2047} = 2.442\ \Omega = 2.7\ \Omega \quad \text{(eq. 24)}$$

The voltage drop across the sense resistor needs to be recalculated:

$$V_{CS} = R_{CS} \cdot I_{ppk} = 2.7 \cdot 0.2047 = 0.553 \text{ V} \quad \text{(eq. 25)}$$

Using the above results the value of the shift resistor is:

$$R_{shift} = \frac{V_{CS}}{I_{CS}} = \frac{0.553}{50 \cdot 10^{-6}} = 11.06\ k\Omega = 11\ k\Omega \quad \text{(eq. 26)}$$

The value of timing capacitor for the off time control has to be calculated for minimum bulk capacitor voltage since at these conditions the converter should be able to deliver specified maximum output power. The value of the timing capacitor is then given by the following equation:

$$C_T = \frac{\frac{1}{f_{sw}} - \frac{L_p \cdot I_{ppk}}{V_{bulk-min}}}{1.2 \cdot 10^6} = \frac{\frac{1}{75 \cdot 10^3} - \frac{4.14 \cdot 10^{-3} \cdot 0.2047}{127}}{0.12 \cdot 10^6} = 55.5 \text{ pF} = 56 \text{ pF} \quad \text{(eq. 27)}$$

The value of the startup resistor for startup time of 200 ms and V_{CC} capacitor of 200 nF is following:

$$R_{startup} = \frac{V_{bulk-min}}{C_{Vcc} \frac{V_{startup}}{t_{startup}} + I_{CC-start\ MAX}} = \frac{127}{200 \cdot 10^{-9} \frac{12}{0.2} + 10 \cdot 10^{-6}} = 5.77\ M\Omega = 5.6\ M\Omega \quad \text{(eq. 28)}$$

The result of all the calculations is the application schematic depicted in Figure 21.

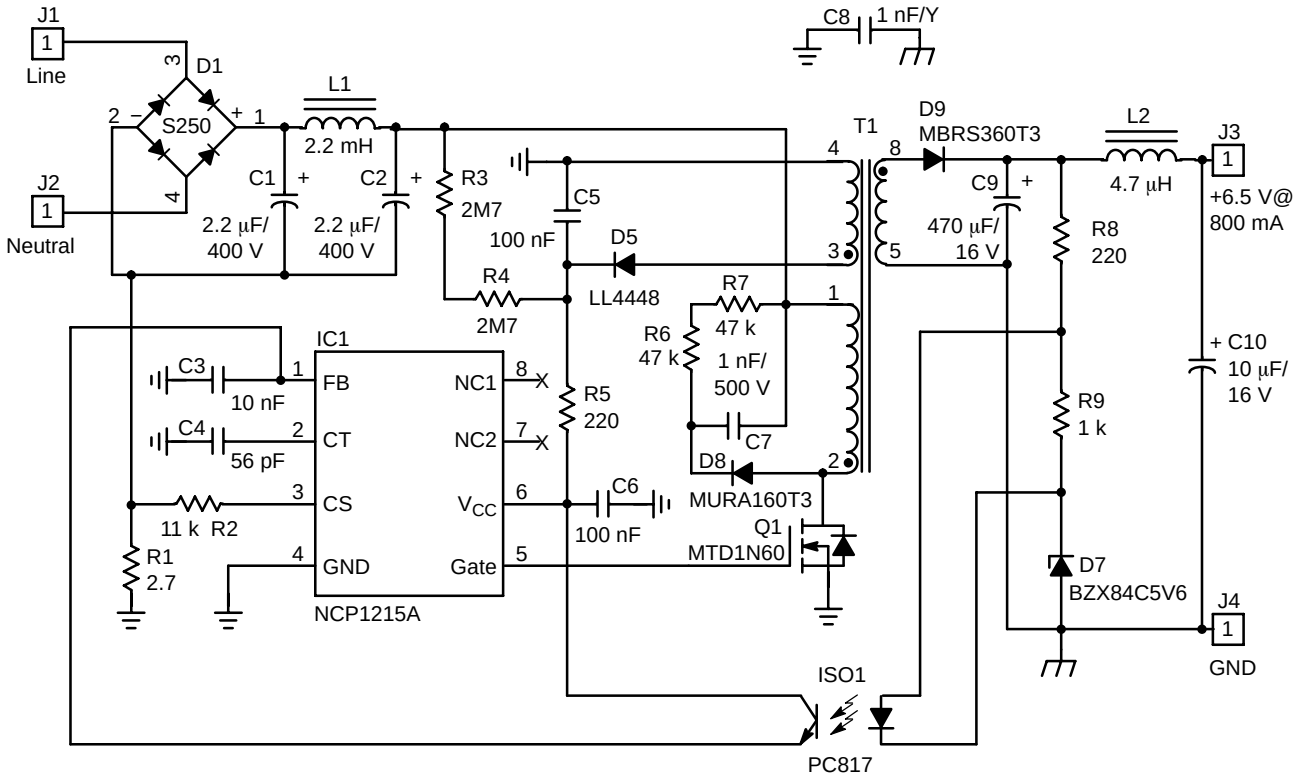


Figure 21. Adaptor Application Schematic

The following oscilloscope snapshots illustrate the operation of the working adapter. The Channel 3 in Figure 22 shows CT pin voltage at full output load. The Channel 1 is a gate driver output.

The CT voltage at no load condition is depicted in Figure 23.

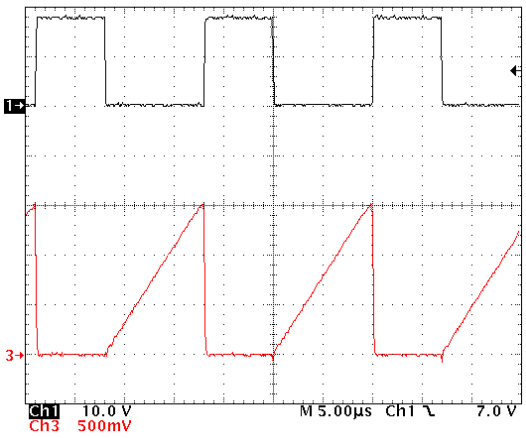


Figure 22. CT Voltage at Full Load Condition

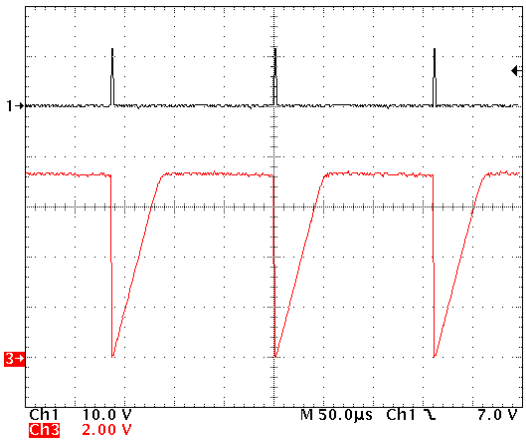


Figure 23. CT Voltage at No Load Condition

Figure 24 shows CT voltage and also by Channel 2 the switch's drain voltage at light load conditions.

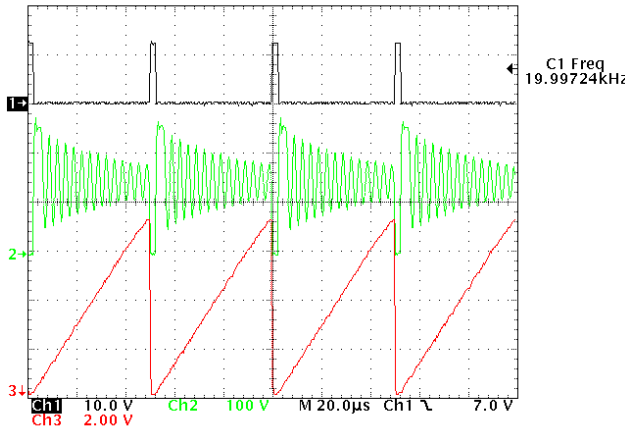


Figure 24. CT and Drain at Light Load

The waveform on the current sense pin at full load conditions can be observed from Channel 3 in Figure 25.

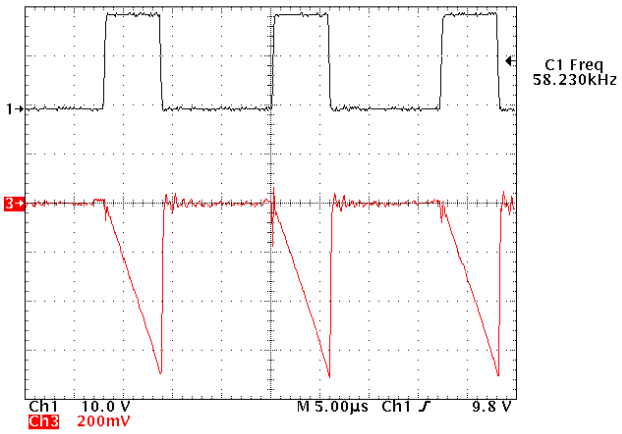


Figure 25. CS Pin at Full Load Condition

Figure 26 demonstrates the reduction of the peak primary current at light load conditions.

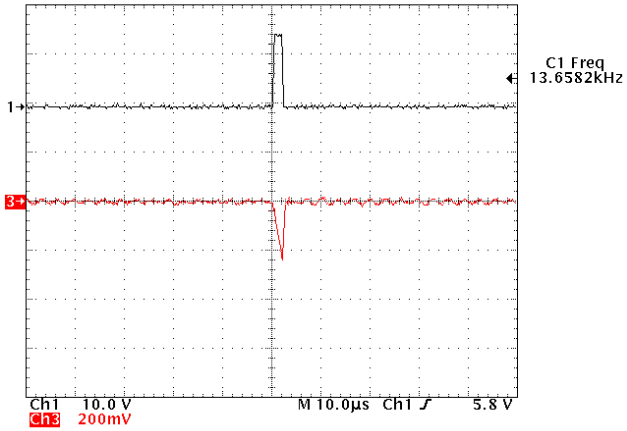


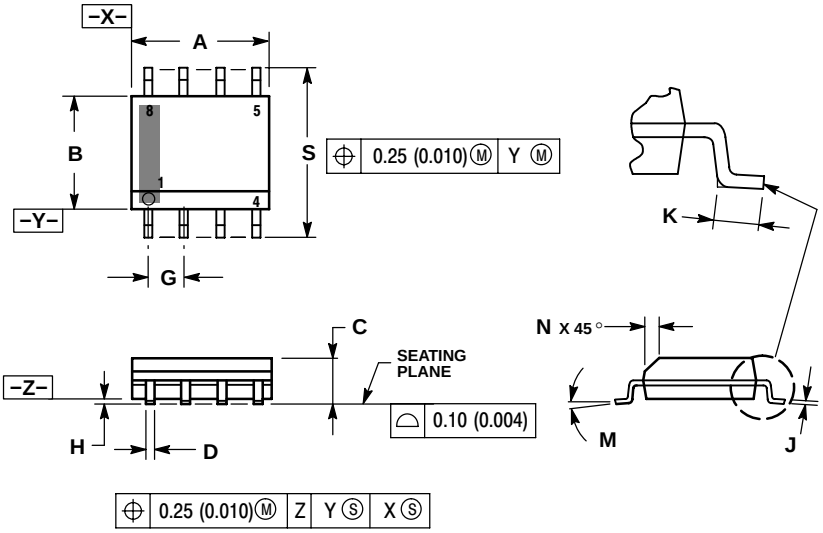
Figure 26. CS Pin at Light Load Condition

Gate−Source Resistor Design Guidelines

In some applications, there is a need to wire a resistor between the MOSFET gate and source connections. This can preclude an eventual MOSFET destruction if, in the production stage, the converter is powered whilst the gate is left unconnected. However, dealing with an extremely low startup current implies a careful selection of the gate−source resistance. With the NCP1215A, the gate−source resistor must be calculated to allow the growth of the V_{CC} capacitor to 4.0 V in order to not interfere with the power−on sequence. The following equation helps deriving $R_{gate-source}$, accounting for the minimum rectified input voltage and the startup resistor: Vin_{min} x $R_{gate-source}/(R_{gate-source} + R_{startup}) > 4.0$ V. If we take a Vin_{min} of 100 VDC, a startup resistor of 4.0 MΩ, then $R_{gate-source}$ equals 180 kΩ as a minimum normalized value.

PACKAGE DIMENSIONS

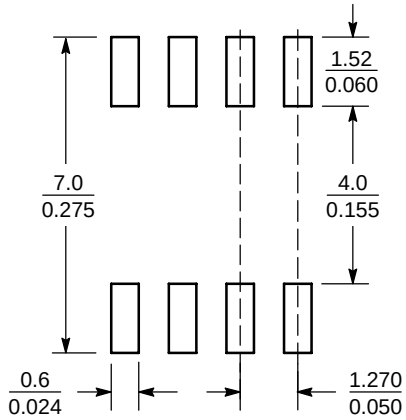
SOIC−8
D SUFFIX
CASE 751−07
ISSUE AG



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

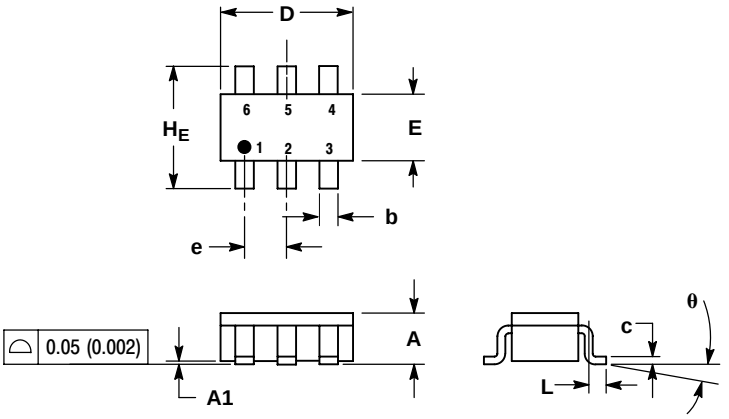


SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

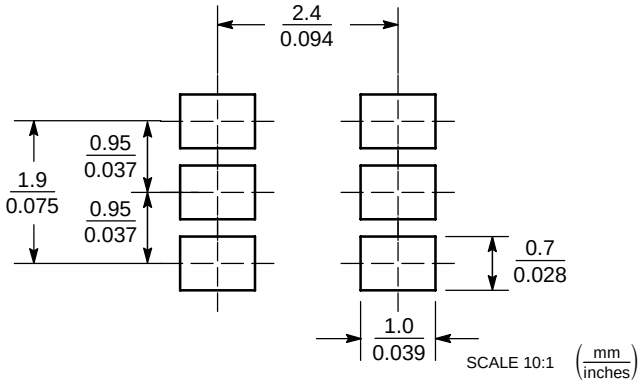
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CASE 318G−02
ISSUE P



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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