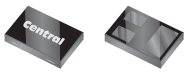
CEDM7002AE

ENHANCED SPECIFICATION
SURFACE MOUNT SILICON N-CHANNEL ENHANCEMENT-MODE MOSFET

TLP™ Tiny Leadless Package



Top View Bottom View

ENHANCED E SPECIFICATION

SOT-883L CASE

Central Semiconductor Corp.

www.centralsemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CEDM7002AE is a special ESD protected version of the 2N7002 enhancement-mode N-Channel MOSFET designed for high speed pulsed amplifier and driver applications.

MARKING CODE: 7

APPLICATIONS:

- Load/Power switches
- DC-DC converter circuits
- Power management

FEATURES:

- ♦ ESD protection up to 1800V
- 350mW power dissipation
- Low gate charge
- Low $r_{DS(ON)}$

MAXIMUM RATINGS: (T_A=25°C)	**SYMBOL**		**UNITS**
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage	V_{DG}	60	V
Gate-Source Voltage	V_{GS}	20	V
Continuous Drain Current	I_D	300	mA
Maximum Pulsed Drain Current	I_{DM}	800	mA
Power Dissipation	P_D	100	mW
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance	Θ_{JA}	1250	°C/W

ELECTRICAL CHARACTERISTICS: (T_A=25°C unless otherwise noted)

SYMBOL	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{GSSF}, I_{GSSR}	V_{GS}=20V, V_{DS}=0			10	μA
♦ I_{DSS}	V_{DS}=60V, V_{GS}=0			100	nA
I_{DSS}	V_{DS}=60V, V_{GS}=0, T_J=125°C			500	μA
♦ BV_{DSS}	V_{GS}=0, I_D=10μA	60	70		V
$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.2	1.5	2.0	V
V_{SD}	V_{GS}=0, I_S=115mA (Note 1)	0.5		1.1	V
♦ $r_{DS(ON)}$	V_{GS}=10V, I_D=500mA (Note 1)		1.0	1.4	Ω
$r_{DS(ON)}$	V_{GS}=5.0V, I_D=100mA (Note 1)		1.1	1.8	Ω
$r_{DS(ON)}$	V_{GS}=2.5V, I_D=10mA (Note 1)		3.0	6.0	Ω
g_{FS}	V_{DS}=10V, I_D=200mA	220			mS
C_{rss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz			5.0	pF
C_{iss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz			50	pF
C_{oss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz			25	pF

♦ Enhanced specification

Notes: (1) tp=380μs

R1 (3-October 2013)

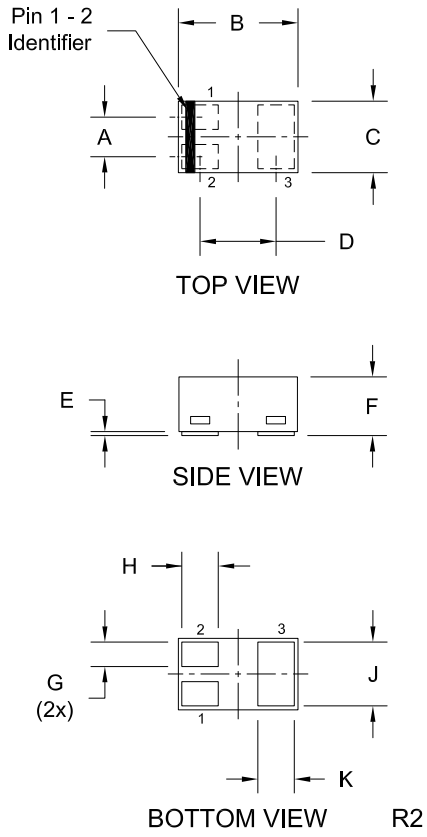
CEDM7002AE

ENHANCED SPECIFICATION
SURFACE MOUNT SILICON
N-CHANNEL
ENHANCEMENT-MODE
MOSFET

ELECTRICAL CHARACTERISTICS - Continued: (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	TYP	MAX	UNITS
$Q_{g(tot)}$	V_{DS}=10V, V_{GS}=4.5V, I_D=200mA	0.5		nC
Q_{gs}	V_{DS}=10V, V_{GS}=4.5V, I_D=200mA	0.2		nC
Q_{gd}	V_{DS}=10V, V_{GS}=4.5V, I_D=200mA	0.14		nC
t_{on}	V_{DD}=30V, V_{GS}=10V, I_D=200mA		20	ns
t_{off}	R_G=25Ω, R_L=150Ω		45	ns

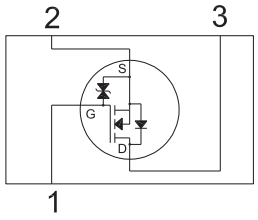
SOT-883L CASE - MECHANICAL OUTLINE



DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.014		0.35	
B	0.037	0.041	0.95	1.05
C	0.022	0.026	0.55	0.65
D	0.026		0.65	
E	0.000	0.002	0.00	0.05
F	0.012	0.016	0.30	0.40
G	0.005	0.007	0.13	0.18
H	0.008	0.012	0.20	0.30
J	0.018	0.022	0.45	0.55
K	0.008	0.012	0.20	0.30

SOT-883L (REV:R2)

PIN CONFIGURATION
(Bottom View)



LEAD CODE:
1) Gate
2) Source
3) Drain

MARKING CODE: 7

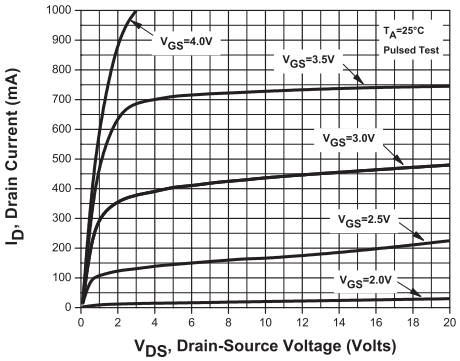
R1 (3-October 2013)

CEDM7002AE

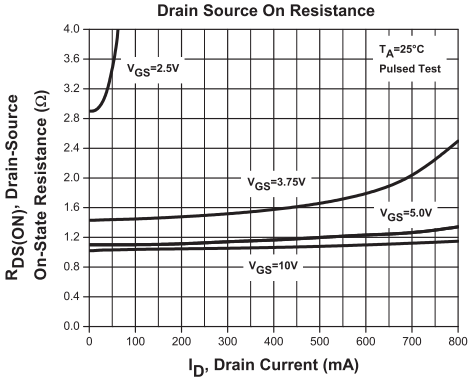
ENHANCED SPECIFICATION
SURFACE MOUNT SILICON
N-CHANNEL
ENHANCEMENT-MODE
MOSFET

TYPICAL ELECTRICAL CHARACTERISTICS

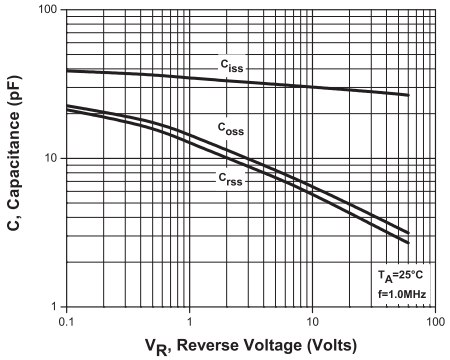
Output Characteristics



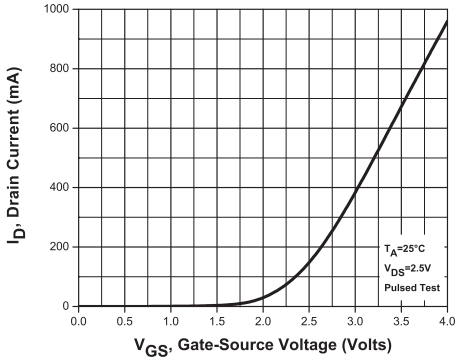
Drain Source On Resistance



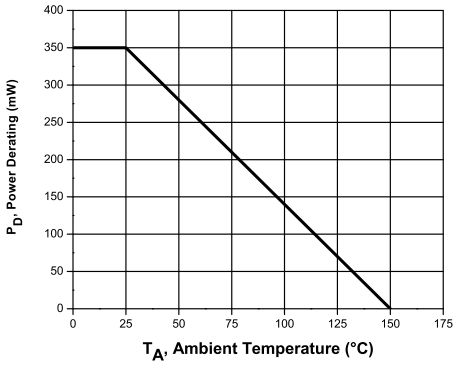
Capacitance



Transfer Characteristics



Power Derating



R1 (3-October 2013)