MAX25520 Automotive 2-Channel TFT-LCD Power Supply

General Description

The MAX25520 is a dual-output power IC that provides symmetrical or asymmetrical positive and negative voltages up to 10.5V and down to -10.5V (+/-12V in the case of MAX25520ATEC) with an input voltage between 2.65V and 5.5V. It incorporates a fully integrated current-mode boost converter and a current-mode inverter with external rectifier. The device operates at one of two switching frequencies, 420kHz or 2.1MHz. Operation at 2.1MHz permits very compact dual-output power supplies.

The two output voltages can be programmed independently or can be made to track each other. Independent enable pins allow complete flexibility in powering the outputs up and down.

The outputs are protected against overcurrent and undervoltage.

The MAX25520 is available in a compact 3x3mm TQFN package and operates over the -40 to 125°C temperature range.

Applications

- Infotainment Displays
- Central Information Displays
- Instrument Clusters

Benefits and Features

- High Integration
  - Synchronous Boost Provides Positive Output at up to 10.5V/200mA (+12V for MAX25520ATEC)
  - Inverter Output Provides up to -10.5V/-200mA (-12V for MAX25520ATEC)
- Low EMI
  - 420kHz/2.1MHz Switching Frequency
  - Spread Spectrum
- UV Diagnostics on All Outputs
- Versatile
  - Complete Sequencing Flexibility
  - Compact TQFN Package
  - -40°C to +125°C Operating Temperature Range
- AECQ100 Grade 1

Ordering Information appears at end of datasheet.

19-100974; Rev 0; 1/21

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Simplified Block Diagram

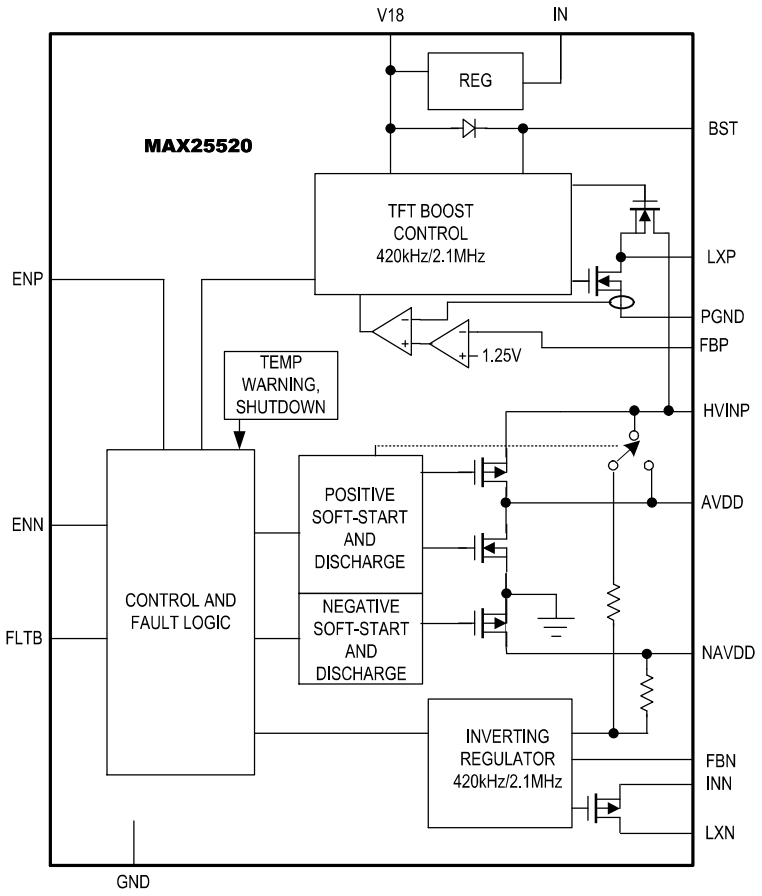


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Absolute Maximum Ratings

IN, INN to GND ..... -0.3V to +6V
FBP to GND ..... -0.3V to +2.2V
HVINP to GND ..... -0.3V to 16V
BST to GND ..... -0.3V to +16V
BST to LXP ..... -0.3V to +2.2V
LXP, AVDD to GND ..... -0.3V to HVINP + 0.3V
LXN to INN ..... -22V to +0.3V
V18 to GND ..... -0.3V to +2.2V
PGND, CPGND to GND ..... -0.3V to +0.3V
NAVDD to GND ..... IN-22V to IN+0.3V
ENP, ENN to GND ..... -0.3V to 6V
FLTB, FBN to GND ..... -0.3V to +6V
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 21.3mW/°C above +70°C.) ..... mW to 2222mW
Operating Temperature Range ..... -40°C to 125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN

Package Code	T1633+7C
Outline Number	21-0136
Land Pattern Number	90-0032
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	68°C/W
Junction to Case (θ_{JC})	10°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	43.3°C/W
Junction to Case (θ_{JC})	4°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 3.3V, V_{INN} = 3.3V, ENP = ENN = 3.3V, C_{V18} = 1µF, (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
IN Voltage Range	V_{IN_RNG}		2.65		5.5	V
		MAX25520ATEC	4.5		5.5	
IN UVLO Threshold	V_{IN_UVLO}	IN Voltage Rising	2.4	2.5	2.57	V
IN UVLO Hysteresis	$V_{IN_UVLO_HYS}$			100		mV
Start-Up Delay	T_{SU_DEL}	ENP or ENN high		50	100	µs
IN Shutdown Current	I_{IN_SHDN}	ENN = ENP = GND, V_{IN} = 3.3V, T_A = 25°C		4	6	µA
IN Quiescent Current	I_{IN_Q}	V_{ENN} = V_{ENP} = 3.3V, no switching.		1	1.8	mA
V18 REGULATOR						
V18 Output Voltage	V_{V18_ACC}	No load on V18	1.764	1.8	1.836	V
V18 Current Limit	I_{LIM_V18}		50			mA

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{INN} = 3.3V, ENP = ENN = 3.3V, C_{V18} = 1µF, (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V18 Undervoltage Lockout	V_{V18_UVLO}	V18 Voltage Rising	1.6	1.65	1.7	V
V18 Undervoltage Hysteresis	$V_{V18_UVLO_HYS}$			150		mV
OSCILLATOR						
Operating Frequency	f_{BOOSTH}	MAX25520ATEB/C, dither disabled. Switching frequency for boost and inverter.	1950	2100	2250	kHz
	f_{BOOSTL}	MAX25520ATEA, dither disabled. Switching frequency for boost and inverter.	390	420	450	
Frequency Dither	f_{BOOSTD}			±6		%
BOOST REGULATOR						
HVINP Output Voltage Range	V_{HVINP}	MAX25520ATEA/B	V_{IN} + 1		10.5	V
		MAX25520ATEC	V_{IN} + 1		12	
AVDD Output Voltage Range	V_{AVDD}	MAX25520ATEA/B	4.2		10.5	V
		MAX25520ATEC	6		12	
AVDD Default Output Voltage	V_{AVDD_ACC}	FBP connected to V18	6.66	6.8	6.94	V
FBP Regulation Voltage	V_{FBP}	Full input voltage and output current range	0.89	0.9	0.91	V
LXP Maximum Duty Cycle	D_{LXP_MAX}	420kHz switching frequency	86	88	90	%
		2.1MHz switching frequency	85	88	91	
Low-Side Switch On-Resistance	$R_{ON_LS_LXP}$	I_{LXP} = 0.1A		0.1	0.2	Ω
Synchronous Rectifier On-Resistance	$R_{ON_HS_LXP}$	I_{LXP} = -0.1A		0.1	0.2	Ω
Synchronous Rectifier Zero-Crossing Threshold	I_{ZX_TH}	I_{ZX} decreasing		70		mA
LXP Leakage Current	I_{LEAK_LXP}	V_{ENP} = 0V, V_{LXP} = 10.5V			5	µA
LXP Current Limit	I_{LIMPH}	Duty cycle = 50%	1.64	2.1	2.3	A
Soft-Start Period	t_{BOOST_SS}	Current-limit ramp		5		ms
AVDD Discharge Resistance	R_{AVDD_DIS}	ENP = 0V, V_{V18} > V_{V18_UVLO}		1.2		kΩ
INVERTING REGULATOR						
INN Voltage Range	V_{INN_RNG}		2.65		5.5	V
INN Shutdown Current	I_{INN_SHDN}	V_{ENN} = 0V, T_A = 25°C			1	µA
INN Quiescent Current	I_{INN_Q}			0.2		mA
LXN Maximum Duty Cycle	D_{LXN_MAX}	F_{SW} = 420kHz or 2.1MHz	85	88		%
FBN Regulation Voltage	V_{FBN}		-20	0	+20	mV

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{INN} = 3.3V, ENP = ENN = 3.3V, C_{V18} = 1µF, (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{AVDD} + V_{NAVDD} Regulation Voltage	$V_{NAVDD_AVDD_REG}$	V_{INN} = 2.65V to 5.5V, V_{AVDD} = 6.8V, 1mA < I_{NAVDD} < 200mA, I_{AVDD} = same load as NAVDD, FBN connected to IN	-34	0	34	mV
Low-Side LXN On-Resistance	R_{ON_LXN}	I_{LXN} = 0.1A		0.25	0.5	Ω
LXN Leakage Current	I_{LXN_LEAK}	V_{LXN} = V_{NAVDD} = -6.8V, T_A = +25°C			20	µA
LXN Current Limit	I_{LIMNH}	Duty cycle = 80%	1.55	1.9	2.25	A
Soft-Start Period	t_{INV_SS}	Current-limit ramp		5		ms
NAVDD Discharge Resistance	R_{NAVDD_DIS}			2		kΩ
AVDD SWITCH						
AVDD ON Resistance	R_{ONAVDD}	Between HVINP and AVDD, I_{AVDD} = 200mA		0.5	0.9	Ω
AVDD Current Limit	I_{LIM_AVDD}		320	460	580	mA
FAULT PROTECTION						
Fault Timeout	T_{FAULT}	Applies to both outputs		30		ms
Fault Retry Time	T_{AUTO}			1.9		s
AVDD Undervoltage Fault Threshold	V_{AVDD_UV}	Relative measurement between HVINP and AVDD, AVDD falling	80	85	90	%
FBP Undervoltage Fault Threshold	V_{FBP_UV}	External feedback, FBP falling	720	765	810	mV
NAVDD Undervoltage Fault Threshold	$NAVDD_{UV}$	FBN = IN, NAVDD rising	80	85	90	%
FBN Undervoltage Fault Threshold	V_{FBN_UV}	External resistor-divider connected to FBN, NAVDD = -6.8V, FBN rising	200	210	220	mV
AVDD Short-Circuit Fault Threshold	$AVDD_{SHRT_TH}$	As a percentage of set voltage, AVDD falling	35	40	45	%
FBP Short-Circuit Threshold	V_{FBP_SHRT}	External feedback, FBP falling	315	360	405	mV
NAVDD Short-Circuit Fault Threshold	$NAVDD_{SHRT_TH}$	FBN = IN, NAVDD rising	35	40	45	%
FBN Short-Circuit Fault Threshold	V_{FBN_SHRT}	External resistor-divider connected to FBN, NAVDD = -6.8V, FBN rising	835	850	865	mV
Short-Circuit and Overload Fault Delay		After completion of soft-start		10		µs
LOGIC INPUTS and OUTPUTS						
ENP, ENN Glitch Filter	T_{EN_FLT}			10		µs
ENN, ENP Minimum Low Time For Reset	T_{EN_MIN}		1			ms
ENP, ENN Input Logic-High	V_{IH_EN}		1.22			V
ENP, ENN Input Logic-Low	V_{IL_EN}				0.6	V

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{INN} = 3.3V, ENP = ENN = 3.3V, C_{V18} = 1µF, (Note 1))

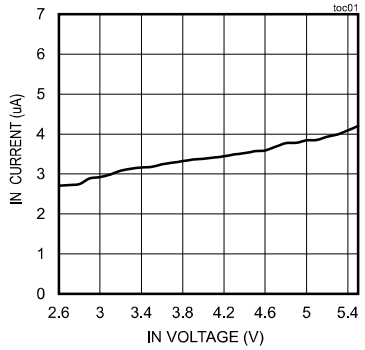
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENP, ENN Input Pulldown Resistor	R_{PD_EN}			200		kΩ
FLTB Output Low Voltage	V_{OL}	Sinking 5mA			0.4	V
FLTB Output Leakage Current	I_{LEAK_FLTB}	V_{FLTB} = 5.5V			+1	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	T_{SHDN}			160		°C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}			15		°C

Note 1: Limits are 100% tested at T_A = +25ºC and +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

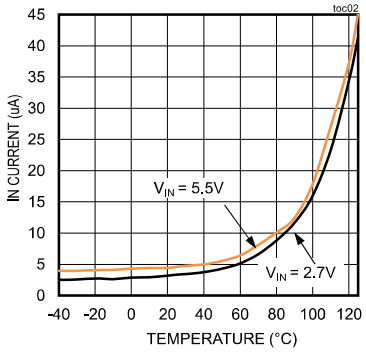
Typical Operating Characteristics

(V_{IN} = V_{INN} = +3.3V, F_{SW} = 2.1MHz, T_A = +25°C unless otherwise noted.)

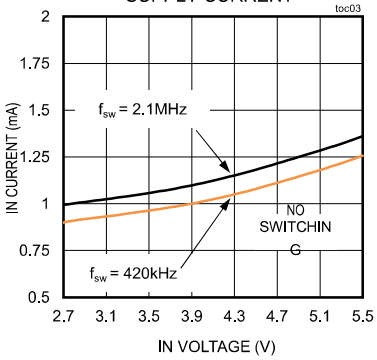
SHUTDOWN SUPPLY CURRENT



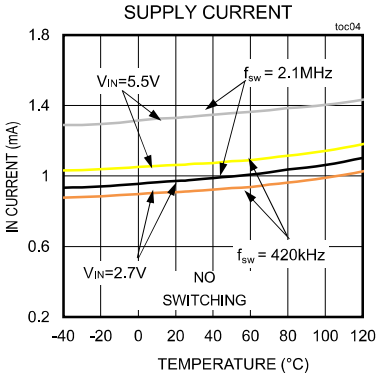
SHUTDOWN SUPPLY CURRENT



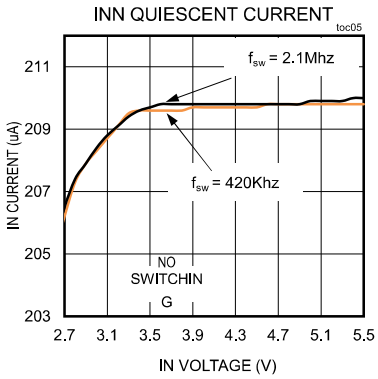
SUPPLY CURRENT



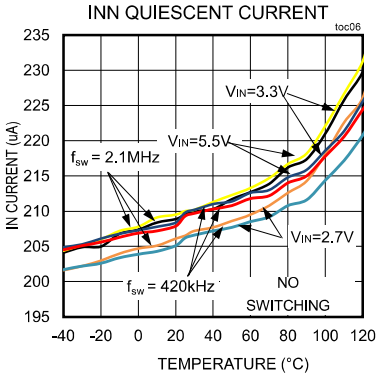
SUPPLY CURRENT



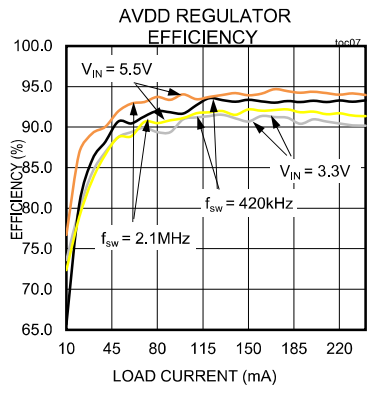
INN QUIESCENT CURRENT



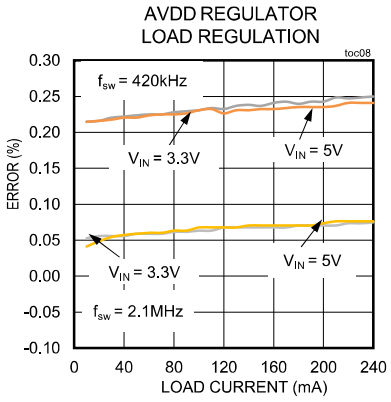
INN QUIESCENT CURRENT



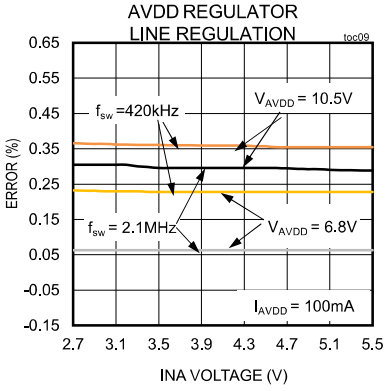
AVDD REGULATOR EFFICIENCY



AVDD REGULATOR LOAD REGULATION



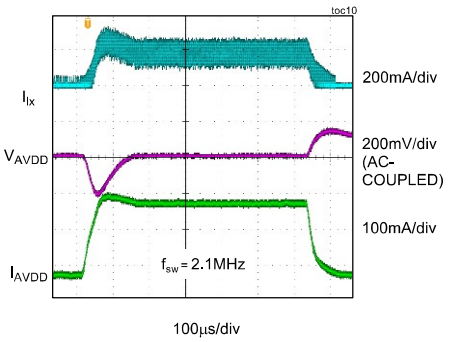
AVDD REGULATOR LINE REGULATION



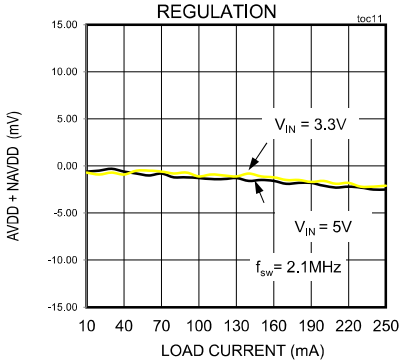
Typical Operating Characteristics (continued)

(V_{IN} = V_{INN} = +3.3V, F_{SW} = 2.1MHz, T_A = +25°C unless otherwise noted.)

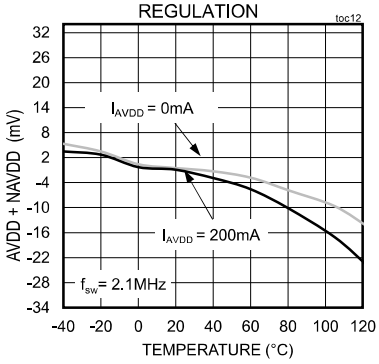
AVDD REGULATOR LOAD STEP 0->200mA->0



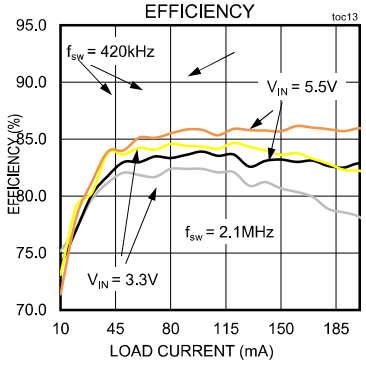
AVDD + NAVDD REGULATION



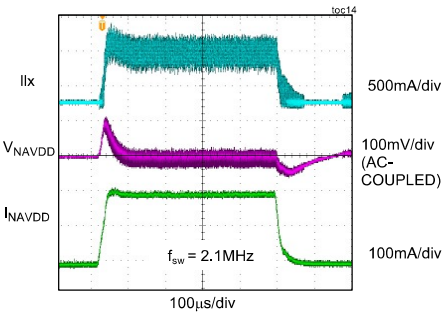
AVDD + NAVDD REGULATION



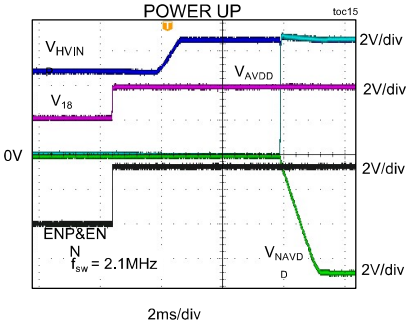
NAVDD REGULATOR EFFICIENCY



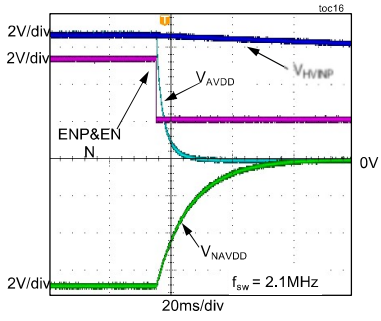
NAVDD REGULATOR LOAD STEP



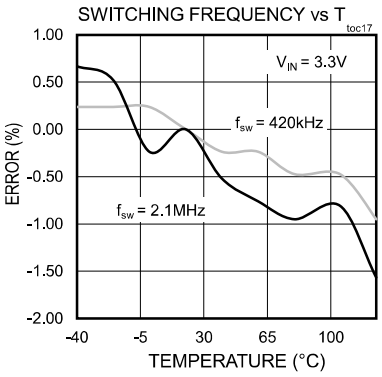
SUPPLY SEQUENCING WAVEFORM POWER UP



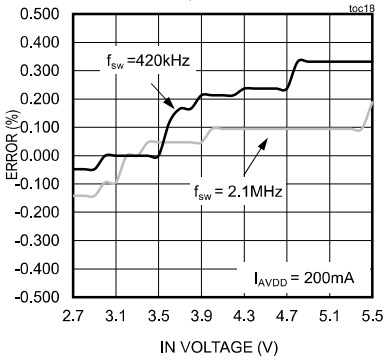
SUPPLY SEQUENCING WAVEFORM POWER DOWN



SWITCHING FREQUENCY vs T

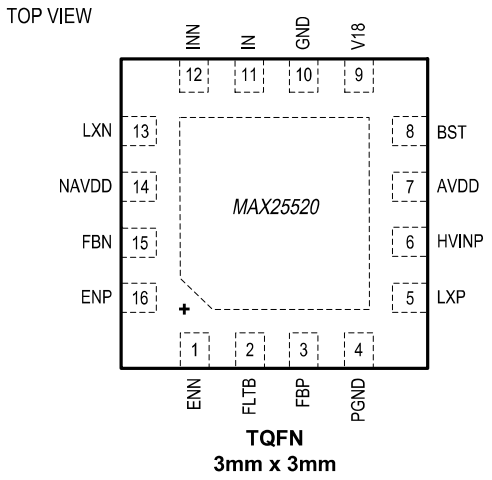


SWITCHING FREQUENCY vs IN VOLTAGE



Pin Configuration

MAX25520



Pin Description

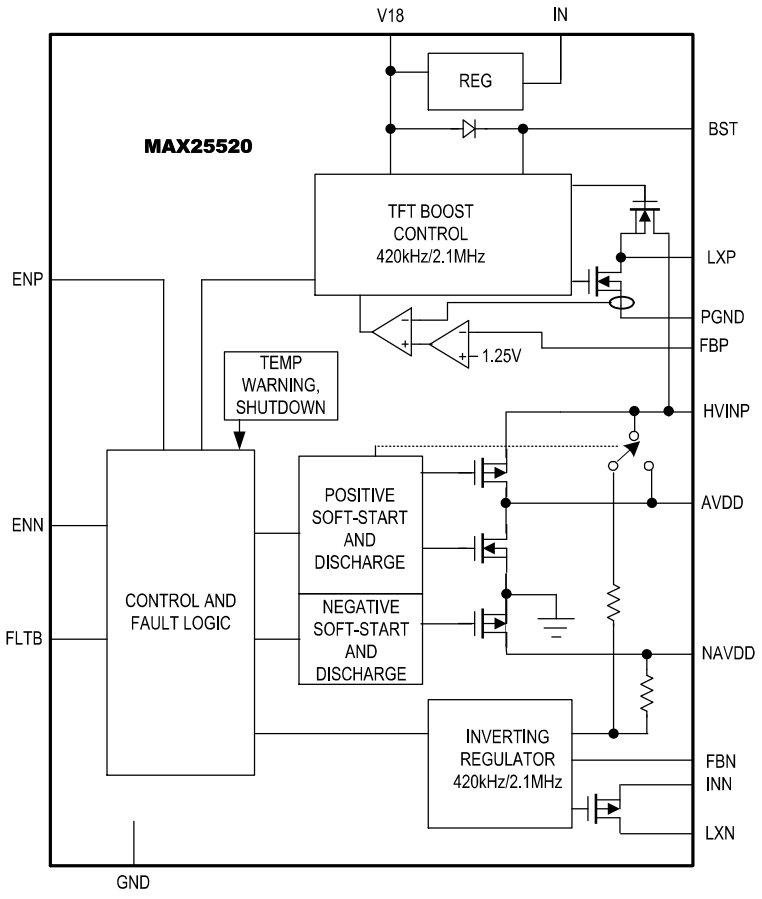
PIN	NAME	FUNCTION
1	ENN	Enable pin for inverting regulator.
2	FLTB	Open-Drain, Active-Low Fault Output. Connect a pullup resistor from FLTB to a logic supply ≤5V.
3	FBP	Boost feedback pin. Connect a resistor-divider between AVDD and GND with its midpoint connected to FBP to set the AVDD output voltage. Connect FBP to V18 to set AVDD to its default value of 6.8V.
4	PGND	Ground Connection for Boost Switching Device. Connect to GND using a low-impedance trace.
5	LXP	Switching Node of Boost Converter. Connect the boost inductor between LXP and IN.
6	HVINP	Boost Output and input to AVDD switch. Bypass HVINP with a 22µF output capacitor placed close to the pin when using 420kHz switching frequency. When the switching frequency is 2.1MHz use a 10µF capacitor on HVINP.
7	AVDD	Switched Output of Boost Converter. Connect a bypass capacitor of value 2.2µF from AVDD to PGND.
8	BST	Bootstrap Capacitor Connection for Synchronous Rectifier Driver. Connect a 0.1µF ceramic capacitor between BST and LXP.
9	V18	Output of internal 1.8V regulator. Connect a 1µF capacitor from V18 to GND.
10	GND	Ground connection.
11	IN	Supply connection for device. Bypass IN with local 10µF and 0.1µF capacitors at the minimum.

Pin Description (continued)

PIN	NAME	FUNCTION
12	INN	Inverting Converter Input. Connect directly to IN.
13	LXN	DC-DC Inverting Converter Inductor/Diode Connection.
14	NAVDD	Negative Source-Driver Output Voltage. Connect a 10µF ceramic capacitor from this pin to GND.
15	FBN	Inverter feedback pin. Connect FBN to INN when NAVDD should track AVDD. When the inverting regulator is used independently connect a resistor divider between V18 and NAVDD with its midpoint connected to FBN to set the output voltage.
16	ENP	Enable pin for boost converter.

Functional Diagrams

MAX25520



Detailed Description

The MAX25520 is a dual-output power IC that provides symmetrical or asymmetrical positive and negative voltages up to 10.5V and down to -10.5V (+/-12V in the case of MAX25520ATEC) with an input voltage between 2.65V and 5.5V. It incorporates a fully integrated current-mode boost converter and a current-mode inverter with external rectifier. The device operates at one of two switching frequencies, 420kHz or 2.1MHz. Operation at 2.1MHz permits very compact dual-output power supplies.

The two output voltages can be programmed independently or can be made to track each other. Independent enable pins allow complete flexibility in powering up and down the outputs.

The outputs are protected against overcurrent and undervoltage.

Input Voltage Restrictions When Using MAX25520ATEC

When using the MAX25520ATEC with output voltages greater than 10.5V a nominal input voltage of 5V should be used.

Power-Up state

When either of the ENP and ENN pins is taken high, the V18 regulator is turned on and the appropriate output(s) is/are turned on. While both ENN and ENP are low, the device is in low-quiescent-current mode.

If at any time the internal 1.8V regulator is out of range, the device stops operation.

When FBN is connected to IN, the device is in tracking mode and NAVDD is regulated to -AVDD. Otherwise, the AVDD and NAVDD outputs are set independently using the FBP and FBN feedback inputs.

Device operation is shown in Table 1.

Table 1. Device Operation

OPERATION MODE	ENP	ENN	HVINP	AVDD	NAVDD	NOTES
Tracking (FBN connected to IN)	0	X	Off	Off	Off	Applies also with FBP connected to V18 (default output voltage)
	1	0	On	On	Off	
	1	1	On	On	On	
Independent Outputs	0	0	Off	Off	Off	
	0	1	Off	Off	On	
	1	0	On	On	Off	
	1	1	On	On	On	

Start-Up Waveforms

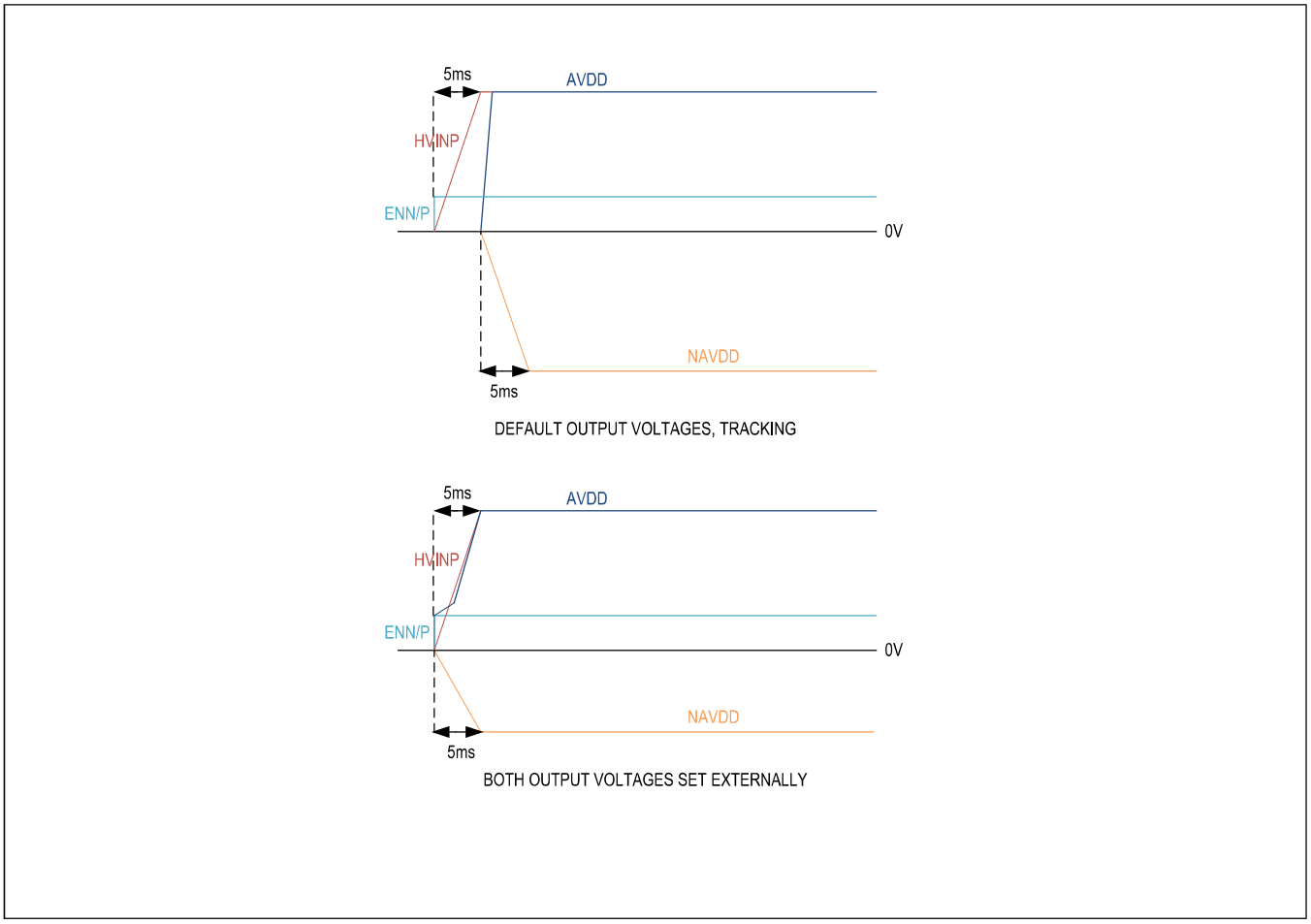


Figure 1. Start-Up Waveforms

Switching Frequency

The two versions of the device provide switching frequencies of 2.1MHz and 420kHz, respectively. The switching frequency has spread-spectrum applied to improve EMI performance.

AVDD Boost Converter

The MAX25520 includes a current-mode boost converter with output switch that generates up to +10.5V (+12V in the case of MAX25520ATEC) at up to 200mA. The boost converter's regulation voltage (AVDD) is set by the resistor-divider connected to the FBP pin. FBP is regulated to a nominal voltage of 0.9V.

Alternatively, the default AVDD output voltage (6.8V) can be chosen by connecting FBP to V18. The converter has an internal soft-start which ramps the HVINP voltage up to its final value in 5ms. The boost converter is internally compensated.

NAVDD Inverting Converter

The inverting buck-boost converter is of the current-mode type and can generate down to -10.5V output voltage (-12V in the case of MAX25520ATEC), delivering up to -200mA. It is internally compensated.

The converter has an internal soft-start that ramps the voltage up to its final value in 5ms. The negative source-driver

supply voltage (NAVDD) is either tightly regulated to -AVDD within ±34mV (when FBN is connected to IN), or its output voltage is set by the resistors connected between V18, FBN and NAVDD

Fault Handling

When a fault is detected, the FLTB pin asserts low. Possible faults are undervoltage on AVDD or NAVDD (when they fall below 85% of their set value), short-circuits on AVDD or NAVDD (when they fall below 40% of their set value), and thermal shutdown.

Undervoltage Faults

The reaction to undervoltage faults depends on whether the device is in tracking mode or the outputs are set independently.

In tracking mode if an undervoltage is detected for 30ms on either of the outputs, both outputs are switched off and FLTB is asserted low. After 1.9s, a retry is performed in which an attempt is made to re-start both outputs if the enable pins are still high. If the fault is still present, the outputs will be disabled again. If the problem persists, the device will continue to retry every 1.9s unless the enable pins are taken low.

When the outputs are set independently, an undervoltage for 30ms causes the affected output to be turned off and the FLTB pin to assert low. After 1.9s, a retry is performed in which an attempt is made to re-start the affected output if its enable pin is still high. If the fault is still present, the output will be disabled again. If the problem persists, the device will continue to retry every 1.9s unless the corresponding enable pin is taken low.

During retry, the FLTB pin remains asserted low until normal operation is resumed.

Thermal Shutdown

When the junction temperature reaches 165°C, the device enters thermal shutdown. A thermal shutdown causes both outputs to turn off immediately. When the junction temperature drops by 15°C, the outputs are re-enabled according to the state of the EN_ pins.

Applications Information

Boost Converter

Boost Converter Inductor Selection

Three key inductor parameters must be specified for operation with the device: Inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DC}). To determine the inductance value, first select the ratio of inductor peak-to-peak ripple current to average output current (LIR). Higher LIR values mean higher RMS inductor current and therefore, higher I^2R losses. To achieve a lower LIR value, a high-valued inductor, which may be physically larger, must be used. A good compromise between size and loss is to select a 30% to 60% peak-to-peak ripple current to average-current ratio (LIR from 0.3 to 0.6). If extremely thin high-resistance inductors are used, as is common for LCD-panel applications, the best LIR may lie between 0.5 and 1.0. The value of the inductor is determined as follows:

$$L = \frac{V_{IN} \times D}{LIR \times I_{IN} \times f_{SW}}$$

using:

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}}$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}}$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, I_{OUT} is the output current, I_{IN} is the calculated average boost input current, η is the efficiency of the boost converter, D is the duty cycle, and f_{SW} is either 420kHz or 2.1MHz (the selected switching frequency of the boost converter). The efficiency of the boost converter can be estimated from the *Typical Operating Characteristics* and accounts for losses in the internal switch, inductor, and capacitors.

The inductor's saturation rating must exceed the maximum current limit of 2.3A.

Boost Output Filter Capacitor Selection

The primary criterion for selecting the output filter capacitor is low effective series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determine the amplitude of the high-frequency ripple seen on the output voltage. For stability, the boost output-filter capacitor should have a value of 22µF or greater at 420kHz and 10µF at 2.1MHz.

To avoid a large drop on HVINP when AVDD is enabled, the capacitance on the HVINP node should be at least 3 times larger than that on AVDD.

Setting the AVDD Voltage

The AVDD output voltage can be set to its default value by connecting FBP to V18. Alternatively, the voltage is set by connecting a resistive divider from AVDD to GND with is midpoint connected to FBP. Choose the value of the resistor connected from AVDD to FBP (R1) using the following equation:

$$R1 = \frac{R2 \times \left(V_{AVDD} - 0.9\right)}{0.9}$$

where R2 is the resistor connected from FBP to ground and V_{AVDD} is the desired output voltage.

NAVDD Inverting Regulator

NAVDD Regulator Inductor Selection

The inductor value for the NEG regulator can be selected using the following formula:

$$L = \frac{V_{NEG} \times (1 - D)}{LIR \times I_{NEG} \times f_{SW}}$$

where V_{NEG} is the output voltage, I_{NEG} the output current, LIR the desired inductor ripple ratio, and f_{SW} the switching frequency.

Calculate the duty-cycle D using the following formula:

$$D = \frac{V_{NEG}}{V_{IN} + V_{NEG}}$$

The inductor's saturation current rating must exceed the maximum current-limit of 2.25A.

NAVDD External Diode Selection

Select a diode with a peak current rating of at least the LXN current limit (2.25A) for use with the NEG output. The diode breakdown-voltage rating should exceed the sum of the maximum INN voltage and the absolute value of the NAVDD voltage. A Schottky diode improves the overall efficiency of the converter.

NAVDD Output Capacitor Selection

The primary criteria for selecting the output filter capacitor are low ESR and capacitance value, as the NAVDD capacitor provides the load current when the internal switch is on. The voltage ripple on the NAVDD output has two components:

- Ripple due to ESR which is the product of the peak inductor current and the output filter capacitor's ESR
- Ripple due to bulk capacitance.

For stability, the NEG output capacitor should have a value of 10µF or greater.

Setting the NAVDD Voltage

When FBN is connected to IN/INN, the NAVDD voltage mirrors the regulated voltage on AVDD.

If a voltage other than $-V_{AVDD}$ is required, connect a resistor-divider from V18 to NAVDD with its midpoint connected to FBN. Select the resistor values using the following equation:

$$R4 = -\frac{V_{NAVDD} \times R3}{1.8}$$

where R4 is the resistor connected between FBN and NAVDD, R3 is the resistor from V18 to FBN, and V_{NAVDD} is the desired output voltage. Use a value greater than 4.7kΩ for R3.

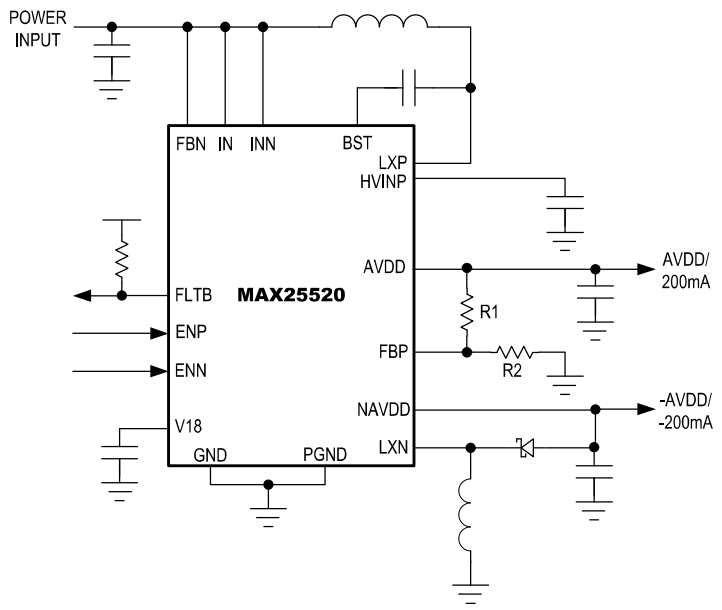
Layout Considerations

When designing a printed circuit board for the MAX25520, minimize the area of the LXP and LXN nodes and the area of the switching current loop. Follow these guidelines for the rest of the layout:

1. Separate power and analog grounds on the board and connect them together at a single point.
2. Connect any feedback resistor-dividers to the analog or "quiet" ground, along with the V18 and IN/INN capacitors. Feedback resistors should be placed close to their associated pins to avoid noise pickup.
3. Place decoupling capacitors as close as possible to their respective pins.
4. Keep high-current paths as short and wide as possible.
5. Route high-speed switching nodes (i.e., LXP, LXN) away from sensitive analog nodes (i.e., FBP, FBN, etc.).

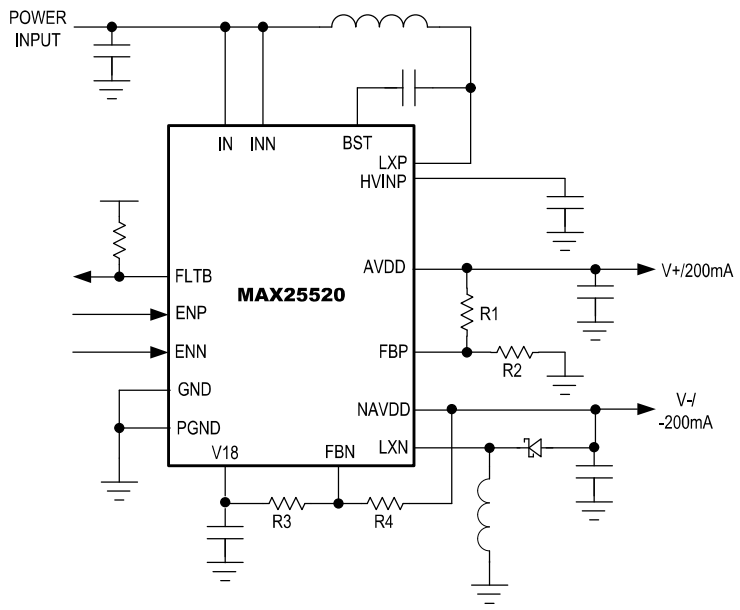
Typical Application Circuits

Application Circuit with Tracking Outputs



Typical Application Circuits (continued)

Application Circuit with Independent Outputs



Ordering Information

PART	TEMPERATURE RANGE	PIN-PACKAGE	SWITCHING FREQUENCY
MAX25520ATEA/V+*	-40 to +125°C	16 TQFN-EP	420kHz
MAX25520ATEB/V+	-40 to +125°C	16 TQFN-EP	2.1MHz
MAX25520ATEA/VY+*	-40 to +125°C	16 SWTQFN-EP	420kHz
MAX25520ATEB/VY+	-40 to +125°C	16 SWTQFN-EP	2.1MHz
MAX25520ATEC/V+	-40 to +125°C	16 TQFN-EP	2.1MHz

** Future product—contact factory for availability.*

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

/V denotes an automotive qualified part.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/21	Initial release	—
1	1/21	Added "C" version.	1, 3, 12, 13, 18

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