2.5Gb/s SONET/SDH FEC Encoder and Decoder

VSC9210

Product Brief

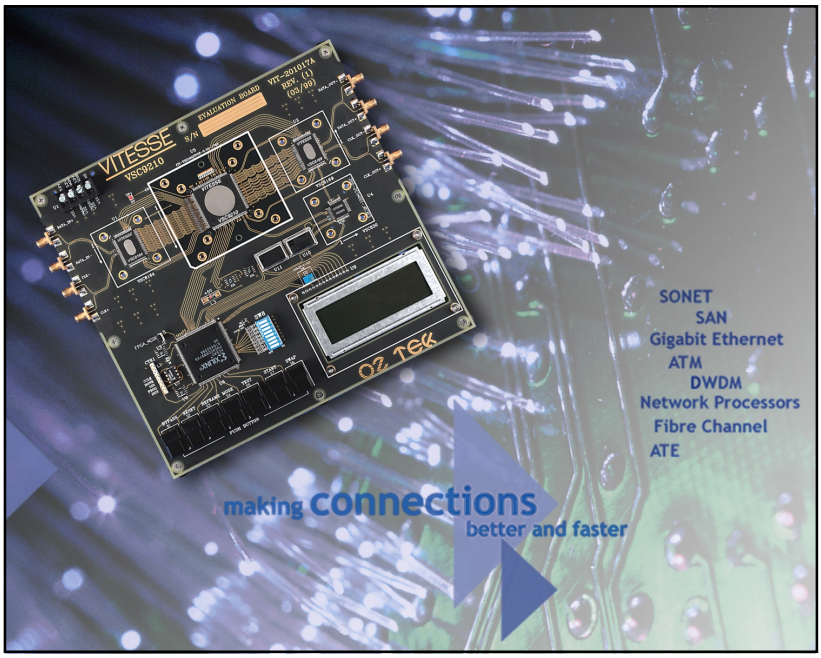
Optical Transport Networking

Features:

- Reed Solomon RS(255,241) Codec
- Bit Error Rate Improvement from 10^5 to 10^{20}
- Includes Optical Channel Overhead (OCh-OH) of 10Mb/s
- Provides Bit Error Rate Monitoring of FEC Line
- Processes Data Rates up to 2.654Gb/s and Information Rates to 2.488Gb/s
- Provides a Dedicated User Defined Data Channel at 10.368Mb/s

Benefits:

- Device Pin Configured as Stand-alone Encoder, Decoder, or Bypass with Cocks Disabled
- Provides Count of Correctable 0's and 1's that are in Error in Prior Code Word
- Interfaces Directly with Vitesse OC-48 Rate Components



Product Description

The VSC9210 provides forward error correction for any data rate and protocol operating up to 2.5Gb/s using a block oriented Reed-Solomon Forward Error Correction (FEC) algorithm RS(255,241). The device can be configured as a FEC encoder or a FEC decoder utilizing two 16-bit differential PECL I/O ports to interface with an external high speed multiplexer/demultiplexer pair. Clock dividers are provided on chip to facilitate control of external PLL circuitry.

For the Encoder, the 1:16 Demultiplexer is used to convert the incoming 2.5Gb/s STS-48 information to a 16 bit parallel data at 155MHz to interface with the VSC9210. After the encoding process, the 16 bit parallel output data from the VSC9210 is obtained at 165MHz and is converted to a 2.65Gb/s data stream using the 16:1 Multiplexer. In the case of the Decoder configuration, the Demultiplexer operates on a 2.65Gb/s data stream while the Multiplexer provides the 2.5Gb/s STS-48 information stream. Clock dividers are incorporated within the VSC9210 to provide control of an external PLL circuit for synthesizing the necessary reference clock for the Multiplexer. In the case of the Bypass mode, the input and output rates are identical and both the Multiplexer and Demultiplexer operate at 2.5Gb/s.

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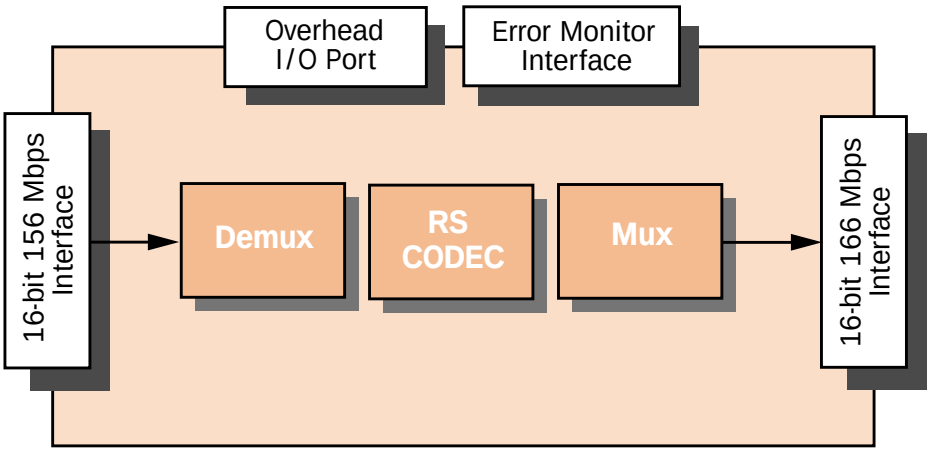
Product Brief

Optical Transport Networking

Specifications:

- Operable at OC-48, OC-12, OC-3 Rates
- 16-Bit PECL Input/Output Bus
- 3.3.V Power Supply
- Telecom Temperature Range: 0°- 85°C Case
- Thermally Enhanced 208-pin PQFP Package

VSC9210 Block Diagram



The User Channel is an 8 bit TTL interface operating at 1.296MHz resulting in an aggregate data rate of 10.368Mb/s. This data channel is encoded and decoded along with the 16-bit STS data, i.e. errors occurring in this User Channel are also corrected.

The VSC9210 can be operated at or below unencoded and encoded data rates of 155Mb/s and 165Mb/s respectively. The ratio of the two input clocks (INCLK and OUTCLK) must be 15/16 for Encoder operation, and 16/15 for Decoder operation.

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