19-1993; Rev 3; 9/02

EVALUATION KIT AVAILABLE

High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

MAX1844

General Description

The MAX1844 pulse-width modulation (PWM) controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high-voltage batteries to generate low-voltage CPU core or chipset/RAM supplies in notebook computers.

Maxim's proprietary Quick-PWM™ quick-response, constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency. Efficiency is enhanced by an ability to drive very large synchronous-rectifier MOSFETs. Accurate current sensing to ensure reliable overload protection is available using an external current-sense resistor in series with the synchronous rectifier. Alternatively, the synchronous rectifier itself can be used for less accurate current sensing at the lowest possible power dissipation.

Single-stage buck conversion allows the MAX1844 to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the 5V system supply instead of the battery) at a higher switching frequency allows the minimum possible physical size.

The MAX1844 is intended for CPU core, chipset, DRAM, or other low-voltage supplies as low as 1V. It is available in 20-pin QSOP, and QFN packages and includes both adjustable overvoltage and undervoltage protection.

For a dual step-down PWM controller with accurate current limit, refer to the MAX1845. The MAX1714/ MAX1715 single/dual PWM controllers are similar to the MAX1844/ MAX1845 but do not use current-sense resistors.

Applications

Notebook Computers

CPU Core Supplies

Chipset/RAM Supplies as Low as 1V

1.8V and 2.5V Supplies

** Contact factory for availability.*

Quick-PWM is a trademark of Maxim Integrated Products.

Pin Configuration appears at end of data sheet.

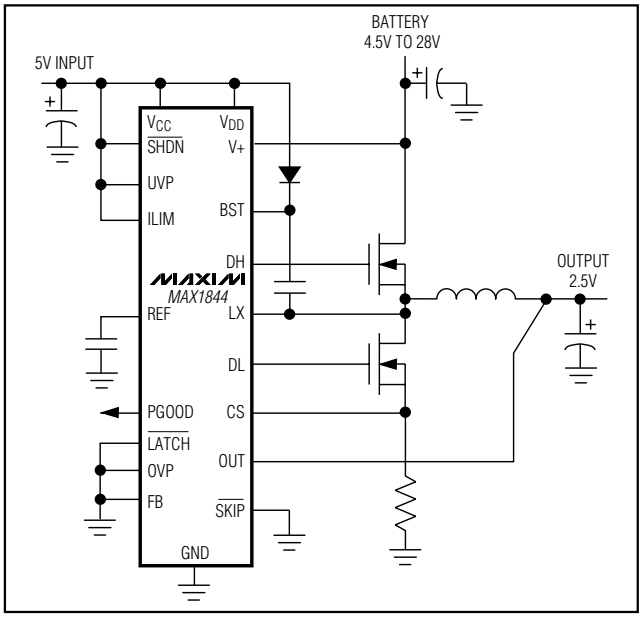
Features

- **Ultra-High Efficiency**
- **Accurate Current-Limit Option**
- **Quick-PWM with 100ns Load-Step Response**
- **1% V_{OUT} Accuracy Over Line and Load**
- **1.8V/2.5V Fixed or 1V to 5.5V Adjustable Output Range**
- **2V to 28V Battery Input Range**
- **200/300/450/600kHz Switching Frequency**
- **Adjustable Overvoltage Protection**
- **Adjustable Undervoltage Protection**
- **1.7ms Digital Soft-Start**
- **Drives Large Synchronous-Rectifier FETs**
- **2V ±1% Reference Output**
- **Power-Good Window Comparator**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1844EEP	-40°C to +85°C	20 QSOP
MAX1844EGP*	-40°C to +85°C	20 QFN
MAX1844ETP	-40°C to +85°C	20 Thin QFN

Minimal Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +28V
V_{CC}, V_{DD} to GND .....-0.3V to +6V
OUT, PGOOD, $\overline{SHDN}$ to GND .....-0.3V to +6V
FB, ILIM, $\overline{LATCH}$, OVP, REF, $\overline{SKIP}$,
TON, UVP to GND .....-0.3V to (V_{CC} + 0.3V)
BST to GND .....-0.3V to +34V
CS to GND .....-6V to +30V
DL to GND .....-0.3V to (V_{DD} + 0.3V)
DH to LX .....-0.3V to (BST + 0.3V)
LX to BST .....-6V to +0.3V
REF Short Circuit to GND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
20-Pin QSOP (derate 9.1mW/°C above +70°C).....727mW
20-Pin 5mm × 5mm QFN (derate 20.0mW/°C
above +70°C).....1.60W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = 5V, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	Battery voltage, V+		2		28	V
	V_{CC} , V_{DD}		4.5		5.5	
Error Comparator Threshold (DC Output Voltage Accuracy) (Note 1)	V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC}	FB = OUT	0.99		1.01	V
		FB = GND	2.475	2.5	2.525	
		FB = V_{CC}	1.782	1.8	1.818	
Load Regulation Error	I_{LOAD} = 0 to 3A, $\overline{SKIP}$ = V_{CC}			9		mV
Line Regulation Error	V_{CC} = 4.5V to 5.5V, V+ = 4.5V to 28V			5		mV
FB Input Bias Current			-0.1		+0.1	µA
Output Adjustment Range			1		5.5	V
OUT Input Resistance	FB = GND		90	190	350	kΩ
	FB = V_{CC} or adjustable feedback mode		70	145	270	
Soft-Start Ramp Time	Rising edge of $\overline{SHDN}$ to full current limit			1.7		ms
On-Time	V+ = 24V, V_{OUT} = 2V (Note 2)	TON = GND (600kHz)	140	160	180	ns
		TON = REF (450kHz)	175	200	225	
		TON = unconnected (300kHz)	260	290	320	
		TON = V_{CC} (200kHz)	380	425	470	
Minimum Off-Time	(Note 2)			400	500	ns
Quiescent Supply Current (V_{CC})	FB forced above the regulation point			550	800	µA
Quiescent Supply Current (V_{DD})	FB forced above the regulation point			<1	5	µA
Quiescent Supply Current (V+)				25	40	µA
Shutdown Supply Current (V_{CC})	$\overline{SHDN}$ = GND			<1	5	µA
Shutdown Supply Current (V_{DD})	$\overline{SHDN}$ = GND			<1	5	µA
Shutdown Supply Current (V+)	$\overline{SHDN}$ = GND, V+ = 28V, V_{CC} = V_{DD} = 0 or 5V			<1	5	µA
Reference Voltage	V_{CC} = 4.5V to 5.5V, no external REF load		1.98	2.00	2.02	V
Reference Load Regulation	I_{REF} = 0 to 50µA				0.01	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = 5V, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
REF Sink Current	REF in regulation		10			µA
REF Fault Lockout Voltage	Falling edge, hysteresis = 40mV			1.6		V
Overvoltage Trip Threshold (Fixed-Threshold Mode)	With respect to error comparator threshold, no load OVP = GND, rising edge, hysteresis = 1%		12	14.5	17	%
Overvoltage Comparator Offset (Adjustable-Threshold Mode)	External feedback, measured at FB with respect to V_{OVP}, 1V < V_{OVP} < 1.8V, rising edge, hysteresis =1%		-30		+30	mV
	Internal feedback, measured at OUT with respect to the nominal OUT regulation voltage, 1V < V_{OVP} < 1.8V, rising edge, hysteresis = 1%		-3.5		+3.5	%
OVP Input Leakage Current	1V < V_{OVP} < 1.8V		-100	0	+100	nA
Overvoltage Fault Propagation Delay	FB forced 2% above trip threshold			1.5		µs
Output Undervoltage Protection Trip Threshold (Fixed-Threshold Mode)	With respect to error comparator threshold, UVP = V_{CC}		65	70	75	%
Output Undervoltage Protection Trip Threshold (Adjustable-Threshold Mode)	External feedback, measured at FB with respect to V_{UVP}, 0.4V < V_{UVP} < 1V		-40		+40	mV
	Internal feedback, measured at OUT with respect to the nominal OUT regulation voltage, 0.4V < V_{UVP} < 1V		-5		+5	%
UVP Input Leakage Current	0.4V < V_{UVP} < 1V		-100	<1	+100	nA
Output Undervoltage Protection Blanking Time	From rising edge of $\overline{SHDN}$		10		30	ms
PGOOD Trip Threshold (Lower)	With respect to error comparator threshold, no load		-12.5	-10	-8	%
PGOOD Trip Threshold (Upper)	With respect to error comparator threshold, no load		8	10	12.5	%
PGOOD Propagation Delay	FB forced 2% beyond PGOOD trip threshold, falling			10		µs
PGOOD Output Low Voltage	I_{SINK} = 1mA				0.4	V
PGOOD Leakage Current	High state, forced to 5.5V				1	µA
ILIM Adjustment Range			0.25		3	V
Current-Limit Threshold (Fixed)	GND - V_{CS}, ILIM = V_{CC}		90	100	110	mV
Current-Limit Threshold (Adjustable)	GND - V_{CS}	V_{ILIM} = 0.5V	40	50	60	mV
		V_{ILIM} = 2V	170	200	230	
Current-Limit Threshold (Negative Direction)	GND - V_{CS}, $\overline{SKIP}$ = V_{CC}, ILIM = V_{CC} ,T_A = +25°C		-140	-117	-95	mV
Current-Limit Threshold (Zero Crossing)	GND - V_{CS}, $\overline{SKIP}$ = GND			3		mV
Thermal Shutdown Threshold	Hysteresis = 10°C			150		°C
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis = 20mV, PWM disabled below this level		4.1		4.4	V

High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = 5V, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DH Gate-Driver On-Resistance (Note 4)	BST - LX forced to 5V	MAX1844EEP		1.5	5	Ω
		MAX1844EGP, MAX1844ETP		1.5	6	
DL Gate-Driver On-Resistance (Note 4)	DL, high state	MAX1844EEP		1.5	5	Ω
		MAX1844EGP, MAX1844ETP		1.5	6	
DL Gate-Driver On-Resistance (Note 4)	DL, low state	MAX1844EEP		0.5	1.7	Ω
		MAX1844EGP, MAX1844ETP		0.5	2.7	
DH Gate-Driver Source/Sink Current	DH forced to 2.5V, BST-LX forced to 5V			1		A
DL Gate-Driver Source Current	DL forced to 2.5V			1		A
DL Gate-Driver Sink Current	DL forced to 5V			3		A
Dead Time	DL rising			35		ns
	DH rising			26		
Logic Input High Voltage	$\overline{LATCH}$, $\overline{SHDN}$, $\overline{SKIP}$		2.4			V
Logic Input Low Voltage	$\overline{LATCH}$, $\overline{SHDN}$, $\overline{SKIP}$				0.8	V
Logic Input Current	$\overline{LATCH}$, $\overline{SHDN}$, $\overline{SKIP}$		-1		+1	µA
Dual Mode Threshold, Low	OVP, UVP, FB		0.15	0.20	0.25	V
Dual Mode Threshold, High	OVP, UVP		V_{CC} - 1.5		V_{CC} - 0.4	V
	FB		1.9	2.0	2.1	
TON V_{CC} Level			V_{CC} - 0.4			V
TON Float Voltage			3.15		3.85	V
TON Reference Level			1.65		2.35	V
TON GND Level					0.5	V
TON Input Current	Forced to GND or V_{CC}		-3		+3	µA
ILIM Input Leakage Current			-100	0	+100	nA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = 5V, $\overline{SKIP}$ = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	Battery voltage, V+		2		28	V
	V_{CC} , V_{DD}		4.5		5.5	
Error Comparator Threshold (DC Output Voltage Accuracy) (Note 1)	V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC}	FB = OUT	0.985		1.015	V
		FB = GND	2.462		2.538	
		FB = V_{CC}	1.773		1.827	
On-Time	V+ = 24V, V_{OUT} = 2V (Note 2)	TON = GND (600kHz)	140		180	ns
		TON = REF(450kHz)	175		225	
		TON = Unconnected (300kHz)	260		320	
		TON = V_{CC}(200kHz)	380		470	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = 5V, $\overline{SKIP}$ = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Off-Time	(Note 2)			500	ns
Quiescent Supply Current (V_{CC})	FB forced above the regulation point			800	µA
Quiescent Supply Current (V_{DD})	FB forced above the regulation point			5	µA
Quiescent Supply Current (V+)	Measured at V+			40	µA
Shutdown Supply Current (V_{CC})	$\overline{SHDN}$ = GND			5	µA
Shutdown Supply Current (V_{DD})	$\overline{SHDN}$ = GND			5	µA
Shutdown Supply Current (V+)	$\overline{SHDN}$ = GND, V+ = 28V, V_{CC} = V_{DD} = 0 or 5V			5	µA
Reference Voltage	V_{CC} = 4.5V to 5.5V, no external REF load	1.98		2.02	V
Overvoltage Trip Threshold (Fixed-Threshold Mode)	With respect to error comparator threshold, no load OVP = GND, rising edge, hysteresis = 1%	12		17	%
Overvoltage Comparator Offset (Adjustable-Threshold Mode)	External feedback, measured at FB with respect to V_{OVP}, 1V < V_{OVP} 1.8V, rising edge, hysteresis = 1%	-30		+30	mV
	Internal feedback, measured at OUT with respect to the nominal OUT regulation voltage, 1V < V_{OVP} < 1.8V	-3.5		+3.5	%
PGOOD Trip Threshold (Lower)	With respect to error comparator threshold, no load OUT falling edge, hysteresis = 1%	-12.5		-7.5	%
PGOOD Trip Threshold (Upper)	With respect to error comparator threshold, no load OUT rising edge, hysteresis = 1%	7.5		12.5	%
PGOOD Output Low Voltage	I_{SINK} = 1mA			0.4	V
PGOOD Leakage Current	High state, forced to 5.5V			1	µA
Current-Limit Threshold (Fixed)	GND - V_{CS}, ILIM = V_{CC}	85		115	mV
Current-Limit Threshold (Adjustable)	GND - V_{CS}, V_{ILIM} = 0.5V	35		65	mV
	GND - V_{CS}, V_{ILIM} = 2V	160		240	
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis = 20mV, PWM disabled below this level	4.1		4.4	V
Logic Input High Voltage	$\overline{LATCH}$, $\overline{SHDN}$, $\overline{SKIP}$	2.4			V
Logic Input Low Voltage	$\overline{LATCH}$, $\overline{SHDN}$, $\overline{SKIP}$			0.8	V
Logic Input Current	$\overline{LATCH}$, $\overline{SHDN}$, $\overline{SKIP}$	-1		1	µA

Note 1: When the inductor is in continuous conduction, the output voltage will have a DC regulation level higher than the error comparator threshold by 50% of the ripple. In discontinuous conduction ($\overline{SKIP}$ = GND, light load), the output voltage will have a DC regulation level higher than the trip level by approximately 1.5% due to slope compensation.

Note 2: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX = GND, V_{BST} = 5V, and a 250pF capacitor connected from DH to LX. Actual in-circuit times may differ due to MOSFET switching speeds.

Note 3: Specifications to -40°C are guaranteed by design, not production tested.

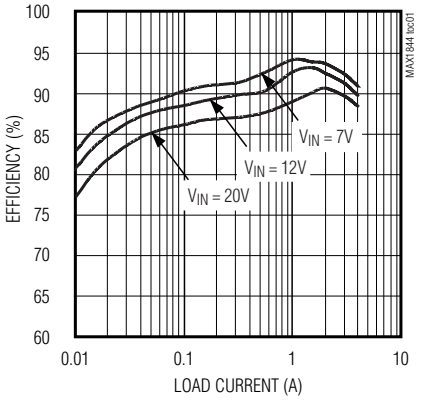
Note 4: Production testing limitations due to package handling require relaxed maximum on-resistance specifications for the QFN package. The MAX1844EEP, MAX1844EGP, and MAX1844ETP contain the same die and the QFN package imposes no additional resistance in-circuit.

High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

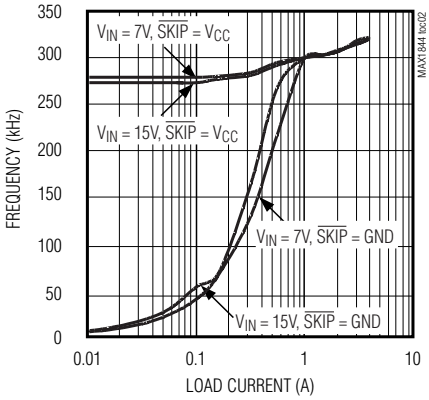
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 15V, $\overline{SKIP}$ = GND, TON = unconnected, T_A = +25°C, unless otherwise noted.)

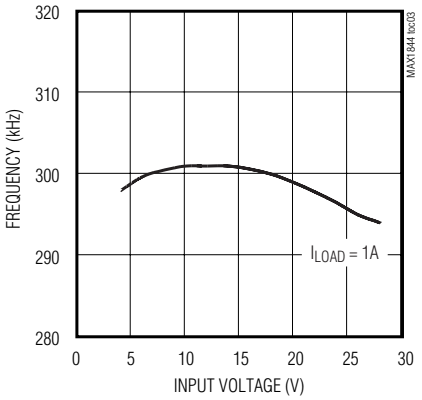
EFFICIENCY vs. LOAD CURRENT



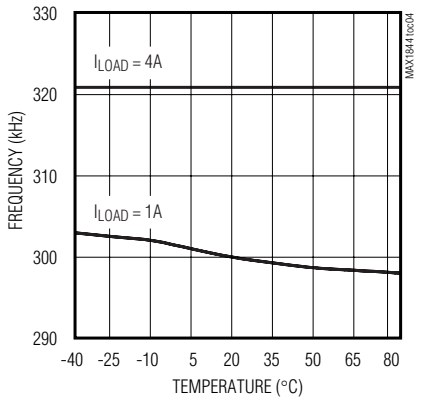
FREQUENCY vs. LOAD CURRENT



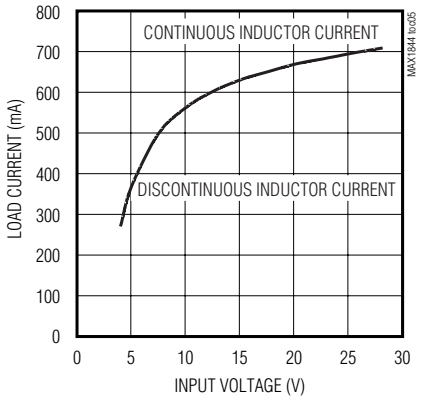
FREQUENCY vs. INPUT VOLTAGE



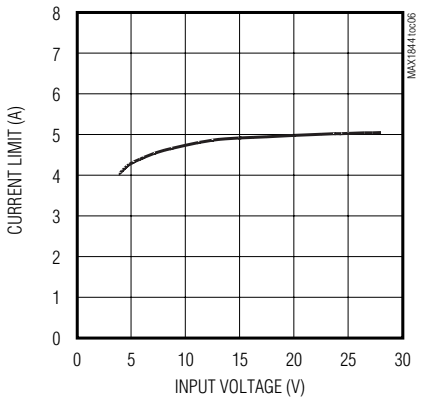
FREQUENCY vs. TEMPERATURE



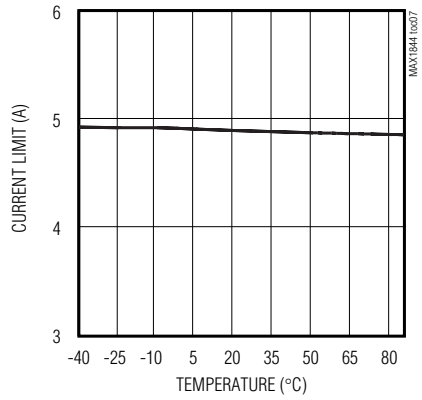
CONTINUOUS-TO-DISCONTINUOUS INDUCTOR CURRENT vs. INPUT VOLTAGE



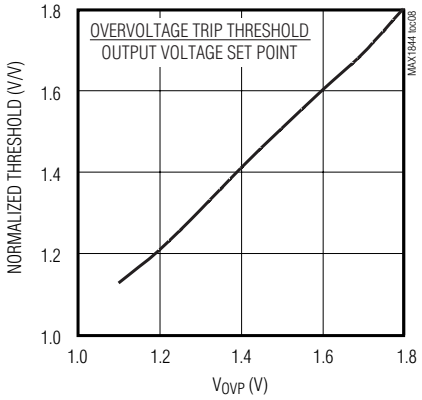
CURRENT LIMIT vs. INPUT VOLTAGE



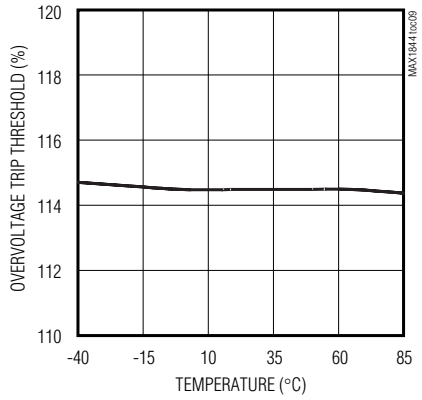
CURRENT LIMIT vs. TEMPERATURE



NORMALIZED OVERVOLTAGE TRIP THRESHOLD vs. V_{OVP}



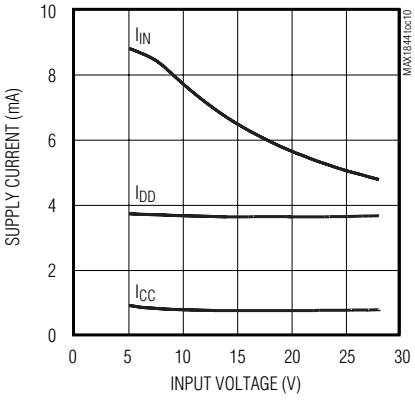
OVERVOLTAGE TRIP THRESHOLD vs. TEMPERATURE



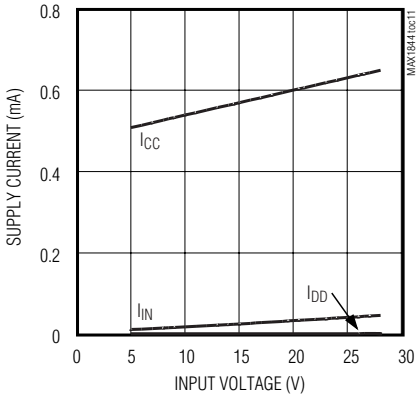
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 15V, $\overline{SKIP}$ = GND, TON = unconnected, T_A = +25°C, unless otherwise noted.)

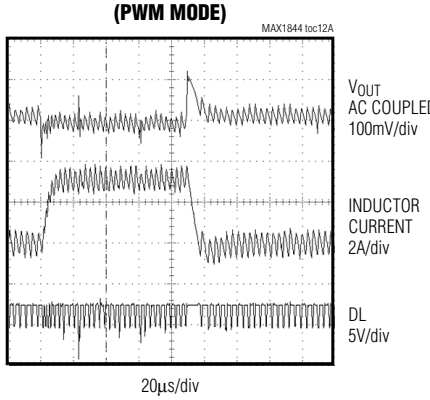
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (PWM MODE)



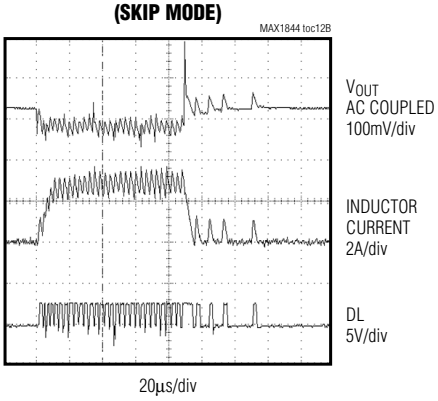
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP MODE)



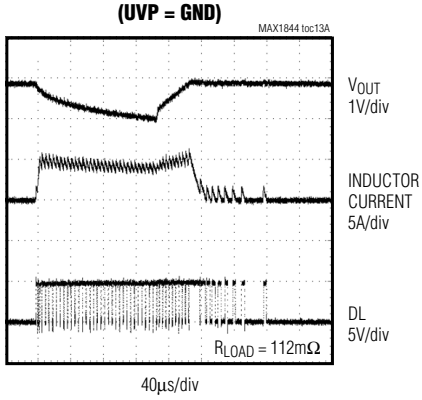
LOAD-TRANSIENT RESPONSE (PWM MODE)



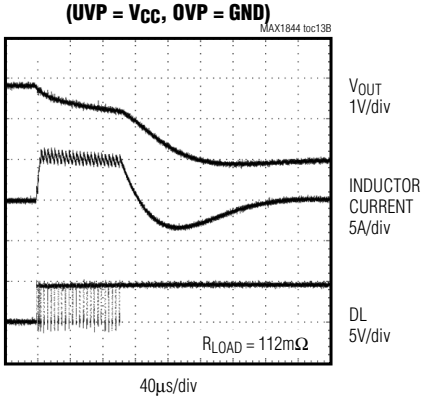
LOAD-TRANSIENT RESPONSE (SKIP MODE)



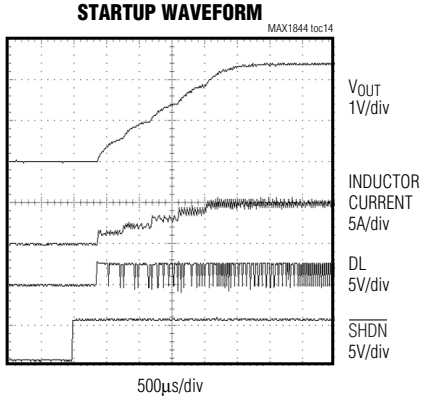
OUTPUT OVERLOAD WAVEFORM (UVP = GND)



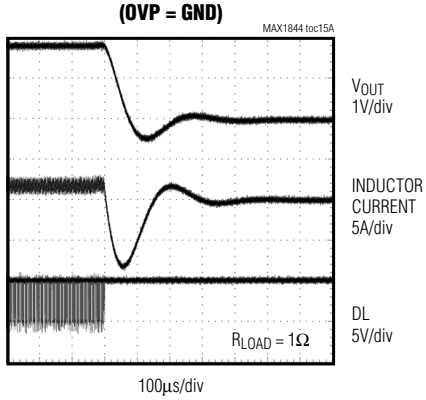
OUTPUT OVERLOAD WAVEFORM (UVP = V_{CC}, OVP = GND)



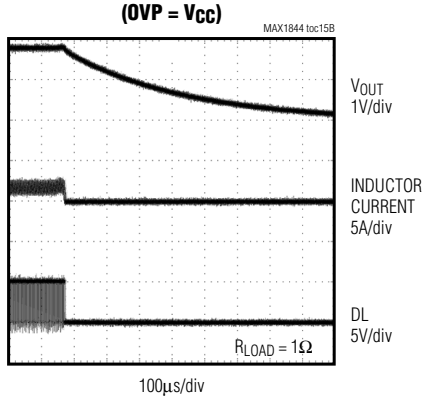
STARTUP WAVEFORM



SHUTDOWN WAVEFORM (OVP = GND)



SHUTDOWN WAVEFORM (OVP = V_{CC})



High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

Pin Description

PIN		NAME	FUNCTION
QSOP	QFN		
1	18	CS	Current-Sense Input. Connect a low-value current-sense resistor between CS and GND for accurate current sensing. For lower power dissipation (less accurate) current sensing, connect CS to LX to use the synchronous rectifier as the sense resistor. The PWM controller will not begin a cycle unless the current sensed at CS is less than the current-limit threshold programmed at ILIM.
2	19	$\overline{\text{LATCH}}$	Overvoltage Protection Latch Control Input. The synchronous rectifier MOSFET is always forced to the on state when an overvoltage fault is detected. If $\overline{\text{LATCH}}$ is low, the synchronous rectifier remains on until either OVP is brought high, $\overline{\text{SHDN}}$ is toggled, or V_{CC} is cycled below 1V. If $\overline{\text{LATCH}}$ is high, normal operation resumes when the overvoltage condition ends.
3	20	$\overline{\text{SHDN}}$	Shutdown Control Input. Drive $\overline{\text{SHDN}}$ to GND to force the MAX1844 into shutdown. Drive or connect to V_{CC} for normal operation. A rising edge on $\overline{\text{SHDN}}$ clears the overvoltage and undervoltage protection fault latches.
4	1	OVP	Overvoltage Protection Control Input. An overvoltage fault occurs if the internal or external feedback voltage exceeds the voltage at OVP. Apply a voltage between 1V and 1.8V to set the overvoltage limit between 100% and 180% of nominal output voltage. Connect to GND to assert the default overvoltage limit at 114% of the nominal output voltage. Connect to V_{CC} to disable overvoltage fault detection and clear the overvoltage protection fault latch.
5	2	FB	Feedback Input. Connect to V_{CC} for a 1.8V fixed output or to GND for a 2.5V fixed output. For an adjustable output (1V to 5.5V), connect FB to a resistive-divider from the output voltage. The FB regulation level is 1V.
6	3	OUT	Output Voltage Sense Connection. Connect directly to the junction of the external output filter capacitors. OUT senses the output voltage to determine the on-time for the high-side switching MOSFET. OUT also serves as the feedback input in fixed-output modes.
7	4	ILIM	Current-Limit Threshold Adjustment. The current-limit threshold at CS is 0.1 times the voltage at ILIM. Connect ILIM to a resistive-divider (typically from REF) to set the current-limit threshold between 25mV and 300mV (with 0.25V to 3V at ILIM). Connect to V_{CC} to assert the 100mV default current-limit threshold.
8	5	REF	2V Reference Voltage Output. Bypass to GND with a 0.22µF (min) bypass capacitor. Can supply 50µA for external loads. Reference turns off in shutdown.
9	6	UVP	Undervoltage Protection Control Input. An undervoltage fault occurs if the internal or external feedback voltage is less than the voltage at UVP. Apply a voltage between 0.4V and 1V to set the undervoltage limit between 40% and 100% of the nominal output voltage. Connect to V_{CC} to assert the default undervoltage limit of 70% of the nominal output voltage. Connect to GND to disable undervoltage fault detection and clear the undervoltage protection latch.
10	7	PGOOD	Power-Good Open-Drain Output. PGOOD is low when the output voltage is more than 10% above or below the normal regulation point or during soft-start. PGOOD is high impedance when the output is in regulation and the soft-start circuit has terminated. PGOOD is low in shutdown.
11	8	GND	Analog and Power Ground
12	9	DL	Synchronous Rectifier Gate-Driver Output. Swings from GND to V_{DD}.
13	10	V_{DD}	Supply Input for the DL Gate Drive. Connect to the system supply voltage, 4.5V to 5.5V. Bypass to GND with a 1µF (min) ceramic capacitor.

Pin Description (continued)

PIN		NAME	FUNCTION
QSOP	QFN		
14	11	V_{CC}	Analog Supply Input. Connect to the system supply voltage, 4.5V to 5.5V, with a series 20Ω resistor. Bypass to GND with a 1µF (min) ceramic capacitor.
15	12	TON	On-Time Selection-Control Input. This four-level logic input sets the nominal DH on-time. Connect to GND, REF, V_{CC}, or leave TON unconnected to select the following nominal switching frequencies: GND = 600kHz, REF = 450kHz, floating = 300kHz, and V_{CC} = 200kHz.
16	13	V+	Battery Voltage Sense Connection. Connect to input power source. V+ is used only to set the PWM one-shot timing.
17	14	$\overline{SKIP}$	Pulse-Skipping Control Input. Connect to V_{CC} for low-noise, forced-PWM mode. Connect to GND to enable pulse-skipping operation.
18	15	BST	Boost Flying-Capacitor Connection. Connect to an external capacitor and diode according to the Standard Application Circuit (Figure 1). See the *MOSFET Gate Drivers (DH, DL)* section.
19	16	LX	External Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver.
20	17	DH	High-Side Gate-Driver Output. Swings from LX to BST.

Table 1. Component Selection for Standard Applications

COMPONENT	2.5V AT 4A
C1 Input Capacitor	10µF, 25V Taiyo Yuden TMK432BJ106KM or TDK C4532X5R1E106M
C2 Output Capacitor	330µF, 6V Kemet T510X477108M006AS or Sanyo 6TPB330M
D1 Schottky	Nihon EP10QY03
L1 Inductor	4.7µH Coilcraft DO33116P-682 or Sumida CDRH124-4R7MC
Q1 High-Side MOSFET	Fairchild Semiconductor 1/2 FDS6982A
Q2 Low-Side MOSFET	Fairchild Semiconductor 1/2 FDS6982A
R_{SENSE}	0.015Ω ±1%, 0.5W resistor IRC LR2010-01-R015F or Dale WSL-2010-R015F

Table 2. Component Suppliers

SUPPLIER	USA PHONE	FACTORY FAX
Coilcraft	847-639-6400	1-847-639-1469
Dale-Vishay	203-452-5664	1-203-452-5670
Fairchild	408-822-2181	1-408-721-1635
IRC	800-752-8708	1-828-264-7204
Kemet	408-986-0424	1-408-986-1442
NIEC (Nihon)	805-867-2555*	81-3-3494-7414
Sanyo	619-661-6835	81-7-2070-1174
Sumida	847-956-0666	81-3-3607-5144
Taiyo Yuden	408-573-4150	1-408-573-4159
TDK	847-390-4461	1-847-390-4405

**Distributor*

Standard Application Circuit

The standard application circuit (Figure 1) generates a 2.5V rail for general-purpose use in a notebook computer.

See Table 1 for component selections. Table 2 lists component manufacturers.

High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

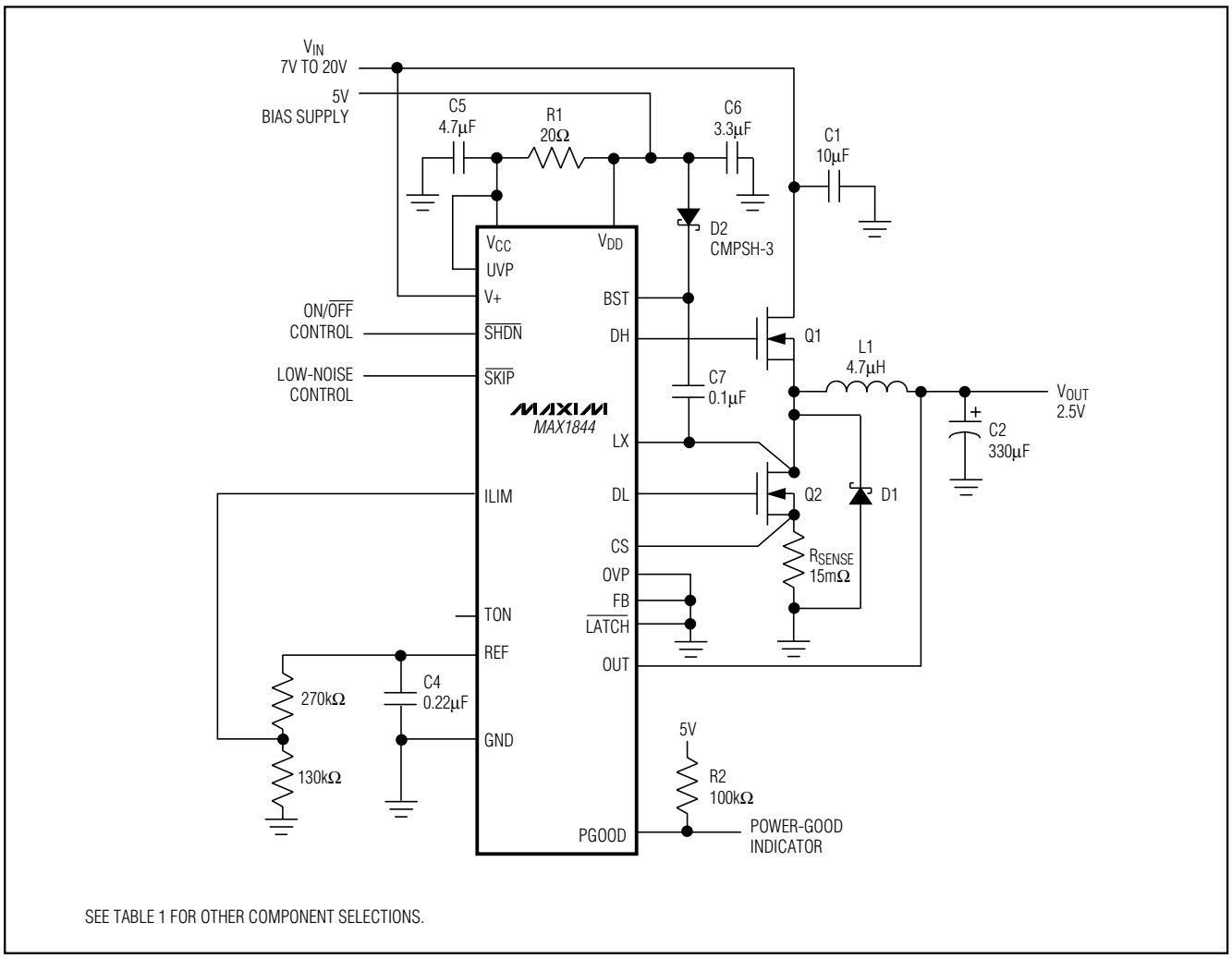


Figure 1. Standard Application Circuit

Detailed Description

The MAX1844 buck controller is targeted for low-voltage power supplies for notebook computers. Maxim's proprietary Quick-PWM pulse-width modulator in the MAX1844 is specifically designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes.

5V Bias Supply (V_{CC} and V_{DD})

The MAX1844 requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's 95% efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the 5V supply can be generated with an external linear regulator such as the MAX1615.

The battery and 5V bias inputs can be connected together if the input source is a fixed 4.5V to 5.5V supply. If the 5V bias supply is powered up prior to the

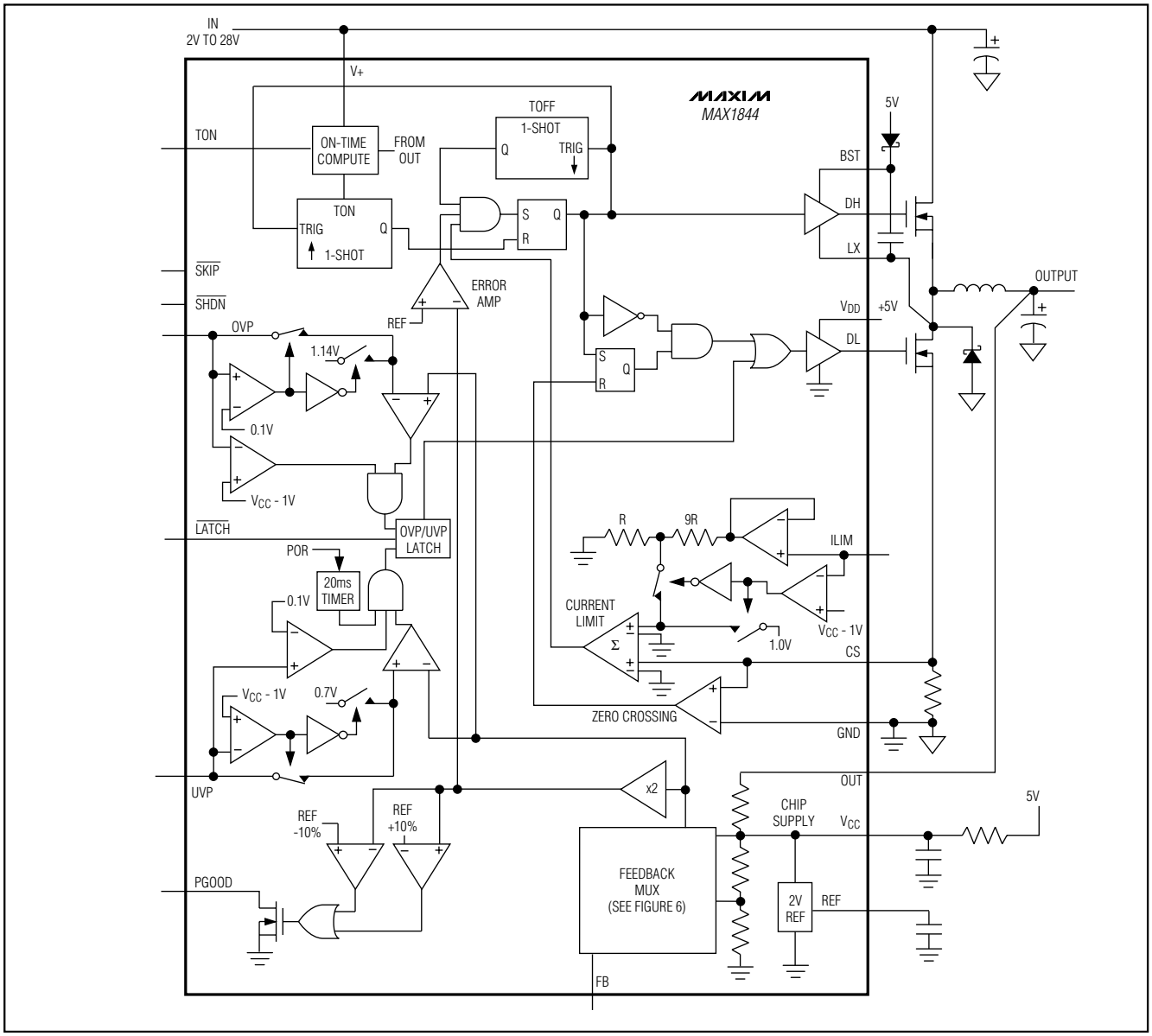


Figure 2. MAX1844 Functional Diagram

battery supply, the enable signal ($\overline{SHDN}$) must be delayed until the battery voltage is present in order to ensure startup. The 5V bias supply provides V_{CC} and gate-drive power, so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f (Q_{G1} + Q_{G2}) = 5mA \text{ to } 30mA \text{ (typ)}$$

where I_{CC} is 550µA (typ), f is the switching frequency, and Q_{G1} and Q_{G2} are the MOSFET data sheet total gate-charge specification limits at V_{GS} = 5V.

Free-Running, Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time on-demand PWM with voltage feed-forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse

High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

Table 3. Operating Mode Truth Table

$\overline{SHDN}$	$\overline{SKIP}$	DL	MODE	COMMENTS
0	X	High or Low	Shutdown	Low-power shutdown state. DL is forced to V_{DD} if OVP is enabled and to GND if OVP is disabled. I_{CC} < 1µA typ.
1	V_{CC}	Switching	Run (PWM), Low Noise	Low-noise operation with no automatic switchover. Fixed-frequency PWM action is forced regardless of load. Inductor current reverses at light load levels. Low noise, high I_Q.
1	GND	Switching	Run (PFM/PWM)	Normal operation with automatic PWM/PFM switchover for pulse skipping at light loads. Best light-load efficiency.
1	X	High	Fault	Fault latch has been set by overvoltage protection, output UVLO, or thermal shutdown. Device will remain in FAULT mode until V_{CC} power is cycled or $\overline{SHDN}$ is toggled.

Table 4. Frequency Selection Guidelines

FREQUENCY (kHz)	TYPICAL APPLICATION	COMMENTS
200 TON = V_{CC}	4-cell Li+ notebook	Use for absolute best efficiency.
300 TON = Float	4-cell Li+ notebook	Considered mainstream by current standards.
450 TON = REF	3-cell Li+ notebook	Useful in 3-cell systems for lighter loads than the CPU core or where size is key.
600 TON = GND	+5V input	Good operating point for compound buck designs or desktop circuits.

width is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (400ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot (TON)

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as measured by the V+ input, and proportional to the output voltage. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The on-time is given by:

$$\text{On-Time} = K (V_{OUT} + 0.075V) / V_{IN}$$

where K (switching period) is set by the TON pin-strap connection (Table 4), and 0.075V is an approximation to accommodate for the expected drop across the low-side MOSFET switch. One-shot timing error increases for the shorter on-time settings due to fixed propagation delays; it is approximately ±12.5% at 600kHz and 450kHz, and ±10% at the two slower settings. This translates to reduced switching-frequency accuracy at higher frequencies (Table 5). Switching frequency increases as a function of load current due to the increasing drop across the low-side MOSFET, which causes a faster inductor-current discharge ramp. The on-times guaranteed in the *Electrical Characteristics* are influenced by switching delays in the external high-side power MOSFET.

Two external factors that influence switching-frequency accuracy are resistive drops in the two conduction loops (including inductor and PC board resistance) and the dead-time effect. These effects are the largest contributors to the change of frequency with changing load current. The dead-time effect increases the effective on-time, reducing the switching frequency as one or both dead times are added to the effective on-time. It occurs only in PWM mode ($\overline{SKIP}$ = high) when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the low-to-high dead time.

For loads above the critical conduction point, the actual switching frequency is:

$$f = \frac{V_{OUT} + V_{DROP1}}{t_{ON}(V_{IN} + V_{DROP2})}$$

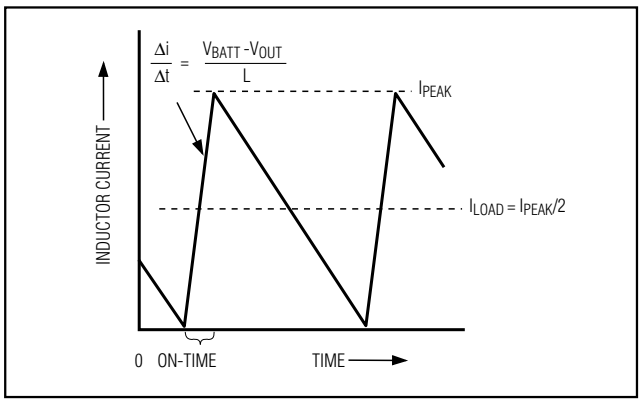


Figure 3. Pulse-Skipping/Discontinuous Crossover Point

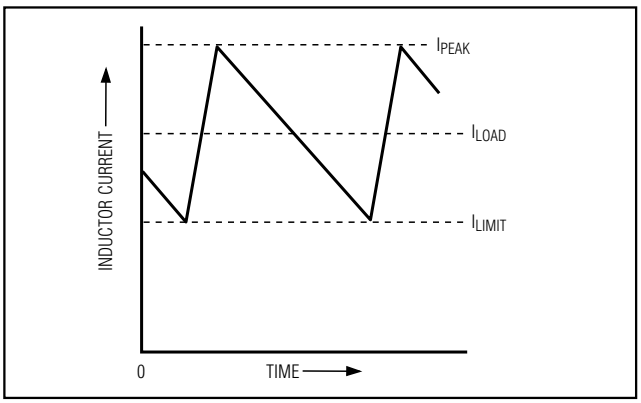


Figure 4. "Valley" Current-Limit Threshold Point

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the resistances in the charging path, and t_{ON} is the on-time calculated by the MAX1844.

Automatic Pulse-Skipping Switchover

In skip mode ($\overline{SKIP}$ low), an inherent automatic switchover to PFM takes place at light loads (Table 3). This switchover is effected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the "critical conduction" point; see the Continuous to Discontinuous Inductor Current vs. Input Voltage graph in the *Typical Operating Characteristics*). In low-duty-cycle applications, this threshold is relatively constant, with only a minor dependence on battery voltage.

$$I_{LOAD(SKIP)} \approx \frac{KV_{OUT}}{2L} \times \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

where K is the on-time scale factor (Table 5). The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(\overline{SKIP})}$, is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 3). For example, in the standard application circuit with K = 3.3µs (Table 5), V_{OUT} = 2.5V, V_{IN} = 15V, and L = 6.8µH, switchover to pulse-skipping operation occurs at I_{LOAD} = 0.51A or about 1/8 full load. The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used.

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input voltage levels).

DC output accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the output voltage will have a DC regulation level higher than the trip level by 50% of the ripple. In discontinuous conduction ($\overline{SKIP}$ = GND, light load), the output voltage will have a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation.

Forced-PWM Mode ($\overline{SKIP}$ = High)

The low-noise forced-PWM mode ($\overline{SKIP}$ = high) disables the zero-crossing comparator, which controls the low-side switch on-time. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads while DH maintains a duty factor of V_{OUT}/V_{IN}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant, but it comes at a cost: the no-load battery current can be 10mA to 40mA, depending on the external MOSFETs.

Forced-PWM mode is most useful for reducing audio-frequency noise, improving load-transient response, providing sink-current capability for dynamic output voltage adjustment, and improving the cross-regulation of multiple-output applications that use a flyback transformer or coupled inductor.

High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

Current-Limit Circuit (ILIM)

The current-limit circuit employs a unique "valley" current-sensing algorithm (Figure 4). If the magnitude of the current-sense voltage at CS is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and battery voltage.

There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit and therefore tracks the positive current limit when ILIM is adjusted.

The current-limit threshold is adjusted with an external resistor-divider at ILIM. A 1µA (min) divider current is recommended. The current-limit threshold adjustment range is from 25mV to 300mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/10 the voltage seen at ILIM. The threshold defaults to 100mV when ILIM is connected to V_{CC}. The logic threshold for switchover to the 100mV default value is approximately V_{CC} - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signal seen by CS. Mount or place the IC close to the low-side MOSFET and sense resistor with short, direct traces, making a Kelvin sense connection to the sense resistor.

In Figure 1, the Schottky diode (D1) provides a current path parallel to the Q2/R_{SENSE} current path. Accurate current sensing demands D1 to be off while Q2 conducts. Avoid large current-sense voltages that, combined with the voltages across Q2, would allow D1 to conduct. If very large sense voltages are used, connect D1 in parallel with Q2.

MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook environment, where a large V_{BATT} - V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL output and prevents the high-side FET from turning on until DL is fully off. There must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate for the adaptive dead-time circuit to work properly; otherwise, the sense circuitry in the MAX1844 will interpret the MOSFET gate as "off" while there is actually still charge left on the gate. Use very short, wide traces measuring no more than 20 squares (50 to 100 mils wide if the MOSFET is 1 inch from the MAX1844).

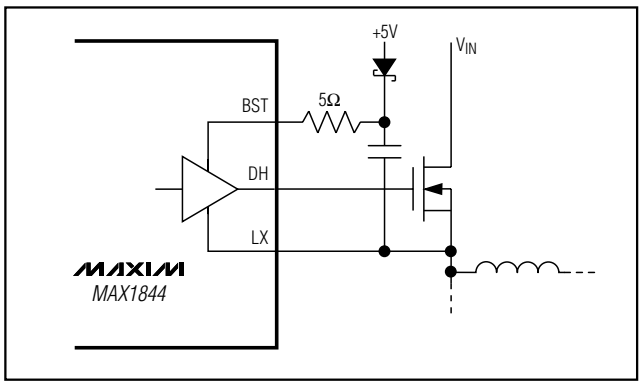


Figure 5. Reducing the Switching-Node Rise Time

The dead time at the other edge (DH turning off) is determined by a fixed 35ns (typ) internal delay.

The internal pulldown transistor that drives DL low is robust, with a 0.5Ω (typ) on-resistance. This helps prevent DL from being pulled up during the fast rise-time of the inductor node, due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFET. However, for high-current applications, there are still some combinations of high- and low-side FETs that will cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with BST, which increases the turn-on time of the high-side FET without degrading the turn-off time (Figure 5).

POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and soft-start counter, and preparing the PWM for operation. Until V_{CC} reaches 4.2V, V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching. DL is held low if overvoltage protection is disabled, and held high if overvoltage protection is enabled. See the *Output Overvoltage Protection* section. When V_{CC} rises above 4.2V, an internal digital soft-start timer begins to ramp up the maximum allowed current limit. The ramp occurs in five steps: 20%, 40%, 60%, 80%, and 100%; 100% current is available after 1.7ms ±50%.

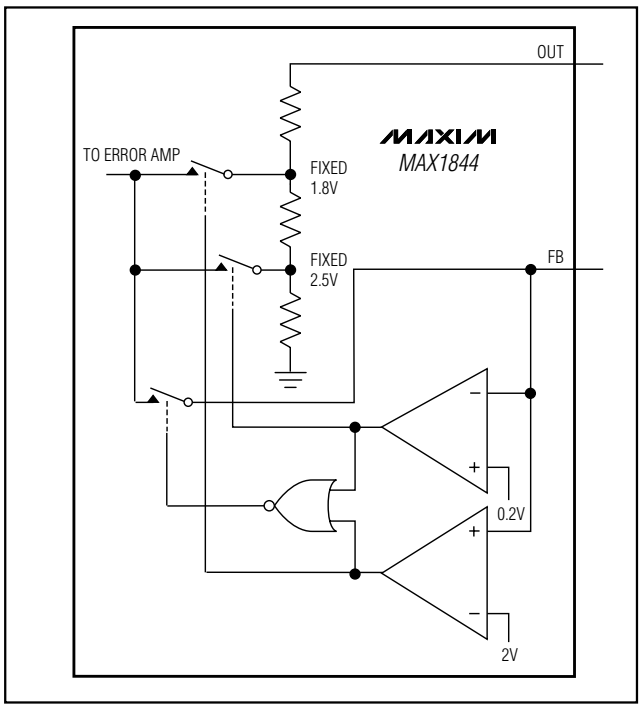


Figure 6. Feedback Mux

Power-Good Output (PGOOD)

The PGOOD window comparator continuously monitors the output. PGOOD is actively held low in shutdown, standby, and soft-start. After digital soft-start terminates, PGOOD is released if the output is within 10% of the nominal output voltage setting. Note that the PGOOD window detector is completely independent of the overvoltage and undervoltage protection fault detectors.

Output Overvoltage Protection

OVP controls the output overvoltage protection function. Connect OVP to V_{CC} to disable overvoltage protection. If overvoltage protection is enabled, the output is continuously monitored. If the output exceeds the overvoltage protection threshold, overvoltage protection is triggered and the DL low-side gate-driver output is forced high. This turns on the low-side MOSFET switch to rapidly discharge the output capacitor and reduce the output voltage.

If $\overline{LATCH}$ is high, normal operation resumes when the overvoltage condition ends. If $\overline{LATCH}$ is low, the DL gate-driver output remains high until OVP is brought high, $\overline{SHDN}$ is toggled, or V_{CC} is cycled below 1V. When the condition that caused the overvoltage persists (such as a shorted high-side MOSFET), the battery fuse will open. If overvoltage protection is enabled,

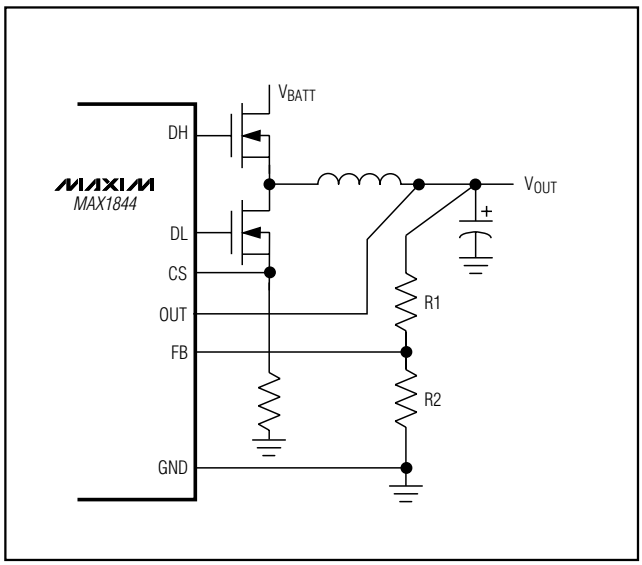


Figure 7. Setting V_{OUT} with a Resistor-Divider

DL is kept high continuously in shutdown mode or when UVLO is active.

Note that forcing DL high in shutdown causes the output voltage to go slightly negative when energy has been previously stored in the LC tank circuit (see the shutdown waveforms in the *Typical Operating Characteristics*). If the load cannot tolerate being forced to a negative voltage, it may be desirable to place a power Schottky diode across the output to act as a reverse-polarity clamp.

Output Undervoltage Protection

UVP controls the output undervoltage protection function. Connect UVP to GND to disable undervoltage protection. The output undervoltage protection function is similar to foldback current limiting but employs a timer and latch rather than a variable current limit. If the output voltage is below the undervoltage protection threshold after the output undervoltage protection blanking time has elapsed, the PWM is latched off and does not restart until V_{CC} power is cycled. $\overline{SHDN}$ is toggled, or UVP is brought low.

Connect UVP to V_{CC} to enable the default undervoltage trip threshold of 70% of nominal. To select a different threshold, drive UVP to a voltage between 0.4V and 1V for a threshold between 40% and 100% of nominal.

High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

Fixed Output Voltages

The MAX1844's Dual Mode™ operation allows the selection of common voltages without requiring external components (Figure 6). Connect FB to GND for a fixed 2.5V output or to V_{CC} for a 1.8V output, or connect FB directly to OUT for a fixed 1V output.

Setting V_{OUT} with a Resistor-Divider

The output voltage can be adjusted from 1V to 5.5V with a resistor-divider if desired (Figure 7). The equation for adjusting the output voltage is:

$$V_{OUT} = V_{FB}\left(1 + \frac{R1}{R2}\right)$$

where V_{FB} is 1V.

Design Procedure

Component selection for the MAX1844 is primarily dictated by the following four criteria:

1) **Input voltage range**. The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. Lower input voltages result in better efficiency.

2) **Maximum load current**. There are two values to consider. The *peak load current* ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The *continuous load current* (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.

3) **Switching frequency**. This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical (Table 4).

4) **Inductor operating point**. This choice provides trade-offs between size vs. efficiency. Low inductor values cause large ripple currents, resulting in the smallest size, but poor efficiency and high output ripple. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit.

   The MAX1844's pulse-skipping algorithm initiates skip mode at the critical conduction point. So, the inductor operating point also determines the load-current value at which PFM/PWM switchover occurs.

These four factors impact the component selection process. Selecting components and calculating their effect on the MAX1844's operation is best done with a spreadsheet. Using the formulas provided, calculate the LIR (the ratio of the inductor ripple current to the designed maximum load current) for both the minimum and maximum input voltages. Maintaining an LIR within a 20% to 50% range is recommended. The use of a spreadsheet allows quick evaluation of component selection.

Inductor Selection

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f \times LIR \times I_{LOAD(MAX)}}$$

Example: $I_{LOAD(MAX)}$ = 8A, V_{IN} = 7V, V_{OUT} = 1.5V, f = 300kHz, 33% ripple current or LIR = 0.33.

$$L = \frac{1.5V\,(7V - 1.5V)}{7V \times 300kHz \times 0.33 \times 8A} = 1.49\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}).

$$I_{PEAK} = I_{LOAD(MAX)} + [(LIR / 2) \times I_{LOAD(MAX)}]$$

Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values.

Transient Response

The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step.

Dual Mode is a trademark of Maxim Integrated Products.

The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{(\Delta I_{LOAD(MAX)})^2 \times L}{2 \times C_{OUT} \times DUTY\ (V_{IN(MIN)} - V_{OUT})}$$

where

$$DUTY = \frac{K\ (V_{OUT} + 0.075V)/\ V_{IN}}{K\ (V_{OUT} + 0.075V)/\ V_{OUT} + \text{min off-time}}$$

and minimum off-time = 400ns (typ) (see Table 5 for K values).

The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{L \times \left(\Delta I_{LOAD(MAX)}\right)^2}{2C_{OUT}V_{OUT}}$$

Setting the Current Limit

For most applications, set the MAX1844 current limit by the following procedure:

1) Determine the minimum (valley) inductor current $I_{L(MIN)}$ under conditions when V_{IN} is small, V_{OUT} is large, and load current is maximum. The minimum inductor current is I_{LOAD} minus half the ripple current (Figure 4).
2) The sense resistor determines the achievable current-limit accuracy. There is a trade-off between current-limit accuracy and sense-resistor power dissipation. Most applications employ a current-sense voltage of 50mV to 100mV. Choose a sense resistor so that:

$$R_{SENSE} = \text{CS Threshold Voltage} / I_{L(MIN)}$$

Extremely cost-sensitive applications that do not require high-accuracy current sensing can use the on-resistance of the low-side MOSFET switch in place of the sense resistor by connecting CS to LX (Figure 8b). Use the worst-case value for $R_{DS(ON)}$ from the MOSFET Q2 data sheet, and add a margin of 0.5%/°C for the rise in $R_{DS(ON)}$ with temperature. Then use that $R_{DS(ON)}$ value and $I_{L(MIN)}$ from step 1 above to determine the CS threshold voltage. If the default 100mV threshold is unacceptable, set the value as in step 2 above.

In all cases, ensure an acceptable CS threshold voltage despite inaccuracies in resistor values.

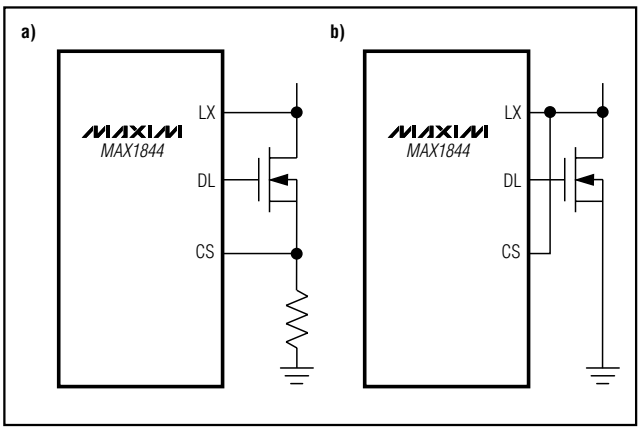


Figure 8. Current-Sense Circuits

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

For CPU core voltage converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{DIP}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output voltage ripple:

$$R_{ESR} \le \frac{V_{P-P}}{LIR \times I_{LOAD(MAX)}}$$

The actual microfarad capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, and other electrolytics).

When using low-capacity filter capacitors, such as ceramic or polymer types, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (also, see the V_{SAG} and V_{SOAR} equation in the *Transient Response* section).

High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

Output Capacitor Stability Considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation:

$$f_{ESR} = \frac{f}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz.

Tantalum and OS-CON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 25kHz. In the design example used for inductor selection, the ESR needed to support 60mV$_{P-P}$ ripple is 60mV/2.7A = 22mΩ. Two 470µF/4V Kemet T510 low-ESR tantalum capacitors in parallel provide 22mΩ (max) ESR. Their typical combined ESR results in a zero at 27kHz, well within the bounds of stability.

Do not put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic, unstable operation. However, it's easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and fast-feedback loop instability.

Double-pulsing occurs due to noise on the output or because the ESR is so low that there isn't enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillations at the output after line or load perturbations that can trip the overvoltage protection latch or cause the output voltage to fall below the tolerance limit.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to monitor simultaneously the inductor current with an AC current probe. Don't allow more than one cycle of ringing after the initial step-response under- or overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-up surge currents.

$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}}{V_{IN}}\right)$$

For optimal circuit reliability, choose a capacitor that has less than 10°C temperature rise at the peak ripple current.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability (>5A) when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

For maximum efficiency, choose a high-side MOSFET (Q1) that has conduction losses equal to the switching losses at the optimum battery voltage (15V). Check to ensure that the conduction losses at **minimum** input voltage do not exceed the package thermal limits or violate the overall thermal budget. Check to ensure that conduction losses plus switching losses at the **maximum** input voltage do not exceed the package ratings or violate the overall thermal budget.

Choose a low-side MOSFET (Q2) that has the lowest possible $R_{DS(ON)}$, comes in a moderate to small package (i.e., SO-8), and is reasonably priced. Ensure that the MAX1844 DL gate driver can drive Q2; in other words, check that the gate is not pulled up by the high-side switch turn on, due to parasitic drain-to-gate capacitance, causing cross-conduction problems. Switching losses are not an issue for the low-side MOSFET since it is a zero-voltage switched device when used in the buck topology.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET, the worst-case power dissipation due to resistance occurs at minimum battery voltage:

$$PD(Q1\ Resistive) = (V_{OUT} / V_{IN(MIN)}) \times I_{LOAD}^2 \times R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissi-

pation limits often limits how small the MOSFET can be. Again, the optimum occurs when the switching (AC) losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the CV^2f switching loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, reconsider the choice of MOSFET.

Calculating the power dissipation in Q1 due to switching losses is difficult, since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including a sanity check using a thermocouple mounted on Q1.

$$PD(Q1\ switching) = \frac{C_{RSS} \times V_{IN(MAX)}^2 \times f \times I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of Q1, and I_{GATE} is the peak gate-drive source/sink current (1A typ).

For the low-side MOSFET, Q2, the worst-case power dissipation always occurs at maximum battery voltage:

$$PD(Q2) = (1 - V_{OUT} / V_{IN(MAX)}) \times I_{LOAD}^2 \times R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit. To protect against this possibility, you must "overdesign" the circuit to tolerate $I_{LOAD} = I_{LIMIT(HIGH)} + [(LIR / 2) \times I_{LOAD(MAX)}]$, where $I_{LIMIT(HIGH)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and sense-resistance variation. If short-circuit protection without overload protection is adequate, enable undervoltage protection, and use $I_{LOAD(MAX)}$ to calculate component stresses.

Choose a Schottky diode D1 having a forward voltage drop low enough to prevent the Q2 MOSFET body diode from turning on during the dead time. As a general rule, a diode having a DC current rating equal to 1/3 of the load current is sufficient. This diode is optional, and if efficiency isn't critical it can be removed.

Applications Information

Dropout Performance

The output voltage adjust range for continuous-conduction operation is restricted by the nonadjustable 500ns (max) minimum off-time one-shot. For best dropout performance, use the slower (200kHz) on-time settings. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies (Table 5). Also, keep in mind that transient response performance of buck regulators operated close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Transient Response* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP} / \Delta I_{DOWN}$ indicates the circuit's ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current will be less able to increase during each switching cycle, and V_{SAG} will greatly increase unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but this may be adjusted up or down to allow trade-offs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \frac{\left(V_{OUT} + V_{DROP1}\right)}{1 - \left(\frac{t_{OFF(MIN)} \times h}{K}\right)} + V_{DROP2} - V_{DROP1}$$

where V_{DROP1} and V_{DROP2} are the parasitic voltage drops in the discharge and charge paths, $t_{OFF(MIN)}$ is from the *Electrical Characteristics* table, and K is taken from Table 5. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then operating frequency must be reduced or output capacitance added to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

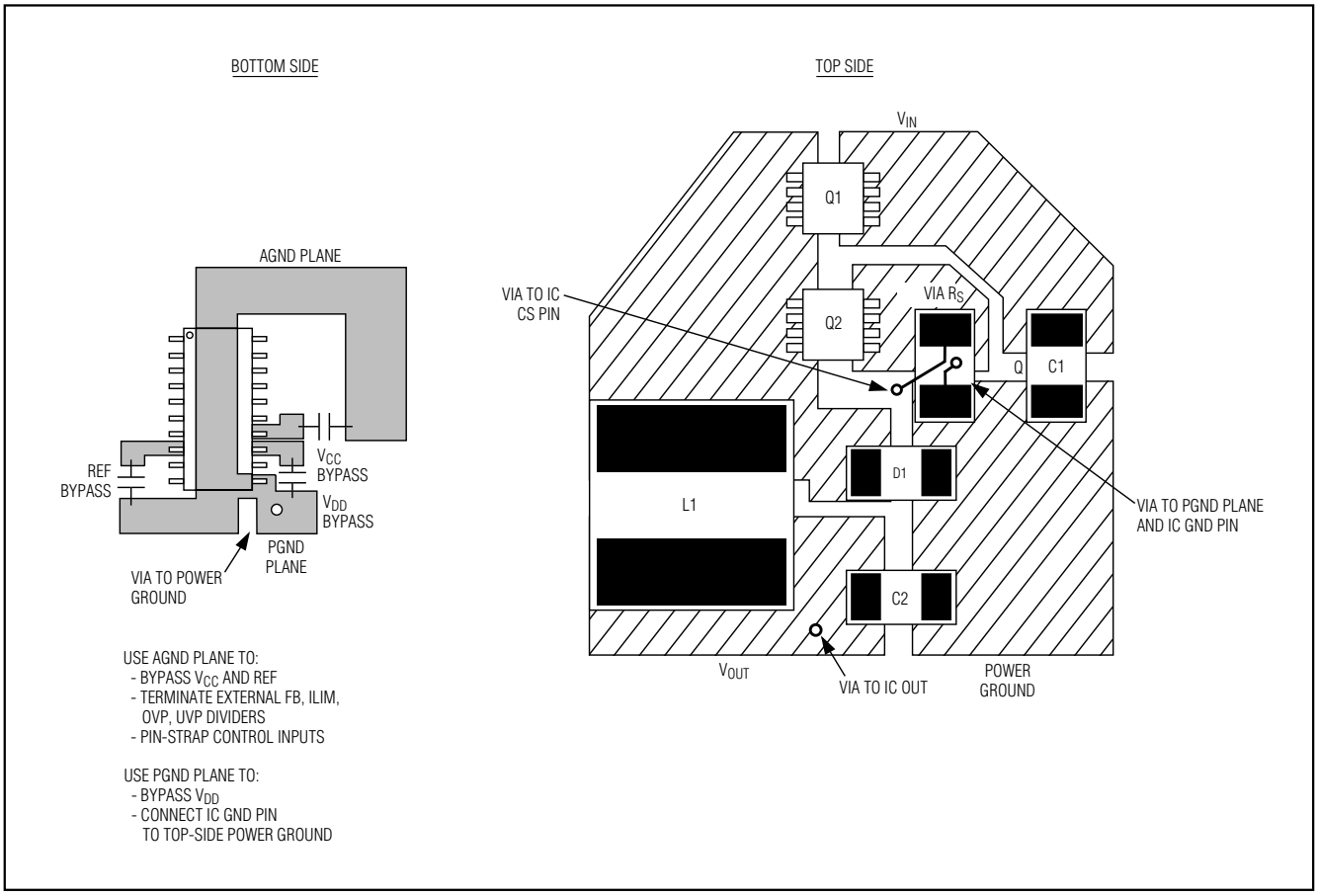


Figure 9. Power-Stage PC Board Layout Example

Table 5. Approximate K-Factor Errors

TON SETTING (kHz)	K FACTOR (µs)	APPROXIMATE K-FACTOR ERROR (%)	MINIMUM V_{IN} AT V_{OUT} = 2V (V)
200	5	±10	2.6
300	3.3	±10	2.9
450	2.2	±12.5	3.2
600	1.7	±12.5	3.6

Dropout Design Example:

V_{OUT} = 2.5V

fsw = 300kHz

K = 1.8µs, worst-case K = 2.97µs

$t_{OFF(MIN)}$ = 500ns

$V_{DROP1} = V_{DROP2}$ = 100mV

h = 1.5

$$V_{IN(MIN)} = \frac{\left(2.5V + 0.1V\right)}{1-\left(\frac{0.5\mu s \times 1.5}{2.97\mu s}\right)} + 0.1V - 0.1V = 3.48V$$

Calculating again with h = 1 gives the absolute limit of dropout:

$$V_{IN(MIN)} = \frac{\left(2.5V + 0.1V\right)}{1-\left(\frac{0.5\mu s \times 1}{2.97\mu s}\right)} - 0.1V + 0.1V = 3.13V$$

Therefore, V_{IN} must be greater than 3.13V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 3.48V.

PC Board Layout Guidelines

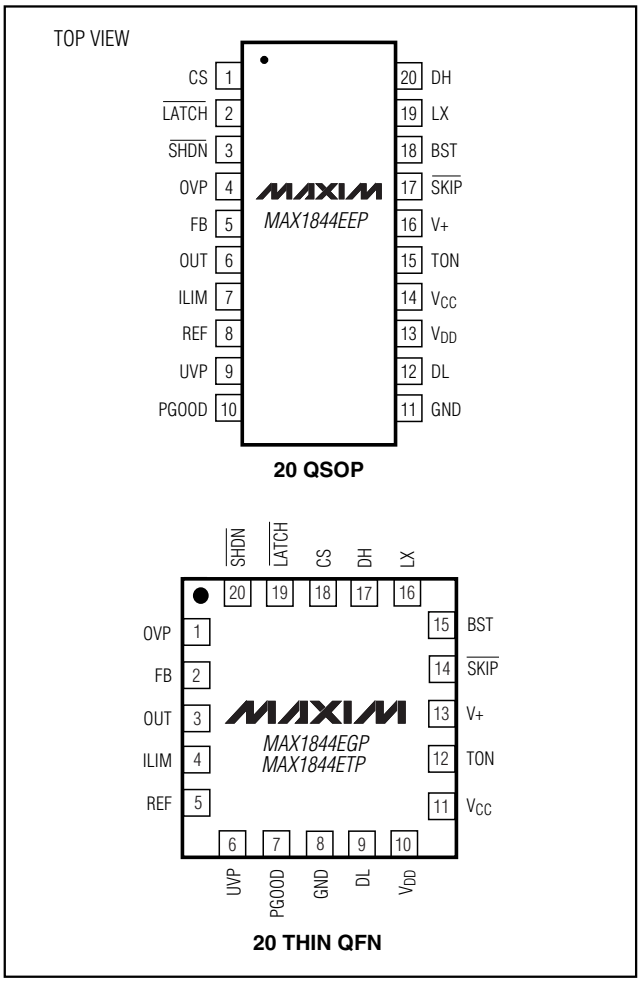
Careful PC board layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 9). If possible, mount all of the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.
- Minimize current sensing errors by connecting CS directly to the R_{SENSE} terminal.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BST, LX, DH, and DL) away from sensitive analog areas (REF, FB, CS).

Layout Procedure

1) Place the power components first, with ground terminals adjacent (Q2 source, C_{IN}-, C_{OUT}-, D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to MOSFET Q2, preferably on the back side opposite Q2 in order to keep LX, GND, and the DL gate-drive lines short and wide. The DL gate trace must be short and wide, measuring 10 to 20 squares (50 to 100 mils wide if the MOSFET is 1 inch from the controller IC GND pin.
3) Group the gate-drive components (BST diode and capacitor, V_{DD} bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figure 9. This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go; and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly at the IC.
5) Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.

Pin Configuration



Chip Information

TRANSISTOR COUNT: 2963

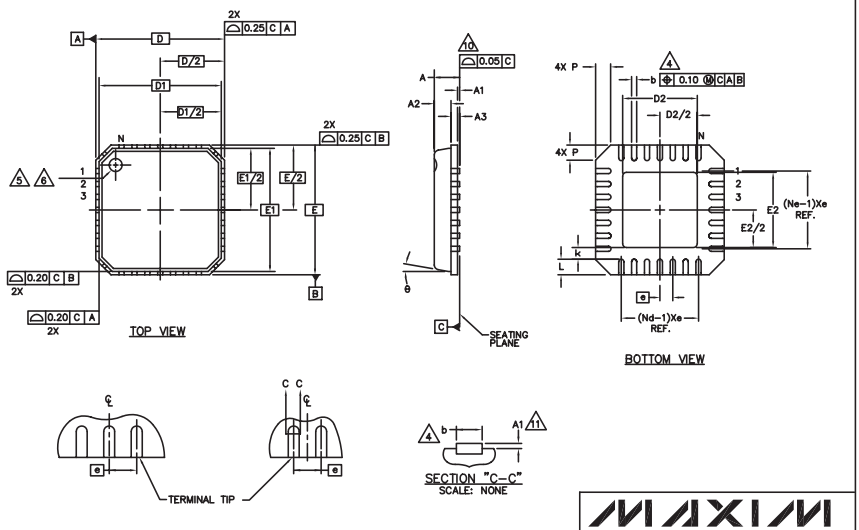
PROCESS: BiCMOS

High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32L QFN.EPS



COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
θ	0°		12°	0°		12°	0°		12°	0°		12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

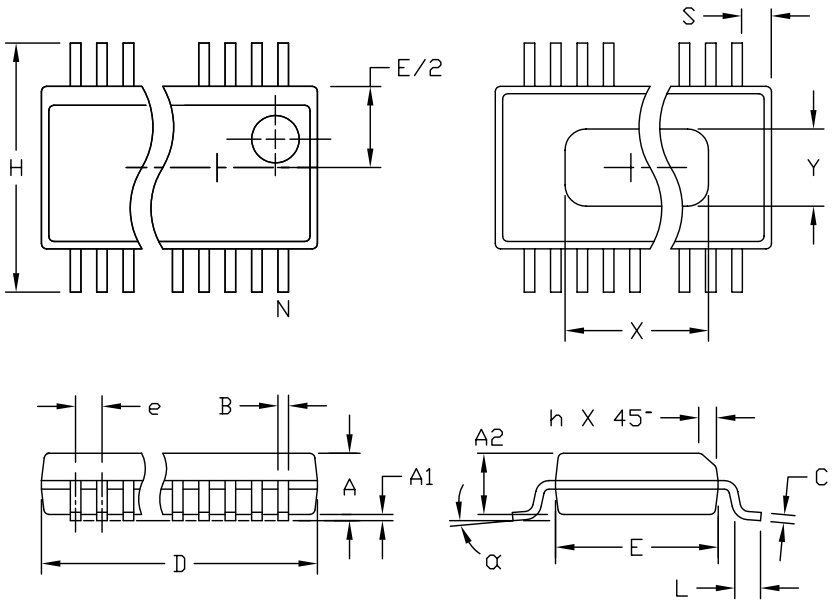
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM
APPROVAL
DOCUMENT CONTROL NO. 21-0091
REV H
2/2

High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

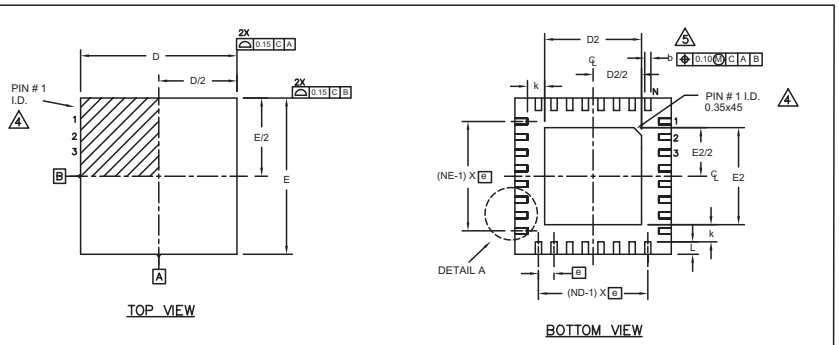
APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1

High-Speed Step-Down Controller with Accurate Current Limit for Notebook Computers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN 5x5x0.8 .EPS



PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. C | 1/2

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. C | 2/2

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