OKI Semiconductor

MSC23CV23257A-xxBS4

2,097,152-Word × 32-Bit DRAM MODULE : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The Oki MSC23CV23257A-xxBS4 is a fully decoded 2,097,152-word × 32-bit CMOS dynamic random access memory composed of four 16-Mb DRAMs (2M × 8) in TSOP packages mounted with decoupling capacitors on a 72-pin glass epoxy Small Outline DIMM Package supports any application where high density and large capacity of storage memory are required.

FEATURES

- 2,097,152-word × 32-bit organization
- 72-pin Small Outline DIMM
- Single 3.3 V supply ±0.3 V tolerance
- Input : LVTTL compatible
- Output : LVTTL compatible, 3-state
- Refresh : 2048 cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$-only refresh capability
- Multi-bit test mode capability
- Fast Page Mode with EDO capability

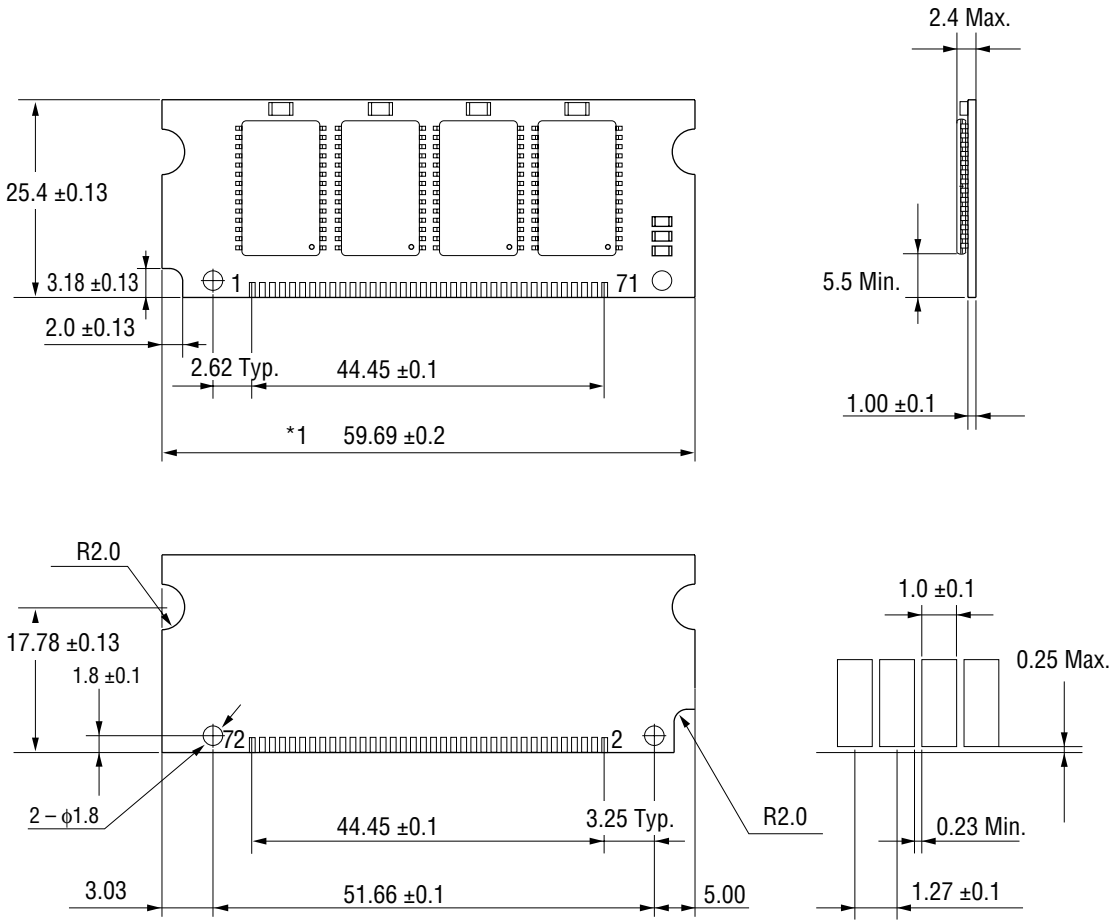
PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating (Max.)	Standby (Max.)
MSC23CV23257A-60BS4	60 ns	30 ns	15 ns	110 ns	2160 mW	14.4 mW
MSC23CV23257A-70BS4	70 ns	35 ns	20 ns	130 ns	1872 mW	

PIN CONFIGURATION

MSC23CV23257A-xxBS4

(Unit : mm)



*1 The common size difference of the board width 19.78 mm of its height is specified as ±0.2. The value above 19.78 mm is specified as ±0.5.

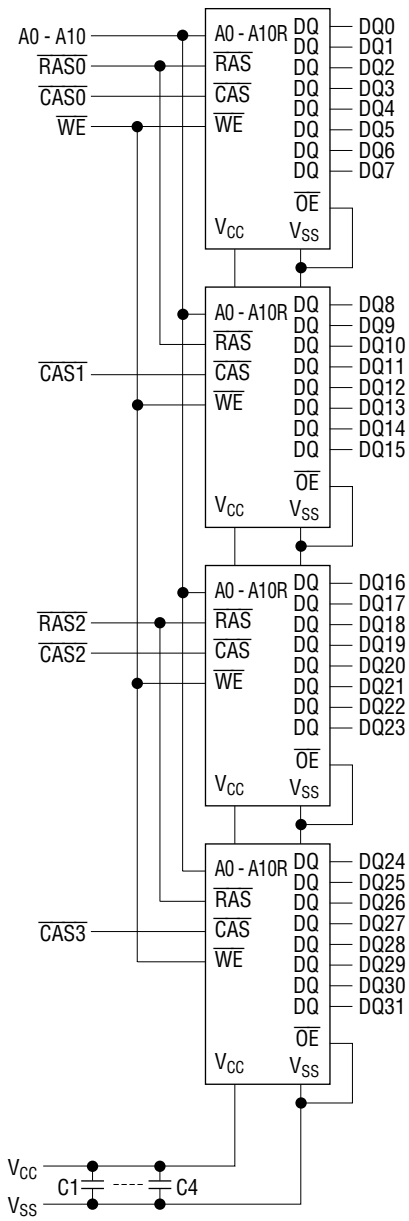
Pin Configuration

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	16	A4	31	A8	46	NC	61	V_{CC}
2	DQ0	17	A5	32	A9	47	$\overline{WE}$	62	DQ29
3	DQ1	18	A6	33	NC	48	NC	63	DQ30
4	DQ2	19	A10	34	$\overline{RAS2}$	49	DQ18	64	DQ31
5	DQ3	20	NC	35	DQ15	50	DQ19	65	NC
6	DQ4	21	DQ8	36	NC	51	DQ20	66	PD2
7	DQ5	22	DQ9	37	DQ16	52	DQ21	67	PD3
8	DQ6	23	DQ10	38	DQ17	53	DQ22	68	PD4
9	DQ7	24	DQ11	39	V_{SS}	54	DQ23	69	PD5
10	V_{CC}	25	DQ12	40	$\overline{CAS0}$	55	NC	70	PD6
11	PD1	26	DQ13	41	$\overline{CAS2}$	56	DQ24	71	PD7
12	A0	27	DQ14	42	$\overline{CAS3}$	57	DQ25	72	V_{SS}
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ26		
14	A2	29	NC	44	$\overline{RAS0}$	59	DQ27		
15	A3	30	V_{CC}	45	NC	60	DQ28		

Presence Detect Pins

Pin No.	Pin Name	MSC23CV23257A -60BS4	MSC23CV23257A -70BS4
11	PD1	V_{SS}	V_{SS}
66	PD2	NC	NC
67	PD3	V_{SS}	V_{SS}
68	PD4	NC	NC
69	PD5	NC	V_{SS}
70	PD6	NC	NC
71	PD7	NC	NC

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to 4.6	V
Voltage V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.5 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	4	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	–40 to 125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A10)	C_{IN1}	—	27	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{IN2}	—	20	pF
Input Capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{IN3}	—	13	pF
Input Capacitance ($\overline{WE}$)	C_{IN4}	—	35	pF
I/O Capacitance (DQ0 - DQ31)	C_{DQ}	—	13	pF

Note : Capacitance measured with Boonton Meter.

DC Characteristics

(V_{CC} = 3.3 V ±0.3 V, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSC23CV23257A -60BS4		MSC23CV23257A -70BS4		Unit	Note
			Min.	Max.	Min.	Max.		
Input Leakage Current	I_{LI}	0 V ≤ V_I ≤ V_{CC} + 0.3 V; All other pins not under test = 0 V	–40	40	–40	40	µA	
Output Leakage Current	I_{LO}	D_{OUT} disable 0 V ≤ V_O ≤ 3.6 V	–10	10	–10	10	µA	
Output High Voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA	0	0.4	0	0.4	V	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.	—	600	—	520	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	8	—	8	mA	1
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} –0.2 V	—	4	—	4	mA	1
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	600	—	520	mA	1, 2
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = Min.	—	600	—	520	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{HPC} = Min.	—	600	—	520	mA	1, 3

Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 3.3 V ±0.3 V, Ta = 0°C to 70°C) Note 1,2,3,10,11

Parameter	Symbol	MSC23CV23257A -60BS4		MSC23CV23257A -70BS4		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	ns	
Fast Page Mode Cycle Time	t_{HPC}	25	—	30	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	—	35	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	ns	4
Output Hold Time from $\overline{CAS}$ Low	t_{DOH}	5	—	5	—	ns	
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t_{CEZ}	0	15	0	15	ns	7, 8
$\overline{RAS}$ to Data Output Buffer Turn-off Delay Time	t_{REZ}	0	15	0	15	ns	7, 8
$\overline{WE}$ to Data Output Buffer Turn-off Delay Time	t_{WEZ}	0	15	0	15	ns	7
Transition Time	t_T	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	32	—	32	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10k	70	10k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	100k	70	100k	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10k	10	10k	ns	
$\overline{RAS}$ Low to $\overline{CAS}$ High Delay Time	t_{CSH}	40	—	45	—	ns	
$\overline{CAS}$ High to $\overline{RAS}$ Low Delay Time	t_{CRP}	5	—	5	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	ns	6
$\overline{RAS}$ to Second $\overline{CAS}$ Delay Time	t_{RSCD}	60	—	70	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	40	—	45	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	ns	

AC Characteristics (2/2)

(V_{CC} = 3.3 V ±0.3 V, Ta = 0°C to 70°C) Note 1,2,3,10,11

Parameter	Symbol	MSC23CV23257A -60BS4		MSC23CV23257A -70BS4		Unit	Note
		Min.	Max.	Min.	Max.		
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	9
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	9
Write Command Set-up Time	t_{WCS}	0	—	0	—	ns	
Write Command Hold Time	t_{WCH}	10	—	15	—	ns	
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	40	—	45	—	ns	
Write Command Pulse Width	t_{WP}	10	—	15	—	ns	
Write Command Pulse Width (Output Disable)	t_{WPE}	5	—	10	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	
Data-in Hold Time	t_{DH}	15	—	15	—	ns	
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	40	—	45	—	ns	
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	—	15	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	—	10	—	ns	
$\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Set-up Time (Test Mode)	t_{WTS}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Hold Time (Test Mode)	t_{WTH}	10	—	10	—	ns	

Notes:

1. A start-up delay of 200 µs is required after power-up, followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.

2. The AC characteristics assume t_T = 5 ns.

3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.

4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.

5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC}.

6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA}.

7. t_{CEZ} (Max.), t_{REZ} (Max.) and t_{WEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition.

9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 2-bit parallel test function. CA9 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

11. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.

See ADDENDUM I for AC Timing Waveforms