UCC21736-Q1 10-A Source and Sink Reinforced Isolated Single Channel Gate Driver for SiC/IGBT with Active Protection and High-CMTI

1 Features

- 5.7-kV_{RMS} single channel isolated gate driver
- AEC-Q100 qualified for automotive applications
- SiC MOSFETs and IGBTs up to 2121 V_{pk}
- 33-V maximum output drive voltage (VDD-VEE)
- ±10-A drive strength and split output
- 150-V/ns minimum CMTI
- 200-ns response time fast overcurrent protection
- External active miller clamp
- 900-mA soft turn-off when fault happens
- ASC input on isolated side to turn on power switch during system fault
- Alarm $\overline{FLT}$ on over current and reset from $\overline{RST}$/EN
- Fast enable/disable response on $\overline{RST}$/EN
- Reject <40-ns noise transient and pulse on input pins
- 12V VDD UVLO and -3V VEE UVLO with power good on RDY
- Inputs/outputs with over/under-shoot transient voltage Immunity up to 5 V
- 130-ns (maximum) propagation delay and 30-ns (maximum) pulse/part skew
- SOIC-16 DW package with creepage and clearance distance > 8 mm
- Operating junction temperature –40°C to 150°C

2 Applications

- Traction inverter for EVs
- On-board charger and charging pile
- DC-to-DC converter for HEV/EVs

3 Description

The UCC21736-Q1 is a galvanic isolated single channel gate driver designed for SiC MOSFETs and IGBTs up to 2121-V DC operating voltage with advanced protection features, best-in-class dynamic performance and robustness. UCC21736-Q1 has up to ±10-A peak source and sink current.

The input side is isolated from the output side with SiO_2 capacitive isolation technology, supporting up to 1.5-kV_{RMS} working voltage, 12.8-kV_{PK} surge immunity with longer than 40 years Isolation barrier life, as well as providing low part-to-part skew, >150V/ns common mode noise immunity (CMTI).

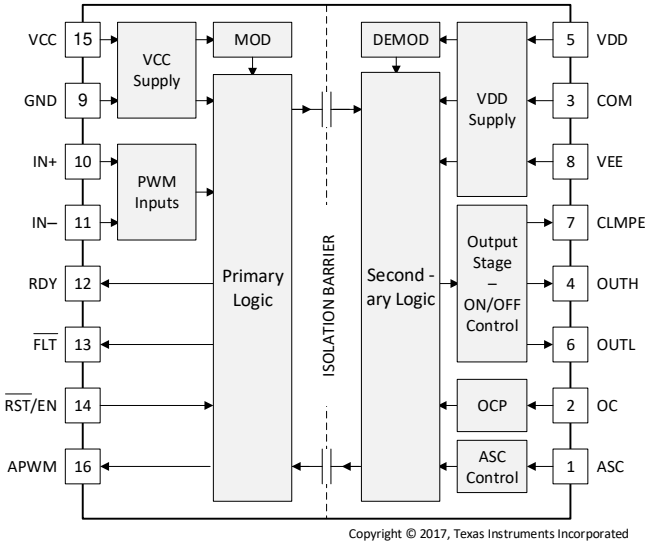
The UCC21736-Q1 includes the state-of-art protection features, such as fast overcurrent and short circuit detection, shunt current sensing support, fault reporting, active miller clamp, input and output side power supply UVLO to optimize SiC and IGBT switching behavior and robustness. The ASC feature can be utilized to force ON power switch during system failure events, further increasing the drivers' versatility and simplifying the system design effort, size and cost.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC21736-Q1	DW SOIC-16	10.3 mm × 7.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Device Pin Configuration



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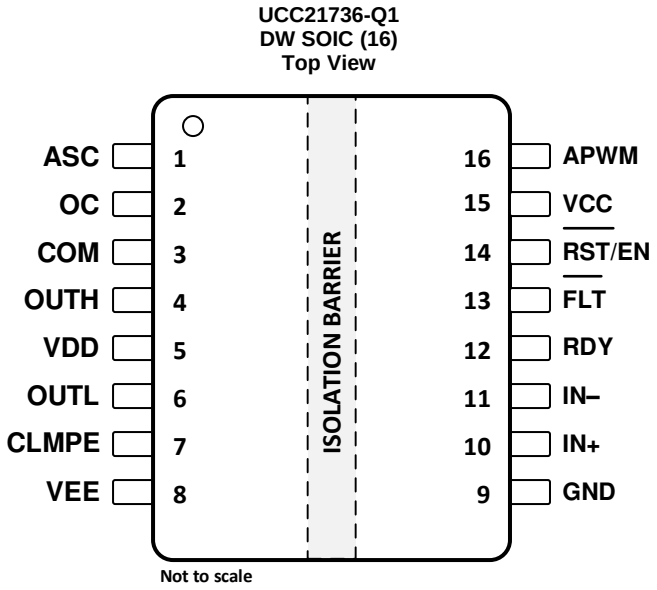
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2019	*	Advance Information release

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5 Pin Configuration and Functions



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Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
ASC	1	I	Active high to enable active short circuit function to force output high during system failure events
OC	2	I	Over current detection pin, support lower threshold for SenseFET, DESAT, and Shunt resistor sensing
COM	3	P	Common ground reference, connecting to emitter pin for IGBT and source pin for SiC-MOSFET
OUTH	4	O	Gate driver output pull up
VDD	5	P	Positive supply rail for gate drive voltage, Bypassing a >220nF capacitor to COM to support specified gate driver source peak current capability
OUTL	6	O	Gate driver output pull down
CLMPE	7	O	External Active miller clamp, connecting this pin to the gate of the external miller clamp MOSFET
VEE	8	P	Negative supply rail for gate drive voltage. Bypassing a >220nF capacitor to COM to support specified gate driver sink peak current capability
GND	9	P	Input power supply and logic ground reference
IN+	10	I	Non-inverting gate driver control input
IN–	11	I	Inverting gate driver control input
RDY	12	O	Power good for VCC-GND and VDD-COM. RDY is open drain configuration and can be paralleled with other RDY signals
$\overline{\text{FLT}}$	13	O	Active low fault alarm output upon over current or short circuit. $\overline{\text{FLT}}$ is in open drain configuration and can be paralleled with other faults
$\overline{\text{RST}}$/EN	14	I	The $\overline{\text{RST}}$/EN serves two purposes: 1) Enable / shutdown of the output side. The FET is turned off by a general turn-off, if terminal EN is set to low; 2) Resets the OC condition signaled on $\overline{\text{FLT}}$ pin. if terminal $\overline{\text{RST}}$/EN is set to low for more than 1000ns. A reset of signal $\overline{\text{FLT}}$ is asserted at the rising edge of terminal $\overline{\text{RST}}$/EN. For automatic RESET function, this pin only serves as an EN pin. Enable / shutdown of the output side. The FET is turned off by a general turn-off, if terminal EN is set to low.
VCC	15	P	Input power supply from 3V to 5.5V, bypassing a >100nF capacitor to GND
APWM	16	O	Isolated PWM output monitoring ASC pin status

(1) P = Power, G = Ground, I = Input, O = Output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER			MIN	MAX	UNIT
VCC	VCC – GND		–0.3	6	V
VDD	VDD – COM		–0.3	36	V
VEE	VEE – COM		–17.5	0.3	V
V_{MAX}	VDD – VEE		–0.3	36	V
IN+, IN–, $\overline{RST}$/EN		DC	GND–0.3	VCC	V
		Transient, less than 100 ns(2)	GND–5.0	VCC+5.0	V
ASC	Reference to COM		–0.3	6	V
OC	Reference to COM		-0.3	6	
OUTH, OUTL		DC	VEE–0.3	VDD	V
		Transient, less than 100 ns(2)	VEE–5.0	VDD+5.0	V
CLMPE	Reference to VEE		–0.3	5	V
RDY, $\overline{FLT}$			GND–0.3	VCC	V
$I_{\overline{FLT}}$, I_{RDY}	$\overline{FLT}$, and RDY pin input current			20	mA
I_{APWM}	APWM pin output current			20	mA
T_J	Junction temperature range		–40	150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Values are verified by characterization on bench.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

PARAMETER			MIN	MAX	UNIT
VCC	VCC–GND		3.0	5.5	V
VDD	VDD–COM		13	33	V
V_{MAX}	VDD–VEE		–	33	V
IN+, IN–, $\overline{RST}$/EN	Reference to GND	High level input voltage	0.7×VCC	VCC	V
		Low level input voltage	0	0.3×VCC	
ASC	Reference to COM		0	5	V
$t_{RST/EN}$	Minimum pulse width that reset the fault		1000		ns
T_A	Ambient Temperature		–40	125	°C
T_J	Junction temperature		–40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC21736-Q1 DW (SOIC) 16	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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Thermal Information (continued)

THERMAL METRIC(1)		UCC21736-Q1 DW (SOIC) 16	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.3	°C/W

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	Value	UNIT
P_D	Maximum power dissipation (both sides)	VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IN+/- = 5V, 150kHz, 50% Duty Cycle for 10nF load, T_a=25°C	985	mW
P_{D1}	Maximum power dissipation by transmitter side		20	mW
P_{D2}	Maximum power dissipation by receiver side		965	mW

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6.6 Electrical Characteristics

VCC=3.3V or 5.0V, 1uF capacitor from VCC to GND, VDD–COM=20V, 18V or 15V, COM–VEE =0V, 5V, 8V or 15V, C_L=100pF, –40°C<T_J<150°C (unless otherwise noted)(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC UVLO THRESHOLD AND DELAY						
V_{VCC_ON}	VCC–GND		2.55	2.7	2.85	V
V_{VCC_OFF}			2.35	2.5	2.65	
V_{VCC_HYS}				0.2		
t_{VCCFIL}	VCC UVLO Deglitch time			10		µs
$t_{VCC+ to OUT}$	VCC UVLO on delay to output high	IN+ = VCC, IN– = GND		37.8		
$t_{VCC– to OUT}$	VCC UVLO off delay to output low			10		
$t_{VCC+ to RDY}$	VCC UVLO on delay to RDY high	$\overline{RST}$/EN = VCC		37.8		
$t_{VCC– to RDY}$	VCC UVLO off delay to RDY low			10		
VDD UVLO THRESHOLD AND DELAY						
V_{VDD_ON}	VDD–COM		11.2	12.0	12.8	V
V_{VDD_OFF}			9.9	10.7	11.5	
V_{VDD_HYS}				0.8		
t_{VDDFIL}	VDD UVLO Deglitch time			5		µs
$t_{VDD+ to OUT}$	VDD UVLO on delay to output high	IN+ = VCC, IN– = GND		5		
$t_{VDD– to OUT}$	VDD UVLO off delay to output low			5		
$t_{VDD+ to RDY}$	VDD UVLO on delay to RDY high	$\overline{RST}$/EN = $\overline{FLT}$=High		10		
$t_{VDD– to RDY}$	VDD UVLO off delay to RDY low			10		
VEE UVLO THRESHOLD AND DELAY						
V_{VEE_ON}	VEE–COM		–3.3	–3.0	–2.7	V
V_{VEE_OFF}			–2.9	–2.6	–2.3	
V_{VEE_HYS}				0.4		
t_{VEEFIL}	VEE UVLO Deglitch time			5		µs
$t_{VEE+ to OUT}$	VEE UVLO on delay to output high	IN+ = VCC, IN– = GND		5		
$t_{VEE– to OUT}$	VEE UVLO off delay to output low			5		
$t_{VEE+ to RDY}$	VEE UVLO on delay to RDY high	$\overline{RST}$/EN = $\overline{FLT}$=High		10		
$t_{VEE– to RDY}$	VEE UVLO off delay to RDY low			10		
VCC, VDD QUIESCENT CURRENT						
I_{VCCQ}	VCC quiescent current	OUT(H) = High, f_S = 0Hz, AIN=2V		3		mA
		OUT(L) = Low, f_S = 0Hz, AIN=2V		2		
I_{VDDQ}	VDD quiescent current	OUT(H) = High, f_S = 0Hz, AIN=2V		4		mA
		OUT(L) = Low, f_S = 0Hz, AIN=2V		3.7		
LOGIC INPUTS — IN+, IN–, and $\overline{RST}$/EN						
V_{INH}	Input high threshold	V_{CC}=3.3V		1.85	2.31	V
V_{INL}	Input low threshold	V_{CC}=3.3V	0.99	1.52		V
V_{INHYS}	Input threshold hysteresis	V_{CC}=3.3V		0.33		V
I_{IH}	Input high level input leakage current	V_{IN} = VCC		90		µA
I_{IL}	Input low level input leakage	V_{IN} = GND		–90		µA
R_{IND}	Input pins pull down resistance	see Detailed Description for more information		55		kΩ
R_{INU}	Input pins pull up resistance	see Detailed Description for more information		55		
T_{INFIL}	IN+, IN– and $\overline{RST}$/EN deglitch (ON and OFF) filter time	f_S = 50kHz	28	40		ns
T_{RSTFIL}	Deglitch filter time to reset /FLT		500	650	800	ns
GATE DRIVER STAGE						
I_{OUT}, I_{OUTH}	Peak source current	C_L=0.18µF, f_S=1kHz		–10		A
I_{OUT}, I_{OUTL}	Peak sink current			10		A
R_{OUTH}	Output pull-up resistance	I_{OUT} = –0.1A		2.5		Ω

(1) Current are positive into and negative out of the specified terminal.
(2) All voltages are referenced to COM unless otherwise notified.

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Electrical Characteristics (continued)

VCC=3.3V or 5.0V, 1uF capacitor from VCC to GND, VDD–COM=20V, 18V or 15V, COM–VEE =0V, 5V, 8V or 15V, C_L=100pF, –40°C<T_J<150°C (unless otherwise noted)(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{OUTL}	Output pull-down resistance	I_{OUT} = 0.1A		0.3		Ω
V_{OUTH}	High level output voltage	I_{OUT} = –0.2A, V_{DD}=15V		14.5		V
V_{OUTL}	Low level output voltage	I_{OUT} = 0.2A		60		mV
ACTIVE PULLDOWN						
V_{OUTPD}	Output active pull down on OUT, OUTL	I_{OUTL} or I_{OUT} = 0.1×$I_{OUT(L)(tpy)}$, VDD=OPEN, VEE=COM			2.5	V
EXTERNAL MILLER CLAMP						
V_{CLMPTH}	Miller clamp threshold voltage	Reference to VEE	1.5	2.0	2.5	V
V_{CLMPE}	Output high voltage	Reference to VEE	4.4	4.8		V
I_{CLMPEH}	Peak source current	C_{CLMPE} = 10nF	0.12	0.25		A
I_{CLMPEL}	Peak sink current		0.12	0.25		A
t_{CLMPER}	Rising time	C_{CLMPE} = 330pF		20	40	ns
t_{DCLMPE}	Miller clamp ON delay time			40		ns
SHORT CIRCUIT CLAMPING						
$V_{CLP-OUT(H)}$	V_{OUT}–VDD, V_{OUTH}–VDD	OUT = Low, $I_{OUT(H)}$ = 500mA, t_{CLP}=10us		0.9		V
$V_{CLP-OUT(L)}$	V_{OUT}–VDD, V_{OUTL}–VDD	OUT = High, $I_{OUT(L)}$ = 500mA, t_{CLP}=10us		1.8		V
$V_{CLP-CLMPI}$	V_{CLMPI}–VDD	OUT = High, I_{CLMPI} = -20mA, t_{CLP}=10us		1.0		V
OC PROTECTION						
I_{DCHG}	OC pull down current when	V_{OC} = 1V		40		mA
V_{OCTH}	Detection Threshold		0.63	0.7	0.77	V
V_{OCL}	Voltage when OUT(L) = LOW, Reference to COM	I_{OC} = 5mA		0.13		V
t_{OCFIL}	OC fault deglitch filter			150		ns
t_{OCOFF}	OC propagation delay to OUT(L) 90%			200		ns
t_{OCFLT}	OC to $\overline{FLT}$ low delay			600		ns
INTERNAL SOFT TURN-OFF						
I_{STO}	Soft turn-off current on fault conditions			900		mA
ASC - Active Short Circuit						
V_{ASCL}	ASC Input low threshold			1.7		V
V_{ASCH}	ASC Input high threshold			3.2		V
t_{ASC_r}	ASC to output rising edge delay			660		ns
t_{ASC_f}	ASC to output falling edge delay			227		ns
ISOLATED ASC MONITOR (APWM)						
f_{APWM}	APWM output frequency		360	400	440	kHz
D_{APWM}	APWM Dutycycle —	V_{ASC} = 0.5V	7	10	13	%
		V_{ASC} = 2.5V	47	50	53	
		V_{ASC} = 4.5V	87	90	93	
$\overline{FLT}$ AND RDY REPORTING						
t_{RDYHLD}	VDD UVLO RDY low minimum holding time		0.55		1	ms
$t_{FLTMUTE}$	Output mute time on fault	Reset fault through $\overline{RST}$/EN	0.55		1	ms
R_{ODON}	Open drain output on resistance	I_{ODON} = 5mA		30		Ω
V_{ODL}	Open drain low output voltage	IODON = 5mA			0.3	V
COMMON MODE TRANSIENT IMMUNITY						
CMTI	Common-mode transient immunity		150			V/ns

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6.7 Switching Characteristics

VCC=5.0V, 1uF capacitor from VCC to GND, VDD–COM=20V, 18V or 15V, COM–VEE = 3V, 5V or 8V, C_L=100pF, –40°C<T_J<150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PDHL}	Propagation delay time – High to Low			90		ns
t_{PDLH}	Propagation delay time – Low to High			90		
PWD	Pulse width distortion $\lvert t_{PDHL} - t_{PDLH} \rvert$				25	
t_{sk-pp}	Part to Part skew	Rising or Falling Propagation Delay			30	
t_r	Driver output rise time	C_L=10nF			28	
t_f	Driver output fall time	C_L=10nF			24	
f_{MAX}	Maximum switching frequency				1	MHz

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6.8 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (Internal clearance) of the double insulation (2 × 0.0085 mm)	> 17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664–1	I	
	Overvoltage Category per IEC 60664–1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-11 (VDE V 0884-11):2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST}=V_{IOTM}, t = 60 s (qualification test)	8000	V_{PK}
		V_{TEST}=1.2 x V_{IOTM}, t = 1 s (100% production test)	9600	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, V_{TEST} = 1.6 × V_{IOSM} = 12800 V_{PK} (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} = 2545 V_{PK}, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM} = 3394 V_{PK}, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test) V_{ini} = V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM} = 3977 V_{PK}, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 sin (2πft), f = 1 MHz	~ 1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	≥ 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	≥ 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	≥ 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 5700 V_{RMS}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} = 6840 V_{RMS}, t = 1 s (100% production)	5700	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device

6.9 Safety-Related Certifications

VDE	UL
Plan to certify according to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01; DIN EN 61010-1 (VDE 0411-1):2011-07	Plan to certify according to UL 1577 Component Recognition Program

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Safety-Related Certifications (continued)

VDE	UL
Reinforced insulation Maximum transient isolation voltage, 8000 V_{PK}; Maximum repetitive peak isolation voltage, 2121 V_{PK}; Maximum surge isolation voltage, 8000 V_{PK}	Single protection, 5700 V_{RMS}
Certification Planned	Certification Planned

6.10 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ =68.3°C/W, V_{DD} = 20V, V_{EE}=-5V, T_J = 150°C, T_A = 25°C			TBD	mA
		$R_{\theta JA}$ =68.3°C/W, V_{DD} = 20V, V_{EE}=-5V, T_J = 150°C, T_A = 25°C			TBD	
P_S	Safety input, output, or total power	$R_{\theta JA}$ =68.3°C/W, V_{DD} = 20V, V_{EE}=-5V, T_J = 150°C, T_A = 25°C			TBD	mW
T_S	Safety temperature				150	°C

(1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

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6.11 Insulation Characteristics Curves

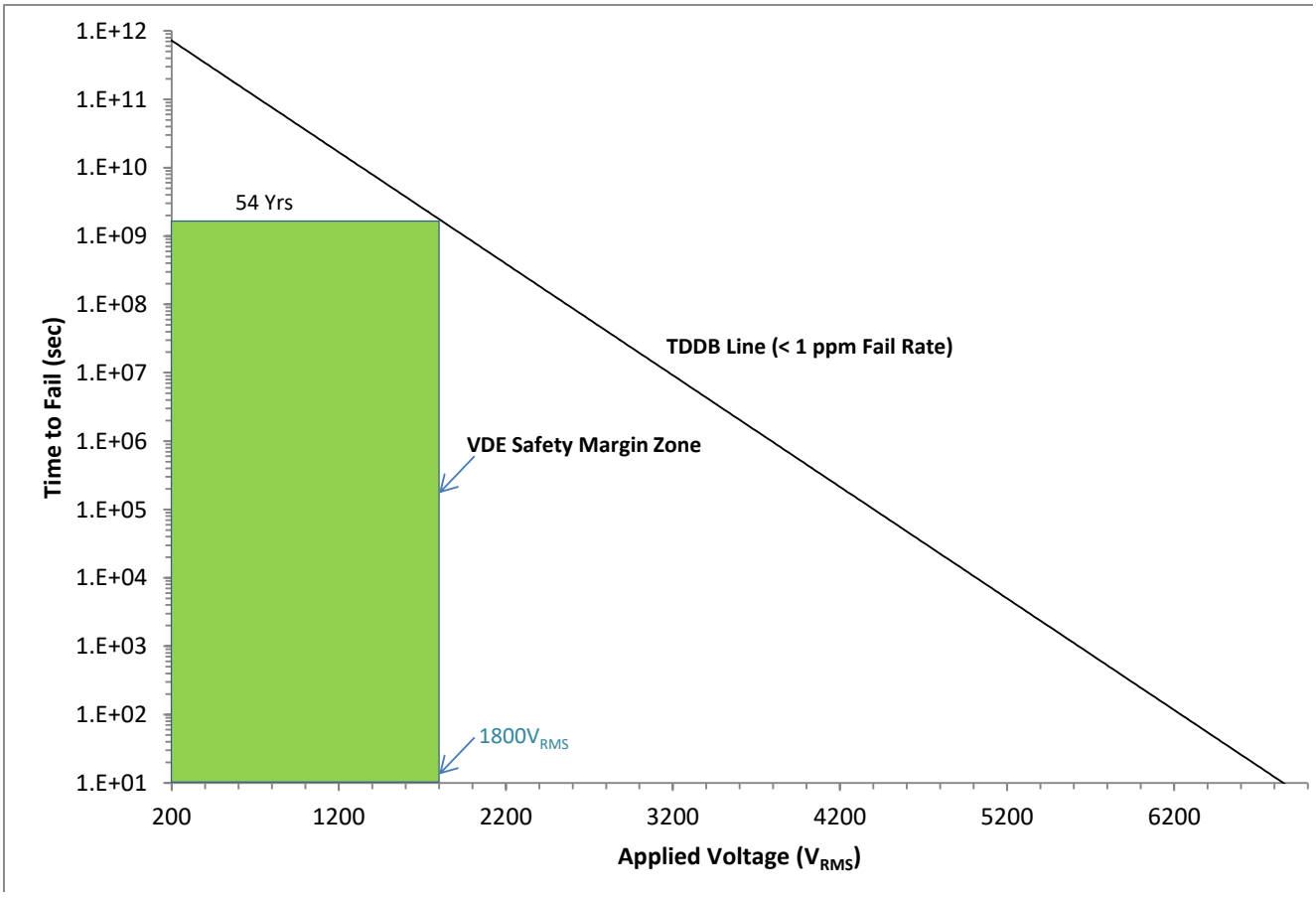


Figure 1. Reinforced Isolation Capacitor Life Time Projection

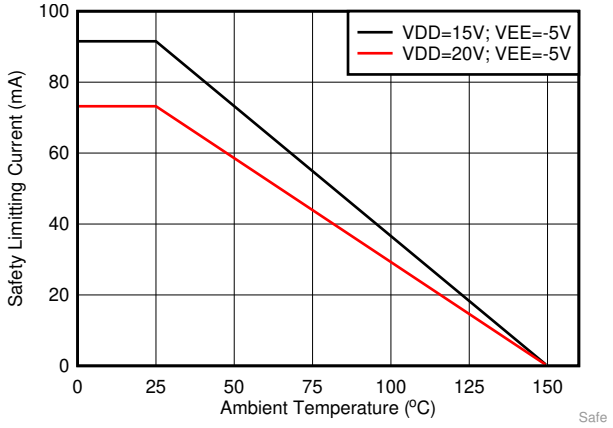


Figure 2. Thermal Derating Curve for Limiting Current per VDE

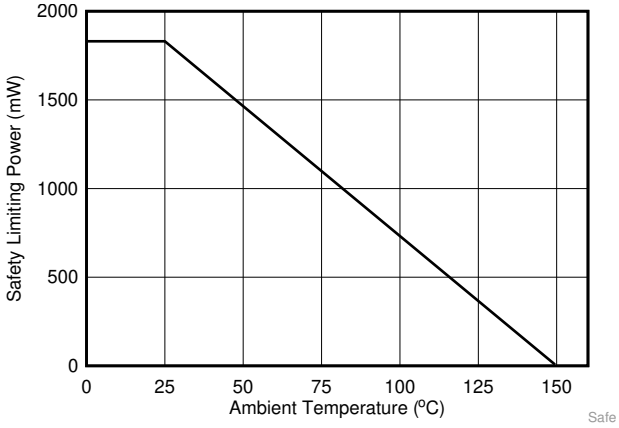


Figure 3. Thermal Derating Curve for Limiting Power per VDE

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6.12 Typical Characteristics

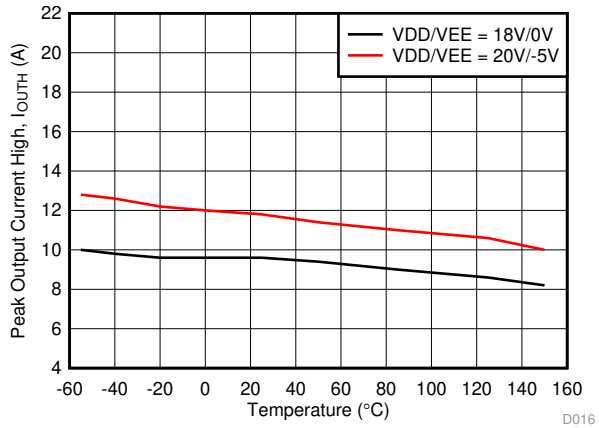


Figure 4. Output High Drive Current vs. Temperature

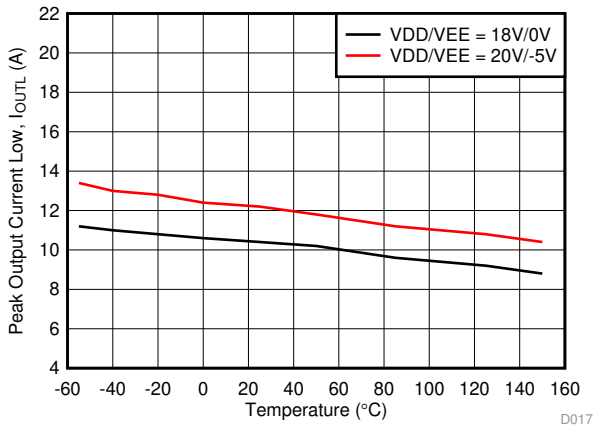


Figure 5. Output Low Driver Current vs. Temperature

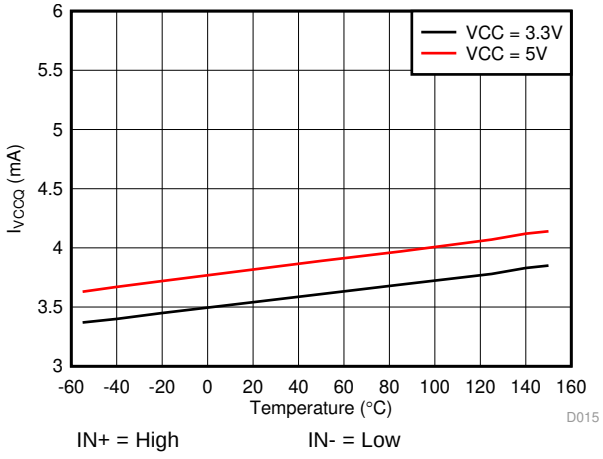


Figure 6. I_{VCCQ} Supply Current vs. Temperature

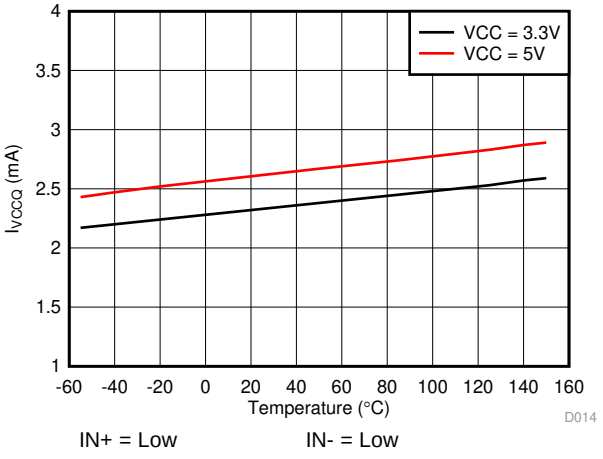


Figure 7. I_{VCCQ} Supply Current vs. Temperature

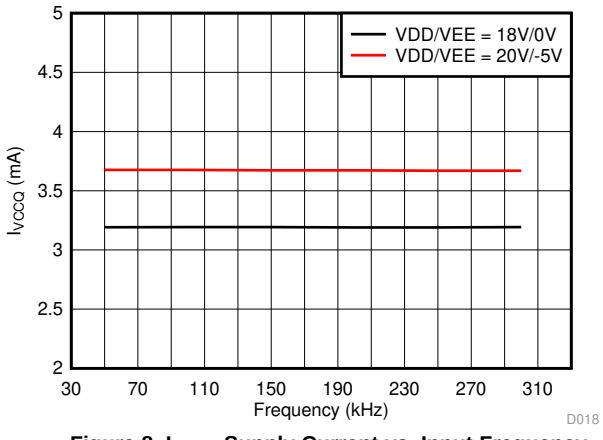


Figure 8. I_{VCCQ} Supply Current vs. Input Frequency

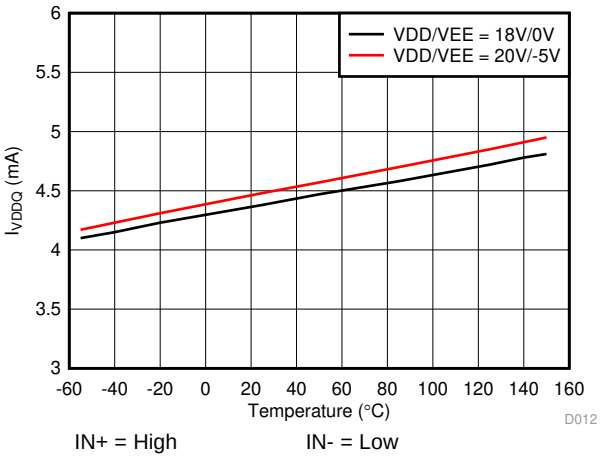


Figure 9. I_{VDDQ} Supply Current vs. Temperature

ADVANCE INFORMATION

Typical Characteristics (continued)

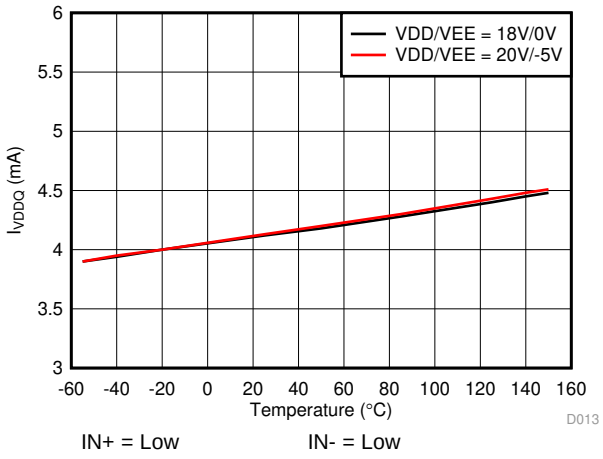


Figure 10. I_{VDDQ} Supply Current vs. Temperature

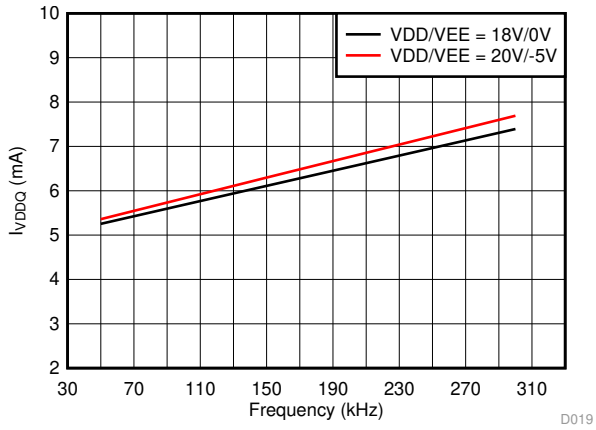


Figure 11. I_{VDDQ} Supply Current vs. Input Frequency

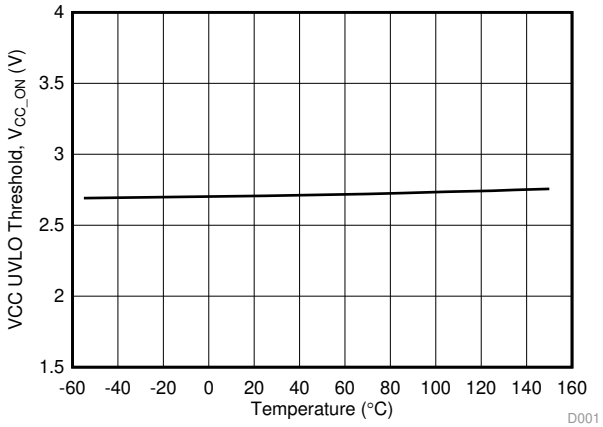


Figure 12. VCC UVLO vs. Temperature

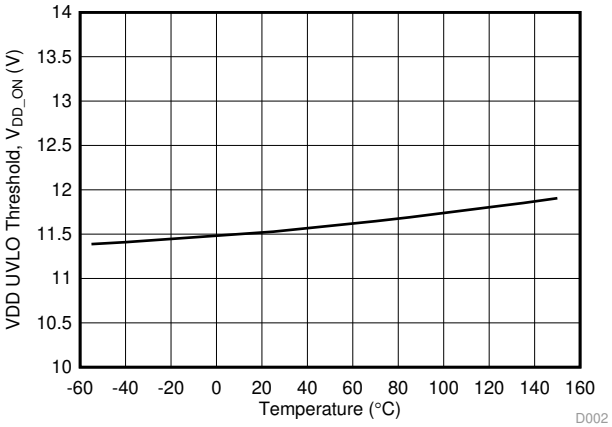


Figure 13. VDD UVLO vs. Temperature

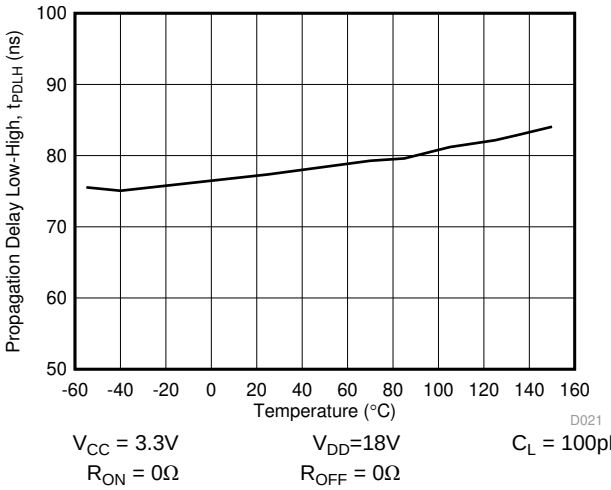


Figure 14. Propagation Delay t_{PDLH} vs. Temperature

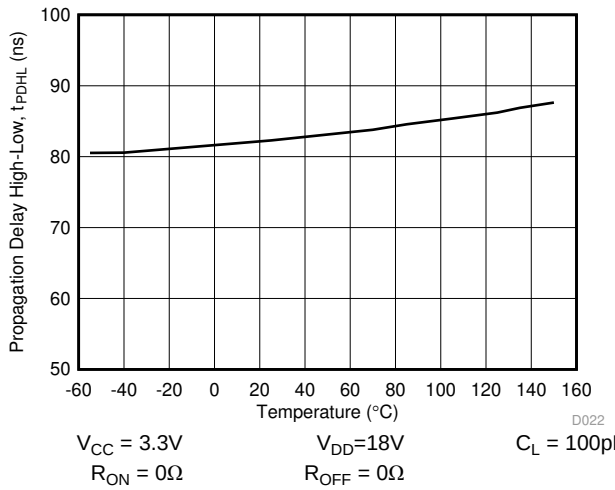
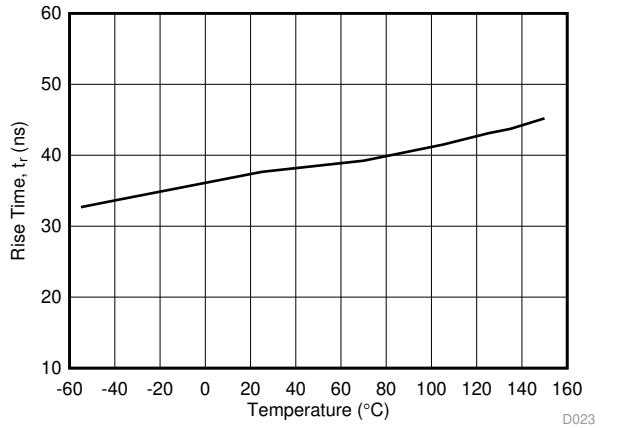


Figure 15. Propagation Delay t_{PDHL} vs. Temperature

ADVANCE INFORMATION

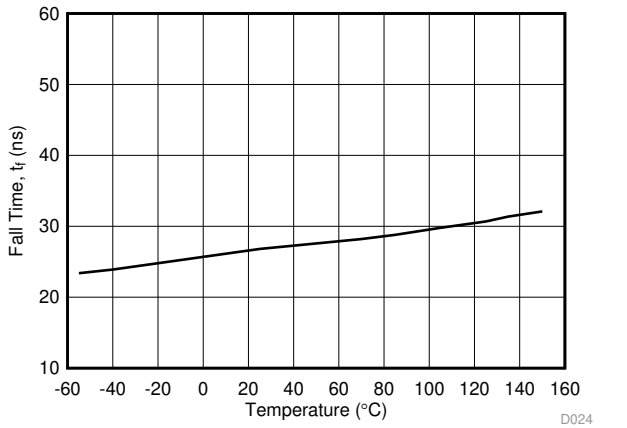
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Typical Characteristics (continued)



V_{CC} = 3.3V V_{DD}=18V C_L = 10nF
R_{ON} = 0Ω R_{OFF} = 0Ω

Figure 16. t_r Rise Time vs. Temperature



V_{CC} = 3.3V V_{DD}=18V C_L = 10nF
R_{ON} = 0Ω R_{OFF} = 0Ω

Figure 17. t_f Fall Time vs. Temperature

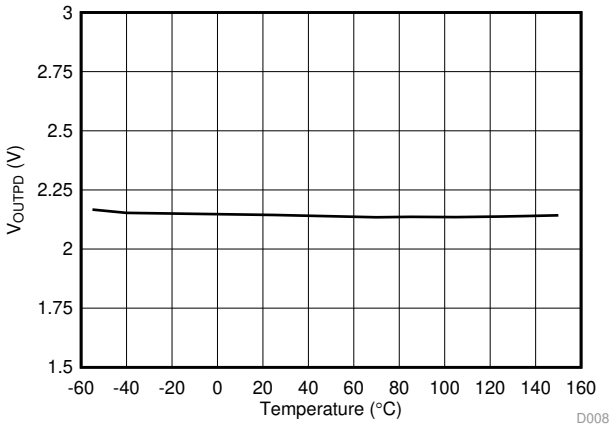


Figure 18. V_{OUTPD} Output Active Pulldown Voltage vs. Temperature

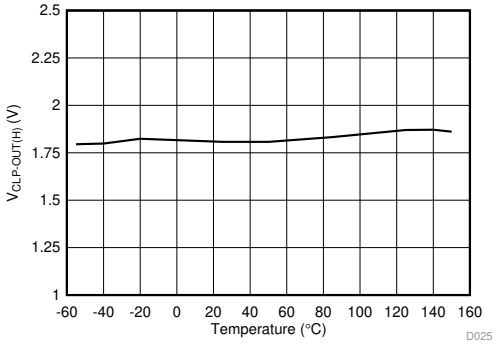


Figure 19. $V_{CLP-OUT(H)}$ Short Circuit Clamping Voltage vs. Temperature

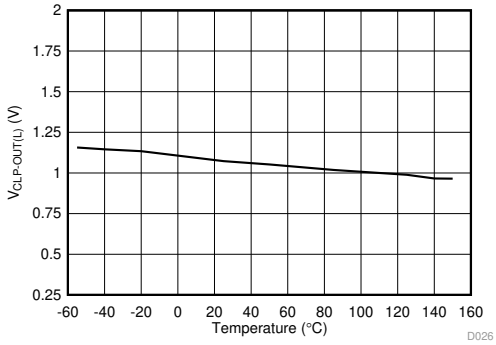


Figure 20. $V_{CLP-OUT(L)}$ Short Circuit Clamping Voltage vs. Temperature

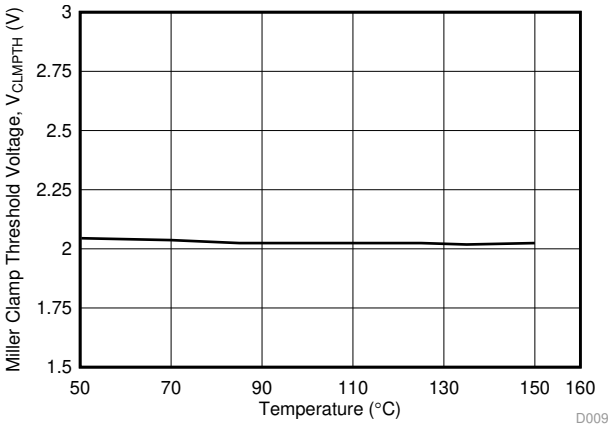


Figure 21. V_{CLMPTH} Miller Clamp Threshold Voltage vs. Temperature

ADVANCE INFORMATION

Typical Characteristics (continued)

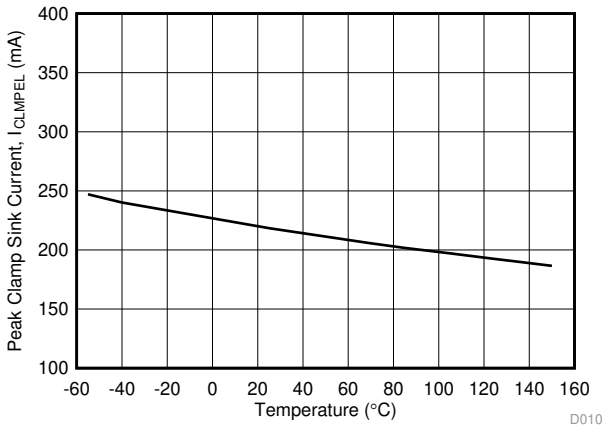


Figure 22. I_{CLMPEL} Miller Clamp Sink Current vs. Temperature

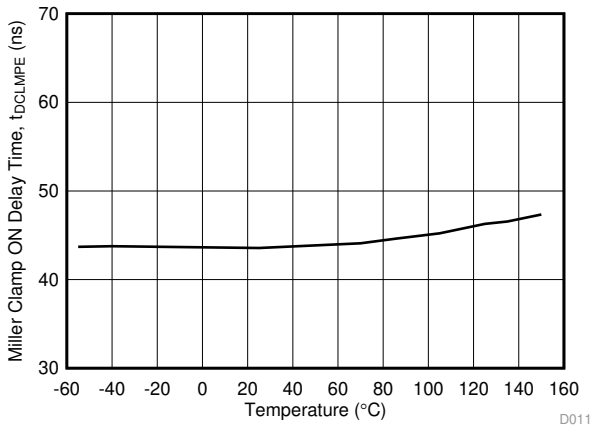


Figure 23. t_{DCLMPE} Miller Clamp ON Delay Time vs. Temperature

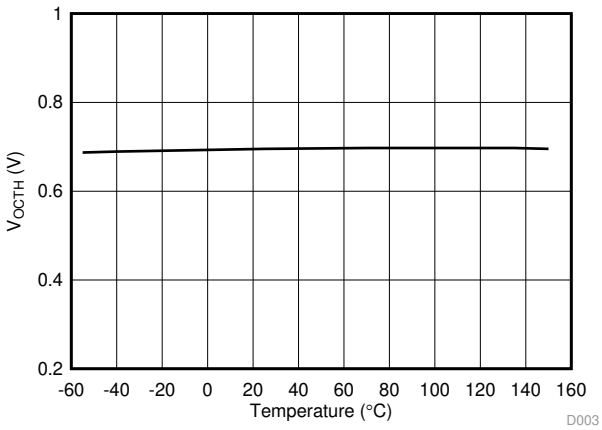


Figure 24. V_{OCTH} OC Detection Threshold vs. Temperature

ADVANCE INFORMATION

7 Parameter Measurement Information

7.1 Propagation Delay

7.1.1 Regular Turn-OFF

Figure 25 shows the propagation delay measurement for non-inverting configurations. Figure 26 shows the propagation delay measurement with the inverting configurations.

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Propagation Delay (continued)

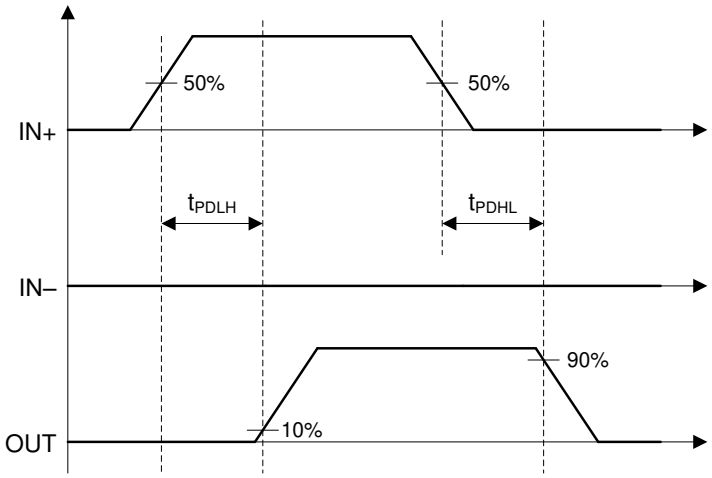


Figure 25. Non-inverting Logic Propagation Delay Measurement

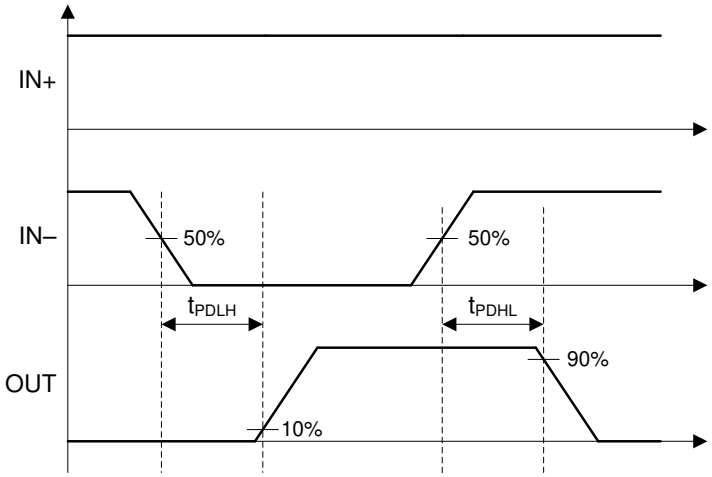


Figure 26. Inverting Logic Propagation Delay Measurement

ADVANCE INFORMATION

7.2 Input Deglitch Filter

In order to increase the robustness of gate driver over noise transient and accidental small pulses on the input pins, i.e. IN+, IN–, $\overline{\text{RST}}$/EN, a 40ns deglitch filter is designed to filter out the transients and make sure there is no faulty output responses or accidental driver malfunctions. When the IN+ or IN– PWM pulse is smaller than the input deglitch filter width, T_{INFIL}, there will be no responses on OUT drive signal. Figure 27 and Figure 28 shows the IN+ pin ON and OFF pulse deglitch filter effect. Figure 29 and Figure 30 shows the IN– pin ON and OFF pulse deglitch filter effect.

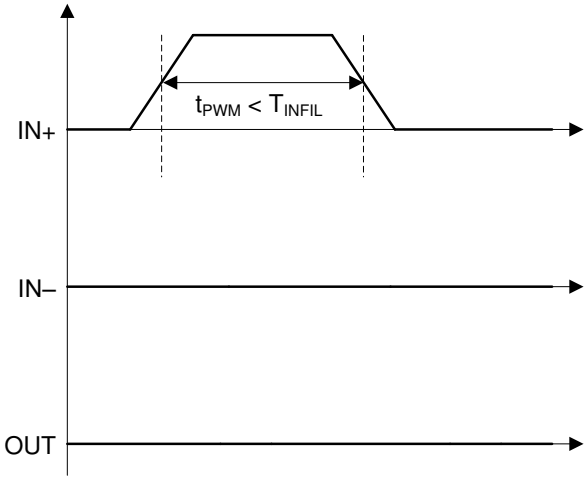


Figure 27. IN+ ON Deglitch Filter

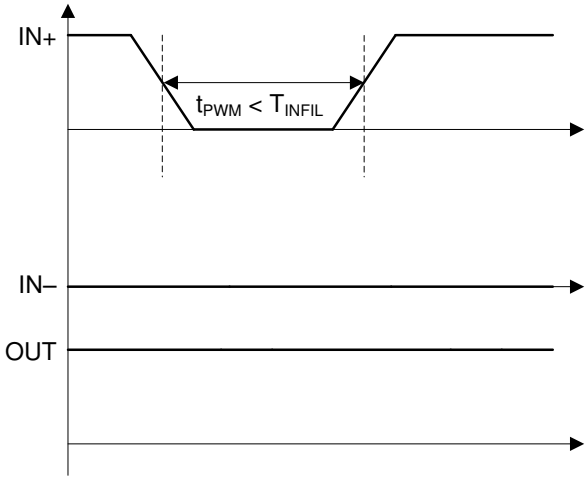


Figure 28. IN+ OFF Deglitch Filter

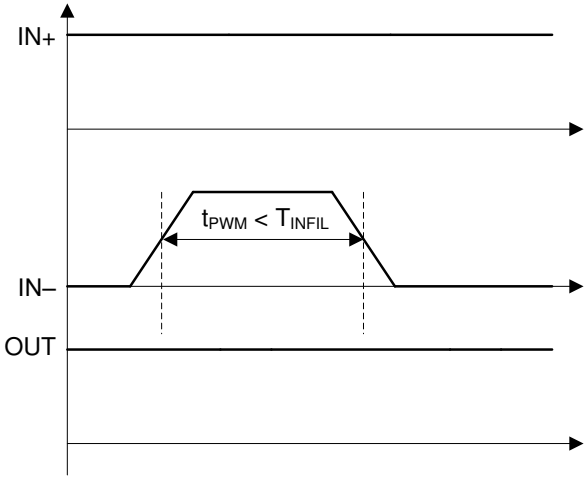


Figure 29. IN– ON Deglitch Filter

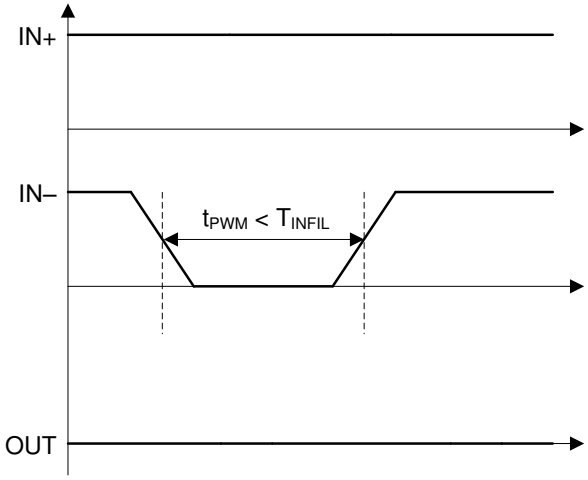


Figure 30. IN– OFF Deglitch Filter

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7.3 Active Miller Clamp

7.3.1 External Active Miller Clamp

For gate driver application with unipolar bias supply or bipolar supply with small negative turn-off voltage, active miller clamp can help add an additional low impedance path to bypass the miller current and prevent the high dV/dt introduced unintentional turn-on through the miller capacitance. Different from the internal active miller clamp, external active miller clamp function is used for applications where the gate driver may not be close to the power device or power module due to system layout considerations. External active miller clamp function provide a 5V gate drive signal to turn-on the external miller clamp FET when the gate driver voltage is less than miller clamp threshold, V_{CLMPTH}. Figure 31 shows the timing diagram for external active miller clamp function.

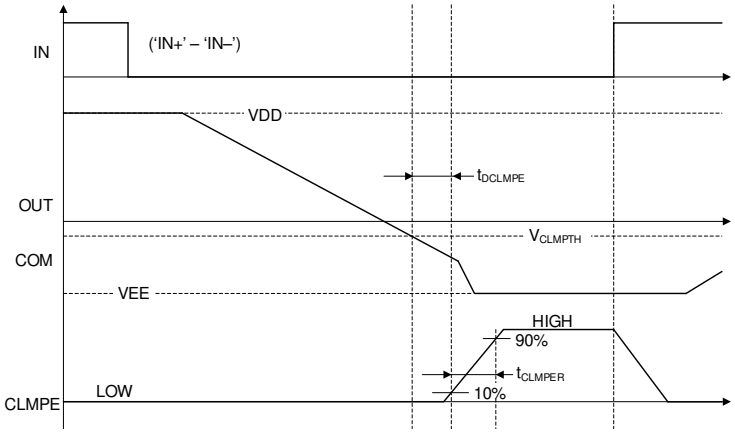


Figure 31. Timing Diagram for External Active Miller Clamp Function

ADVANCE INFORMATION

7.4 Under Voltage Lockout (UVLO)

UVLO is one of the key protection features designed to protect the system in case of bias supply failures on VCC — primary side power supply, and VDD — secondary side power supply.

7.4.1 VCC UVLO

The VCC UVLO protection details are discussed in this section. Figure 32 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN–APWM.

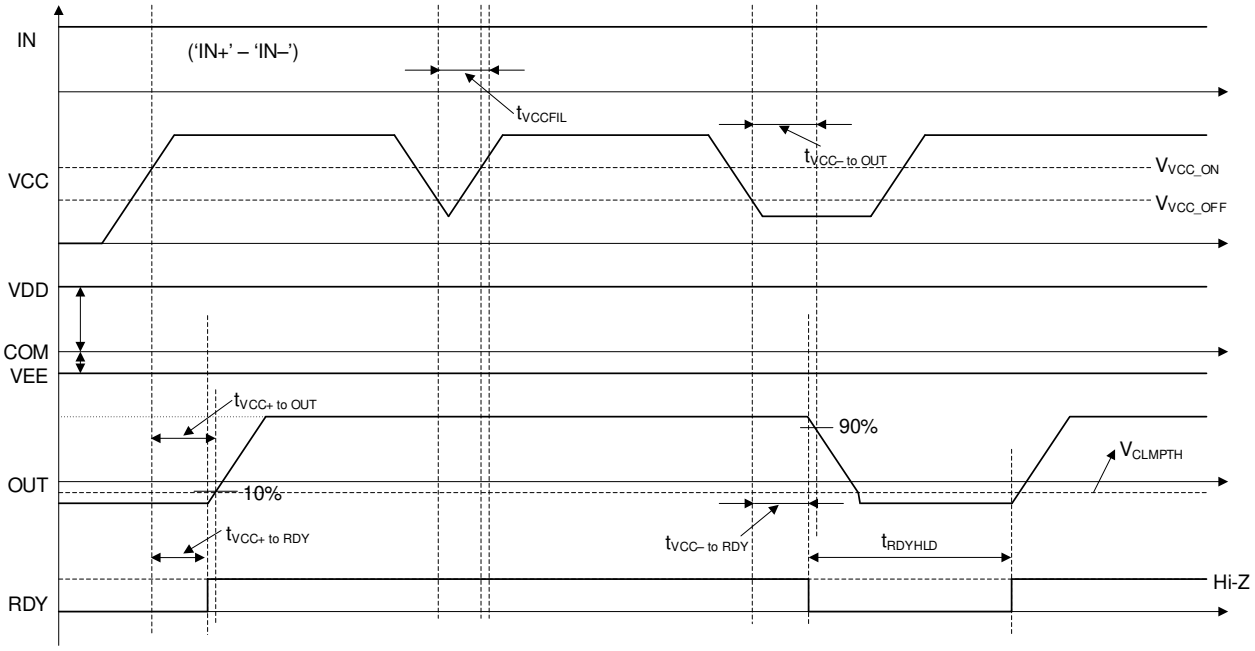


Figure 32. VCC UVLO Protection Timing Diagram

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Under Voltage Lockout (UVLO) (continued)

7.4.2 VDD UVLO

The VDD UVLO protection details are discussed in this section. Figure 33 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN–APWM.

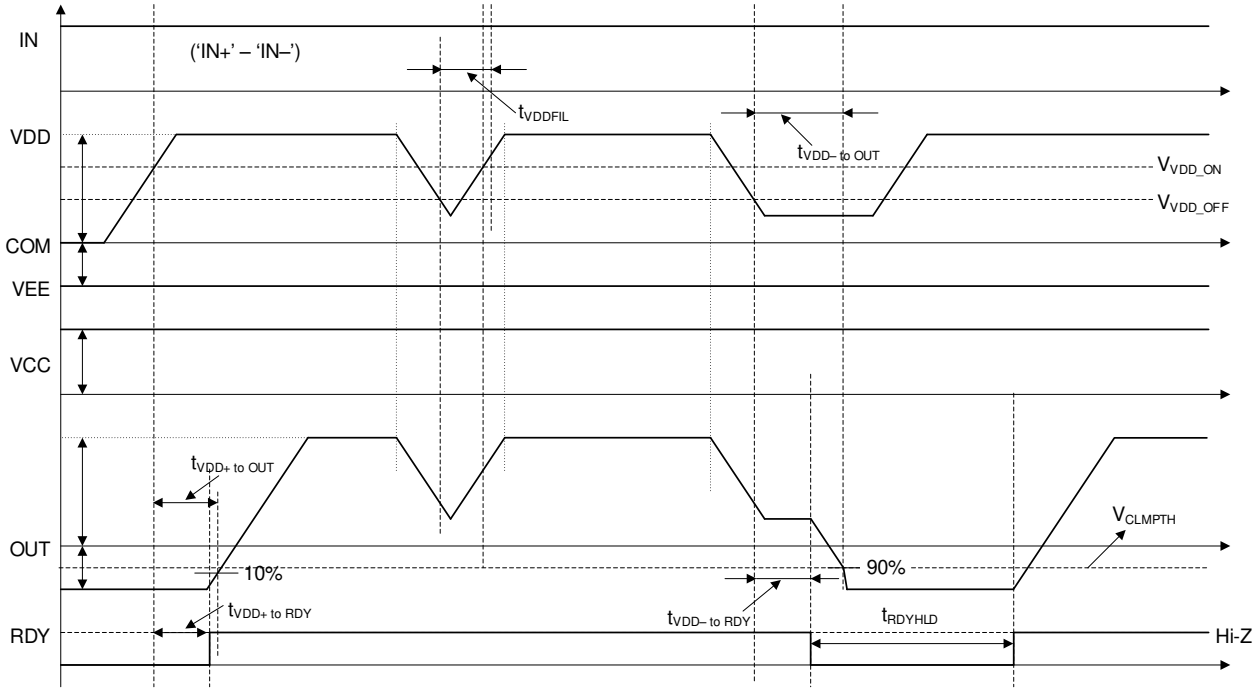


Figure 33. VDD UVLO Protection Timing Diagram

ADVANCE INFORMATION

Under Voltage Lockout (UVLO) (continued)

7.4.3 VEE UVLO

The VEE UVLO protection details are discussed in this section. Figure 34 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, and RDY.

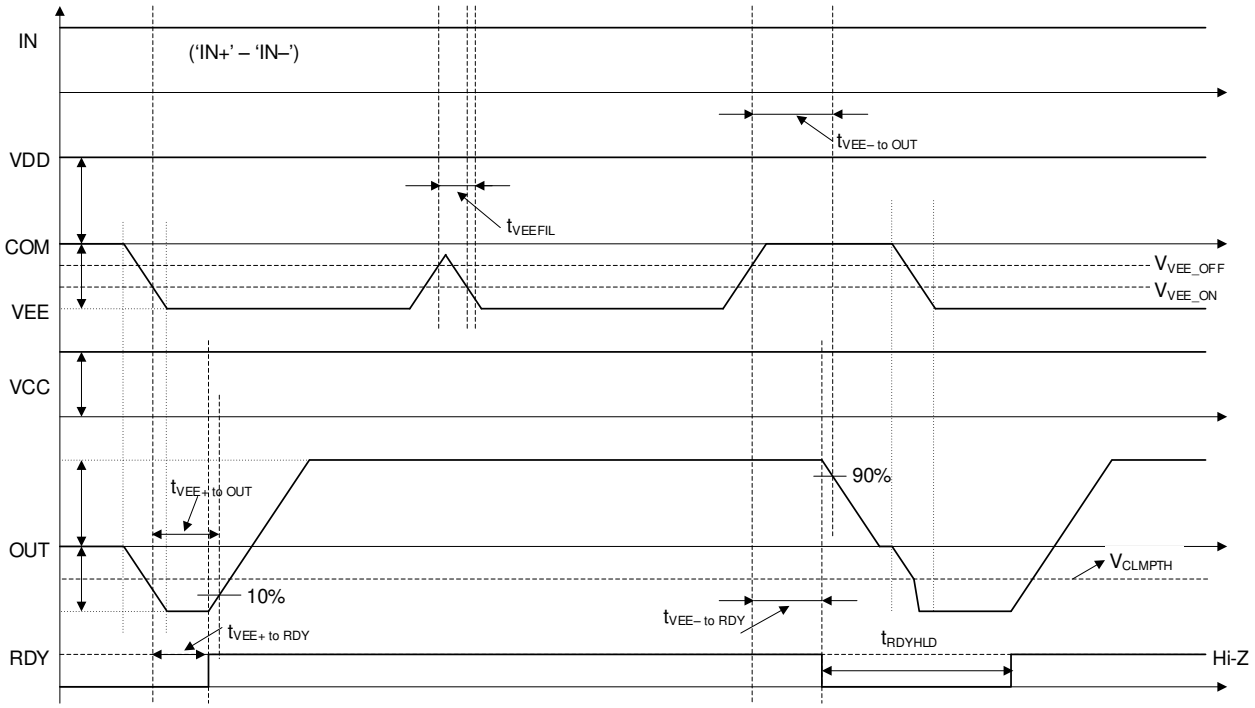


Figure 34. VEE UVLO Protection Timing Diagram

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7.5 OC (Over Current) Protection

7.5.1 OC Protection with Soft Turn-OFF

OC Protection is used to sense the current of SiC-MOSFETs and IGBTs under over current or shoot-through condition. Figure 35 shows the timing diagram of OC operation with soft turn-off.

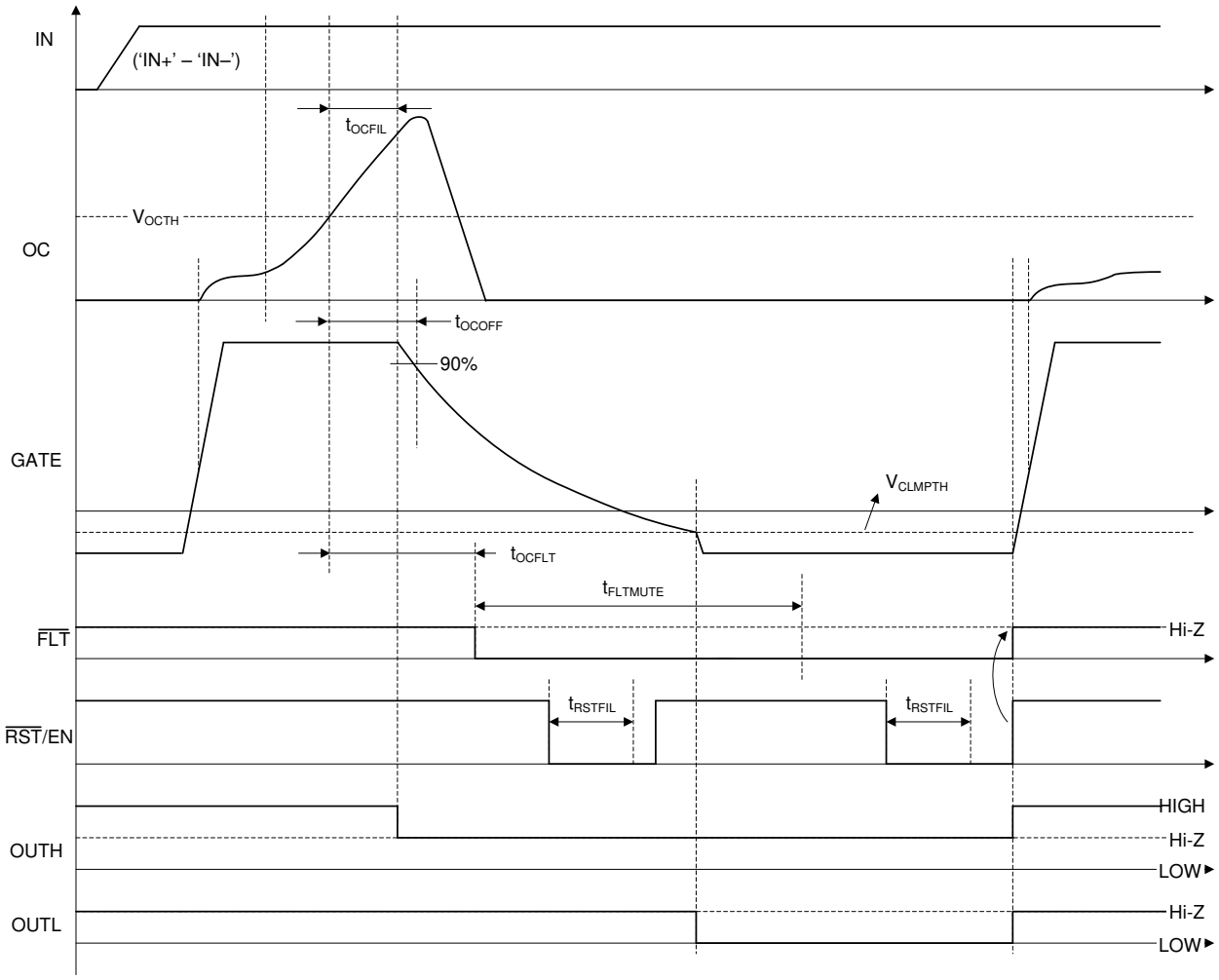


Figure 35. OC Protection with Soft Turn-OFF

7.6 ASC Protection

When ASC pin receives a logic high signal, the output will be forced high regardless of the input side pin conditions. The ASC function has higher priority than the input signal and VCC UVLO. The priority of VDD and VEE UVLO, and the overcurrent fault event are higher than ASC function.

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ASC Protection (continued)

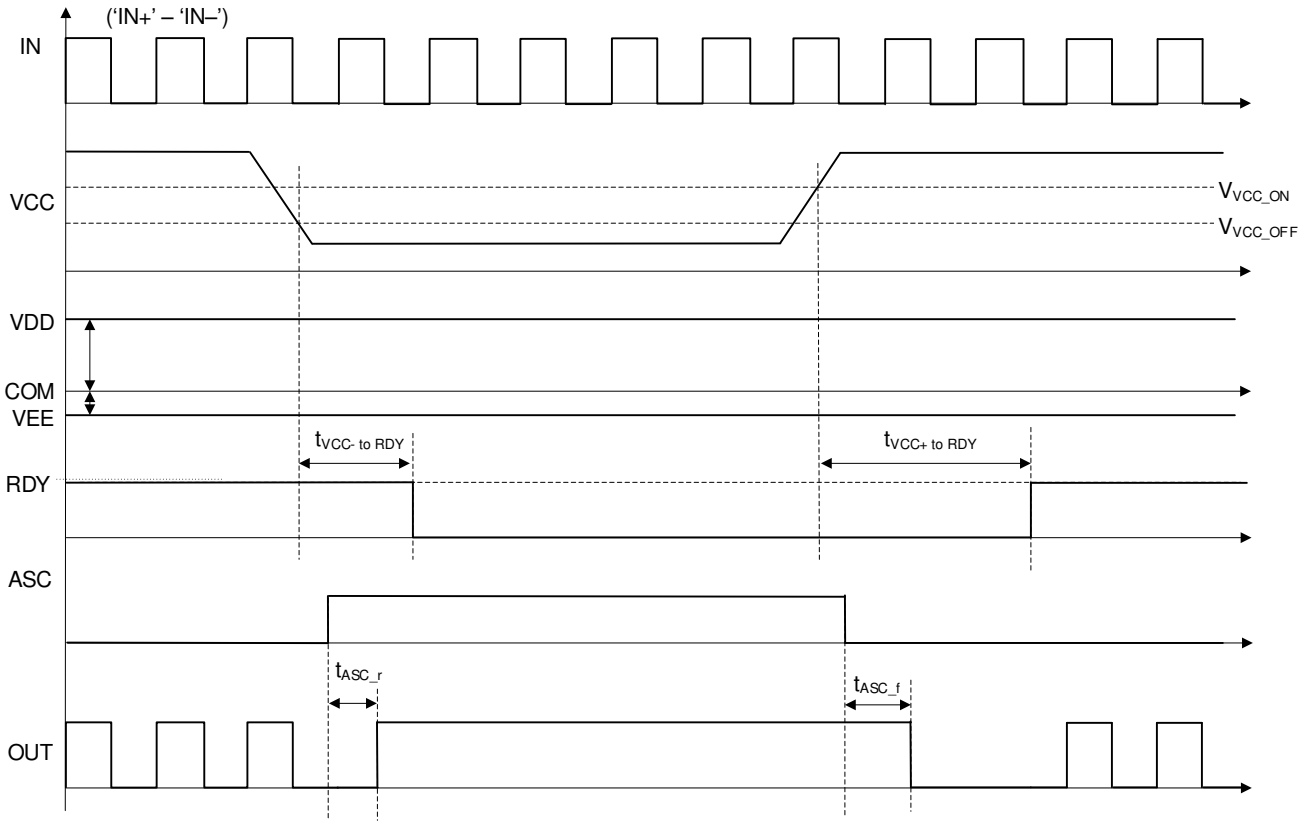


Figure 36. ASC Protection with VCC UVLO

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ASC Protection (continued)

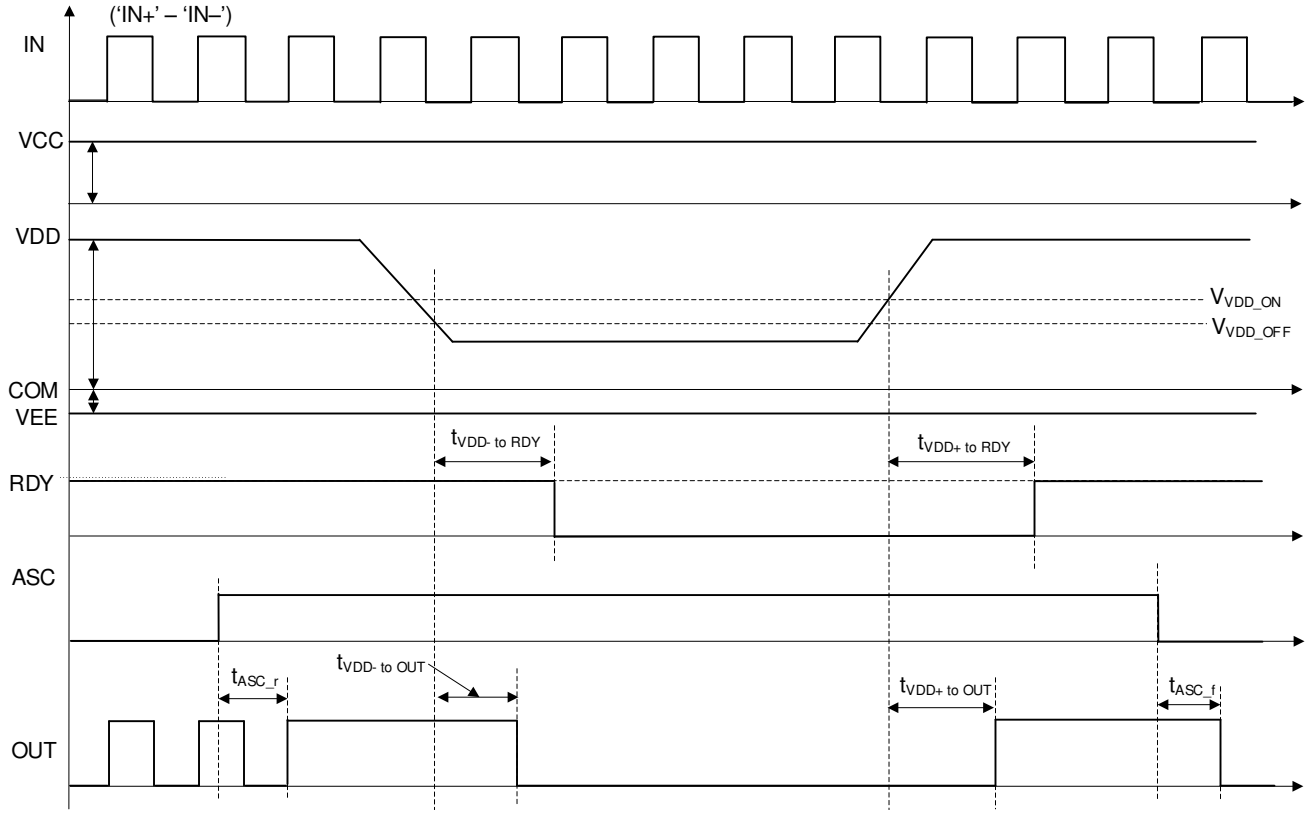


Figure 37. ASC Protection with VDD UVLO

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ASC Protection (continued)

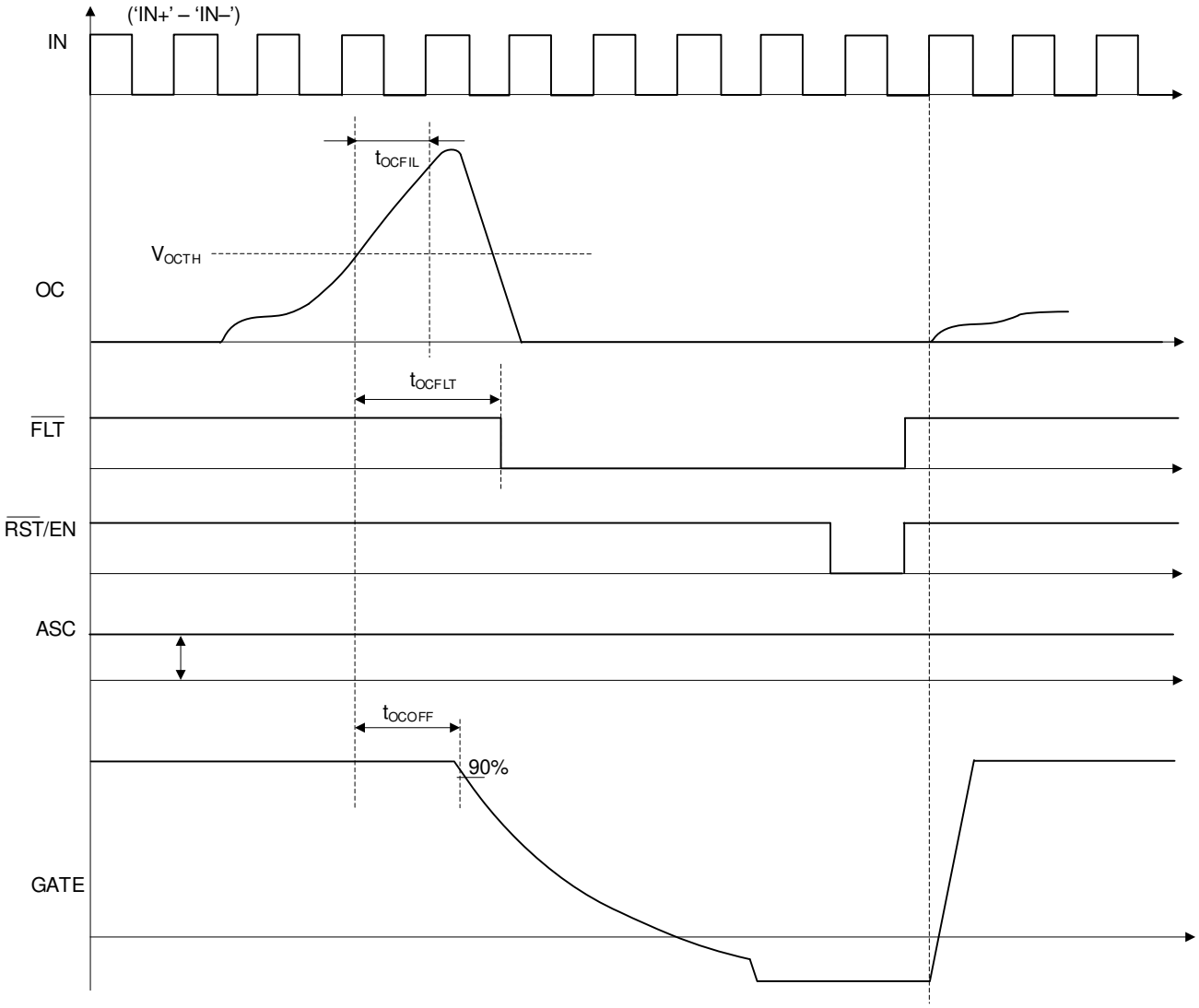


Figure 38. ASC Protection with OC Fault

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8 Detailed Description

8.1 Overview

The UCC21736-Q1 device is an advanced isolated gate driver with state-of-art protection and sensing features for SiC MOSFETs and IGBTs. The device can support up to 2121V DC operating voltage based on SiC MOSFETs and IGBTs, and can be used to above 10kW applications such as HEV/EV traction inverter, motor drive, on-board and off-board battery charger, solar inverter, etc. The galvanic isolation is implemented by the capacitive isolation technology, which can realize a reliable reinforced isolation between the low voltage DSP/MCU and high voltage side.

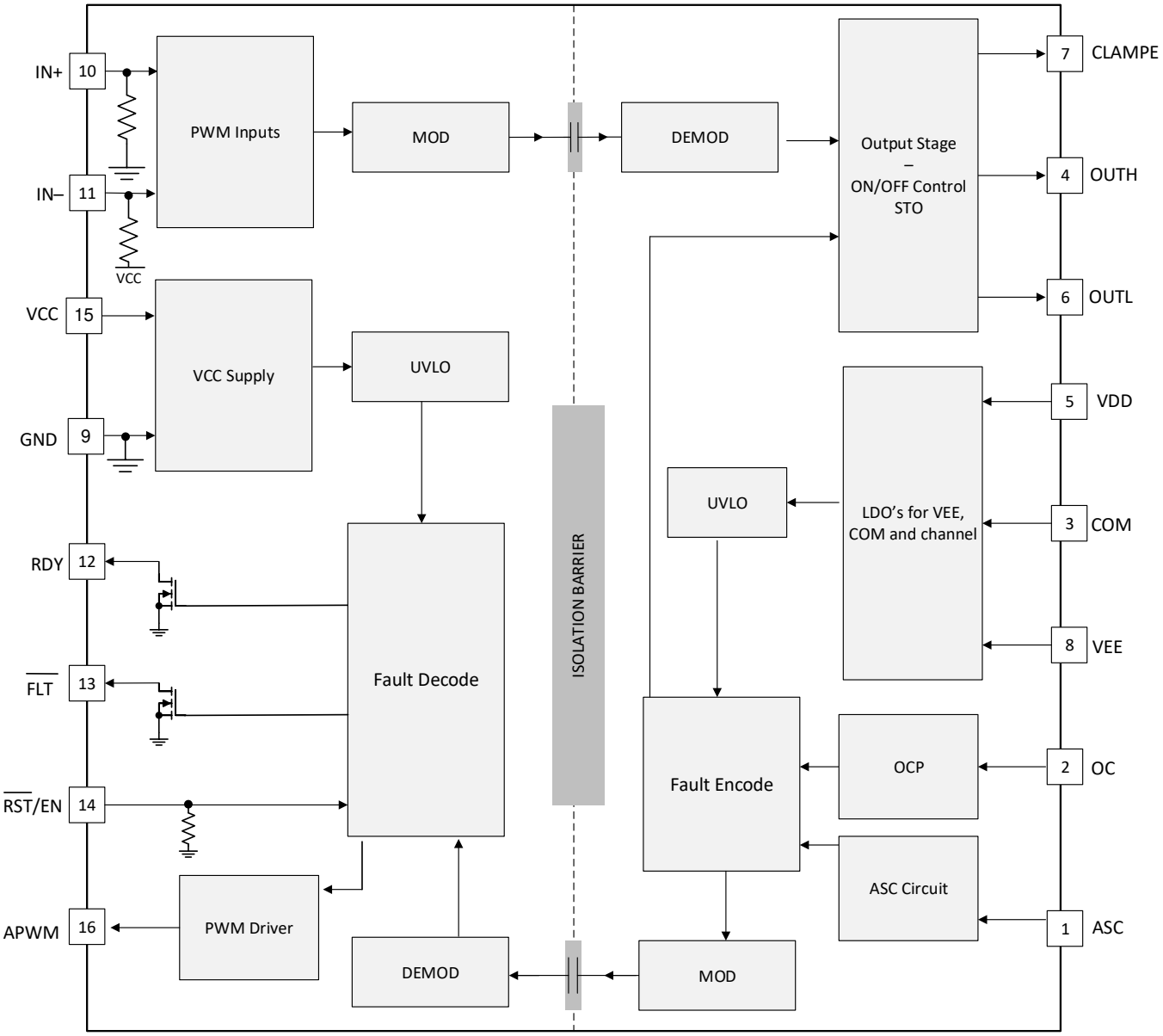
The ±10A peak sink and source current of UCC21736-Q1 can drive the SiC MOSFET modules and IGBT modules directly without an extra buffer. The driver can also be used to drive higher power modules or parallel modules with external buffer stage. The input side is isolated with the output side with a reinforced isolation barrier based on capacitive isolation technology. The device can support up to 1.5-kV_{RMS} working voltage, 12.8-kV_{PK} surge immunity with longer than 40 years isolation barrier life. The strong drive strength helps to switch the device fast and reduce the switching loss. While the 150V/ns minimum CMTI guarantees the reliability of the system with fast switching speed. The small propagation delay and part-to-part skew can minimize the deadtime setting, so the conduction loss can be reduced.

The device includes extensive protection and monitor features to increase the reliability and robustness of the SiC MOSFET and IGBT based systems. The 12V output side power supply UVLO is suitable for switches with gate voltage ≥ 15V. The active miller clamp feature prevents the false turn on causing by miller capacitance during fast switching. External miller clamp FET can be used, providing more versatility to the system design. The device has the state-of-art overcurrent and short circuit detection time, and fault reporting function to the low voltage side DSP/MCU. The soft turn off is triggered when the overcurrent or short circuit fault is detected, minimizing the short circuit energy while reducing the overshoot voltage on the switches.

The active short circuit feature can create a phase to phase short circuit for a three-phase inverter, which is useful for the motor drive applications to protect the battary if the microcontroller loses control.

ADVANCE INFORMATION

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power Supply

The input side power supply VCC can support a wide voltage range from 3V to 5.5V. The device supports both unipolar and bipolar power supply on the output side, with a wide range from 13V to 33V from VDD to VEE. The negative power supply with respect to switch source or emitter is usually adopted to avoid false turn on when the other switch in the phase leg is turned on. The negative voltage is especially important for SiC MOSFET due to its fast switching speed.

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Feature Description (continued)

8.3.2 Driver Stage

UCC21736-Q1 has ±10A peak drive strength and is suitable for high power applications. The high drive strength can drive a SiC MOSFET module, IGBT module or paralleled discrete devices directly without extra buffer stage. UCC21736-Q1 can also be used to drive higher power modules or parallel modules with extra buffer stage. Regardless of the values of VDD, the peak sink and source current can be kept at 10A. The driver features an important safety function wherein, when the input pins are in floating condition, the OUTH/OUTL is held in LOW state. The split output of the driver stage is depicted in . The driver has rail-to-rail output by implementing a hybrid pull-up structure with a P-Channel MOSFET in parallel with an N-Channel MOSFET, and an N-Channel MOSFET to pulldown. The pull-up NMOS is the same as the pull down NMOS, so the on resistance R_{NMOS} is the same as R_{OL}. The hybrid pull-up structure delivers the highest peak-source current when it is most needed, during the miller plateau region of the power semiconductor turn-on transient. The R_{OH} in represents the on-resistance of the pull-up P-Channel MOSFET. However, the effective pull-up resistance is much smaller than R_{OH}. Since the pull-up N-Channel MOSFET has much smaller on-resistance than the P-Channel MOSFET, the pull-up N-Channel MOSFET dominates most of the turn-on transient, until the voltage on OUTH pin is about 3V below VDD voltage. The effective resistance of the hybrid pull-up structure during this period is about 2 x R_{OL} . Then the P-Channel MOSFET pulls up the OUTH voltage to VDD rail. The low pull-up impedance results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor and reduces the turn on switching loss.

The pull-down structure of the driver stage is implemented solely by a pull-down N-Channel MOSFET. The on-resistance of the N-Channel MOSFET R_{OL} can be found in the . This MOSFET can ensure the OUTL voltage be pulled down to VEE rail. The low pull-down impedance not only results in high sink current to reduce the turn-off time, but also helps to increase the noise immunity considering the miller effect.

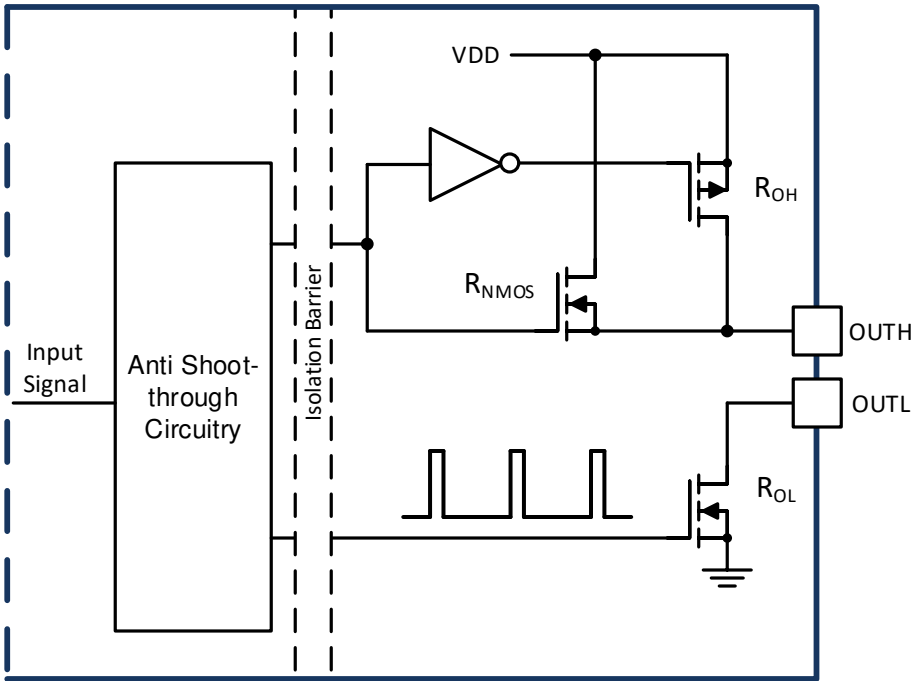


Figure 39. Gate Driver Output Stage

8.3.3 VCC, VDD and VEE Undervoltage Lockout (UVLO)

UCC21736-Q1 implements the internal UVLO protection feature for both input and output power supplies VCC and VDD. When the supply voltage is lower than the threshold voltage, the driver output is held as LOW. The output only goes HIGH when both VCC and VDD are out of the UVLO status. The UVLO protection feature not only reduces the power consumption of the driver itself during low power supply voltage condition, but also increases the efficiency of the power stage. For SiC MOSFET and IGBT, the on-resistance reduces while the

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Feature Description (continued)

gate-source voltage or gate-emitter voltage increases. If the power semiconductor is turned on with a low VDD value, the conduction loss increases significantly and can lead to a thermal issue and efficiency reduction of the power stage. UCC21736-Q1 implements 12V threshold voltage of VDD UVLO, with 800mV hysteresis; -3V threshold voltage of VEE UVLO, with 400mV hysteresis. This threshold voltage is suitable for both SiC MOSFET and IGBT.

The UVLO protection block features with hysteresis and deglitch filter, which help to improve the noise immunity of the power supply. During the turn on and turn off switching transient, the driver sources and sinks a peak transient current from the power supply, which can result in sudden voltage drop of the power supply. With hysteresis and UVLO deglitch filter, the internal UVLO protection block will ignore small noises during the normal switching transients.

The timing diagrams of the UVLO feature of VCC, VDD and VEE are shown in Figure 32, Figure 33 and Figure 34.The RDY pin on the input side is used to indicate the power good condition. The RDY pin is open drain. During UVLO condition, the RDY pin is held in low status and connected to GND. Normally the pin is pulled up externally to VCC to indicate the power good.

8.3.4 Active Pulldown

UCC21736-Q1 implements an active pulldown feature to ensure the OUTH/OUTL pin clamping to VEE when the VDD is open. The OUTH/OUTL pin is in high-impedance status when VDD is open, the active pulldown feature can prevent the output be false turned on before the device is back to control.

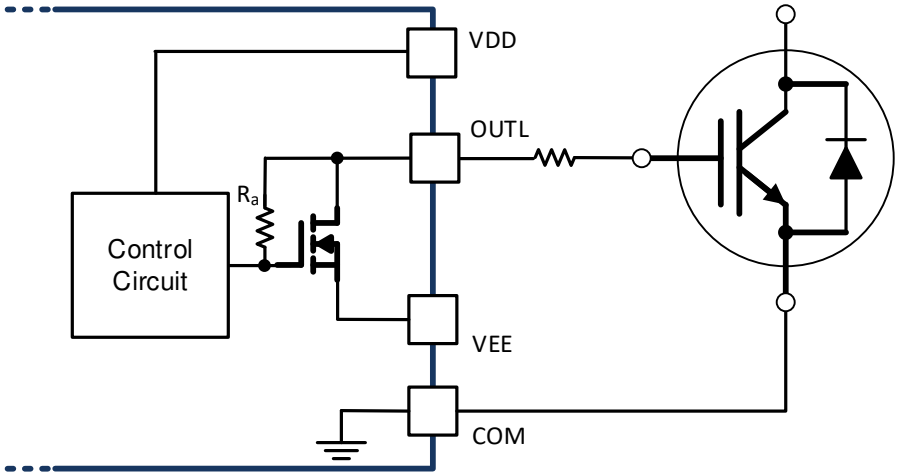


Figure 40. Active Pulldown

8.3.5 Short Circuit Clamping

During short circuit condition, the miller capacitance can cause a current sinking to the OUTH/OUTL pin due to the high dV/dt and boost the OUTH/OUTL voltage. The short circuit clamping feature of UCC21736-Q1 can clamp the OUTH/OUTL pin voltage to be slightly higher than VDD, which can protect the power semiconductors from a gate-source and gate-emitter overvoltage breakdown. This feature is realized by an internal diode from the OUTH/OUTL to VDD.

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Feature Description (continued)

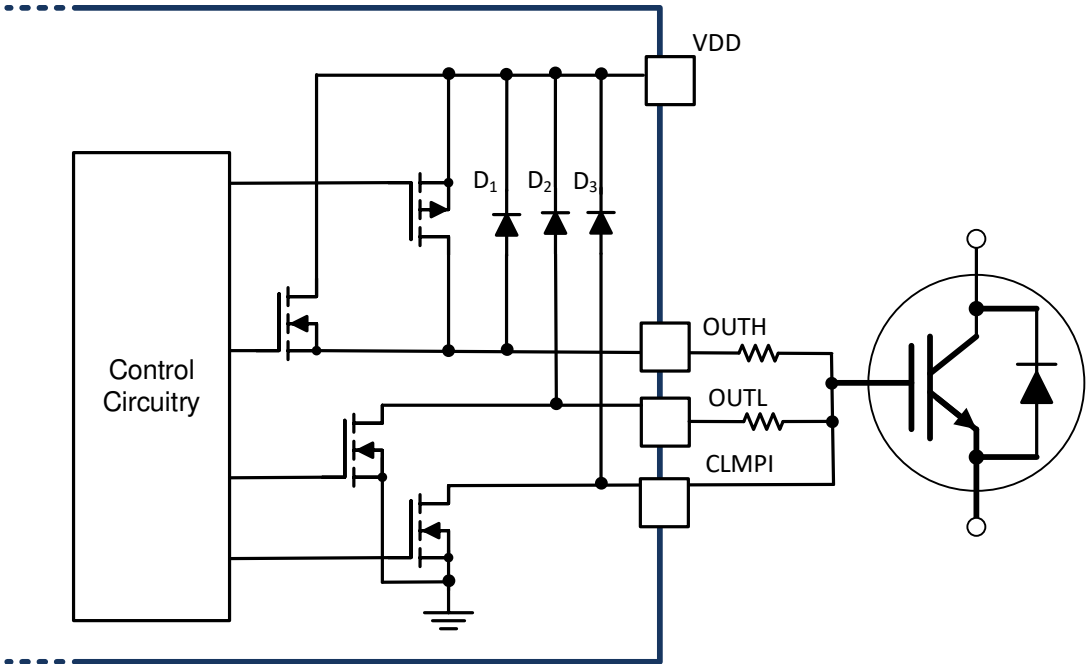


Figure 41. Short Circuit Clamping

8.3.6 External Active Miller Clamp

Active miller clamp feature is important to prevent the false turn-on while the driver is in OFF state. In applications which the device can be in synchronous rectifier mode, the body diode conducts the current during the deadtime while the device is in OFF state, the drain-source or collector-emitter voltage remains the same and the dV/dt happens when the other power semiconductor of the phase leg turns on. The low internal pull-down impedance of UCC21736-Q1 can provide a strong pulldown to hold the OUTL to VEE. However, external gate resistance is usually adopted to limit the dV/dt. The miller effect during the turn on transient of the other power semiconductor can cause a voltage drop on the external gate resistor, which boost the gate-source or gate-emitter voltage. If the voltage on V_{GS} or V_{GE} is higher than the threshold voltage of the power semiconductor, a shoot through can happen and cause catastrophic damage. The active miller clamp feature of UCC21736-Q1 drives an external MOSFET, which connects to the device gate. The external MOSFET is triggered when the gate voltage is lower than V_{CLMPTH}, which is 2V above VEE, and creates a low impedance path to avoid the false turn on issue.

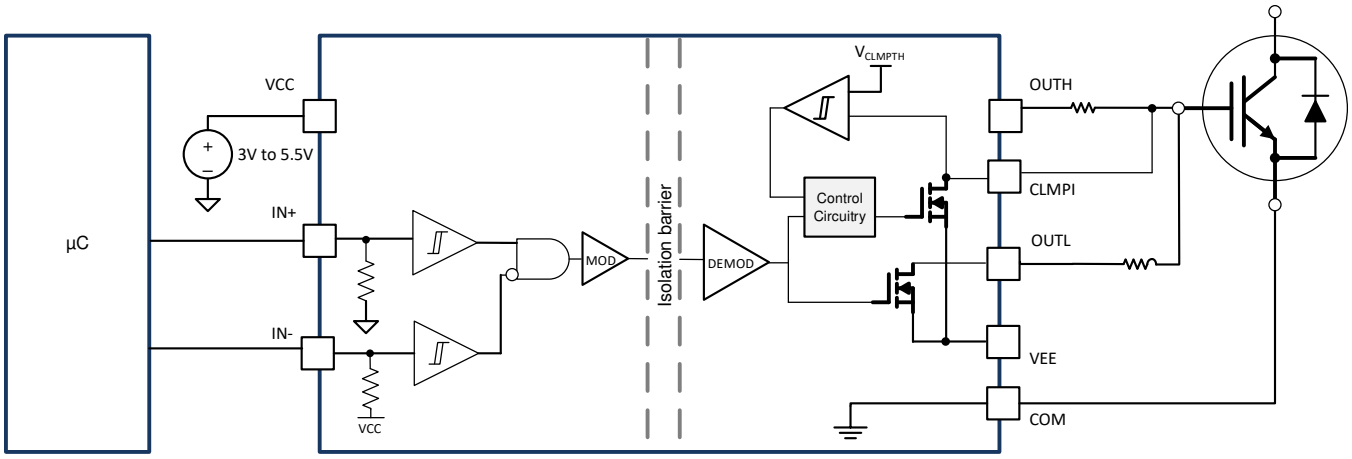


Figure 42. Active Miller Clamp

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Feature Description (continued)

8.3.7 Overcurrent and Short Circuit Protection

The UCC21736-Q1 implements a fast overcurrent and short circuit protection feature to protect the SiC MOSFET or IGBT from catastrophic breakdown during fault. The OC pin of the device has a typical 0.7V threshold with respect to COM, source or emitter of the power semiconductor. When the input is in floating condition, or the output is held in low state, the OC pin is pulled down by an internal MOSFET and held in LOW state, which prevents the overcurrent and short circuit fault from false triggering. The OC pin is in high-impedance state when the output is in high state, which means the overcurrent and short circuit protection feature only works when the power semiconductor is in on state. The internal pulldown MOSFET helps to discharge the voltage of OC pin when the power semiconductor is turned off.

The overcurrent and short circuit protection feature can be used to SiC MOSFET module or IGBT module with SenseFET, traditional desaturation circuit and shunt resistor in series with the power loop for lower power applications. For SiC MOSFET module or IGBT module with SenseFET, the SenseFET integrated in the module can scale down the drain current or collector current. With an external high precision sense resistor, the drain current or collector current can be accurately measured. If the voltage of the sensed resistor higher than the overcurrent threshold V_{OCTH} is detected, the soft turn-off is initiated. A fault will be reported to the input side $\overline{FLT}$ pin to DSP/MCU. The output is held to LOW after the fault is detected, and can only be reset by the $\overline{RST}$/EN pin. The state-of-art overcurrent and short circuit detection time helps to ensure a short shutdown time for SiC MOSFET and IGBT.

The overcurrent and short circuit protection feature can also be paired with desaturation circuit and shunt resistors. The DESAT threshold can be programmable in this case, which increases the versatility of the device. Detailed application diagrams of desaturation circuit and shunt resistor will be given in .

- High current and high dI/dt during the overcurrent and short circuit fault can cause a voltage bounce on shunt resistor's parasitic inductance and board layout parasitic, which results in false trigger of OC pin. High precision, low ESL and small value resistor must be used in this approach.
- Shunt resistor approach is not recommended for high power applications and short circuit protection of the low power applications.

The detailed applications of the overcurrent and short circuit feature will be discussed in the Application and Implementation section.

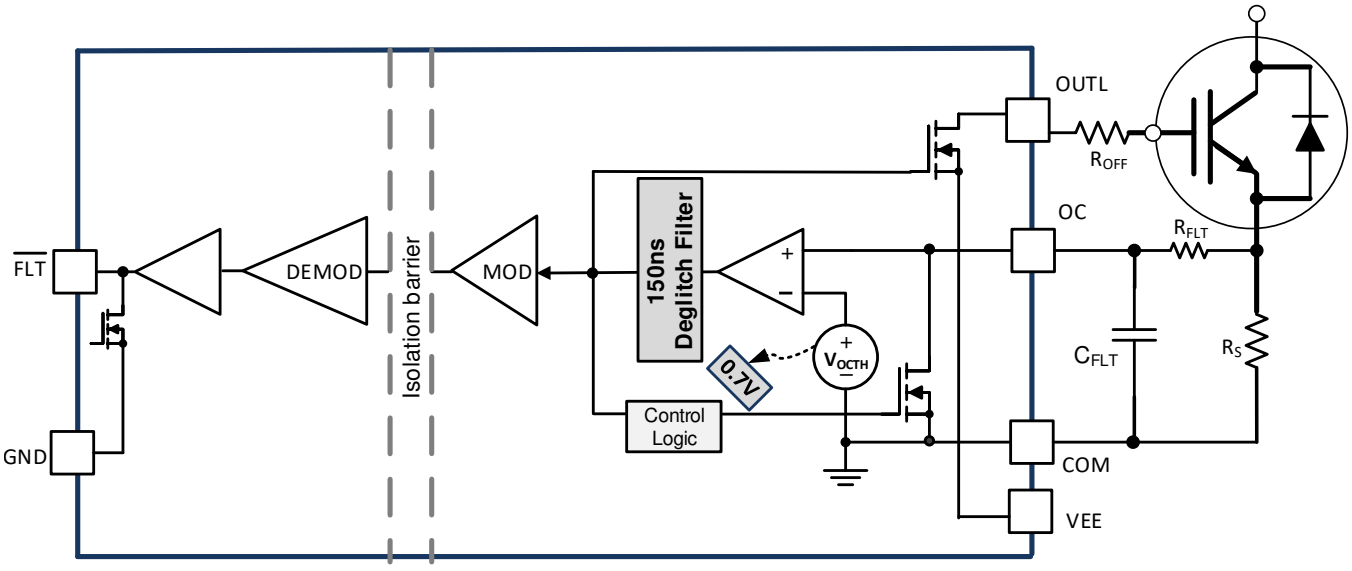


Figure 43. Overcurrent and Short Circuit Protection

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Feature Description (continued)

8.3.8 Fault ($\overline{\text{FLT}}$, Reset and Enable ($\overline{\text{RST}}$/EN)

The $\overline{\text{FLT}}$ pin of UCC21736-Q1 is open drain and can report a fault signal to the DSP/MCU when the overcurrent and short circuit fault is detected through OC pin. The $\overline{\text{FLT}}$ pin is pulled down to GND, and is held in low state unless a reset signal is received from $\overline{\text{RST}}$/EN. The device has a fault mute time $t_{FLTMUTE}$, within which the device ignores any reset signal.

The $\overline{\text{RST}}$/EN is pulled down internally. The device is disabled by default if the $\overline{\text{RST}}$/EN pin is floating. The pin has two purposes:

- Resets the overcurrent and short circuit fault signaled on $\overline{\text{FLT}}$ pin. The $\overline{\text{RST}}$/EN pin is active low, if the pin is set and held in low state for more than t_{RSTFIL}, the fault signal is reset and $\overline{\text{FLT}}$ is reset back to the high impedance status at the rising edge of $\overline{\text{RST}}$/EN pin.
- Enable and shutdown the device. If the $\overline{\text{RST}}$/EN pin is pulled low, the driver is disabled and shut down by the regular turn off. The pin must be pulled up externally to enable the part, otherwise the device is disabled by default.

8.3.9 ASC Protection and APWM Monitor

When VCC loses power, or MCU is malfunctional, the motor can lose control and reversely charging the battery. Overvoltage of the battery can cause battery break down, or even the fire hazard. In this case, the active short circuit (ASC) function is used to protect the system by forcing the output signal high, turning on the switch and creating an active short circuit loop between the phases to bypass the battery. The timing diagram of ASC protection with VCC UVLO, VDD UVLO and OC fault are shown in Figure 36, Figure 37, and Figure 38.

The UCC21736-Q1 encodes the voltage signal V_{ASC} to a PWM signal, passing through the reinforced isolation barrier, and output to APWM pin on the input side. Thus the ASC pin status can be monitored. The PWM signal can either be transferred directly to DSP/MCU to calculate the duty cycle, or filtered by a simple RC filter as an analog signal. The ASC input voltage varies from 0V to 5V, and the corresponding duty cycle of the APWM output ranges from 95% to 5% with 400kHz frequency.

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8.4 Device Functional Modes

lists the device function.

Table 1. Function Table

Input							Output			
VCC	VDD	VEE	IN+	IN-	$\overline{RST}$/EN	ASC	RDY	$\overline{FLT}$	OUTH/OUTL	CLMPE
X	PU	PU	X	X	X	High	X	X	High	Low
PU	PD	PU	X	X	High	X	Low	HiZ	Low	High
PU	PU	PD	X	X	High	X	Low	HiZ	Low	High
PU	PD	X	X	X	X	Low	Low	HiZ	Low	Low
PD	PU	X	X	X	X	Low	HiZ	HiZ	Low	High
PU	PU	X	X	X	Low	Low	HiZ	HiZ	Low	High
PU	Open	X	X	X	X	Low	Low	HiZ	HiZ	HiZ
PU	PU	Open	X	X	X	Low	Low	HiZ	Low	High
PU	PU	X	Low	X	High	Low	HiZ	HiZ	Low	High
PU	PU	X	X	High	High	Low	HiZ	HiZ	Low	High
PU	PU	X	High	Low	High	Low	HiZ	HiZ	HiZ	Low

PU: Power Up (VCC ≥ 3V, VDD ≥ 12.8V; VEE ≤ -3.3V); PD: Power Down (VCC ≤ 2.2V, VDD ≤ 10.4V, VEE ≥ -2.3V); X: Irrelevant; P*: PWM Pulse; HiZ: High Impedance

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9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC21736-Q1 device is very versatile because of the strong drive strength, wide range of output power supply, high isolation ratings, high CMTI and superior protection and sensing features. The 1.5-kVRMS working voltage and 12.8-kVPK surge immunity can support up both SiC MOSFET and IGBT modules with DC bus voltage up to 2121V. The device can be used in both low power and high power applications such as the traction inverter in HEV/EV, on-board charger and charging pile, motor driver, solar inverter, industrial power supplies and etc. The device can drive the high power SiC MOSFET module, IGBT module or paralleled discrete device directly without external buffer drive circuit based on NPN/PNP bipolar transistor in totem-pole structure, which allows the driver to have more control to the power semiconductor and saves the cost and space of the board design. UCC21736-Q1 can also be used to drive very high power modules or paralleled modules with external buffer stage. The input side can support power supply and microcontroller signal from 3.3V to 5V, and the device level shifts the signal to output side through reinforced isolation barrier. The device has wide output power supply range from 13V to 33V and support wide range of negative power supply. This allows the driver to be used in SiC MOSFET applications, IGBT application and many others. The 12V UVLO benefits the power semiconductor with lower conduction loss and improves the system efficiency. As a reinforced isolated single channel driver, the device can be used to drive either a low-side or high-side driver.

UCC21736-Q1 device features extensive protection and monitoring features, which can monitor, report and protect the system from various fault conditions.

- Fast detection and protection for the overcurrent and short circuit fault. The feature is preferable in a split source SiC MOSFET module or a split emitter IGBT module. For the modules with no integrated current mirror or paralleled discrete semiconductors, the traditional desaturation circuit can be modified to implement short circuit protection. The semiconductor is shutdown when the fault is detected and FLTb pin is pulled down to indicate the fault detection. The device is latched unless reset signal is received from the $\overline{\text{RST}}$/EN pin.
- Soft turn-off feature to protect the power semiconductor from catastrophic breakdown during overcurrent and short circuit fault. The shutdown energy can be controlled while the overshoot of the power semiconductor is limited.
- UVLO detection to protect the semiconductor from excessive conduction loss. Once the device is detected to be in UVLO mode, the output is pulled down and RDY pin indicates the power supply is lost. The device is back to normal operation mode once the power supply is out of the UVLO status. The power good status can be monitored from the RDY pin.
- Active short circuit feature creates phase to phase short circuit in three-phase inverter to protect the battery from overvoltage breakdown.
- The active miller clamp feature protects the power semiconductor from false turn on by driving an external MOSFET. This feature allows the flexibility of the board layout design and the pulldown strength of miller clamp FET.
- Enable and disable function through the RSTb/EN pin.
- Short circuit clamping.
- Active pulldown.

9.2 Typical Application

shows the typical application of a half bridge using two UCC21736-Q1 isolated gate drivers. The half bridge is a basic element in various power electronics applications such as traction inverter in HEV/EV to convert the DC current of the electric vehicle's battery to the AC current to drive the electric motor in the propulsion system. The topology can also be used in motor drive applications to control the operating speed and torque of the AC motors.

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Typical Application (continued)

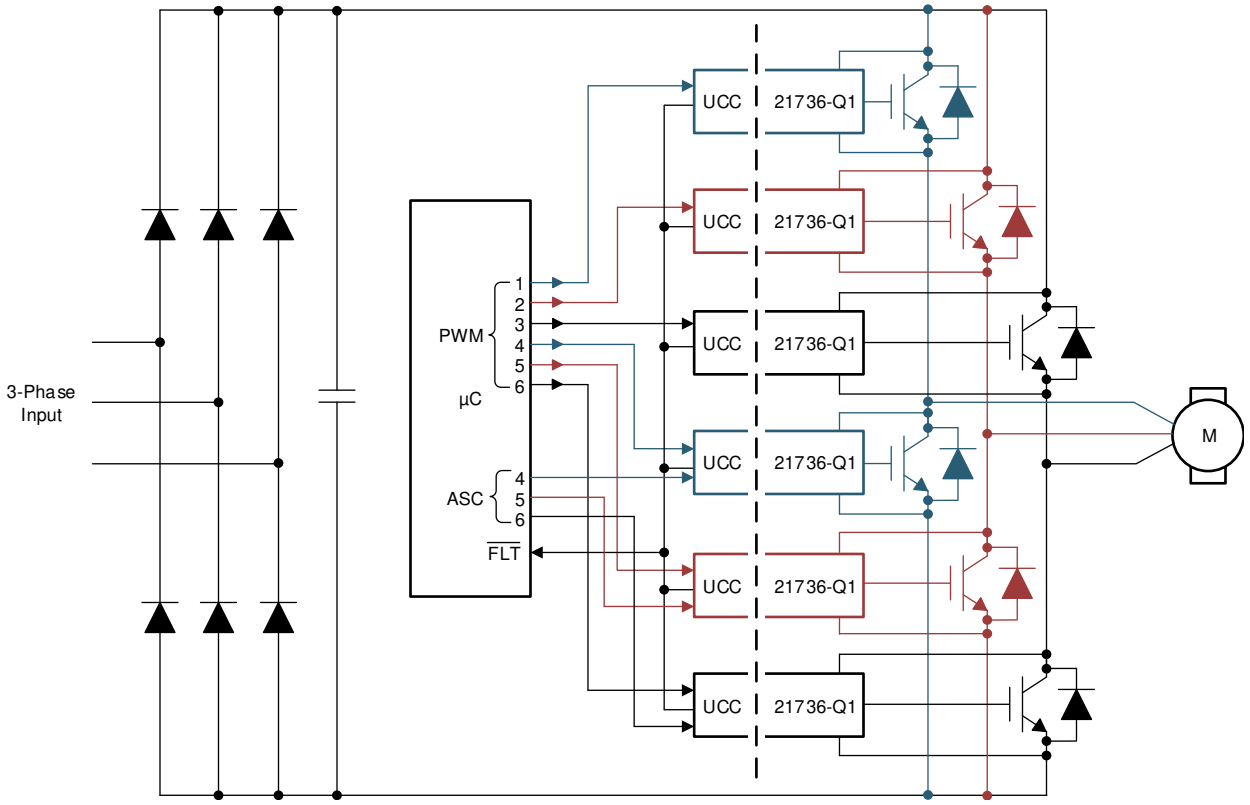


Figure 44. Typical Application Schematic

9.2.1 Design Requirements

The design of the power system for end equipment should consider some design requirements to ensure the reliable operation of UCC1736-Q1 through the load range. The design considerations include the peak source and sink current, power dissipation, overcurrent and short circuit protection and etc.

A design example for a half bridge based on IGBT is given in this subsection. The design parameters are show in .

Table 2. Design Parameters

Parameter	Value
Input Supply Voltage	5V
IN-OUT Configuration	Non-inverting
Positive Output Voltage VDD	15V
Negative Output Voltage VEE	-5V
DC Bus Voltage	800V
Peak Drain Current	300A
Switching Frequency	50kHz
Switch Type	IGBT Module

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9.2.2 Detailed Design Procedure

9.2.2.1 Input filters for IN+, IN- and $\overline{\text{RST}}$/EN

In the applications of traction inverter or motor drive, the power semiconductors are in hard switching mode. With the strong drive strength of UCC21736-Q1, the dV/dt can be high, especially for SiC MOSFET. Noise can not only be coupled to the gate voltage due to the parasitic inductance, but also to the input side as the non-ideal PCB layout and coupled capacitance.

UCC21736-Q1 features a 40ns internal deglitch filter to IN+, IN- and $\overline{\text{RST}}$/EN pin. Any signal less than 40ns can be filtered out from the input pins. For noisy systems, external low pass filter can be added externally to the input pins. Adding low pass filters to IN+, IN- and $\overline{\text{RST}}$/EN pins can effectively increase the noise immunity and increase the signal integrity. When not in use, the IN+, IN- and $\overline{\text{RST}}$/EN pins should not be floating. IN- should be tied to GND if only IN+ is used for non-inverting input to output configuration. The purpose of the low pass filter is to filter out the high frequency noise generated by the layout parasitics. While choosing the low pass filter resistors and capacitors, both the noise immunity effect and delay time should be considered according to the system requirements.

9.2.2.2 PWM Interlock of IN+ and IN-

UCC21736-Q1 features the PWM interlock for IN+ and IN- pins, which can be used to prevent the phase leg shoot through issue. As shown in , the output is logic low while both IN+ and IN- are logic high. When only IN+ is used, IN- can be tied to GND. To utilize the PWM interlock function, the PWM signal of the other switch in the phase leg can be sent to the IN- pin. As shown in , the PWM_T is the PWM signal to top side switch, the PWM_B is the PWM signal to bottom side switch. For the top side gate driver, the PWM_T signal is given to the IN+ pin, while the PWM_B signal is given to the IN- pin; for the bottom side gate driver, the PWM_B signal is given to the IN+ pin, while PWM_T signal is given to the IN- pin. When both PWM_T and PWM_B signals are high, the outputs of both gate drivers are logic low to prevent the shoot through condition.

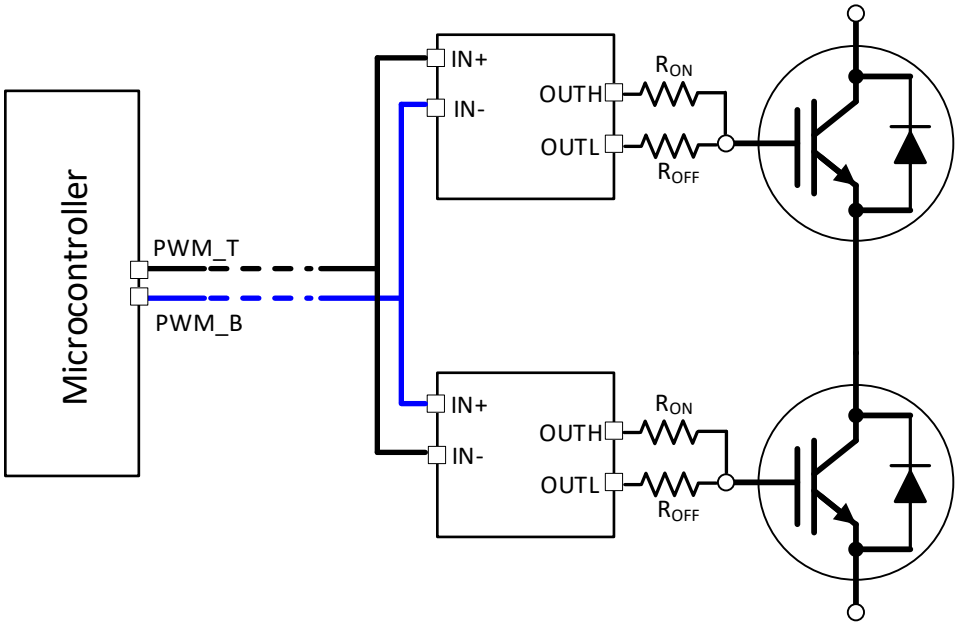


Figure 45. PWM Interlock for a Half Bridge

9.2.2.3 $\overline{\text{FLT}}$, RDY and $\overline{\text{RST}}$/EN Pin Circuitry

Both $\overline{\text{FLT}}$ and RDY pin are open-drain output. The $\overline{\text{RST}}$/EN pin has 50kΩ internal pulldown resistor, so the driver is in OFF status if the $\overline{\text{RST}}$/EN pin is not pulled up externally. A 5kΩ resistor can be used as pullup resistor for the $\overline{\text{FLT}}$, RDY and $\overline{\text{RST}}$/EN pins.

To improve the noise immunity due to the parasitic coupling and common mode noise, low pass filters can be added between the $\overline{\text{FLT}}$, RDY and $\overline{\text{RST}}$/EN pins and the microcontroller. A filter capacitor between 100pF to 300pF can be added.

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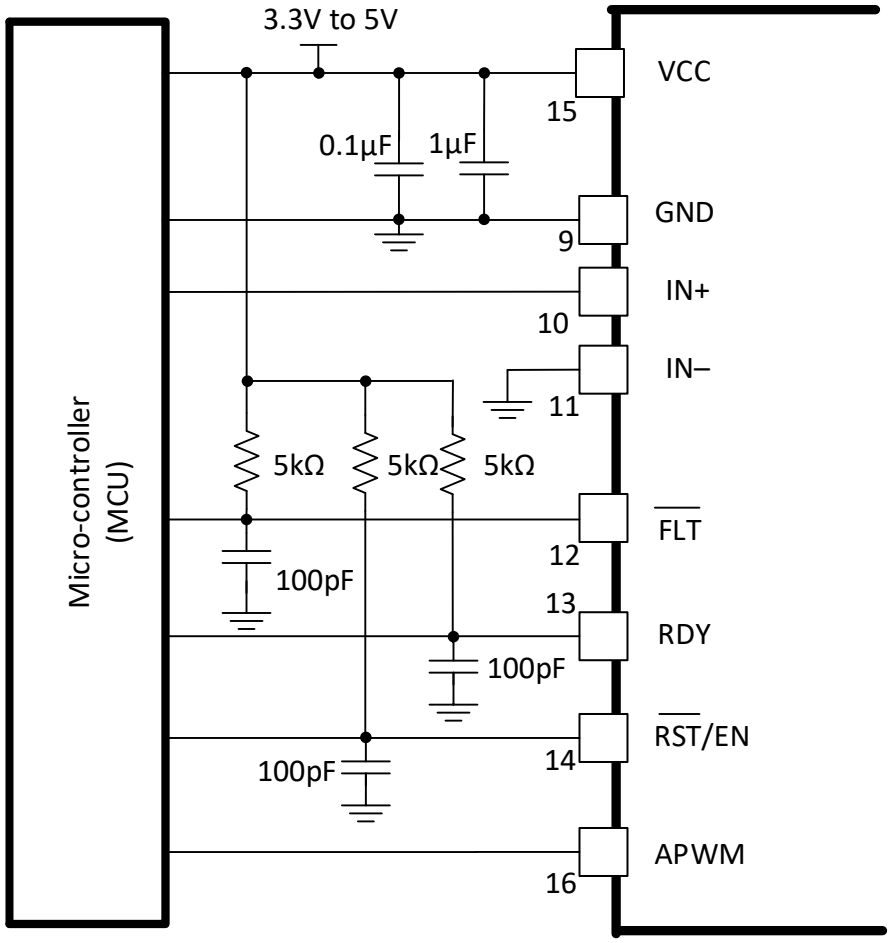


Figure 46. $\overline{\text{FLT}}$, RDY and $\overline{\text{RST}}$/EN Pins Circuitry

9.2.2.4 $\overline{\text{RST}}$/EN Pin Control

$\overline{\text{RST}}$/EN pin has two functions. It can be used to enable and shutdown the outputs of the driver, and reset the fault signaled on the $\overline{\text{FLT}}$ pin. $\overline{\text{RST}}$/EN pin needs to be pulled up to enable the device; when the pin is pulled down, the device is in disabled status. With a 50kΩ pulldown resistor existing, the driver is disabled by default.

When the driver is latched after overcurrent or short circuit fault is detected, the $\overline{\text{FLT}}$ pin and output are latched low and need to be reset by$\overline{\text{RST}}$/EN pin. $\overline{\text{RST}}$/EN pin is active low. The microcntroller needs to send a signal to $\overline{\text{RST}}$/EN pin after the fault mute time $t_{FLTMUTE}$ to reset the driver. This pin can also be used to automatically reset the driver. The continuous input signal IN+ or IN- can be applied to $\overline{\text{RST}}$/EN pin, so the microcontroller does not need to generate another control signal to reset the driver. If non-inverting input IN+ is used, then IN+ can be tied to $\overline{\text{RST}}$/EN pin. If inverting input IN- is used, then a NOT logic is needed between the inverting PWM signal from the microcontroller and the $\overline{\text{RST}}$/EN pin. In this case, the driver can be reset in every switching cycle without an extra control signal from microcontroller to $\overline{\text{RST}}$/EN pin.

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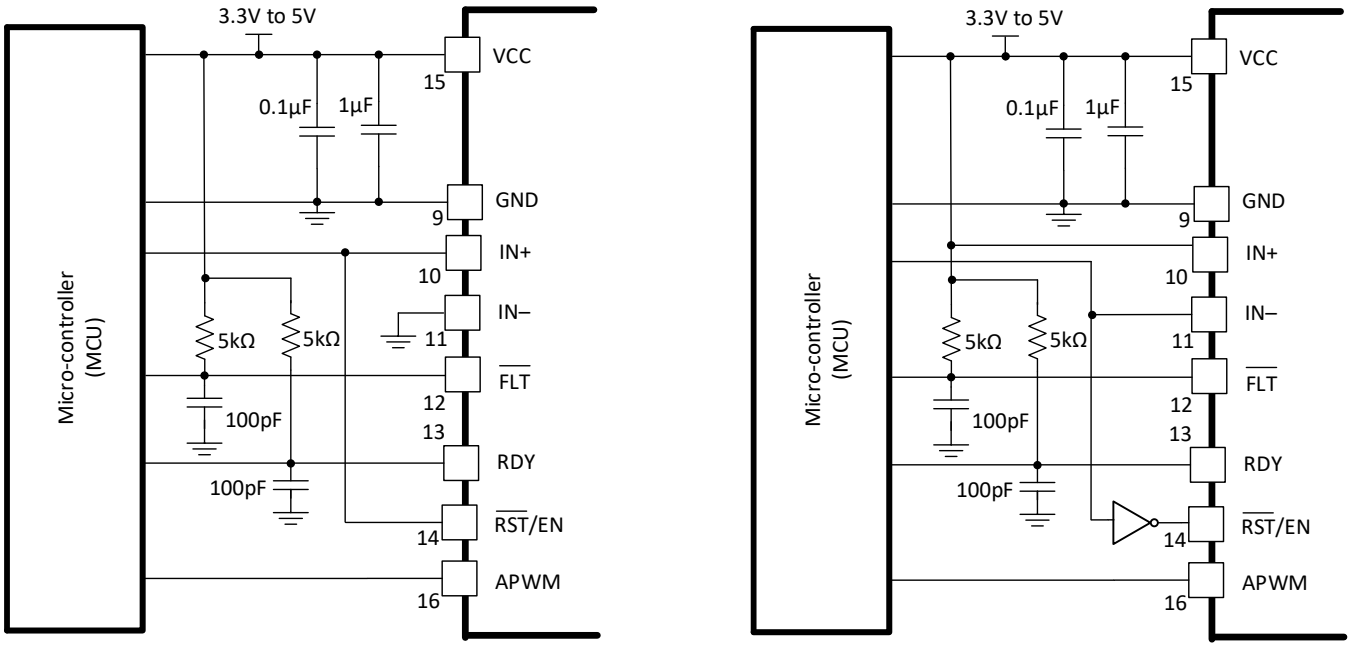


Figure 47. Automatic Reset Control

9.2.2.5 Turn on and turn off gate resistors

UCC21736-Q1 features split outputs OUTH and OUTL, which enables the independent control of the turn on and turn off switching speed. The turn on and turn off resistance determine the peak source and sink current, which controls the switching speed in turn. Meanwhile, the power dissipation in the gate driver should be considered to ensure the device is in the thermal limit. At first, the peak source and sink current are calculated as:

$$I_{source_pk} = \min(10A, \frac{VDD - VEE}{R_{OH_EFF} + R_{ON} + R_{G_Int}})$$

$$I_{sink_pk} = \min(10A, \frac{VDD - VEE}{R_{OL} + R_{OFF} + R_{G_Int}}) \quad (1)$$

Where

- R_{OH_EFF} is the effective internal pull up resistance of the hybrid pull-up structure, which is approximately 2 x R_{OL}, about 0.7 Ω
- R_{OL} is the internal pulldown resistance, about 0.3 Ω
- R_{ON} is the external turn on gate resistance
- R_{OFF} is the external turn off gate resistance
- R_{G_Int} is the internal resistance of the SiC MOSFET or IGBT module

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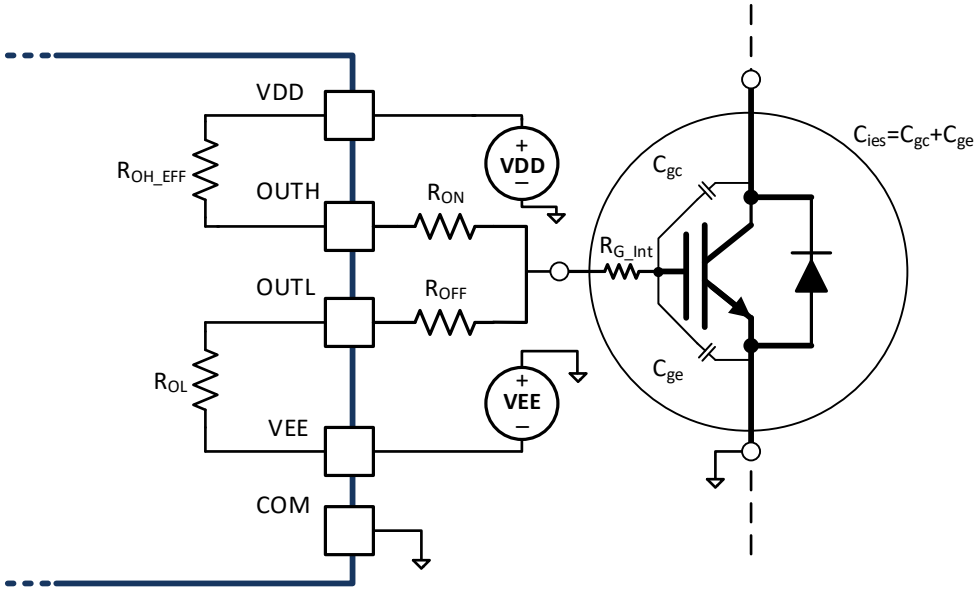


Figure 48. Output Model for Calculating Peak Gate Current

For example, for an IGBT module based system with the following parameters:

- Q_g = 3300 nC
- R_{G_Int} = 1.7 Ω
- R_{ON}=R_{OFF}= 1 Ω

The peak source and sink current in this case are:

$$I_{source_pk} = \min(10A, \frac{VDD - VEE}{R_{OH_EFF} + R_{ON} + R_{G_Int}}) \approx 5.9A$$

$$I_{sink_pk} = \min(10A, \frac{VDD - VEE}{R_{OL} + R_{OFF} + R_{G_Int}}) \approx 6.7A \quad (2)$$

Thus by using 1Ω external gate resistance, the peak source current is 5.9A, the peak sink current is 6.7A. The collector-to-emitter dV/dt during the turn on switching transient is dominated by the gate current at the miller plateau voltage. The hybrid pullup structure ensures the peak source current at the miller plateau voltage, unless the turn on gate resistor is too high. The faster the collector-to-emitter, V_{ce}, voltage rises to V_{DC}, the smaller the turn on switching loss is. The dV/dt can be estimated as Q_{gc}/I_{source_pk}. For the turn off switching transient, the drain-to-source dV/dt is dominated by the load current, unless the turn off gate resistor is too high. After V_{ce} reaches the dc bus voltage, the power semiconductor is in saturation mode and the channel current is controlled by V_{ge}. The peak sink current determines the dI/dt, which dominates the V_{ce} voltage overshoot accordingly. If using relatively large turn off gate resistance, the V_{ce} overshoot can be limited. The overshoot can be estimated by:

$$\Delta V_{ce} = L_{stray} \cdot I_{load} / ((R_{OFF} + R_{OL} + R_{G_Int}) \cdot C_{ies} \cdot \ln(V_{plat} / V_{th})) \quad (3)$$

Where

- L_{stray} is the stray inductance in power switching loop, as shown in Figure 49
- I_{load} is the load current, which is the turn off current of the power semiconductor
- C_{ies} is the input capacitance of the power semiconductor
- V_{plat} is the plateau voltage of the power semiconductor
- V_{th} is the threshold voltage of the power semiconductor

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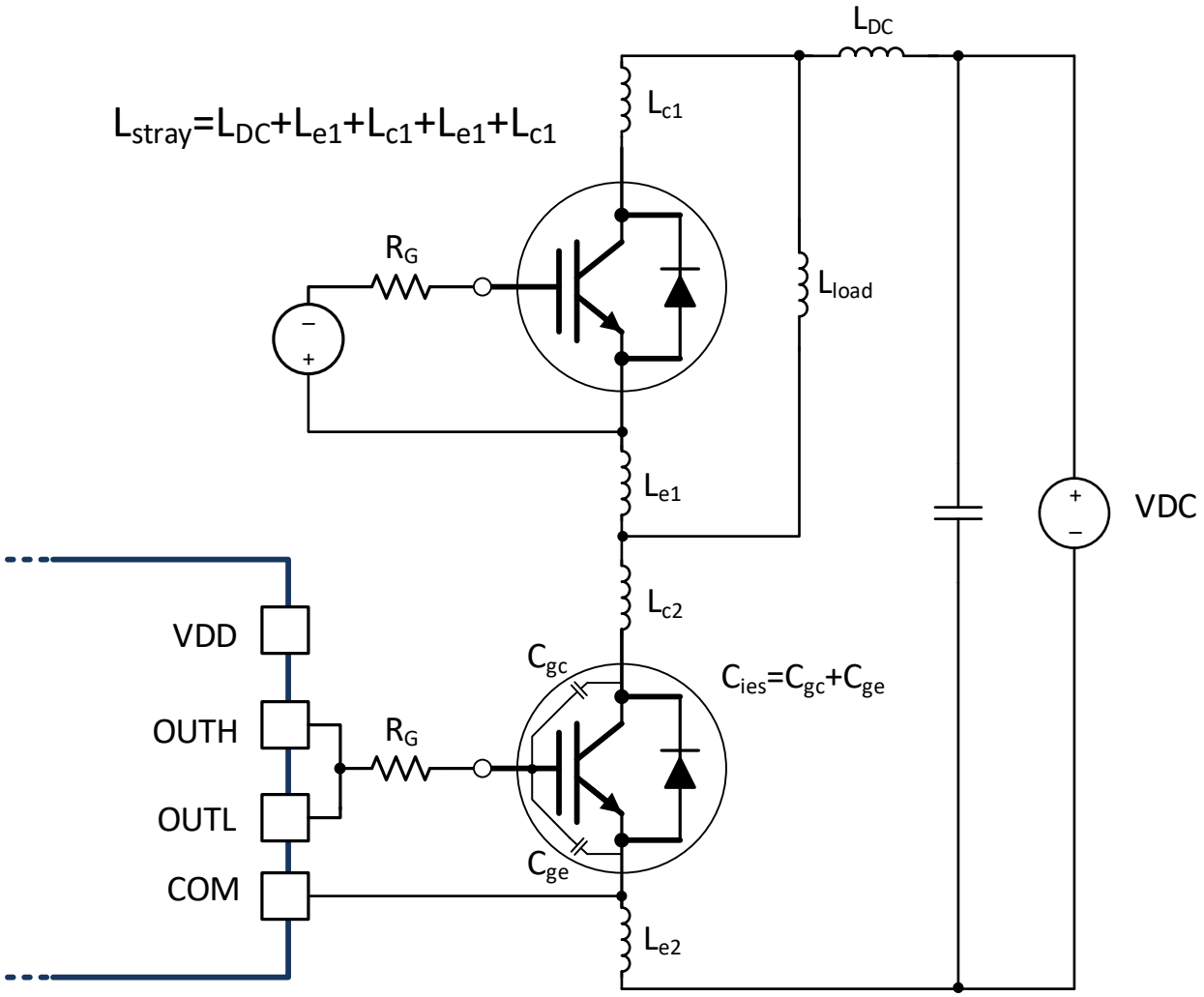


Figure 49. Stray Parasitic Inductance of IGBTs in a Half-Bridge Configuration

The power dissipation should be taken into account to maintain the gate driver within the thermal limit. The power loss of the gate driver includes the quiescent loss and the switching loss, which can be calculated as:

$$P_{DR} = P_Q + P_{SW} \tag{4}$$

P_Q is the quiescent power loss for the driver, which is I_q x (VDD-VEE) = 5mA x 20V = 0.100W. The quiescent power loss is the power consumed by the internal circuits such as the input stage, reference voltage, logic circuits, protection circuits when the driver is swithing when the driver is biased with VDD and VEE, and also the charging and discharing current of the internal circuit when the driver is switching. The power dissipation when the driver is switching can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{R_{OH_EFF}}{R_{OH_EFF} + R_{ON} + R_{G_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G_Int}} \right) \cdot (VDD - VEE) \cdot f_{sw} \cdot Q_g \tag{5}$$

Where

- Q_g is the gate charge required at the operation point to fully charge the gate voltage from VEE to VDD
- f_{sw} is the switching frequency

In this example, the P_{SW} can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{R_{OH_EFF}}{R_{OH_EFF} + R_{ON} + R_{G_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G_Int}} \right) \cdot (VDD - VEE) \cdot f_{sw} \cdot Q_g = 0.505W \tag{6}$$

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Thus, the total power loss is:

$$P_{DR} = P_Q + P_{SW} = 0.10W + 0.505W = 0.605W \quad (7)$$

When the board temperature is 125°C, the junction temperature can be estimated as:

$$T_j = T_b + \psi_{jb} \cdot P_{DR} \approx 150°C \quad (8)$$

Therefore, for the application in this example, with 125°C board temperature, the maximum switching frequency is ~50kHz to keep the gate driver in the thermal limit. By using a lower switching frequency, or increasing external gate resistance, the gate driver can be operated at a higher switching frequency.

9.2.2.6 External Active Miller Clamp

External active miller clamp feature allows the gate driver to stay at the low status when the gate voltage is detected below V_{CLMPTH}. When the other switch of the phase leg turns on, the dV/dt can cause a current through the parasitic miller capacitance of the switch and sink in the gate driver. The sinking current causes a negative voltage drop on the turn off gate resistance, and bumps up the gate voltage to cause a false turn on. The external active miller clamp features allows flexibility of board layout and active miller clamp pulldown strength. Limited by the board layout, if the driver cannot be placed close enough to the switch, external active miller clamp MOSFET can be placed close to the switch and the MOSFET can be chosen according to the peak current needed. Caution must be exercised when the driver is place far from the power semiconductor. Since the device has high peak sink and source current, the high dI/dt in the gate loop can cause a ground bounce on the board parasitics. The ground bounce can cause a positive voltage bump on CLMPE pin during the turn off transient, and results in the external active miller clamp MOSFET to turn on shortly and add extra drive strength to the sink current. To reduce the ground bounce, a 2Ω resistance is recommended to the gate of the external active clamp MOSFET.

When the V_{OUTH} is detected to be lower than V_{CLMPTH} above VEE, the CLMPE pin outputs a 5V voltage with respect to VEE, the external clamp FET is in linear region and the pulldown current is determined by the peak drain current, unless the on-resistance of the external clamp FET is large.

$$I_{CLMPE_PK} = \min(I_{D_PK}, \frac{V_{DS}}{R_{DS_ON}}) \quad (9)$$

Where

- I_{D_PK} is the peak drain current of the external clamp FET
- V_{DS} is the drain-to-source voltage of the clamp FET when the CLMPE is activated
- R_{DS_ON} is the on-resistance of the external clamp FET

The total delay time of the active miller clamp circuit from the gate voltage detection threshold V_{CLMPTH} can be calculated as t_{DCLMPE}+t_{CLMPER}. t_{CLMPER} depends on the parameter of the external active miller clamp MOSFET. As long as the total delay time is longer than the deadtime of high side and low side switches, the driver can effectively protect the switch from false turn on issue caused by miller effect.

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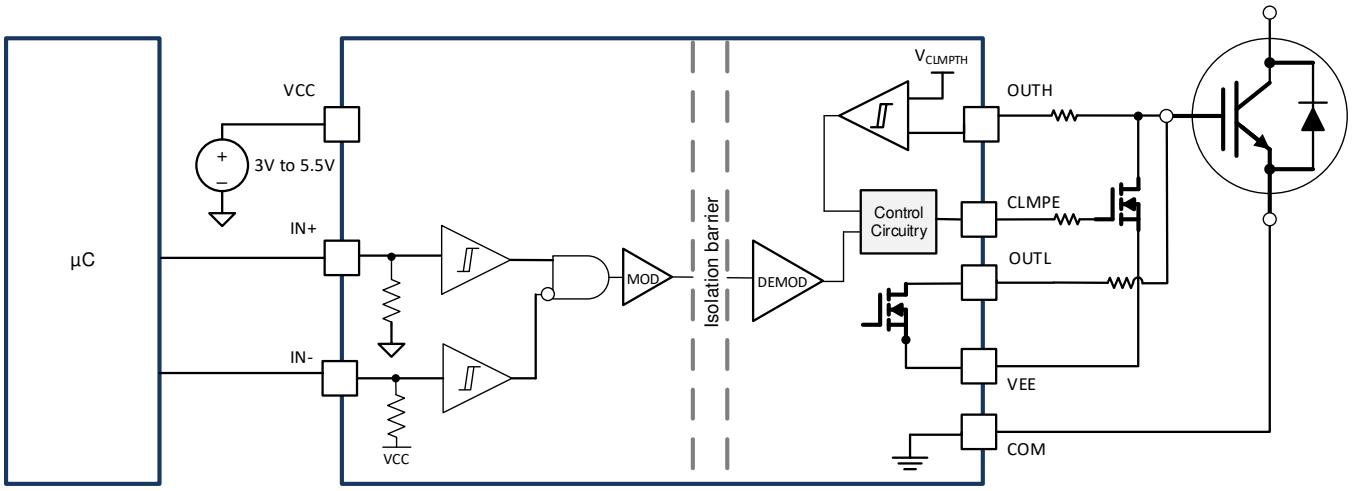


Figure 50. External Active Miller Clamp Configuration

9.2.2.7 Overcurrent and Short Circuit Protection

Fast and reliable overcurrent and short circuit protection is important to protect the catastrophic break down of the SiC MOSFET and IGBT modules, and improve the system reliability. The UCC21736-Q1 features a state-of-art overcurrent and short circuit protection, which can be applied to both SiC MOSFET and IGBT modules with various detection circuits.

9.2.2.7.1 Protection Based on Power Modules with Integrated SenseFET

The overcurrent and short circuit protection function is suitable for the SiC MOSFET and IGBT modules with integrated SenseFET. The SenseFET scales down the main power loop current and outputs the current with a dedicated pin of the power module. With external high precision sensing resistor, the scaled down current can be measured and the main power loop current can be calculated. The value of the sensing resistor R_S sets the protection threshold of the main current. For example, with a ratio of 1:N = 1:50000 of the integrated current mirror, by using the R_S as 20Ω, the threshold protection current is:

$$I_{OC_TH} = \frac{V_{OCTH}}{R_S} \cdot N = 1750A \tag{10}$$

The overcurrent and short circuit protection based on integrated SenseFET has high precision, as it is sensing the current directly. The accuracy of the method is related to two factors: the scaling down ratio of the main power loop current and the SenseFET, and the precision of the sensing resistor. Since the current is sensed from the SenseFET, which is isolated from the main power loop, and the current is scaled down significantly with much less dI/dt, the sensing loop has good noise immunity. To further improve the noise immunity, a low pass filter can be added. A 100pF to 10nF filter capacitor can be added. The delay time caused by the low pass filter should also be considered for the protection circuitry design.

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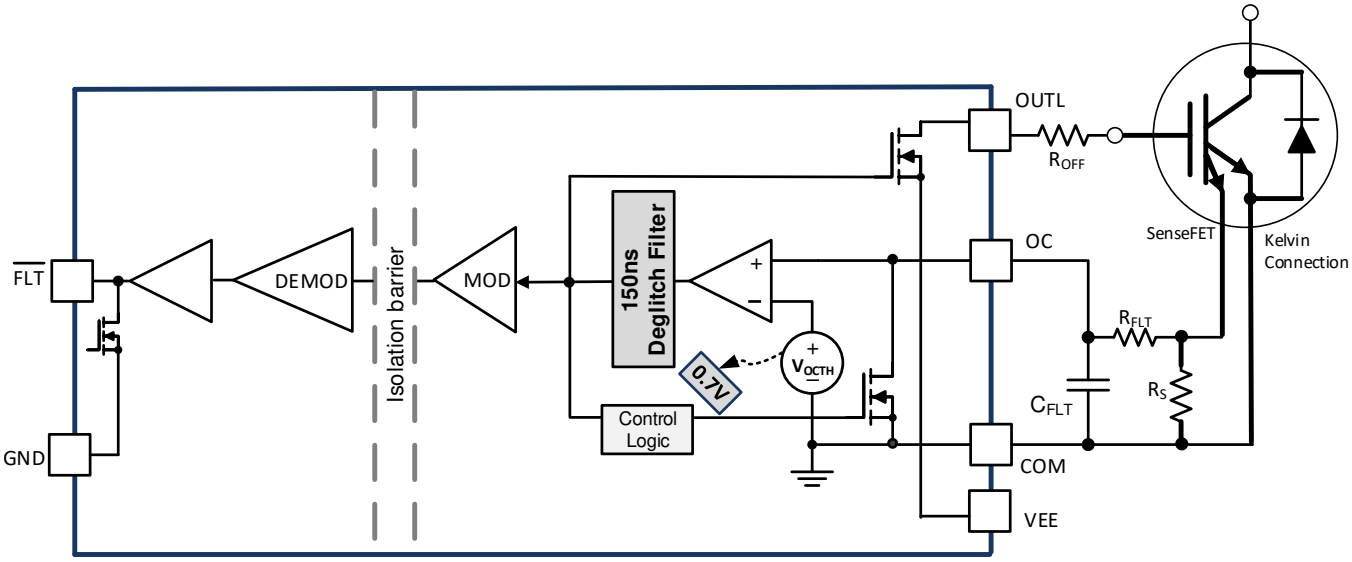


Figure 51. Overcurrent and Short Circuit Protection Based on IGBT Module with SenseFET

9.2.2.7.2 Protection Based on Desaturation Circuit

For SiC MOSFET and IGBT modules without SenseFET, desaturation (DESAT) circuit is the most popular circuit which is adopted for overcurrent and short circuit protection. The circuit consists of a current source, a resistor, a blanking capacitor and a diode. Normally the current source is provided from the gate driver, when the device turns on, a current source charges the blanking capacitor and the diode forward biased. During normal operation, the capacitor voltage is clamped by the switch V_{CE} voltage. When short circuit happens, the capacitor voltage is quickly charged to the threshold voltage which triggers the device shutdown. For the UCC21736-Q1, the OC pin does not feature an internal current source. The current source should be generated externally from the output power supply. When UCC21736-Q1 is in OFF state, the OC pin is pulled down by an internal MOSFET, which creates an offset voltage on OC pin. By choosing R1 and R2 significantly higher than the pulldown resistance of the internal MOSFET, the offset can be ignored. When UCC21736-Q1 is in ON state, the OC pin is high impedance. The current source is generated by the output power supply VDD and the external resistor divider R1, R2 and R3. The overcurrent detection threshold voltage of the IGBT is:

$$V_{DET} = V_{OCTH} \cdot \frac{R_2 + R_3}{R_3} - V_F \tag{11}$$

The blanking time of the detection circuit is:

$$t_{BLK} = -\frac{R_1 + R_2}{R_1 + R_2 + R_3} \cdot R_3 \cdot C_{BLK} \cdot \ln\left(1 - \frac{R_1 + R_2 + R_3}{R_3} \cdot \frac{V_{OCTH}}{V_{DD}}\right) \tag{12}$$

Where:

- V_{OCTH} is the detection threshold voltage of the gate driver
- R_1, R_2 and R_3 are the resistance of the voltage divider
- C_{BLK} is the blanking capacitor
- V_F is the forward voltage of the high voltage diode D_{HV}

The modified desaturation circuit has all the benefits of the conventional desaturation circuit. The circuit has negligible power loss, and is easy to implement. The detection threshold voltage of IGBT and blanking time can be programmed by external components. Different with the conventional desaturation circuit, the overcurrent detection threshold voltage of the IGBT can be modified to any voltage level, either higher or lower than the detection threshold voltage of the driver. A parallel schottky diode can be connected between OC and COM pins to prevent the negative voltage on the OC pin in noisy system. Since the desaturation circuit measures the V_{CE} of the IGBT or V_{DS} of the SiC MOSFET, not directly the current, the accuracy of the protection is not as high as the SenseFET based protection method. The current threshold cannot be accurately controlled in the protection.

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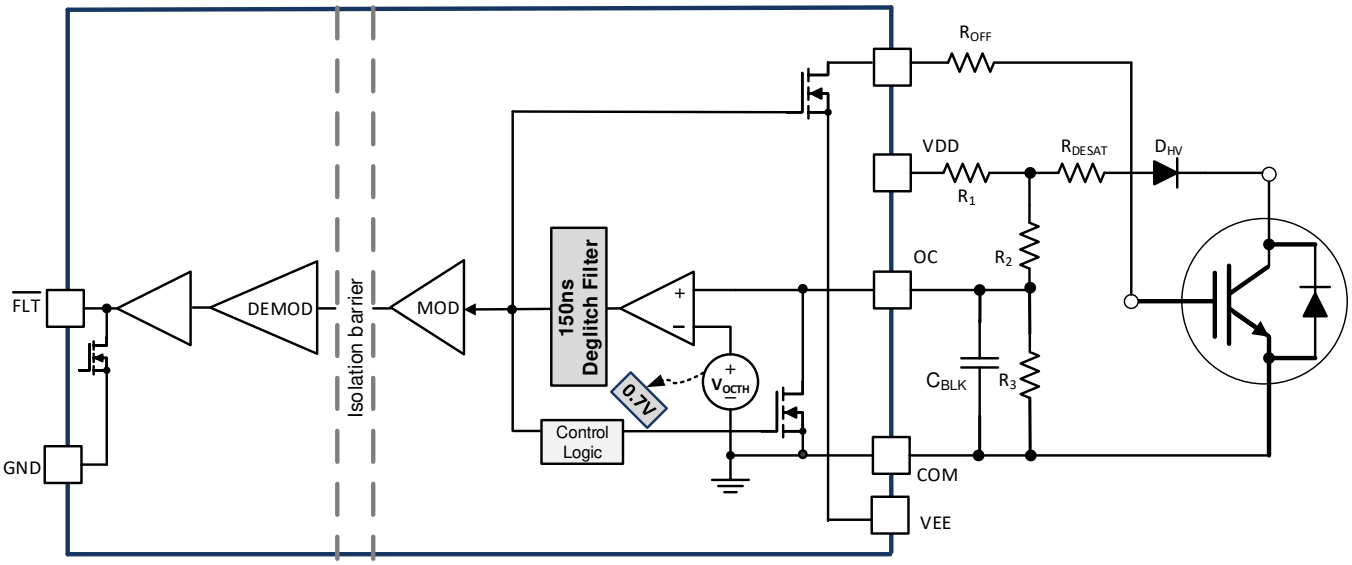


Figure 52. Overcurrent and Short Circuit Protection Based on Desaturation Circuit

9.2.2.7.3 Protection Based on Shunt Resistor in Power Loop

In lower power applications, to simplify the circuit and reduce the cost, a shunt resistor can be used in series in the power loop and measure the current directly. Since the resistor is in series in the power loop, it directly measures the current and can have high accuracy by using a high precision resistor. The resistance needs to be small to reduce the power loss, and should have large enough voltage resolution for the protection. Since the sensing resistor is also in series in the gate driver loop, the voltage drop on the sensing resistor can cause the voltage drop on the gate voltage of the IGBT or SiC MOSFET modules. The parasitic inductance of the sensing resistor and the PCB trace of the sensing loop will also cause a noise voltage source during switching transient, which makes the gate voltage oscillate. Thus, this method is not recommended for high power application, or when dI/dt is high. To use it in low power application, the shunt resistor loop should be designed to have the optimal voltage drop and minimum noise injection to the gate loop.

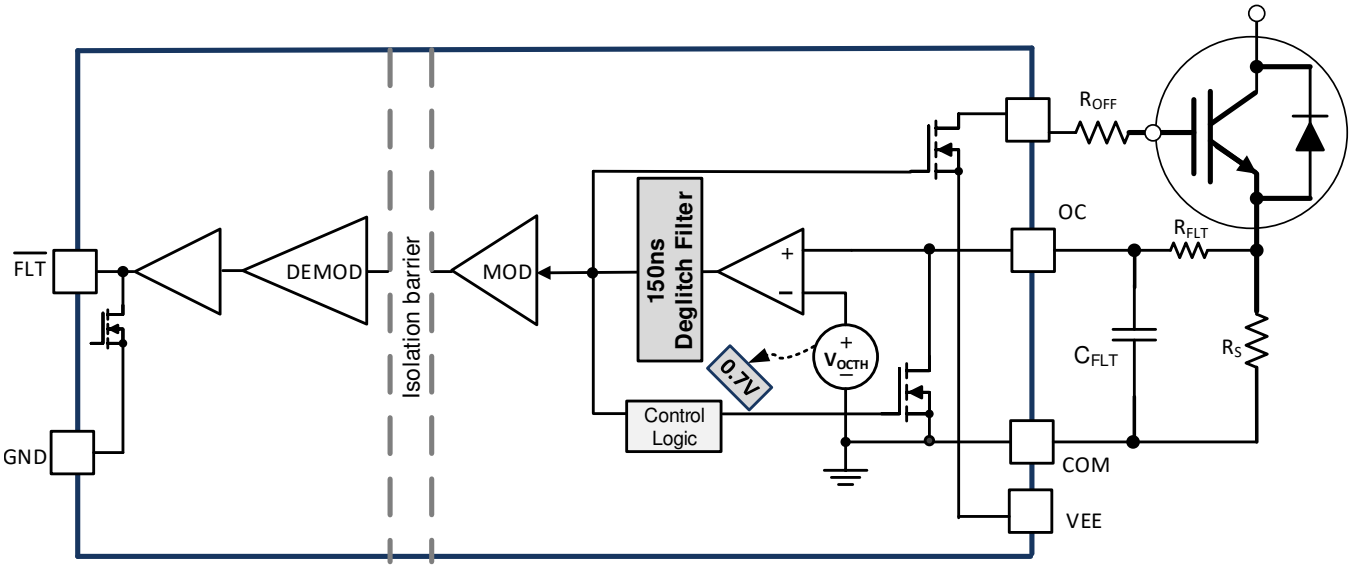


Figure 53. Overcurrent and Short Circuit Protection Based on Shunt Resistor

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9.2.2.8 Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a non-inverting current buffer (such as the NPN/PNP buffer shown in Figure 54) can be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for peak currents up to 15 A, the D44VH10/ D45VH10 pair is up to 20 A peak.

In the case of a over-current detection, the soft turn off (STO) is activated. External components must be added to implement STO instead of normal turn off speed when an external buffer is used. C_{STO} sets the timing for soft turn off and R_{STO} limits the inrush current to below the current rating of the internal FET (10A). R_{STO} should be at least (VDD-VEE)/10. The soft turn off timing is determined by the internal current source of 400mA and the capacitor C_{STO}. C_{STO} is calculated using .

$$C_{STO} = \frac{I_{STO} \cdot t_{STO}}{VDD - VEE} \tag{13}$$

- I_{STO} is the the internal STO current source, 400mA
- t_{STO} is the desired STO timing

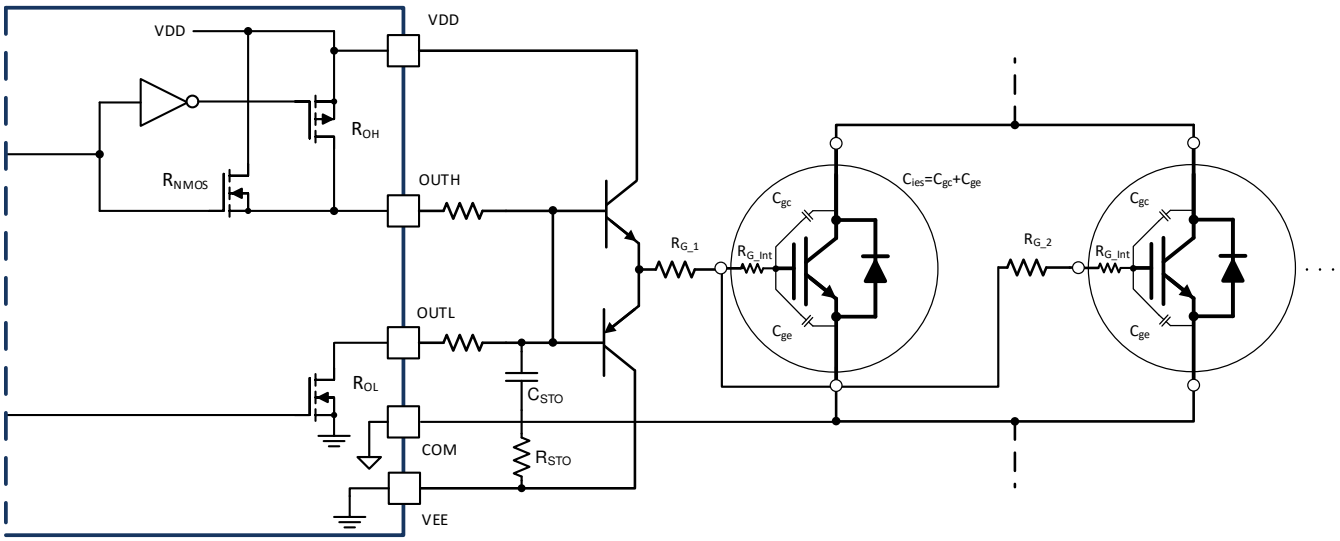


Figure 54. Current Buffer for Increased Drive Strength

10 Power Supply Recommendations

During the turn on and turn off switching transient, the peak source and sink current is provided by the VDD and VEE power supply. The large peak current is possible to drain the VDD and VEE voltage level and cause a voltage droop on the power supplies. To stabilize the power supply and ensure a reliable operation, a set of decoupling capacitors are recommended at the power supplies. Considering UCC21736-Q1 has ±10A peak drive strength and can generate high dV/dt, a 10µF bypass cap is recommended between VDD and COM, VEE and COM. A 1µF bypass cap is recommended between VCC and GND due to less current comparing with output side power supplies. A 0.1µF decoupling cap is also recommended for each power supply to filter out high frequency noise. The decoupling capacitors must be low ESR and ESL to avoid high frequency noise, and should be placed as close as possible to the VCC, VDD and VEE pins to prevent noise coupling from the system parasitics of PCB layout.

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11 Layout

11.1 Layout Guidelines

Due to the strong drive strength of UCC21736-Q1, careful considerations must be taken in PCB design. Below are some key points:

- The driver should be placed as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces
- The decoupling capacitors of the input and output power supplies should be placed as close as possible to the power supply pins. The peak current generated at each switching transient can cause high dI/dt and voltage spike on the parasitic inductance of PCB traces
- The driver COM pin should be connected to the Kelvin connection of SiC MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, the COM pin should be connected as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop
- Use a ground plane on the input side to shield the input signals. The input signals can be distorted by the high frequency noise generated by the output side switching transients. The ground plane provides a low-inductance filter for the return current flow
- If the gate driver is used for the low side switch which the COM pin connected to the dc bus negative, use the ground plane on the output side to shield the output signals from the noise generated by the switch node; if the gate driver is used for the high side switch, which the COM pin is connected to the switch node, ground plane is not recommended
- If ground plane is not used on the output side, separate the return path of the OC and AIN ground loop from the gate loop ground which has large peak source and sink current
- No PCB trace or copper is allowed under the gate driver. A PCB cutout is recommended to avoid any noise coupling between the input and output side which can contaminate the isolation barrier

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11.2 Layout Example

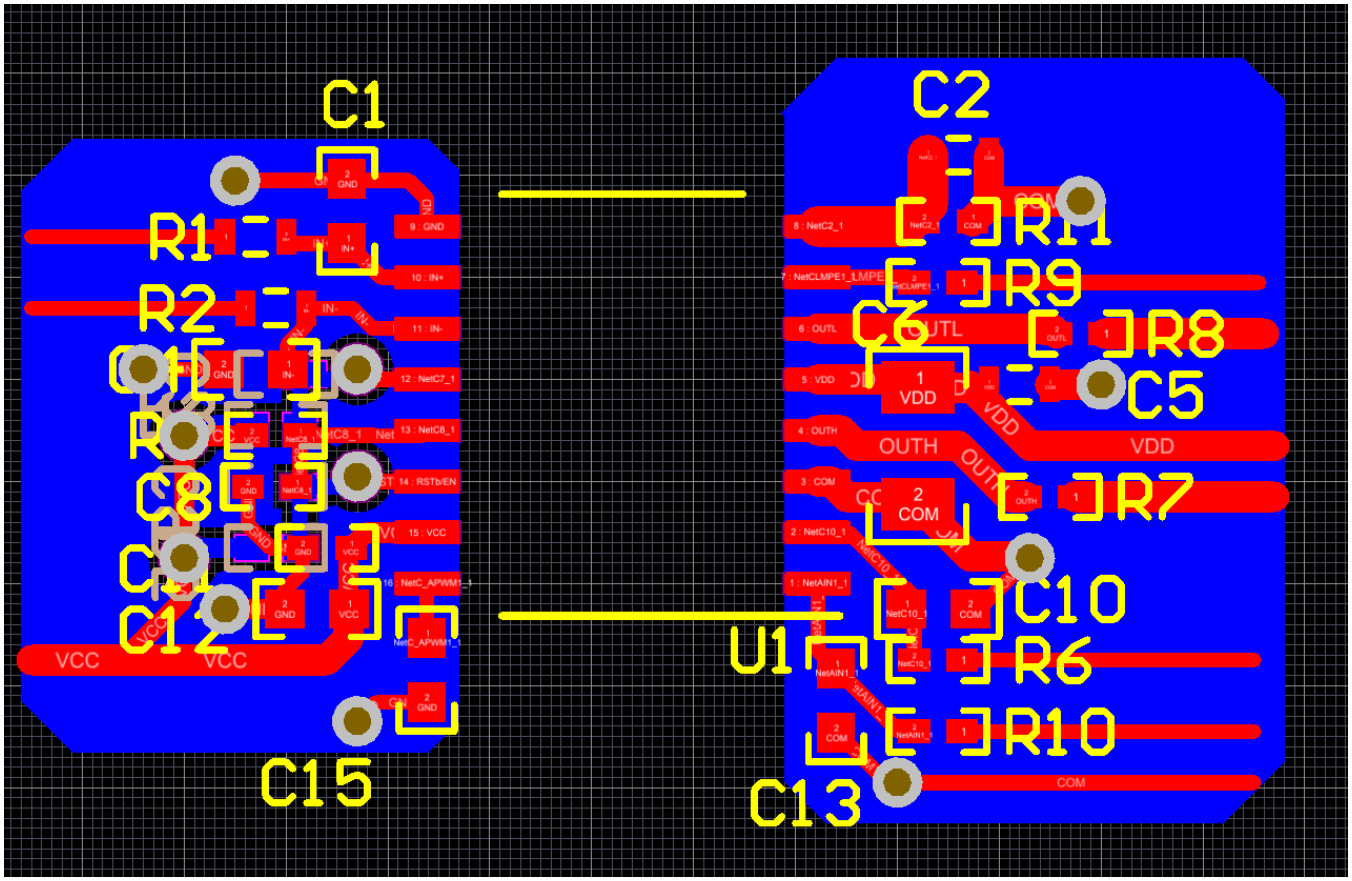


Figure 55. Layout Example

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Isolation Glossary*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resource

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

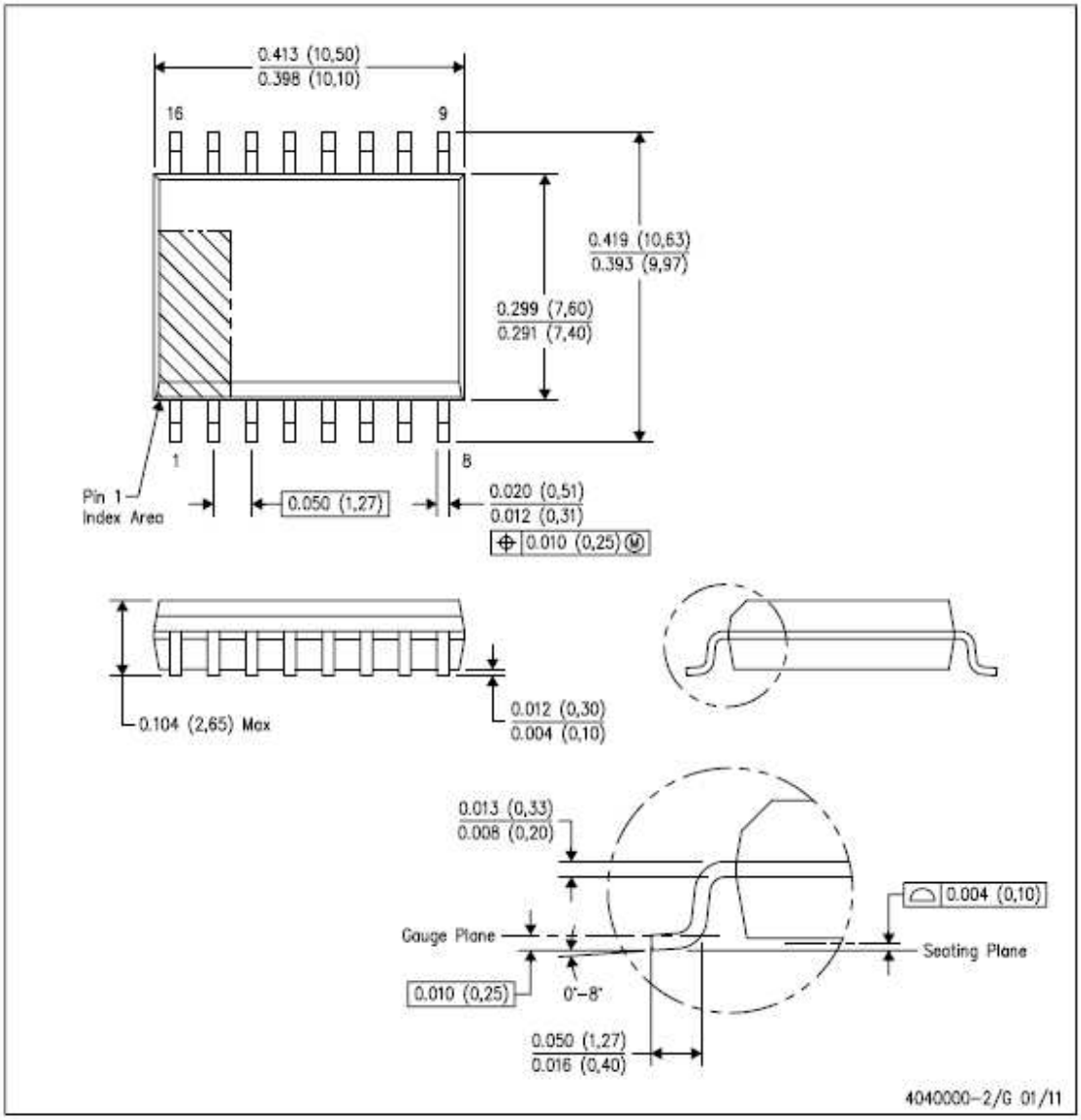
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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MECHANICAL DATA

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUCC21736QDWQ1	ACTIVE	SOIC	DW	16	40	TBD	Call TI	Call TI	-40 to 125		Samples
PUCC21736QDWRQ1	ACTIVE	SOIC	DW	16	2000	TBD	Call TI	Call TI	-40 to 125		Samples
UCC21736QDWQ1	PREVIEW	SOIC	DW	16	40	TBD	Call TI	Call TI	-40 to 125		
UCC21736QDWRQ1	PREVIEW	SOIC	DW	16	2000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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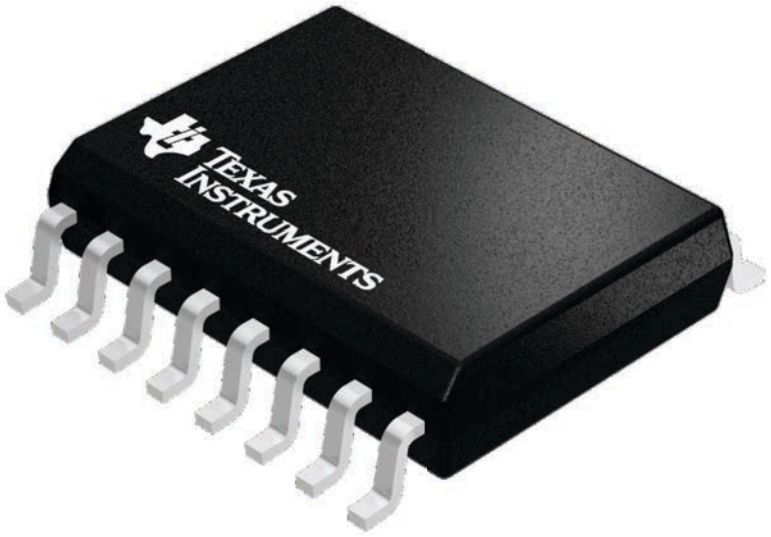
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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