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March 2016

FPF2595

IntelliMAX™ 28 V, Over-Voltage, Over-Current Protection Load Switch with Adjustable Current-Limit Control

Features

- V_{IN}: 2.5 V~5.5 V
- 28 V Absolute Ratings at V_{OUT}
- Current Capability: 3.9 A
  - Typ 0.1 A~3.5 A with 10% Accuracy
- R_{ON}: Typ. 35 mΩ & Max. 50 mΩ at 5 V_{IN} and 1 A I_{OUT}
- Output OVP: Min.=5.6 V, Typ.=5.8 V, Max.=6 V
- No Output Discharge During Off State
- Open-Drain OCP on FLAGB
- Thermal Shutdown
- Under-Voltage Lockout (UVLO)
- True Reverse-Current Blocking (TRCB)
- Logic CMOS IO Meets JESD76 Standard for GPIO Interface and Related Power Supply Requirements
- ESD Protected:
  - Human Body Model: >2 kV
  - Charged Device Model: >1.0 kV
  - IEC 61000-4-2 Air Discharge: >15 kV
  - IEC 61000-4-2 Contact Discharge: >8 kV

Applications

- Type C Power Source Switch
- Computing, Monitor
- Portable Devices

Description

The FPF2595 advanced load-management switch targets applications requiring a highly integrated solution. It disconnects loads powered from the DC power rail (<6 V) with stringent off-state current targets and high load capacitances (<100 µF). The FPF2595 consists of a slew-rate controlled low-impedance MOSFET switch (35 mΩ typical) and integrated analog features. The slew-rate controlled turn-on characteristic prevents inrush current and the resulting excessive voltage droop on power rails. FPF2595 has over-voltage protection and over-temperature protection.

The FPF2595 has a True Reverse-Current Blocking (TRCB) function that obstructs unwanted reverse current from V_{OUT} to V_{IN} during ON and OFF states. The exceptionally low off-state current drain (<2 µA maximum) facilitates compliance with standby power requirements. The input voltage range operates from 2.5 V to 5.5 V_{DC} to support a wide range of applications in consumer, optical, medical, storage, portable, and industrial-device power management. Switch control is managed by a logic input (active HIGH) capable of interfacing directly with low-voltage control signal / General-Purpose Input / Output (GPIO) without an external pull-down resistor.

The device is packaged in advanced, fully “green” compliant, 1.3 mm x 1.8 mm, Wafer-Level Chip-Scale Packages (WLCSP).

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method	Top Mark
FPF2595UCX	-40 to 85°C	12-Ball, WLCSP, 3x4 Array, 0.4 mm Pitch, 250 µm Ball, Wafer-Level Chip-Scale Package (WLCSP)	Tape & Reel	TY

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Application Diagram

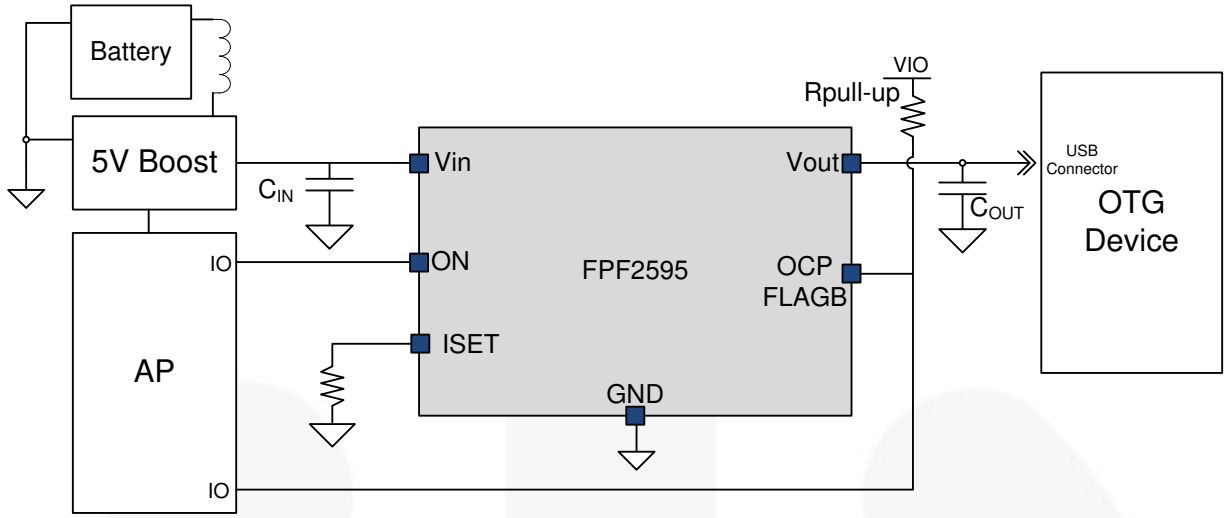


Figure 1. Typical Application

Note:

1. C_{IN} and C_{OUT} capacitors recommended for improvement of device stability.

Functional Block Diagram

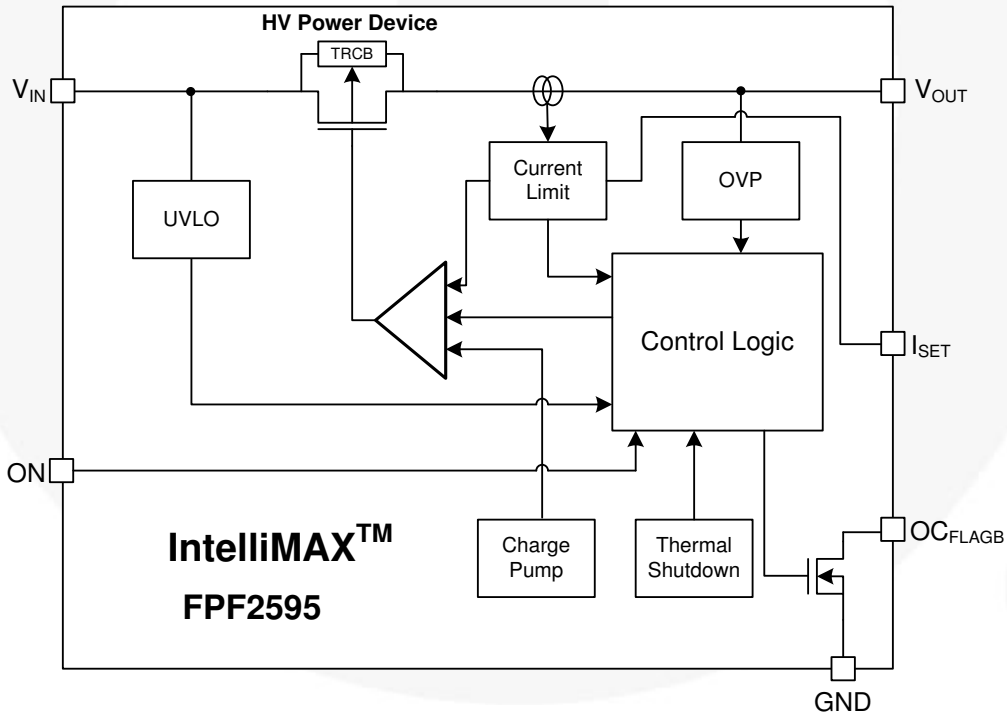


Figure 2. Functional Block Diagram

Pin Configurations

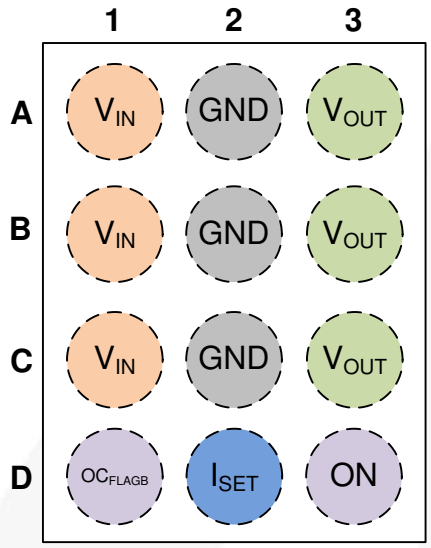


Figure 3. Pin Assignments (Top View)

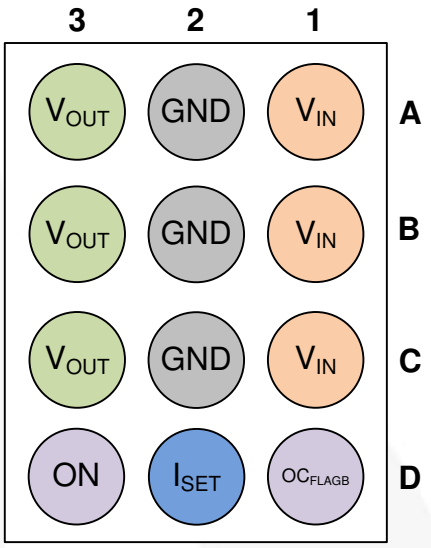


Figure 4. Pin Assignments (Bottom View)

Pin Description

Pin #	Name	Description		
A3, B3, C3	V_{OUT}	**Switch Output**		
A1, B1, C1	V_{IN}	**Supply Input**: Input to the power switch		
A2, B2, C2	GND	**Ground** (True device ground)		
D3	ON	**ON/OFF Control Input**: Active HIGH - GPIO compatible	**Logic HIGH**	Switch Enable
			Logic LOW	Switch Disable
D1	OC_{FLAGB}	**Fault Output**: Active LOW, open-drain output that indicates an input over current. External pull-up resistor to V_{CC} is required.		
D2	I_{SET}	**Current Limit Set Input**: A resistor from ISET to ground sets the current limit for the switch.		

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters		Min.	Max.	Unit
V_{PIN}	V_{OUT} to GND, V_{OUT} to V_{IN}		-0.3	28.0	V
	ON, V_{IN}, FLAGB, I_{SET} to GND		-0.3	6.0	
I_{SW}	Maximum Continuous Switch Current[2]			3.9	A
t_{PD}	Total Power Dissipation at T_A=25°C			1.48	W
T_J	Operating Junction Temperature		-40	+150	°C
T_{STG}	Storage Junction Temperature		-65	+150	°C
Θ_{JA}	Thermal Resistance, Junction-to-Ambient (1-inch Square Pad of 2 oz. Copper)			84.1[3]	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	2.0		kV
		Charged Device Model, JESD22-C101	1.0		
	IEC61000-4-2 System Level	Air Discharge (V_{IN}, V_{ON}, V_{OUT} to GND)	15.0		
		Contact Discharge (V_{IN}, V_{ON}, V_{OUT} to GND)	8.0		

Notes:

2. Maximum Junction Temperature = 85°C.
3. Measured using 2S2P JEDEC std. PCB.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameters	Min.	Max.	Unit
V_{IN}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature	-40	85	°C

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Electrical Characteristics

Unless otherwise noted; V_{IN}=2.5 to 5.5 V, T_A=-40 to +85°C; typical values are at V_{IN}=5 V and T_A=25°C.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Unit
Basic Operation						
V_{IN}	Input Voltage		2.5		5.5	V
$I_{Q(OFF)}$	Off Supply Current	V_{ON}=GND, V_{OUT}=Open		1	2	µA
$I_{SD(OFF)}$	Shutdown Current	V_{IN}=5.5 V, V_{OUT}=0 V, V_{ON}=GND		0.1	4.0	µA
I_Q	Quiescent Current	I_{OUT}=0 mA		65	100	µA
R_{ON}	On Resistance	V_{IN}=5.0 V, I_{OUT}=1 A		35	50	mΩ
		V_{IN}=3.7 V, I_{OUT}=1 A		40	55	
V_{IH}	ON Input Logic HIGH Voltage	V_{IN}=2.5 V to 5.5 V	1.15			V
V_{IL}	ON Input Logic LOW Voltage	V_{IN}=2.5 V to 5.5 V			0.65	V
V_{IL_FLAG}	FLAGB Output Logic LOW Voltage	V_{IN}=5 V, I_{SINK}=10 mA		0.1	0.2	V
		V_{IN}=2.5 V, I_{SINK}=10 mA		0.15	0.30	
I_{FLAGB_LK}	FLAGB Output HIGH Leakage Current	V_{IN}=5 V, Switch On			1	µA
I_{ON}	On Input Leakage	V_{ON}=0 V to V_{IN}			1.0	µA
R_{ON_PD}	Pull-Down Resistance at ON Pin	V_{IN}=2.5~5.5 V, V_{ON}=HIGH, T_A=-40 to 85°C		14		MΩ
Over-Voltage Protection						
V_{OV_TRIP}	Output OVP Lockout	V_{OUT} Rising Threshold	5.50	5.80	6.00	V
		V_{OUT} Falling Threshold		5.50		
OUT_{HYS}	Output OVP Hysteresis	V_{OUT} Falling Threshold		0.3		V
t_{OVP}	OVP Response Time[5]	I_{OUT}=0.5 A, C_L=1 µF, T_A=25°C, V_{OUT} from 5.5 V to 6.0 V	1		4	µs
Over-Current Protection						
I_{LIM}	Current Limit[4]	V_{IN}=5 V, R_{SET}=2300 Ω, V_{OUT}=1.68 to 5 V	450	500	550	mA
		V_{IN}=5 V, R_{SET}=1070 Ω, V_{OUT}=1.68 to 5 V	900	1000	1100	
V_{UVLO}	Under-Voltage Lockout	V_{IN} Increasing		2.4		V
		V_{IN} Decreasing		2.2		
V_{UVLO_HYS}	UVLO Hysteresis			200		mV
V_{T_RCB}	RCB Protection Trip Point	V_{OUT} - V_{IN}		50		mV
V_{R_RCB}	RCB Protection Release Trip Point	V_{IN} - V_{OUT}		50		mV

Continued on the following page…

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Electrical Characteristics (Continued)

Unless otherwise noted; V_{IN}=2.5 to 5.5 V, T_A=-40 to +85°C; typical values are at V_{IN}=5 V and T_A=25°C.

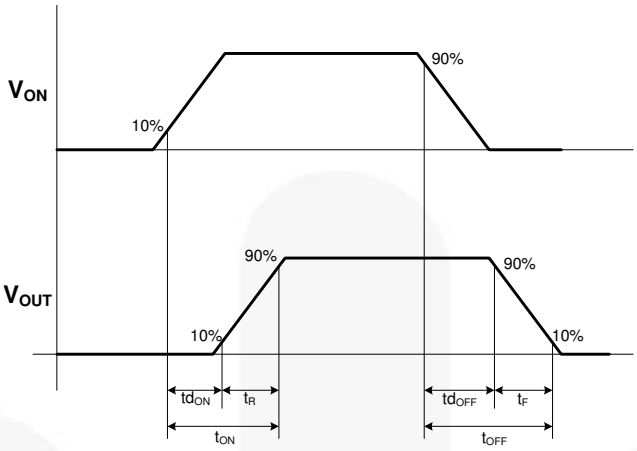
Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
V_{RCB_HYS}	RCB Hysteresis			100		mV
t_{RCB}	Default RCB Response Time	V_{IN}=5 V, V_{ON}=High/Low		2		µs
I_{RCB}	RCB Current	V_{ON}=0 V, V_{OUT}=5.5 V,		7		µA
t_{HOCP}	Hard Over-Current Response Time	Moderate Over-Current Condition, $I_{OUT} \geq I_{LIM}$, V_{OUT}=0 V		6		µs
t_{OCP}	Over-Current Response Time	Moderate Over-Current Condition, $I_{OUT} \geq I_{LIM}$ $V_{OUT} \leq V_{IN}$		7		µs
t_{OC_FLAG}	Over-Current Flag Response Time	When Over-Current Occurs to Flag Pulling LOW		8		ms
TSD	Thermal Shutdown(5)	Shutdown Threshold		150		°C
		Return from Shutdown		130		
		Hysteresis		20		
Dynamic Characteristics						
t_{DON}	Turn-On Delay(5,6)	V_{IN}=5 V, R_L=100 Ω, C_L=1 µF, T_A=25°C, R_{SET}=2040 Ω		0.69		ms
t_R	V_{OUT} Rise Time(5,6)			0.77		ms
t_{ON}	Turn-On Time(5,7)			1.46		ms
t_{DOFF}	Turn-Off Delay(5,6)			10		µs
t_F	V_{OUT} Fall Time(5,6)			220		µs
t_{OFF}	Turn-Off Time(5,8)			230		µs

Notes:

4. Characterization based on 1% tolerance resistor.
5. This parameter is guaranteed by design and characterization; not production tested.
6. t_{DON}/t_{DOFF}/t_R/t_F are defined in Figure 5 below.
7. t_{ON}=t_R + t_{DON}.
8. t_{OFF}=t_F + t_{DOFF}.

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Timing Diagram



where:

t_{DON} = Delay On Time
t_R = V_{OUT} Rise Time
t_{ON} = Turn-On Time
t_{DOFF} = Delay Off Time
t_F = V_{OUT} Fall Time
t_{OFF} = Turn Off Time

Figure 5. Timing Diagram

Operation and Application Description

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into discharge load capacitor; a capacitor must be placed in between the V_{IN} and GND pins. A high-value capacitor on C_{IN} can be used to reduce the voltage drop in high-current applications.

Output Capacitor

An output capacitor should be placed between the V_{OUT} and GND pins. This capacitor prevents parasitic board inductance from forcing V_{OUT} below GND when the switch is on. This capacitor also prevents reverse inrush current from creating a voltage spike that could damage the device in the case of a V_{OUT} short.

Fault Reporting

Upon the detection of an over-current, OC_FLAGB signal the fault by activating LOW.

Current Limiting

The current limit ensures that the current through the switch does not exceed the maximum set value, while not limiting the minimum value. The current at which the part's limit is adjustable through the selection of the external resistor connected to the ISET pin. Information for selecting the resistor is found in the section below. The device acts as a constant-current source when the load draws more than the maximum value set by the device until thermal shutdown occurs. The device recovers if the die temperature drops below the threshold temperature.

Under-Voltage Lockout (UVLO)

The under-voltage lockout turns the switch off if the input voltage drops below the lockout threshold. With the ON pin active, the input voltage rising above the UVLO threshold releases the lockout and enables the switch.

True Reverse-Current Blocking

The true reverse-current blocking feature protects the input source against current flow from output to input regardless of whether the load switch is on or off.

Thermal Shutdown

The thermal shutdown protects the die from internally or externally generated excessive temperature. During an over-temperature condition, the switch is turned off. The switch automatically turns on again if the temperature of the die drops below the threshold temperature.

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Setting Current Limit

The current limit is set with an external resistor connected between the I_{SET} and GND pins. The resistor is selected using Table 1. Resistor tolerance of 1% or less is recommended.

Table 1. Current Limit Settings by R_{SET}[9]

$R_{SET}\Omega$	Min. Current Limit (mA)	Typ. Current Limit (mA)	Max. Current Limit (mA)
290	3150	3500	3850
315	2925	3250	3575
340	2700	3000	3300
375	2475	2750	3025
415	2250	2500	2750
460	2025	2250	2475
520	1800	2000	2200
600	1570	1750	1920
700	1350	1500	1650
850	1125	1250	1375
1070	900	1000	1100
1200	810	900	990
1350	720	800	880
1550	630	700	770
1850	540	600	660
2300	450	500	550
2500	405	450	495
2800	360	400	440
3200	315	350	385
3800	270	300	330
4600	225	250	275
5900	180	200	220
7800	135	150	165
11900	90	100	110

Note:
9. Table values based on 1% tolerance resistor.

Current limit threshold equation (I_{LIM}):

$$R_{SET}(\Omega) = \left(\frac{798439\ mV}{I_{SET}\ mA}\right)^{1.044}$$

Or:

$$I_{SET}\ (mA) = \frac{798439\ mV}{{R_{SET}}^{0.956}\ \Omega} \quad (1)$$

If current limit is not used it is OK for the ISET pin to be connected with GND, but the maximum current must be less than the maximum current capability of 3.9 A.

Board Layout

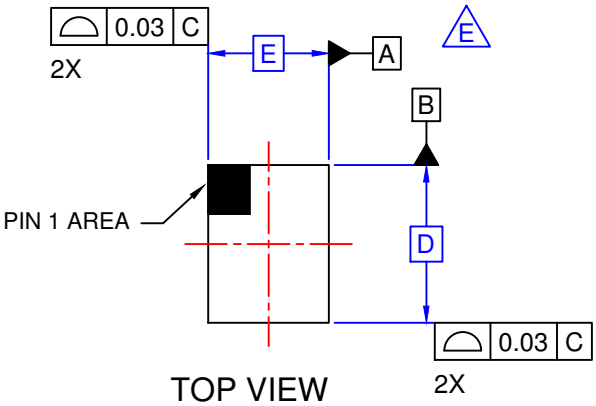
For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effect that parasitic trace inductance may have on normal and short-circuit operation. Using wide traces for VIN, VOUT, GND helps minimize parasitic electrical effects along with minimizing the case-to-ambient thermal impedance.

The table below pertains to the Marketing outline drawing on the following page.

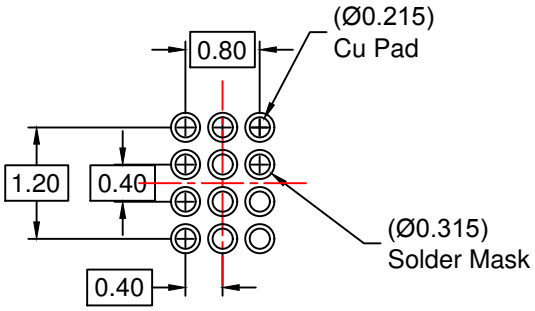
Product-Specific Dimensions

Parts	D	E	X	Y
FPF2595UCX	1800 µm ±30 µm	1300 µm ±30 µm	250 µm	300 µm

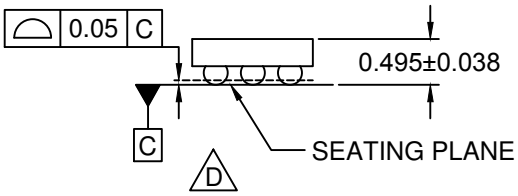
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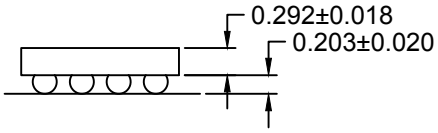


TOP VIEW

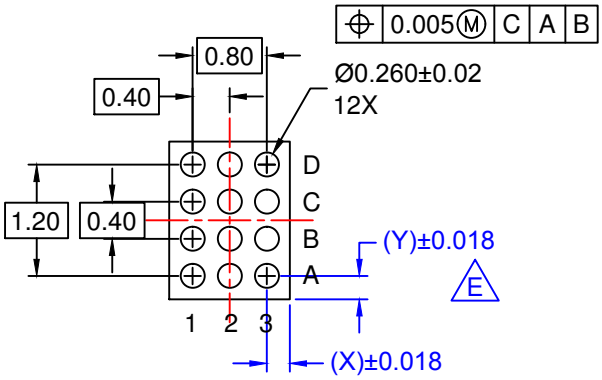


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
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F. DRAWING FILENAME: MKT-UC012AJrev1.

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