

AT24C01A/02N/04N/08AN/16AN

Pin Capacitance

Applicable over recommended operating range from $T_A = 25$ $f = 1.0$ MHz, $V_{CC} = +1.8V$.

Parameter	Symbol	Testconditions	Max	Unit
Input/Output Capacitance (SDA)	$C_{I/O}$	$V_{I/O} = 0V$	8	pF
Input Capacitance (A_0, A_1, A_2, SCL)	C_{IN}	$V_{IN} = 0V$	6	pF

DC Characteristics

Applicable over recommended operating range from :

$T_A = -40$ to $+85$, $V_{CC} = +1.8V$ to $+5.5V$ (unless otherwise noted).

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC1}		1.8		5.5	V
Supply Voltage	V_{CC2}		2.7		5.5	V
Supply Voltage	V_{CC3}		4.5		5.5	V
Supply Current $V_{CC} = 5.0V$	I_{CC}	READ at 100 kHz		0.4	1.0	mA
Supply Current $V_{CC} = 5.0V$	I_{CC}	WRITE at 100 kHz		2.0	3.0	mA
Standby Current $V_{CC} = 1.8V$	I_{SB1}	$V_{IN} = V_{CC}$ or V_{SS}		0.6	3.0	μA
Standby Current $V_{CC} = 2.5V$	I_{SB2}	$V_{IN} = V_{CC}$ or V_{SS}		1.4	4.0	μA
Standby Current $V_{CC} = 2.7V$	I_{SB3}	$V_{IN} = V_{CC}$ or V_{SS}		1.6	4.0	μA
Standby Current $V_{CC} = 5.0V$	I_{SB4}	$V_{IN} = V_{CC}$ or V_{SS}		8.0	18.0	μA
Input Leakage Current	I_{LI}	$V_{IN} = V_{CC}$ or V_{SS}		0.10	3.0	μA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{CC}$ or V_{SS}		0.05	3.0	μA
Input Low Level*1	V_{IL}		-0.6		$V_{CC} \times 0.3$	V
Input High Level*1	V_{IH}		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
Output Low Level $V_{CC} = 3.0V$	V_{OL2}	$I_{OL} = 2.1$ mA			0.4	V
Output Low Level $V_{CC} = 1.8V$	V_{OL1}	$I_{OL} = 0.15$ mA			0.2	V

*1. V_{IL} min and V_{IH} max are reference only and are not tested.

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AC Characteristics

Applicable over recommended operating range from $T_{AI} = -40$ to $+85$, $V_{CC} = +1.8V$ to $+5.5V$, $V_{CC} = +2.7V$ to $+5.5V$,

$C_L = 1$ TTL Gate and 100 pF (unless otherwise noted)

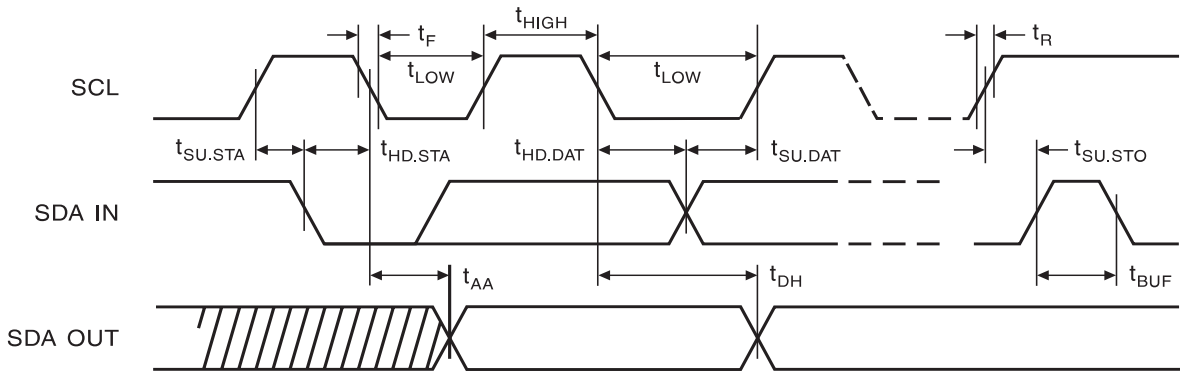
Parameter	Symbol	1.8-V		2.7, 5.0-V		Units
		Min	Max	Min	Max	
Clock Frequency, SCL	fSCL		100		400	kHz
Clock Pulse Width Low	tLOW	4.7		1.2		μ s
Clock Pulse Width High	tHIGH	4.0		0.6		μ s
Noise Suppression Time*1	tI		100		50	ns
Clock Low to Data Out Valid	tAA	0.1	4.5	0.1	0.9	μ s
Time the bus must be free before a new transmission can start*1	tBUF	4.7		1.2		μ s
Start Hold Time	tHD.STA	4.0		0.6		μ s
Start Setup Time	tSU.STA	4.7		0.6		μ s
Data In Hold Time	tHD.DAT	0		0		μ s
Data In Setup Time	tSU.DAT	200		100		ns
Inputs Rise Time*1	tR		1.0		0.3	μ s
Inputs Fall Time*1	tF		300		300	ns
Stop Setup Time	tSU.STO	4.7		0.6		μ s
Data Out Hold Time	tDH	100		50		ns
Write Cycle Time	tWR		5		5	ms
5.0V, 25°, Byte Mode	Endurance*1	1M		1M		Write Cycles

*1. This parameter is characterized.

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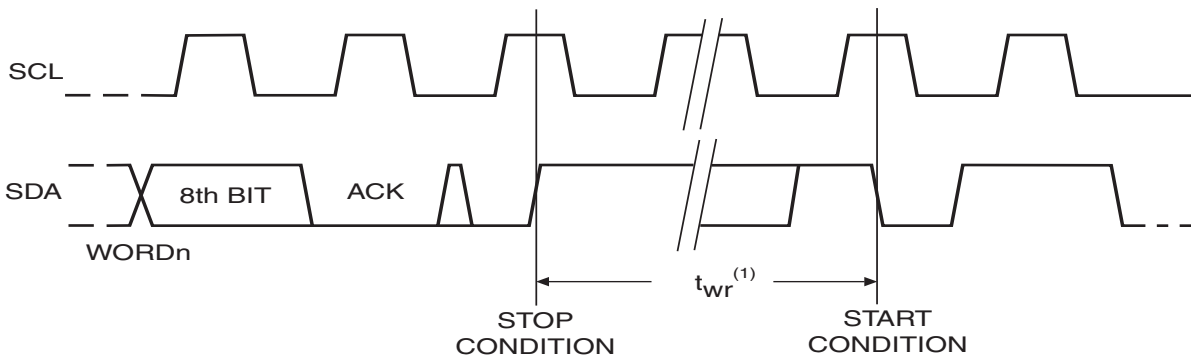
Bus Timing

Figure 1. SCL: Serial Clock, SDA: Serial Data I/O



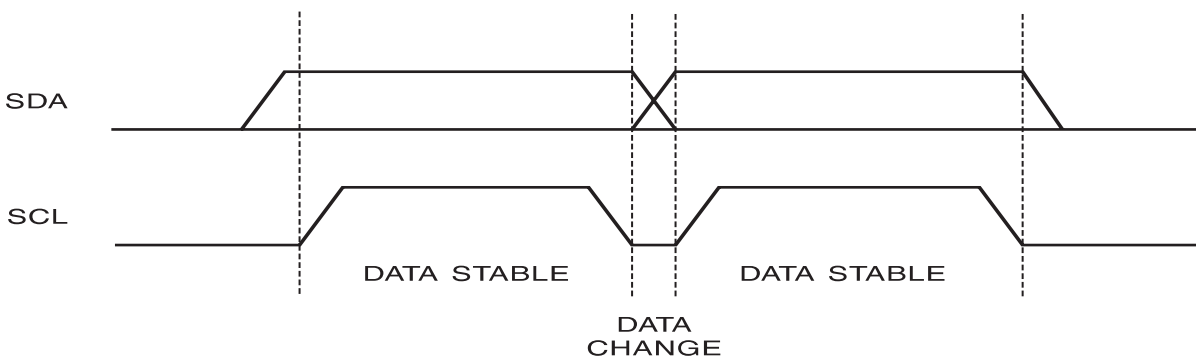
Write Cycle Timing

Figure 2. SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 3. Data Validity



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Figure 4. Start and Stop Definition

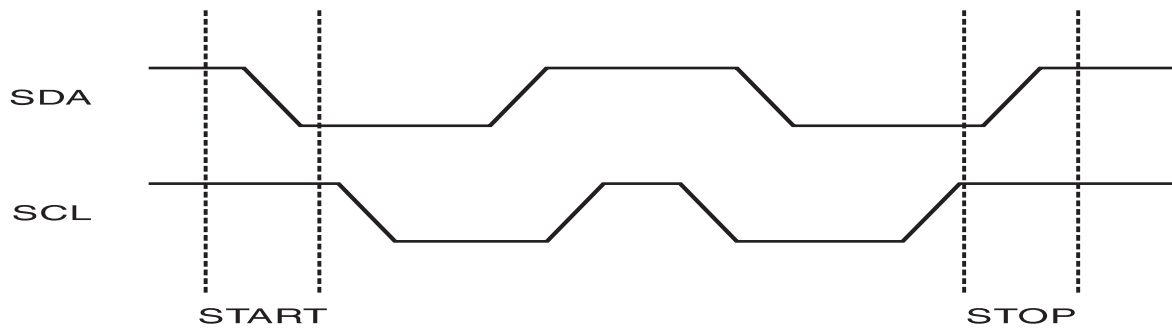


Figure 5. Output Acknowledge

