MITSUBISHI INTEGRATED CIRCUIT

M64080GP

410MHz 2SYSTEM 1CHIP PLL FREQUENCY SYNTHESIZER

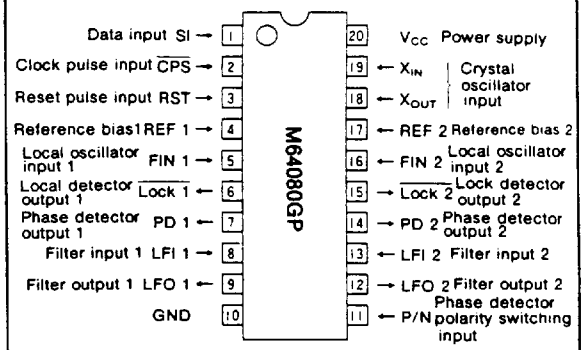
DESCRIPTION

The M64080GP is a 410MHz band 2 system 1 chip PLL frequency synthesizer. With two built-in PLL systems, it is ideal for cordless phones and dual band transceivers.
Two modulus prescalers of 1/128 and 1/129 are built-in to allow direct input of up to 410MHz.

FEATURES

- Two built-in PLLs
- 1/128 and 1/129 prescalers (fmax=410MHz)
- Wide range of operating voltage (V_{CC}=1.8V to 3.3V)
- Low current consumption
  When the two PLLs are operating : I_{CC}=8mA at V_{CC}=2V
  When one is not operating : I_{CC}=5mA at V_{CC}=2V
  When both are not operating : I_{CC}=0.3mA at V_{CC}=2V
- Divider for reference frequency is also programmable.
  Setting range of dividing ratio N(f_{REF})=128 to 16,382)
  (Can be set in multiples of 2)
- Programmable divider for local oscillator
  Setting range of dividing ratio N (V. C. O)=16,384~131,071 (Can be set in integral multiples.)
- Serial data input system (3 data transmission lines)
- PLL lock/unlock status indication function
- Two PLLs can be turned on/off independently with data from controller.
- Two transistor circuits for LPF.

PIN CONFIGURATION (TOP VIEW)

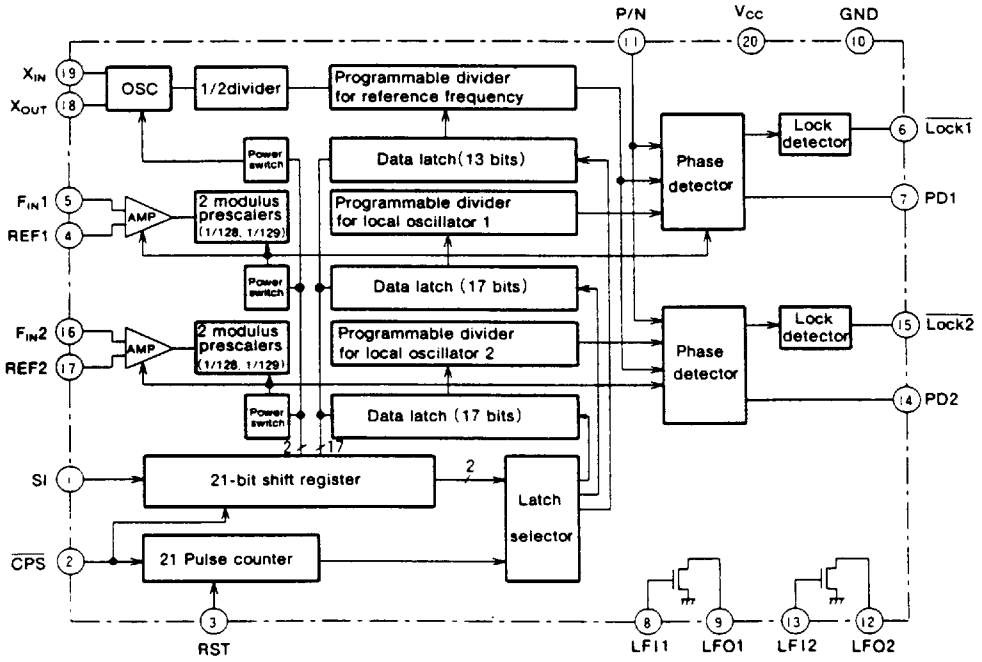


Outline 20P2E-A (20SSOP)

APPLICATION

Cordless phone, wireless phone, etc.

BLOCK DIAGRAM



http://www.chipdocs.com

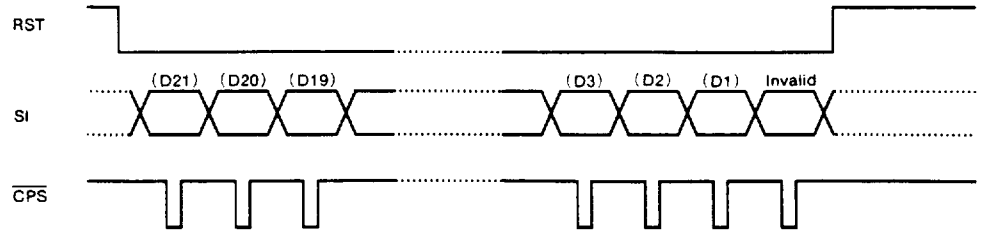
PIN DESCRIPTION

Pin no.	Symbol	Pin name	Description
1	SI	Data input	Shift register data input pin
2	$\overline{CPS}$	Clock pulse input	Shift register clock pulse input pin
3	RST	Reset pulse input	21 pulse counter reset pulse input pin
4	REF 1	Reference bias 1	Grounded with 1000pF capacitor
5	F_{IN} 1	Local oscillator input 1	Local oscillator frequency (V. C. O) input Fmax=410MHz
6	$\overline{Lock\ 1}$	Lock detector output 1	When PLL system is locked : "L" When it is unlocked : "H" PLL 1 power is off : "H" (open drain type)
7	PD 1	Phase detector output 1	Tristate output High Z when PLL 1 power is off
8	LFI 1	Filter input 1	Gate input for LPF transistor
9	LFO 1	Filter output 1	Transistor drain output (open drain type) for LPF
10	GND	Ground	0V
11	P/N	Phase detector polarity switch input	When this pin is "H", PD pin becomes "H" for phase lead and "L" for phase lag. When this pin is "L", PD pin becomes "L" for phase lead and "H" for phase lag.
12	LFO 2	Filter output 2	Transistor drain output (open drain type) for LPF
13	LFI 2	Filter input 2	Transistor gate input for LPF
14	PD 2	Phase detector output	Tristate output High Z when PLL 2 power is off
15	$\overline{Lock\ 2}$	Lock detector output 2	When PLL system is locked : "L" When it is unlocked : "H" PLL 2 power is off : "H" (open drain type)
16	F_{IN} 2	Local oscillator input 2	Local oscillator frequency (V. C. O) input Fmax=410MHz
17	REF 2	Reference dias 2	Grounded with 1000pF capacitor
18	X_{OUT}	Crystal oscillator input	Output from 12.8MHz to 21.25MHz reference oscillator is input to X_{IN}. Oscillator by external crystal resonator is available.
19	X_{IN}		
20	V_{CC}	Power supply pin	1.8V~3.3V

http://www.chipdocs.com

FUNCTION DESCRIPTION

1. Data input

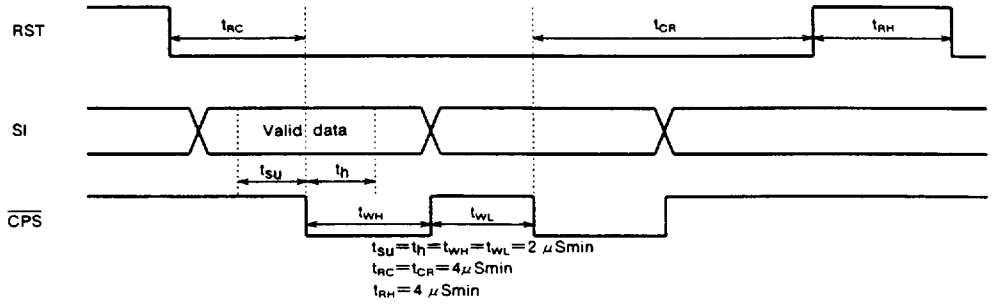


Note1 : SI input status is read into the shift register in sequence at the trailing edge of $\overline{CPS}$ input.

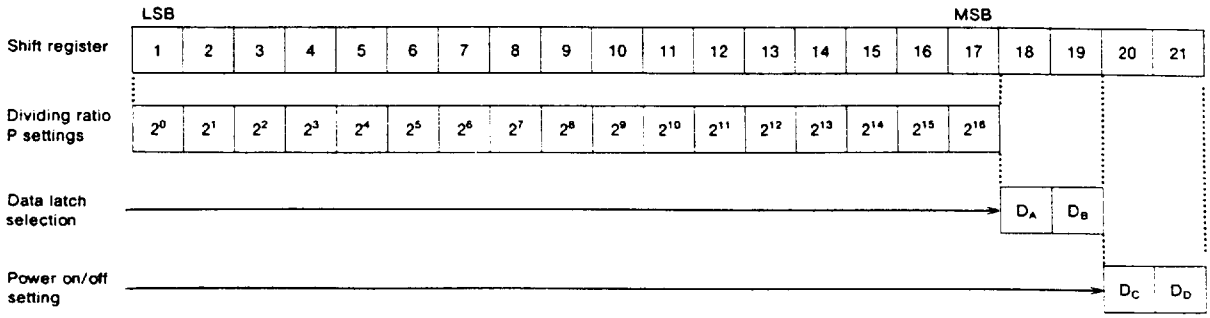
2 : All the data (power on/off, latch selector, N value) is set at the trailing edge of the 21st pulse, and subsequent $\overline{CPS}$ is invalid

3 : Neither $\overline{CPS}$ nor SI is accepted while RST is at "H".

2. Input Signal Timing



3. Bit Configuration of Shift Register



Note4 : Dividing ratio P of the programmable divider is given as 17 bit binary code.

Total dividing ratio of reference frequency N (f_{REF}) is :

N (f_{REF}) =2xP, where P =64~8191

Total dividing ratio of local oscillator frequency N (V C O) is :

N (V.C.O) =P, Where P =16384~131071

Note5 : Data latch to be updated is selected by DA and DB

Data		Description
D_A	D_B	
L	L	This is for test mode. Do not use
H	L	Data of latch for local oscillator 1 is updated
L	H	Data of latch for local oscillator 2 is updated
H	H	Data of latch for reference frequency is updated

Note6 : Power on/off of PLL system is set by DC and DD.

Data		Description
D_C	D_D	
L	L	Both local oscillator 1 and local oscillator 2 are on
H	L	Only local oscillator 1 is on.
L	H	Only local oscillator 2 is on.
H	H	Both oscillators are off.

http://www.chipdocs.com

4. Data Coding Example

(1) Set reference frequency to 12.5kHz and local oscillator 1 and 2 to off.

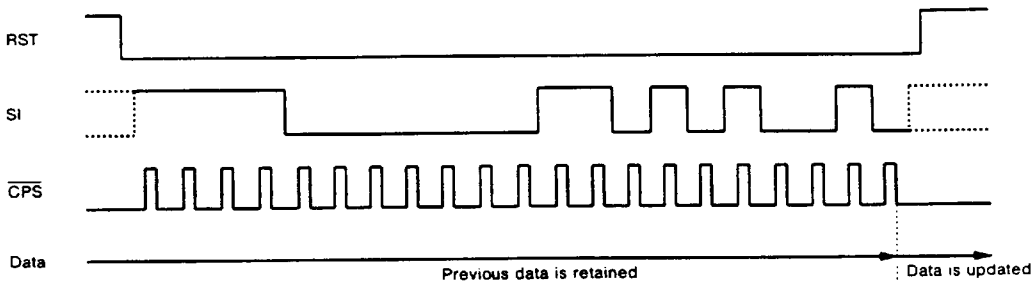
	LSB																MSB				
Shift register	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
Data	L	H	L	L	H	L	H	L	H	H	L	L	L	×	×	×	×	H	H	H	H

Set dividing ratio p of programmable divider*
$P=2^1+2^4+2^6+2^8+2^9=850$

Select updating of data of latch for reference frequency

Set local oscillator 1 and local oscillator 2 to off.

* : The setting of the dividing ratio P of programmable divider for reference frequency is different from previous series (M54958, M64070, M64072) because a swallow counter is used.



Note7 : Total dividing ratio of reference frequency N (f_{REF}) is set at : N (f_{REF}) $=2\times P=2\times 850=1700$
When 21.25 MHz crystal oscillator is used, $f_{REF}=21.25/1700=12.5kHz$

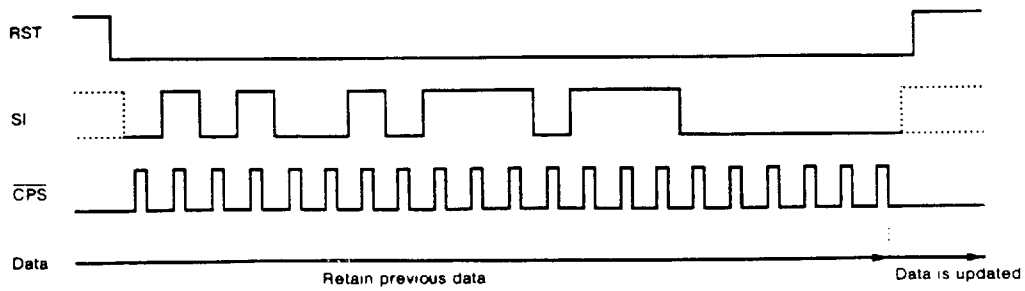
(2) Set dividing ratio of local osillator 1 to 24,000 and turn on only local oscillator 1

	LSB																			MSB
Shift register	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
Data	L	L	L	L	L	L	H	H	H	L	H	H	H	L	H	L	L	H	L	H	L

Setting dividing ratio P of programmable divider
$P=2^6+2^7+2^8+2^{10}+2^{11}+2^{12}+2^{14}=24,000$

Select update of data of latch for local oscillator 1

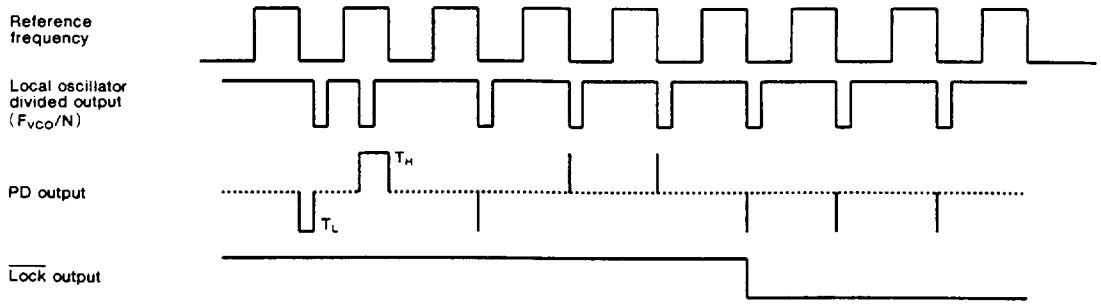
Turn on power of local oscillator 1 only



Note8 : If PLL is locked when the reference frequency is set to 12.5 kHz,
f_{VCO} 1 $=12.5\times 24,000=300,000kHz=300MHz$

http://www.chipdocs.com

5. PD, $\overline{\text{Lock}}$ Signal Detection



Note9 : PD output becomes "L"when the phase of local oscillator divided output (F_{VCO}/N) is behind that of reference frequency (f_{REF}) and "H" when it is faster.

10 : ·····indicates high impedance status.

11 : $\overline{\text{Lock}}$ output becomes"L" when the phase differences TL and TH are kept below 625nS** for more than three cycles of reference frequency (f_{REF}).

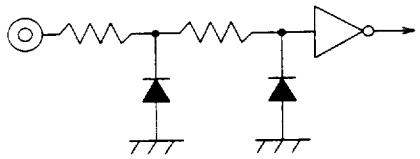
* : The above explanation is the case when P/N input (11pin) is at "H".
When P/N input is at "L", polarity of PD output is reversed.

** : It is the case when 12.8MHz oscillator is used for reference oscillator frequency.

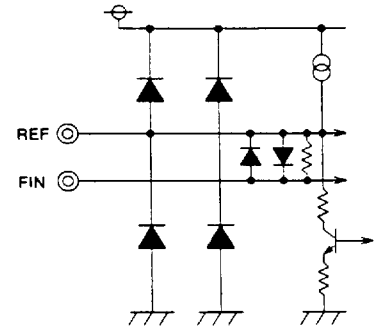
http://www.chipdocs.com

INPUT/OUTPUT CIRCULT DIAGRAM

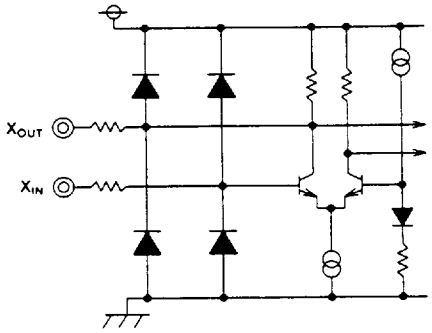
1 Each input SI, $\overline{CPS}$, RST, and P/N



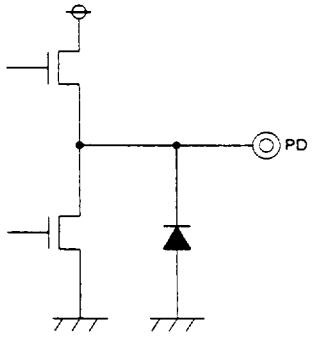
2 Prescaler input



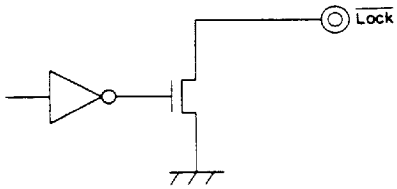
3 OSC input



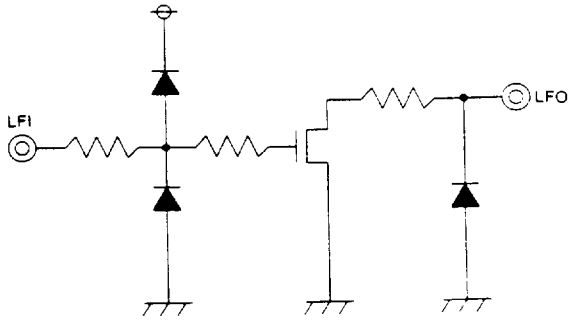
4 PD output



5 $\overline{Lock}$ output



6 Transistor for LPF



http://www.chipdocs.com

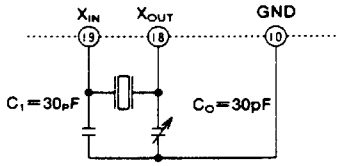
ABSOLUTE MAXIMUM RATINGS (T_a=−20 to 75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings		Unit	Remarks
			Min.	Max.		
V_{CC}	Supply voltage	GND=0 V	−0.3	6.0	V	
V_I	Input voltage	SI, $\overline{CPS}$, RST, GND=0 V	−0.3	6.0	V	
V_O	Output voltage	Each output, GND=0 V	−0.3	6.0	V	
P_d	Power dissipation	T_a=75℃		260	mW	Allowable dissipation of package
Vopd	Open drain voltage	GND=0 V	−0.3	6.0	V	
Topr	Operating temperature		−20	75	℃	
Tstg	Storage temperature		−40	125	℃	

RECOMMENDED OPERATING CONDITIONS (T_a=−20 to 75℃, unless otherwise noted)

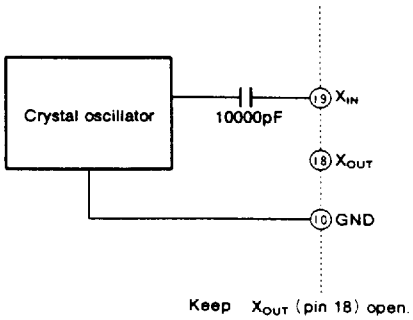
Symbol	Parameter	Conditions	Limits			Unit	Remarks
			Min.	Typ.	Max.		
V_{CC}	Supply voltage	F_{IN}=200~410MHz	1.8		3.3	V	
V_{IN}	Input amplitude	F_{IN}=200~410MHz	−16		−4	dBm	
F_{IN}	Input frequency	V_{CC}=1.8~3.3V	200		410	MHz	
I_{OL}	Low-level output current	Each output of $\overline{Lock1}$, $\overline{Lock2}$, LFO1, and LFO2.			1	mA	
V_{XIN}	X_{IN} input amplitude	V_{CC}=1.8~3.3V F_{OSC}=10~25MHz sine wave	0.4		1.4	V_{P-P}	
f_{OSC}	Reference oscillator frequency	V_{CC}=1.8~3.3V V_{XIN}=0.4~1.4V_{P-P}	10		25	MHz	

1. Crystal Resonator Connection



X'tal load capacitance 20pF or less
Effective resistance 100Ω or less

2. Crystal Oscillator Connection



Keep X_{OUT} (pin 18) open.

http://www.chipdocs.com

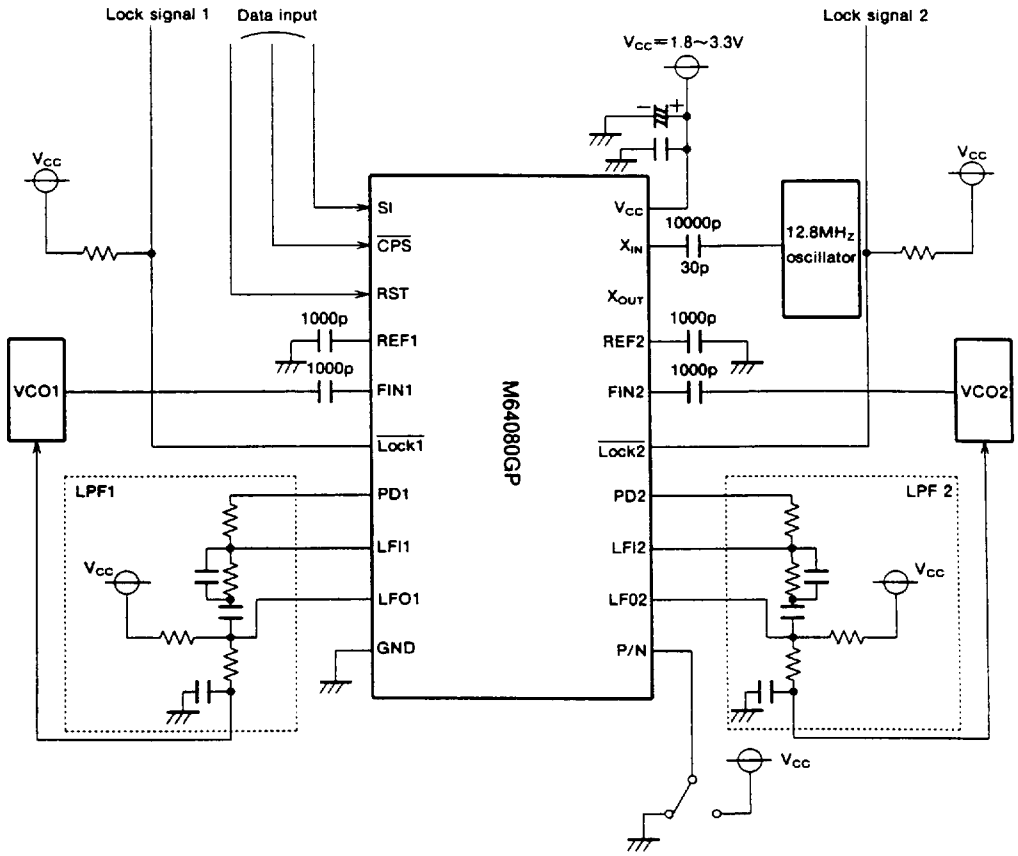
ELECTRICAL CHARACTERISTICS (T_a=−20 to 75℃, unless otherwise noted)

Symbol	Parameter	Pin	condition	Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	High-level input voltage	SI, $\overline{CPS}$, RST, P/N	V_{CC}=1.8~3.3V	0.7×V_{CC}		5.5	V
V_{IL}	Low-level input voltage	SI, $\overline{CPS}$, RST, P/N	V_{CC}=1.8~3.3V	−0.3		0.6	V
I_{IH}	High-level input current	SI, $\overline{CPS}$, RST, P/N	V_{CC}=3.3V V_{IH}=5.5V			2	μA
I_{IL}	Low-level input current	SI, $\overline{CPS}$, RST P/N	V_{CC}=3.3V V_{IL}=0V		−30	2	μA
V_{OL}	Low-level output voltage	$\overline{Lock1}$, $\overline{Lock2}$,	V_{CC}=1.8~3.3V I_O=0mA			0.2	V
V_{OHP1}	PD high-level output voltage	PD1, PD2,	V_{CC}=3.3V I_{OH}=−1mA	2.5			V
V_{OHP2}		PD1, PD2,	V_{CC}=1.8V I_{OH}=−0.1mA	1.5			V
V_{OLP1}	PD low-level output voltage	PD1, PD2,	V_{CC}=3.3V I_{OL}=1mA			0.8	V
V_{OLP2}		PD1, PD2,	V_{CC}=1.8V I_{OL}=0.1mA			0.5	V
I_{PD1}	PD leak current	PD1, PD2,	V_{CC}=3.3V V_O=0~V_{CC}			±0.5	μA
I_{PD2}		PD1, PD2,	V_{CC}=3.3V V_O=1.5V			±100	nA
I_{CC1}	Supply current	V_{CC}	V_{CC}=1.8V	5.0	7.5	13.0	mA
I_{CC2}		V_{CC}	V_{CC}=3.3V	6.0	9.0	13.0	mA
I_{OLK}	Output leak current	$\overline{Lock1}$, $\overline{Lock2}$, LFO1, LFO2	V_{CC}=3.3V, V_{OH}=3.3V LFI1=0V, LFI2=0V			±1.0	μA

Notes : GND pin (pin10) is the reference (0V) for all the voltages.
: Current flowing into the circuit is positive (no symbol) and flowing out is negative (-symbol), and maximum and minimum values are indicated in absolute values.
: Typical value is measured at T_a=25℃.

http://www.chipdocs.com

APPLICATION EXAMPLE



HANDLING PRECAUTIONS

This IC contains fine structure components to achieve high performance. Therefore, take extra precaution to protect the IC from surge voltage caused by static electricity.

http://www.chipdocs.com

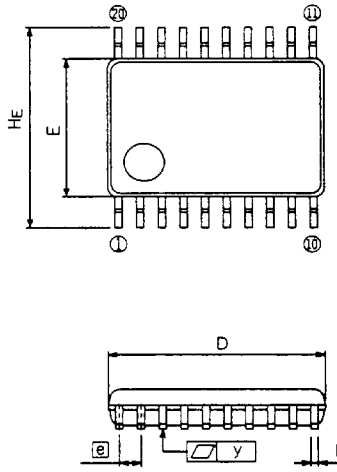
PACKAGE OUTLINE

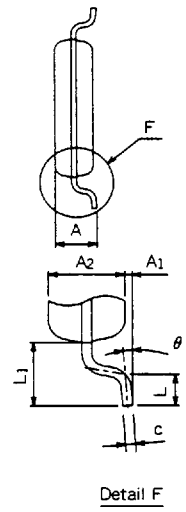
20P2E−A

Plastic 20pin 225mil SSOP

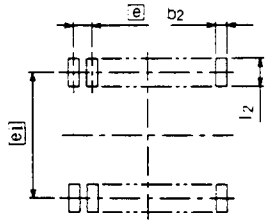
EIAJ Package Code	JEDEC Code	Weight(g)
SSOP020-P-0225	–	0.08

Scale : 4.5/1





Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.45
A_1	0	0.1	0.2
A_2	–	1.15	–
b	0.17	0.22	0.32
c	0.13	0.15	0.2
D	6.4	6.5	6.6
E	4.3	4.4	4.5
e	–	0.65	–
H_E	6.2	6.4	6.6
L	0.3	0.5	0.7
L_1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.35	–
e_1	–	5.8	–
l_2	–	1.0	–

http://www.chipdocs.com