Negative 48V Hot Swap Controller

FEATURES

- **Allows Safe Board Insertion and Removal from a Live –48V Backplane**
- **Circuit Breaker Immunity to Voltage Steps and Current Spikes**
- **Programmable Inrush and Short-Circuit Current Limits**
- Pin Compatible With LT1640L/LT1640H
- Operates from –18V to –80V
- Programmable Overvoltage Protection
- Programmable Undervoltage Lockout
- Power Good Control Output
- Bell-Core Compatible $\overline{ON}$/OFF Threshold

APPLICATIONS

- Central Office Switching
- –48V Distributed Power Systems
- Negative Power Supply Control

DESCRIPTION

The LT®4250L/LT4250H are 8-pin, negative 48V Hot Swap™ controllers that allow a board to be safely inserted and removed from a live backplane. Inrush current is limited to a programmable value by controlling the gate voltage of an external N-channel pass transistor. The pass transistor is turned off if the input voltage is less than the programmable undervoltage threshold or greater than the overvoltage threshold. A programmable current limit protects the system against shorts. After a 500µs timeout the current limit activates the electronic circuit breaker. The $\overline{PWRGD}$ (LT4250L) or PWRGD (LT4250H) signal can be used to directly enable a power module. The LT4250L is designed for modules with a low enable input and the LT4250H for modules with a high enable input.

The LT4250L/LT4250H are available in 8-pin PDIP and SO packages

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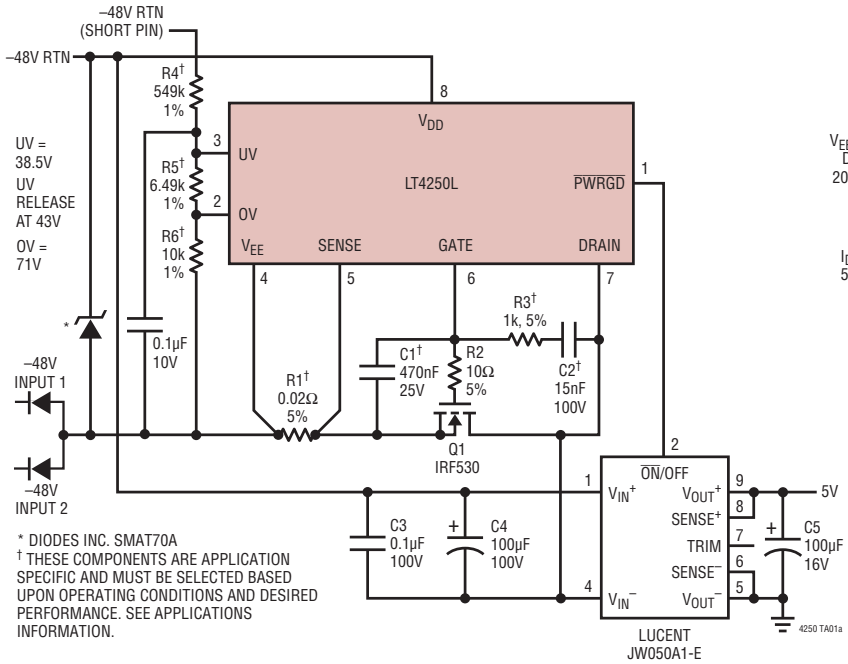
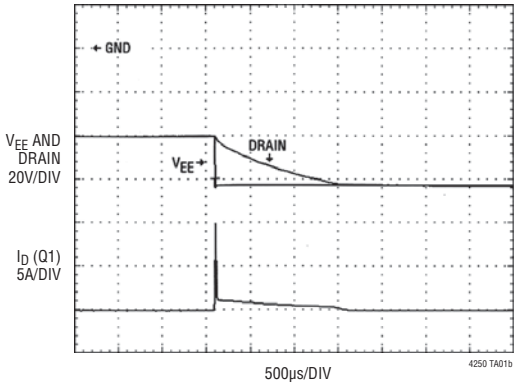
TYPICAL APPLICATION



* DIODES INC. SMAT70A
† THESE COMPONENTS ARE APPLICATION SPECIFIC AND MUST BE SELECTED BASED UPON OPERATING CONDITIONS AND DESIRED PERFORMANCE. SEE APPLICATIONS INFORMATION.

Voltage Step on Input Supply



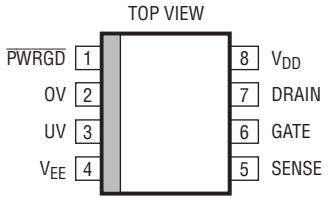
ABSOLUTE MAXIMUM RATINGS

(Note 1), All Voltages Referred to V_{EE}

Supply Voltage (V_{DD} – V_{EE}) ..... –0.3V to 100V
$\overline{PWRGD}$, PWRGD Pins ..... –0.3V to 100V
SENSE, GATE Pins ..... –0.3V to 20V
UV, OV Pins ..... –0.3V to 60V
DRAIN Pin ..... –2V to 100V
Maximum Junction Temperature ..... 125°C

Operating Temperature Range
LT4250LC/LT4250HC ..... 0°C to 70°C
LT4250LI/LT4250HI ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

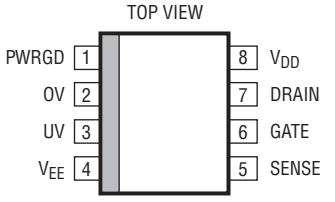
PIN CONFIGURATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 120°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 150°C/W (S8)



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 120°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 150°C/W (S8)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4250LCN8#PBF	LT4250LCN8#TRPBF	4250L	8-Lead PDIP	0°C to 70°C
LT4250LCS8#PBF	LT4250LCS8#TRPBF	4250L	8-Lead PLASTIC SO	0°C to 70°C
LT4250LIN8#PBF	LT4250LIN8#TRPBF	4250LI	8-Lead PDIP	–40°C to 85°C
LT4250LIS8#PBF	LT4250LIS8#TRPBF	4250LI	8-Lead PLASTIC SO	–40°C to 85°C
LT4250HCN8#PBF	LT4250HCN8#TRPBF	4250H	8-Lead PDIP	0°C to 70°C
LT4250HCS8#PBF	LT4250HCS8#TRPBF	4250H	8-Lead PLASTIC SO	0°C to 70°C
LT4250HIN8#PBF	LT4250HIN8#TRPBF	4250HI	8-Lead PDIP	–40°C to 85°C
LT4250HIS8#PBF	LT4250HIS8#TRPBF	4250HI	8-Lead PLASTIC SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2), V_{DD} = 48V, V_{EE} = 0V unless otherwise noted.

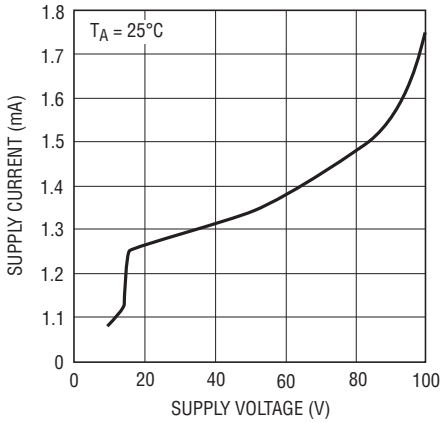
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC							
V_{DD}	Supply Voltage Operating Range		●	18		80	V
I_{DD}	Supply Current	UV = 3V, OV = V_{EE}, SENSE = V_{EE}	●		1.6	5	mA
V_{UVL}	Undervoltage Lockout				15.4		V
V_{CL}	Current Limit Trip Voltage	V_{CL} = (V_{SENSE} – V_{EE})	●	40	50	60	mV
I_{PU}	GATE Pin Pull-Up Current	Gate Drive On, V_{GATE} = V_{EE}	●	–30	–45	–60	µA
I_{PD}	GATE Pin Pull-Down Current	Gate Drive OFF		24	50	70	mA
I_{SENSE}	SENSE Pin Current	V_{SENSE} = 50mV			–20		µA
ΔV_{GATE}	External Gate Drive	(V_{GATE} – V_{EE}), 18V ≤ V_{DD} ≤ 80V	●	10	13.5	18	V
V_{UVH}	UV Pin High Threshold Voltage	UV Increasing	●	1.24	1.255	1.27	V
V_{UVL}	UV Pin Low Threshold Voltage	UV Decreasing	●	1.105	1.125	1.145	V
V_{UVHY}	UV Pin Hysteresis				130		mV
I_{INUV}	UV Pin Input Current	V_{UV} = V_{EE}	●		–0.02	–0.5	µA
V_{OVH}	OV Pin High Threshold Voltage	OV Increasing	●	1.235	1.255	1.275	V
V_{OVL}	OV Pin Low Threshold Voltage	OV Decreasing	●	1.21	1.235	1.255	V
V_{OVHY}	OV Pin Hysteresis				20		mV
I_{INOV}	OV Pin Input Current	V_{OV} = V_{EE}	●		–0.03	–0.5	µA
V_{DL}	DRAIN Low Threshold	V_{DRAIN} – V_{EE}, DRAIN Decreasing		1.1	1.6	2.3	V
V_{GH}	GATE High Threshold	ΔV_{GATE} – V_{GATE} Decreasing			1.3		V
I_{DRAIN}	Drain Input Bias Current	V_{DRAIN} = 48V	●	10	80	500	µA
V_{OL}	$\overline{PWRGD}$ Output Low Voltage	$\overline{PWRGD}$ (LT4250L), (V_{DRAIN} – V_{EE}) < V_{DL} I_{OUT} = 1mA I_{OUT} = 5mA	 ● ●		 0.48 1.2	 0.8 3	 V V
	PWRGD Output Low Voltage (PWRGD – DRAIN)	PWRGD (LT4250H), V_{DRAIN} = 5V I_{OUT} = 1mA	 ●		 0.75	 1	 V
I_{OH}	Output Leakage	$\overline{PWRGD}$ (LT4250L), V_{DRAIN} = 48V, $V_{\overline{PWRGD}}$ = 80V PWRGD (LT4250H), V_{DRAIN} = 0V, V_{PWRGD} = 80V	● ●		0.05 0.05	10 10	µA µA
AC							
t_{PHLOV}	OV High to GATE Low	Figures 1a, 2			1.7		µs
t_{PHLUV}	UV Low to GATE Low	Figures 1a, 3			1.5		µs
t_{PLHOV}	OV Low to GATE High	Figures 1a, 2			5.5		µs
t_{PLHUV}	UV High to GATE High	Figures 1a, 3			6.5		µs
$t_{PHLSENSE}$	SENSE High to Gate Low	Figures 1a, 4a			1	3	µs
t_{PHLCB}	Current Limit to GATE Low	Figures 1b, 4b			500		µs
t_{PHLDL}	DRAIN Low to $\overline{PWRGD}$ Low DRAIN Low to (PWRGD – DRAIN) High	(LT4250L) Figures 1a, 5a (LT4250H) Figures 1a, 5a			1 1		µs µs
t_{PHLGH}	GATE High to $\overline{PWRGD}$ Low GATE High to (PWRGD – DRAIN) High	(LT4250L) Figures 1a, 5b (LT4250H) Figures 1a, 5b			1.5 1.5		µs µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to V_{EE} unless otherwise specified.

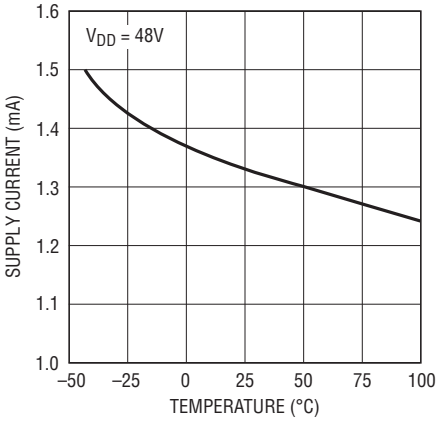
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



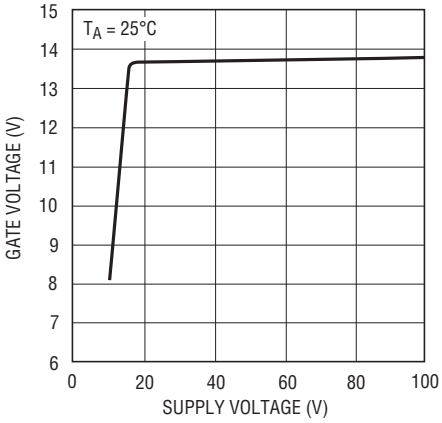
4250 G01

Supply Current vs Temperature



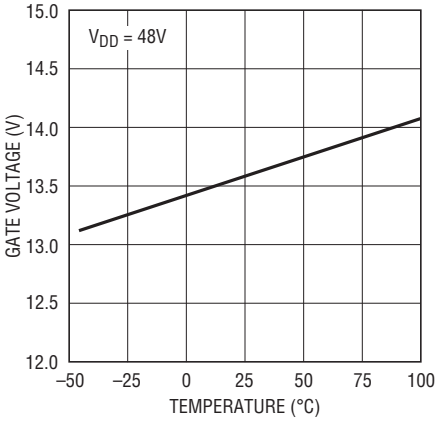
4250 G02

Gate Voltage vs Supply Voltage



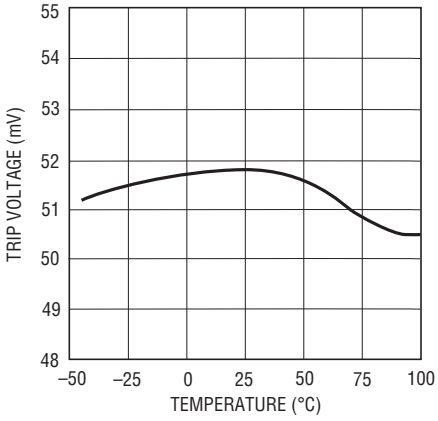
4250 G03

Gate Voltage vs Temperature



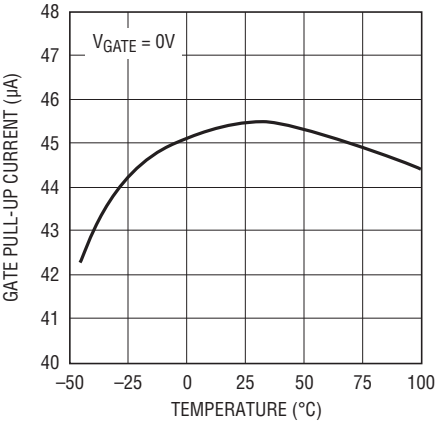
4250 G04

Current Limit Trip Voltage vs Temperature



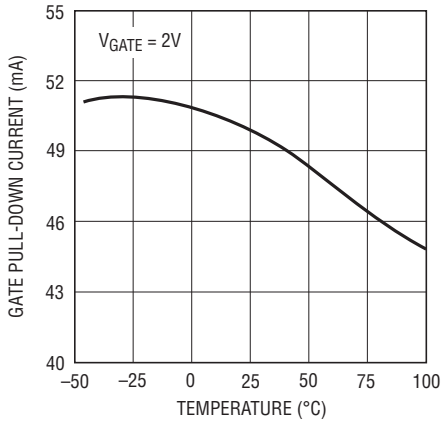
4250 G05

Gate Pull-Up Current vs Temperature



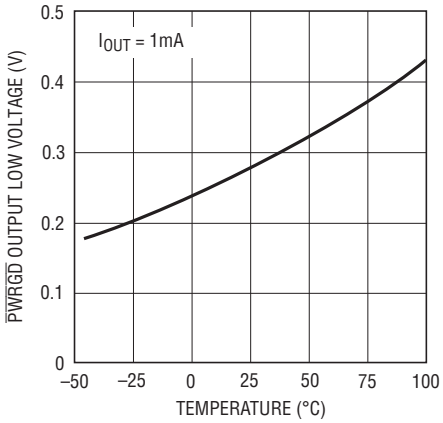
4250 G06

Gate Pull-Down Current vs Temperature



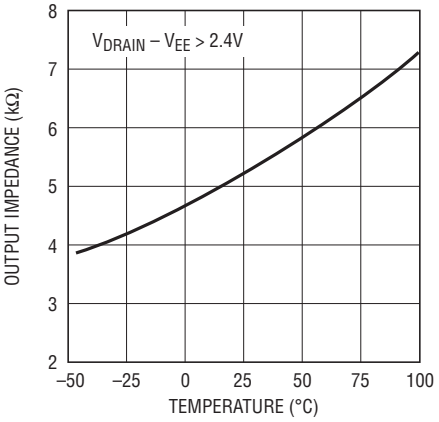
4250 G07

$\overline{PWRGD}$ Output Low Voltage vs Temperature (LT4250L)



4250 G08

PWRGD Output Impedance vs Temperature (LT4250H)



4250 G09

PIN FUNCTIONS

$\overline{\text{PWRGD}}$/PWRGD (Pin 1): Power Good Output Pin. This pin will latch a power good indication when V_{DRAIN} is within V_{DL} of V_{EE} and V_{GATE} is within V_{GH} of ΔV_{GATE}. This pin can be connected directly to the enable pin of a power module.

When the DRAIN pin of the LT4250L is above V_{EE} by more than V_{DL} or V_{GATE} is more than V_{GH} from ΔV_{GATE}, the $\overline{\text{PWRGD}}$ pin will be high impedance, allowing the pull-up current of the module's enable pin to pull the pin high and turn the module off. When V_{DRAIN} drops below V_{DL} and V_{GATE} rises above V_{GH}, the $\overline{\text{PWRGD}}$ pin sinks current to V_{EE}, pulling the enable pin low and turning on the module. This condition is latched until the GATE pin is turned off via the UV, OV, UVLO or the electronic circuit breaker.

When the DRAIN pin of the LT4250H is above V_{EE} by more than V_{DL} or V_{GATE} is more than V_{GH} from ΔV_{GATE}, the PWRGD pin will sink current to the DRAIN pin which pulls the module's enable pin low, forcing it off. When V_{DRAIN} drops below V_{DL} and V_{GATE} rises above V_{GH}, the PWRGD sink current is turned off, allowing the module's pull-up current to pull the enable pin high and turn on the module. This condition is latched until the GATE pin is turned off via the UV, OV, UVLO or the electronic circuit breaker.

OV (Pin 2): Analog Overvoltage Input. When OV is pulled above the 1.255V threshold, an overvoltage condition is detected and the GATE pin will be immediately pulled low. The GATE pin will remain low until OV drops below the 1.235V threshold.

UV (Pin 3): Analog Undervoltage Input. When UV is pulled below the 1.125V threshold, an undervoltage condition is detected and the GATE pin will be immediately pulled low. The GATE pin will remain low until UV rises above the 1.255 threshold.

The UV pin is also used to reset the electronic circuit breaker. If the UV pin is cycled low and high following the trip of the circuit breaker, the circuit breaker is reset and a normal power-up sequence will occur. The response time for this pin is 1.5µs. Add an external capacitor to this pin for additional filtering.

V_{EE} (Pin 4): Negative Supply Voltage Input. Connect to the lower potential of the power supply.

SENSE (Pin 5): Circuit Breaker Sense Pin. With a sense resistor placed in the supply path between V_{EE} and SENSE, the overcurrent condition will pull down the GATE pin and regulate the voltage across the resistor to be 50mV. If the overcurrent condition exists for more than 500µs the electronic circuit breaker will trip and turnoff the external MOSFET.

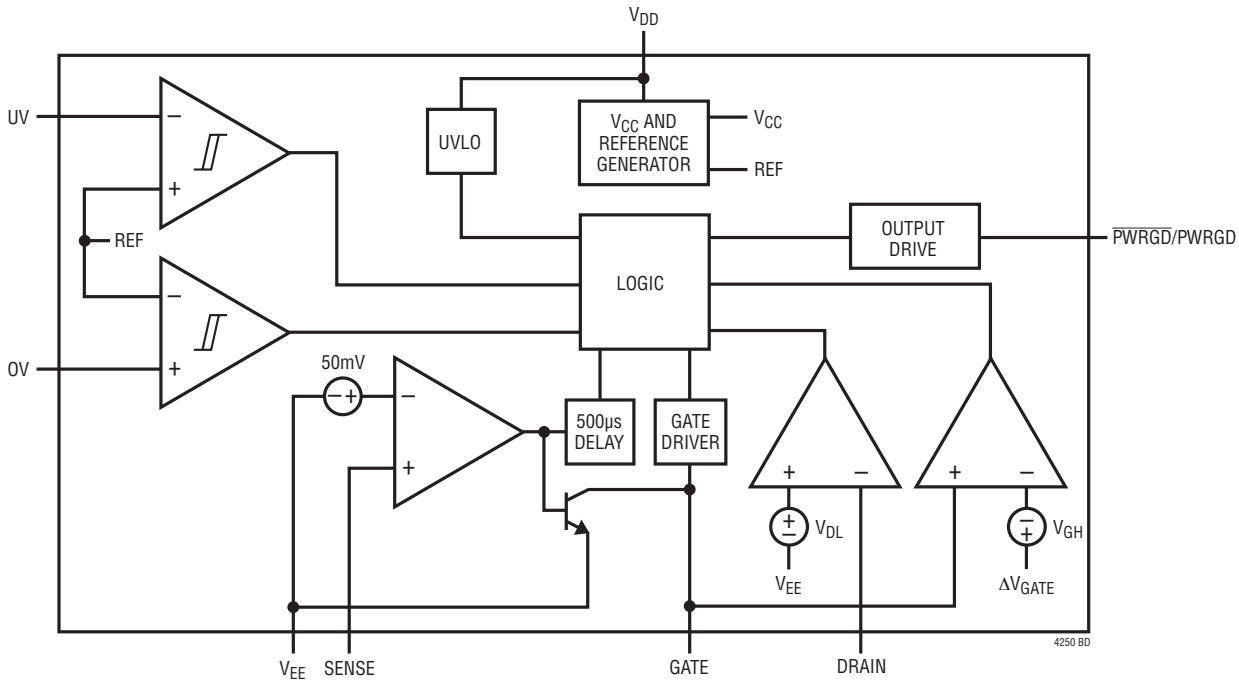
If the current limit value is set to twice the normal operating current, only 25mV is dropped across the sense resistor during normal operation. To disable the current limit feature, V_{EE} and SENSE can be shorted together.

GATE (Pin 6): Gate Drive Output for the External N-channel MOSFET. The GATE pin will go high when the following start-up conditions are met: the UV pin is high, the OV pin is low, $(V_{SENSE} - V_{EE}) < 50mV$ and the V_{DD} pin is greater than V_{UVLOH}. The GATE pin is pulled high by a 45µA current source and pulled low with a 50mA current source. During current limit the GATE pin is pulled low using a 100mA current source.

DRAIN (Pin 7): Analog Drain Sense Input. Connect this pin to the drain of the external N-channel MOSFET and the V^- pin of the power module. When the DRAIN pin is below V_{DL}, the $\overline{\text{PWRGD}}$/PWRGD pin will latch to indicate the switch is on.

V_{DD} (Pin 8): Positive Supply Voltage Input. Connect this pin to the higher potential of the power supply inputs and the V^+ pin of the power module. An undervoltage lockout circuit disables the chip until the V_{DD} pin is greater than the 16V V_{UVLOH} threshold.

BLOCK DIAGRAM



TEST CIRCUIT

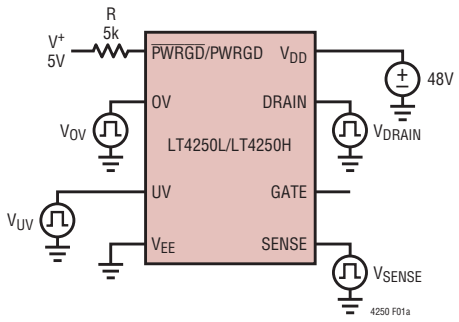


Figure 1a. Test Circuit 1

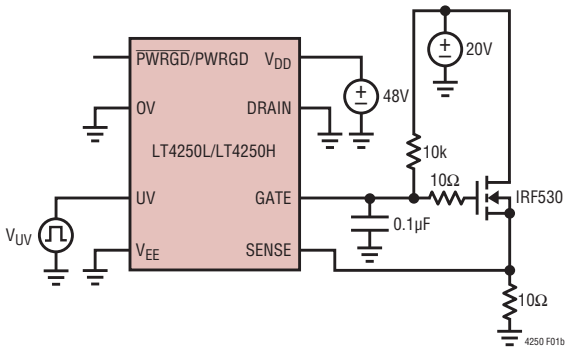


Figure 1b. Test Circuit 2

TIMING DIAGRAM

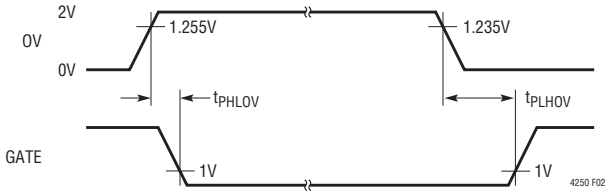


Figure 2. OV to GATE Timing

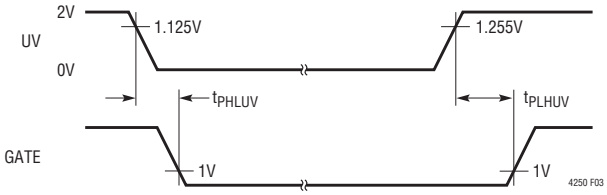


Figure 3. UV to GATE Timing

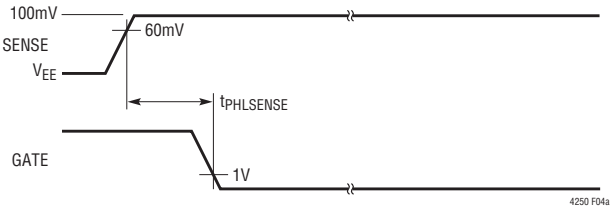


Figure 4a. SENSE to GATE Timing

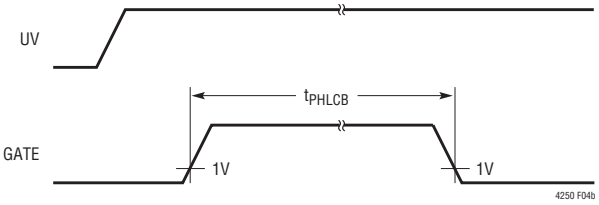


Figure 4b. Active Current Limit Timeout

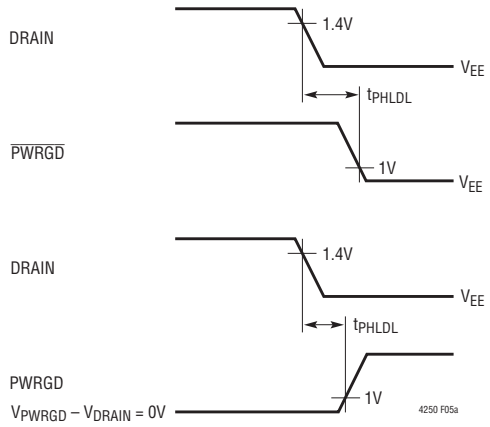


Figure 5a. DRAIN to $\overline{\text{PWRGD}}$/PWRGD Timing

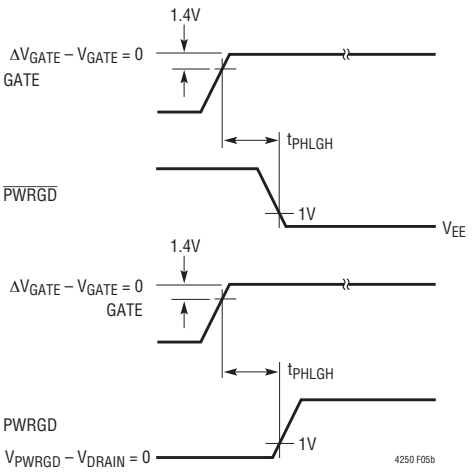


Figure 5b. GATE to $\overline{\text{PWRGD}}$/PWRGD Timing

APPLICATIONS INFORMATION

Hot Circuit Insertion

When circuit boards are inserted into a live –48V backplane, the bypass capacitors at the input of the board's power module or switching power supply can draw huge transient currents as they charge up. The transient currents can cause permanent damage to the board's components and cause glitches on the system power supply.

The LT4250 is designed to turn on a board's supply voltage in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. The chip also provides undervoltage, overvoltage and overcurrent protection while keeping the power module off until its input voltage is stable and within tolerance.

Power Supply Ramping

The input to the power module on a board is controlled by placing an external N-channel pass transistor (Q1) in the power path (Figure 6a). R1 provides current fault detection and R2 prevents high frequency oscillations. Resistors R4, R5 and R6 provide undervoltage and over-voltage sensing. By ramping the gate of Q1 up at a slow rate, the inrush current charging load capacitors C3 and C4 can be limited to a safe value when the board makes connection.

Resistor R3 and capacitor C2 act as a feedback network to accurately control the inrush current. The C2 capacitor can be calculated with the following equation:

$$C2 = (45\mu A \bullet C_L)/I_{INRUSH}$$

where C_L is the total load capacitance = C3 + C4 + module input capacitance.

Capacitor C1 and resistor R3 prevent Q1 from momentarily turning on when the power pins first make contact. Without C1 and R3, capacitor C2 would pull the gate of Q1 up to a voltage roughly equal to $V_{EE} \bullet C2/CGS(Q1)$ before the LT4250 could power up and actively pull the gate low. By placing capacitor C1 in parallel with the gate capacitance of Q1 and isolating them from C2 using resistor R3 the problem is solved. The value of C1 is given by:

$$C1 = \left(\frac{V_{INMAX} - V_{TH}}{V_{TH}}\right) \bullet (C2 + C_{GD})$$

$$C1 \cong 35 \bullet C2 \text{ for } V_{INMAX} = 72V$$

where V_{TH} is the MOSFET's minimum gate threshold and V_{INMAX} is the maximum operating input voltage.

R3 should not exceed a value that produces an R3 • C2 time-constant of 150µs. A 1k value for R3 will ensure this for C2 values up to 150nF.

The waveforms are shown in Figure 6b. When the power pins make contact, they bounce several times. While the contacts are bouncing, the LT4250 senses an undervoltage condition and the GATE is immediately pulled low when the power pins are disconnected.

Once the power pins stop bouncing, the GATE pin starts to ramp up. When Q1 turns on, the GATE voltage is held constant by the feedback network of R3 and C2. When the

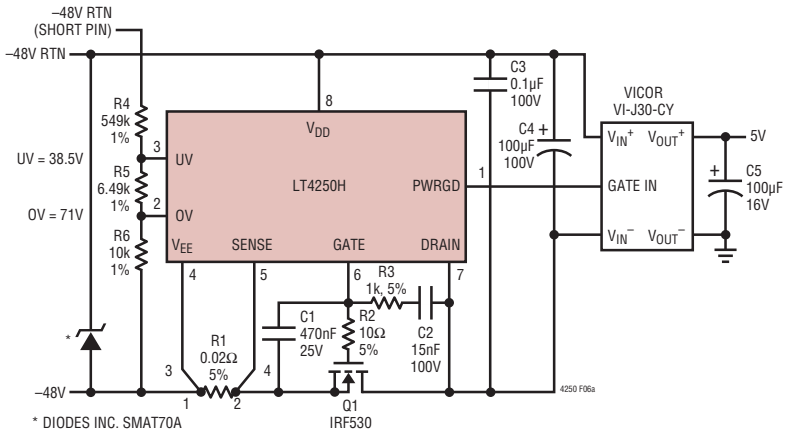


Figure 6a. Inrush Control Circuitry

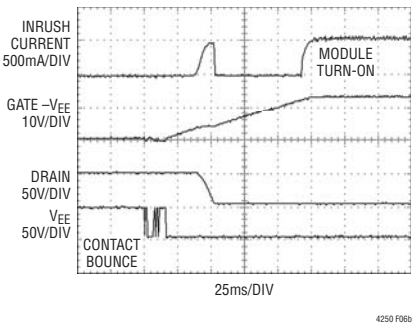


Figure 6b. Inrush Control Waveforms

APPLICATIONS INFORMATION

DRAIN voltage has finished ramping, the GATE pin then ramps to its final value.

Current Limit/Electronic Circuit Breaker

The LT4250 features a current limit function that protects against short circuits or excessive supply currents. If the current limit is active for more than 500µs the electronic circuit breaker will trip. By placing a sense resistor between the V_{EE} and SENSE pin, the current limit will be activated whenever the voltage across the sense resistor is greater than 50mV.

Note that the current limit threshold should be set sufficiently high to account for the sum of the load current and the inrush current. The maximum value of the inrush current is given by:

$$I_{INRUSH} \leq 0.8 \bullet \left(\frac{40mV}{R_{SENSE}} \right) - I_{LOAD},$$

where the 0.8 factor is used as a worst case margin combined with the minimum trip voltage (40mV).

In the case of a short circuit, the current limit circuitry activates and immediately pulls the GATE low, servos the SENSE voltage to 50mV, and starts a 500µs timer. The MOSFET current is limited to $50mV/R_{SENSE}$ (see Figure 7). If the short circuit persists for more than 500µs, the circuit breaker trips and pulls the GATE pin low, shutting off the MOSFET. The circuit breaker is reset by pulling UV low, or by cycling power to the part. If the short circuit clears before the 500µs timing interval the current limit will deactivate and release the GATE.

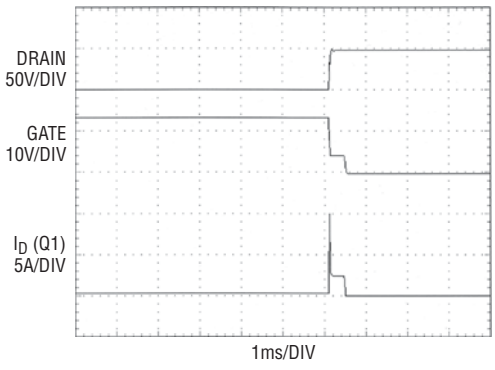


Figure 7. Short-Circuit Protection Waveforms

The LT4250 guards against voltage steps on the input supply. A positive voltage step (increasing in magnitude) on the input supply causes an inrush current that is proportional to the voltage slew rate $I = C_L \bullet \Delta V/\Delta T$. If the inrush exceeds $50mV/R_{SENSE}$, the current limit will activate as shown in Figure 8. The GATE pin pulls low, limiting the current to $50mV/R_{SENSE}$. At this level the MOSFET drain will not follow the source as the input voltage rapidly changes, but instead remains at the voltage stored on the load capacitance. The load capacitance begins to charge at a current of $50mV/R_{SENSE}$, but not for long. As the load capacitance charges, C2 pushes back on the gate and limits the MOSFET current in a manner identical to the initial start-up condition which is less than the short circuit limiting value of $50mV/R_{SENSE}$. Thus the circuit breaker does not trip. To ensure correct operation under input voltage step conditions, R_{SENSE} must be chosen to provide a current limit value greater than the sum of the load current and the dynamic current in the load capacitance.

For C2 values less than 10nF a positive voltage step increasing in magnitude on the input supply can result in the Q1 turning off momentarily due to current limit overshoot which can shut down the output. By adding an additional resistor and diode, Q1 remains on during the voltage step. This is shown as D1 and R7 in Figure 9. The purpose of D1 is to shunt current around R7 when the power pins first make contact and allow C1 to hold the GATE low. The value of R7 should be sized to generate an R7 • C1 time constant of 33µs.

Under some conditions, a short circuit at the output can cause the input supply to dip below the UV threshold. The LT4250 turns off once and then turns on until the electronic circuit breaker is tripped. This can be minimized by adding a deglitching delay to the UV pin with a capacitor from UV to V_{EE}. This capacitor forms an RC time constant with the resistors at UV, allowing the input supply to recover before the UV pin resets the circuit breaker.

APPLICATIONS INFORMATION

A circuit that automatically resets the circuit breaker after a current fault is shown in Figure 10. Transistors Q2 and Q3 along with R7, R8, C4 and D1 form a programmable one-shot circuit. Before a short occurs, the GATE pin is pulled high and Q3 is turned on, pulling node 2 to V_{EE}. Resistor R8 turns off Q2. When a short occurs, the GATE pin is pulled low and Q3 turns off. Node 2 starts to charge C4 and Q2 turns on, pulling the UV pin low and resetting the circuit breaker. As soon as C4 is fully charged, R8 turns off Q2, UV goes high and the GATE starts to ramp up. Q3 turns back on and quickly pulls node 2 back to V_{EE}. Diode D1 clamps node 3 one diode drop below V_{EE}. The duty cycle is set to 10% to prevent Q1 from overheating.

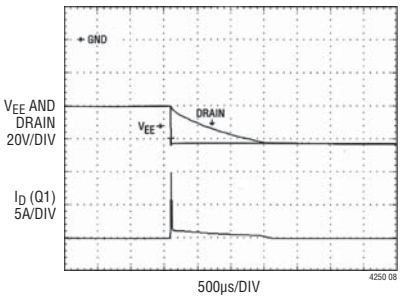


Figure 8. Voltage Step on Input Supply Waveforms

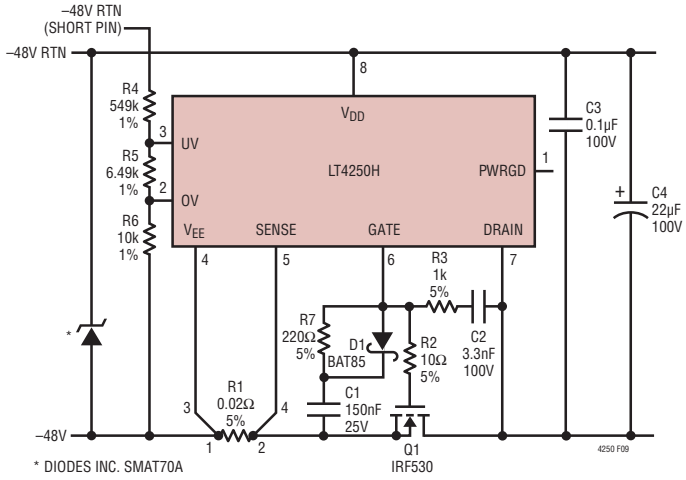


Figure 9. Circuit for Input Steps with Small C2 (<10nF)

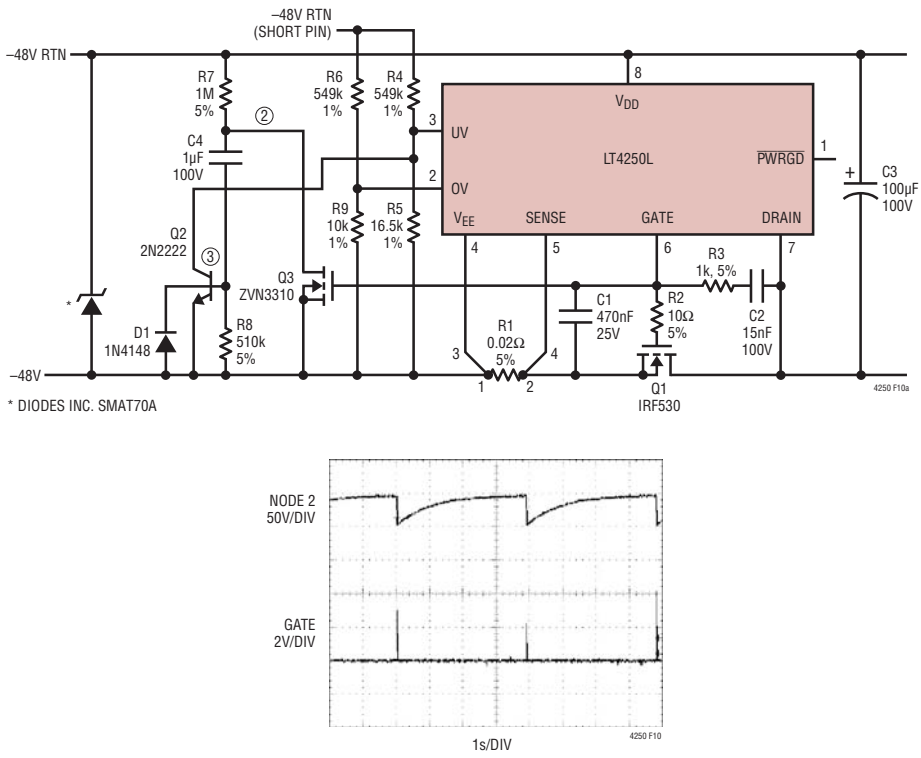


Figure 10. Automatic Restart After Current Fault

APPLICATIONS INFORMATION

Undervoltage and Overvoltage Detection

The UV (Pin 3) and OV (Pin 2) pins can be used to detect undervoltage and overvoltage conditions at the power supply input. The UV and OV pins are internally connected to analog comparators with 130mV and 20mV of hysteresis respectively. When the UV pin falls below its threshold or the OV pin rises above its threshold, the GATE pin is immediately pulled low. The GATE pin will be held low until UV is high and OV is low.

The undervoltage and overvoltage trip voltages can be programmed using a three resistor divider as shown in Figure 11. With R4 = 549k, R5 = 6.49k and R6 = 10K, the undervoltage threshold is set to 38.5V (with a 43V release from undervoltage) and the overvoltage threshold is set to 71V. The resistor divider will also gain up the hysteresis at the UV pin and OV pin to 4.5V and 1.2V at the input respectively.

$\overline{\text{PWRGD}}$/PWRGD Output

The $\overline{\text{PWRGD}}$/PWRGD output can be used to directly enable a power module when the input voltage to the module is within tolerance. The LT4250L has a $\overline{\text{PWRGD}}$ output for modules with an active low enable input, and the LT4250H has a PWRGD output for modules with an active high enable input.

When the DRAIN voltage of the LT4250H is high with respect to V_{EE} (Figure 12) or the GATE voltage is low, the internal transistor Q3 is turned off and I_1 and Q2 clamp the PWRGD pin one SAT drop (≈0.3V) above the DRAIN pin.Transistor Q2 sinks the module's pull-up current and the module turns off.

When the DRAIN voltage drops below V_{DL} and the GATE voltage is high, Q3 will turn on, shorting the bottom of I_1 to DRAIN and turning Q2 off. The pull-up current in the module pulls the PWRGD pin high and enables the module.

When the DRAIN voltage of the LT4250L is high with respect to V_{EE} or the GATE voltage is low, the internal pull-down transistor Q2 is off and the $\overline{\text{PWRGD}}$ pin is in a high impedance state (Figure 13). The $\overline{\text{PWRGD}}$ pin will be pulled high by the module's internal pull-up current source, turning the module off. When the DRAIN voltage drops below V_{DL} and the GATE voltage is high, Q2 will turn on and the $\overline{\text{PWRGD}}$ pin will pull low, enabling the module.

The $\overline{\text{PWRGD}}$ signal can also be used to turn on an LED oroptoisolator to indicate that the power is good as shown in Figure 14.

Gate Pin Voltage Regulation

When the supply voltage to the chip is more than 18V, the GATE pin voltage is regulated at 13.5V above V_{EE}. The gate voltage will be no greater than 18V for supply voltages up to 80V.

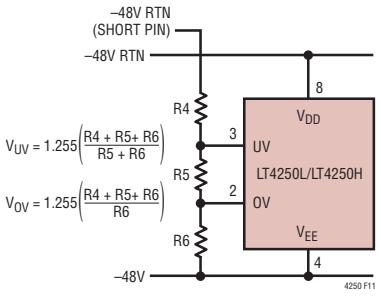


Figure 11. Undervoltage and Overvoltage Sensing

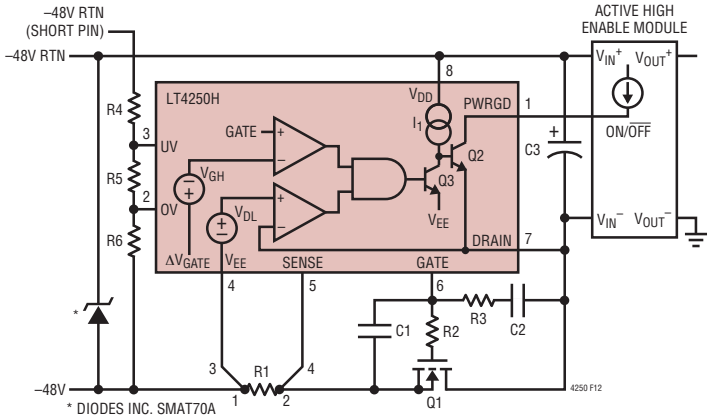


Figure 12. Active High Enable Module

APPLICATIONS INFORMATION

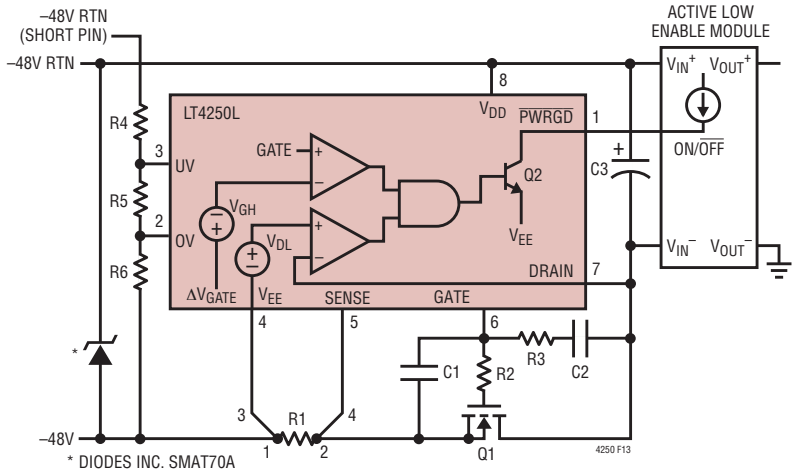


Figure 13. Active Low Enable Module

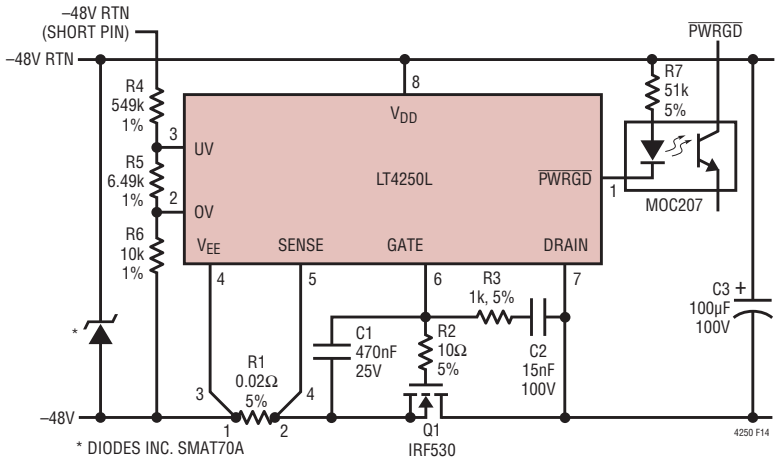
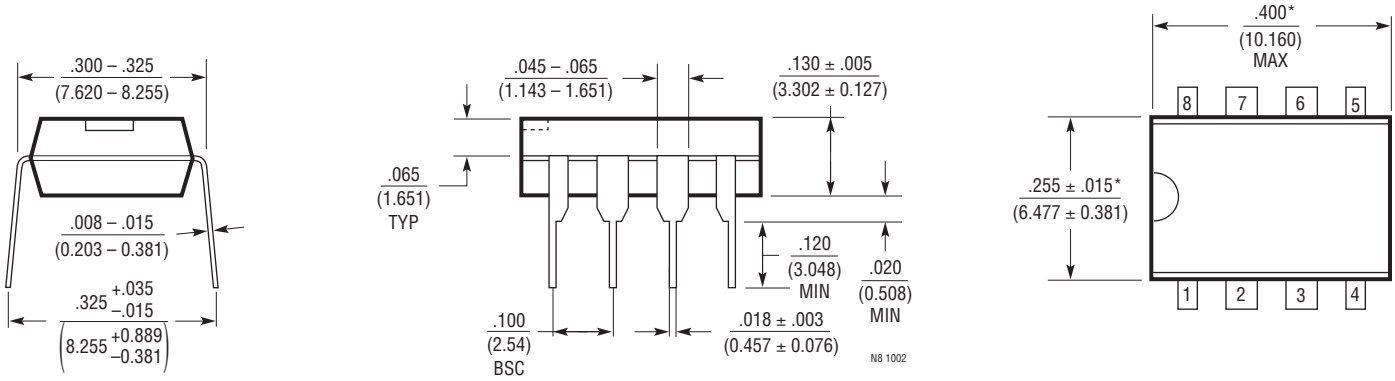


Figure 14. Using $\overline{\text{PWRGD}}$ to Drive an Optoisolator

PACKAGE DESCRIPTION

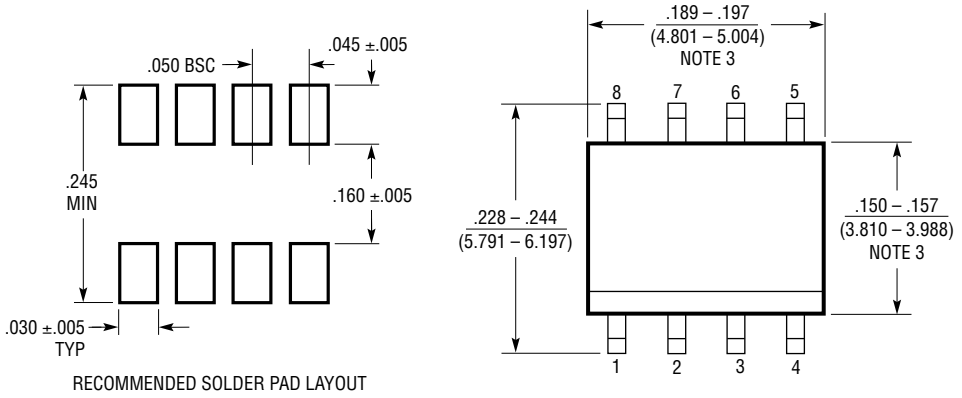
N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

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TYPICAL APPLICATION

Using an EMI Filter Module

Many applications place an EMI filter module in the powerpath to prevent switching noise of the module from being injected back onto the power supply. A typical application using the Lucent FLTR100V10 filter module is shown in Figure 15. When using a filter, an optoisolator is required to prevent common mode transients from destroying the $\overline{PWRGD}$ and $\overline{ON}$/OFF pins.

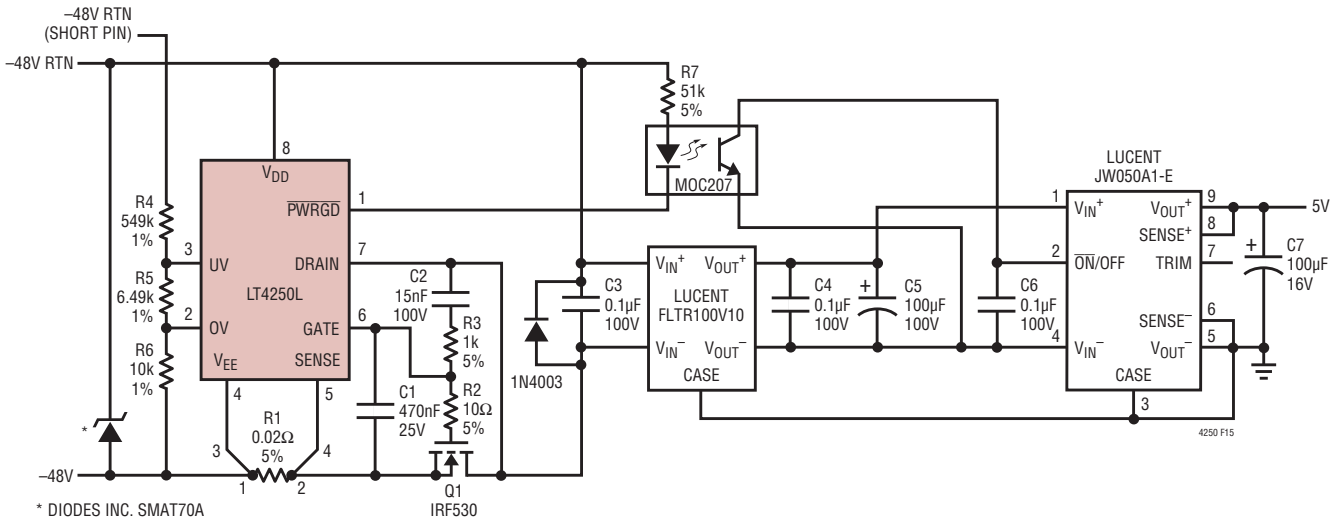

Figure 15. Typical Application Using a Filter Module

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®1421	Dual Hot Swap Controller with Additional –12V Control	Operates from 3V to 12V
LTC1422	Hot Swap Controller in SO-8	System Reset Output With Programmable Delay
LT1640AH/LT1640AL	–48V Hot Swap Controller in SO-8	LT4250 is a Pin-Compatible Upgrade to LT1640
LT1641-1/LT1641-2	48V Hot Swap Controller in SO-8	Foldback Current Limit, 9V to 80V, Auto-Retry/Latch-Off
LTC1642	Fault Protected Hot Swap Controller	Operates Up to 16.5V, Protected to 33V
LTC1643	PCI Hot Swap Controller	3.3V, 5V, 12V, –12V Supplies for PCI Bus
LTC1645	Dual Hot Swap Controller	Operates from 1.2V to 12V, Power Sequencing
LTC1646	Dual CompactPCI Hot Swap Controller	3.3V, 5V Supplies With Precharge and Local PCI Reset Logic
LTC1647	Dual Hot Swap Controller	Dual ON Pins for Supplies from 3V to 15V
LTC4211	Hot Swap Controller With Multifunction Current Control	2.5V to 16.5V Supplies, Active Inrush Current Limiting
LTC4251	–48 Hot Swap Controller in SOT-23	Active Current Limiting, Fast Comparator for Catastrophic Faults
LTC4252	–48 Hot Swap Controller in MSOP	Active Current Limiting, Fast Comparator for Catastrophic Faults, Separate UV/0V Pins, Power-Good Output

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LT 0309 REV A • PRINTED IN USA
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