Oxygen™HD CMI8786

High Performance PCI Audio Processor

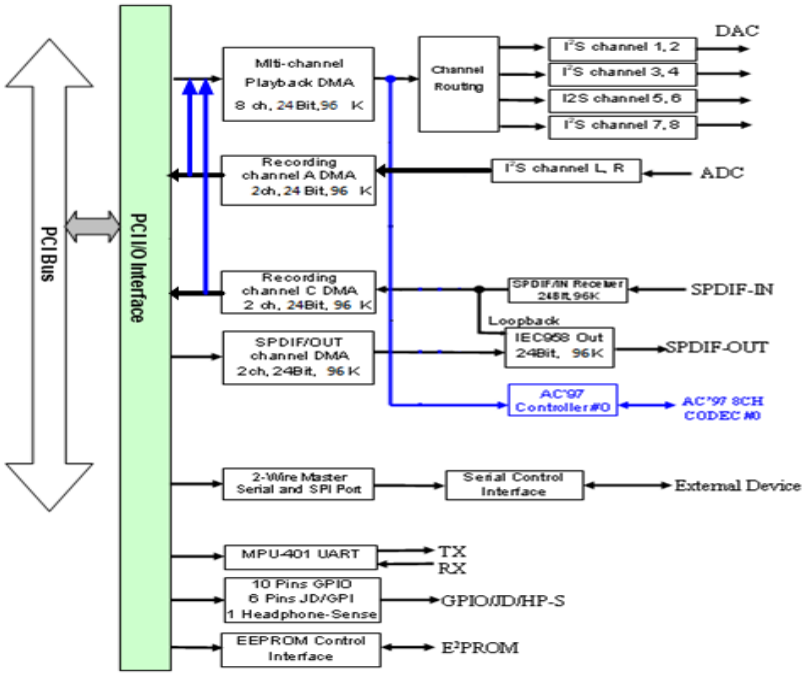
DESCRIPTION

The CMI8786 is a high quality PCI 32-bit multi-channel audio processor that can be built in the home audio electronics or personal computer to provide high fidelity sound and become a professional audio processing center in your life. It supports up to 10 outgoing channels and 4 ingoing channels. The 10 outgoing channels are composed of 2 playback DMA's, which are multi-channel DMA (24 bits, 8 channels, 96k), S/PDIF DMA (24 bits, 2 channels, 192k). The 4 ingoing channels are spread in 2 recording DMA's (24 bits, 96k), namely recording A, B, DMA's. The architecture of recording is a unique point of CMI8786 that makes the recording become the most flexible for the users. The details of the recording mode selection will be explained in the later sections.

FEATURES

- PCI 2.2 interface with bus mastering and burst modes
- Only one 24.576MHz oscillator is needed
- 4 synchronous I2S output data stream pairs within 1 flexible output DMA
- Programmable channel routing mechanism among the 4 I2S output pairs
- An alternatively multi-channel AC-link can support 1 AC97 codec
- Programmable HW monitoring routing from I2S inputs to outputs.
  All I2S I/O pairs support 24-bit high-definition PCM data transfer and adjustable sample rate up to 96KHz

BLOCK DIAGRAM



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Revision History

Date	Rev.	Release Note
2010/3/26	Rev. 0.1	First version

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1. Description and Overview

The CMI8786 is a high quality PCI 32-bit multi-channel audio processor that can be built in the home audio electronics or personal computer to provide high fidelity sound and become a professional audio processing center in your life. It supports up to 10 outgoing channels and 4 ingoing channels. The 10 outgoing channels are composed of 2 playback DMA's, which are multi-channel DMA (24 bits, 8 channels, 96k), S/PDIF DMA (24 bits, 2 channels, 192k). The 4 ingoing channels are spread in 2 recording DMA's (24 bits, 96k), namely recording A, B DMA's. The architecture of recording is a unique point of CMI8786 that makes the recording become the most flexible for the users. The details of the recording mode selection will be explained in the later sections.

The CMI8786 can co-work with all the popular codecs nowadays from I2S codecs with over 120dB quality to the usual AC97 codecs. This ability gives customers the flexibility to design their products. The I2S, AC-Link, 2-wire master bus, and SPI interfaces are used to transfer audio data and control data between the CMI8786 and codecs. To facilitate the connection with the existing home audio electronics, the CMI8786 has incorporated the S/PDIF transmitter and receiver with 192k sampling rate in it.

An EEPROM interface is built for the CMI8786 in connection with the EEPROM to store and retrieve the non-evaporable data for the customer applications, such as board configuration, sub-vender and sub-system IDs of the PCI configuration, or any dynamic data that customers want to save for the next power-on to restore.

The MPU-401 MIDI UART is also integrated in the CMI8786. There are six GPI phone jack detect pins in CMI8786, which can be used to distinguish if a cable is plugged in the phone jack. The GPIO pins of CMI8786 are nine; however.

2. Features

- PCI 2.2 interface with bus mastering and burst modes
- Only one 24.576MHz oscillator is needed
- 4 synchronous I2S output data stream pairs within 1 flexible output DMA
- Programmable channel routing mechanism among the 4 I2S output pairs
- 1 synchronous I2S input data stream pairs.
- An alternatively multi-channel AC-link can support 1 AC97 codec
- Programmable HW monitoring routing from I2S inputs to outputs.
- All I2S I/O pairs support 24-bit high-definition PCM data transfer and adjustable sample rate up to
- 96KHz
- Integrated 192k/24-bit S/PDIF transmitter with 1 dedicated S/PDIF OUT DMA
- Integrated 192k/24-bit S/PDIF receiver with 1 dedicated S/PDIF IN DMA
- S/PDIF IN supports digital loop back path for transforming between optical and RCA connection

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- A 48k/16-bit front panel DMA for AC97 codec
- 2-wire master serial bus or 4-wire SPI (serial port interface) to control I2S codecs
- Interrupt pin to inform external MCU to retrieve the data that system driver wants to pass out
- One MPU-401 MIDI UART port
- EEPROM control interface
- 6 GPI phone jack detection pins to distinguish if a cable is plugged in the jack
- 9 direct access GPIO pins
- 128-pin LQFP high-quality thin package

3. Applications

- Pro-sumer high-quality PCI sound card for retailer market
- PC-based media center
- Wireless media adapter
- Professional PC musician application
- High-end motherboard requiring top audio quality
- Audio up-sell for PC systems
- Bundle selling with high-profile VGA cards
- General purpose multi-channel I/O

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4. Block Diagram

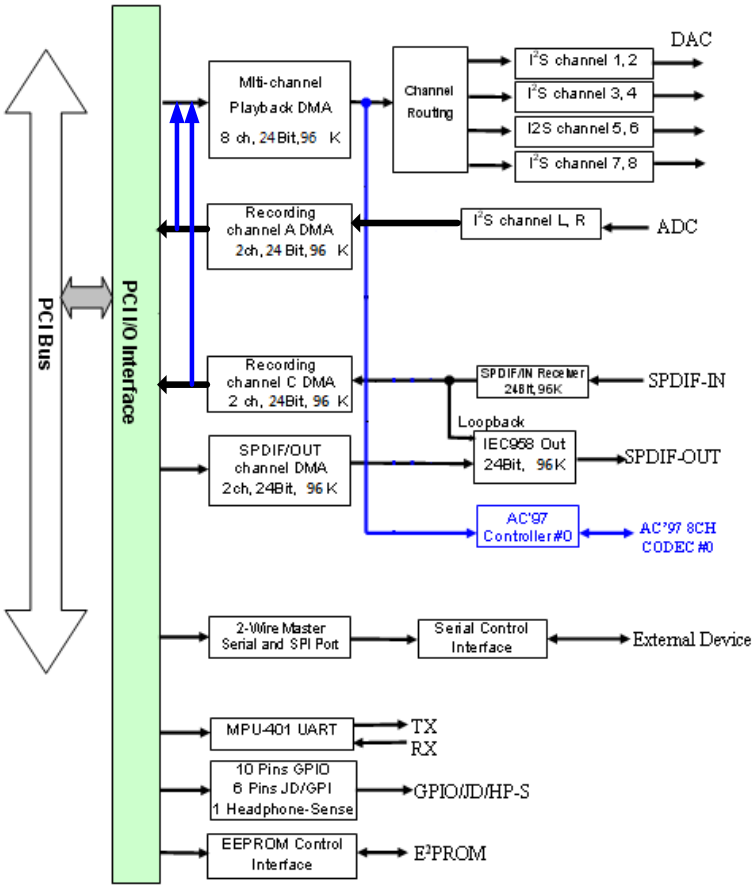


Figure 1. Block Diagram of Oxygen™HD CMI8786

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5. Pin Assignment

5.1 Pin-Out Diagram

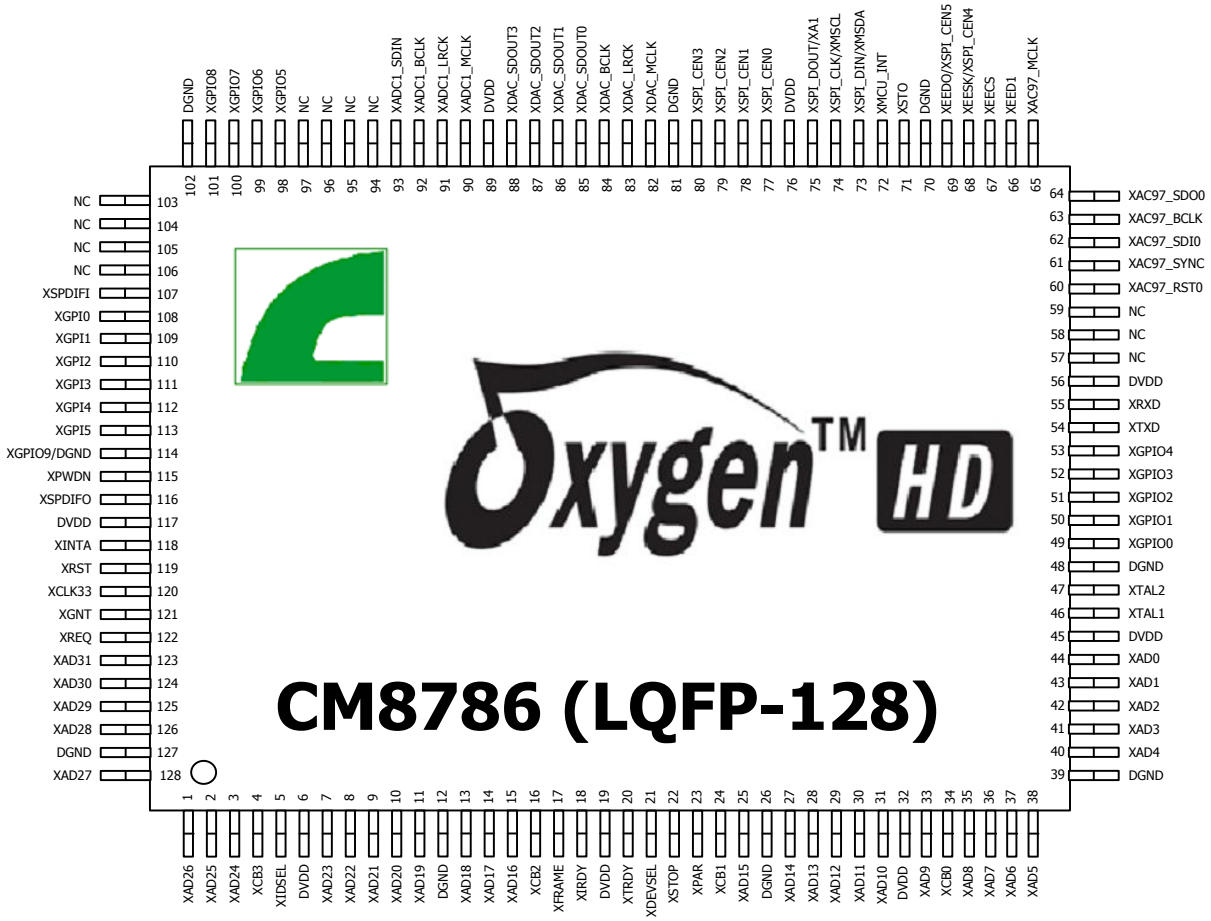


Figure 2. Pin-Out Diagram of Oxygen™HD CMI8786

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5.2 Pin Descriptions

The following table is the pin description of the Oxygen™HD CMI8786. Some of the pins own multiple functions. Therefore, for the sake of consistency, a pin may be listed more than once in the table. The abbreviations used in the pin description table are explained below.

DI: digital input signal
DO: digital output signal
DIO: digital bidirectional signal
AI: analog input
PU: pull-up with 75KΩ resistor
PD: pull-down with 75KΩ resistor
#: low active signal

Table 3.1 Pin description table of Oxygen™HD CMI8786

Symbol	Pin No.	Type	Description
PCI Bus Interface			
XRST	119	DI	PCI Bus Reset.
XCLK33	120	DI	PCI Bus clock, 33MHz.
XIDSEL	5	DI	PCI Initialization Device Select. This is the chip select during PCI configuration access.
XGNT#	121	DI	PCI Bus Grant. When active, PCI bus master is granted to CMI8786.
XREQ#	122	DIO	PCI Bus Master Request. When active means CMI8786 requests to become a bus master.
XAD[31:0]	1-3, 7-11, 13-15, 25, 27, 28-31, 33, 35-38, 40-44, 123-126, 128	DIO	PCI Address / Data Bus
XCB#[3:0]	4, 16, 24, 34	DIO	PCI Bus Command / Byte Enable
XFRAME#	17	DIO	PCI Cycle Frame. It is driven by the current master to indicate the beginning and duration of an access
XDEVSEL#	21	DIO	PCI Device Select. When active, indicates the driving device has decoded its address as the target of the current access.
XIRDY#	18	DIO	PCI Initiator Ready. When active, indicates the initiator has the ability to complete the current data phase of the transaction.
XTRDY#	20	DIO	PCI Target Ready. When active, indicates the target device has the ability to complete the current data phase of the transaction.
XSTOP#	22	DIO	PCI Stop. When active, indicates the current target is requesting the master to stop the current transaction.
XPAR	23	DIO	PCI Parity. It is even parity across XAD[31:0] and XCB#[3:0].
XINTA#	118	DIO	PCI Interrupt Request A.

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MPU-401 MIDI UART Interface			
XTXD	54	DIO, PU	MP-401 MIDI transmitter (output). It is also used as XGPIO5~8 and I2S ADC 3 configuration (input, 0: GPIO5~8, 1: I2S ADC 3) at the rising edge of XRST.
XRXD	55	DI, PU	MPU401 MIDI receiver.
I2S Interface			
XDAC_MCLK	82	DO	I2S DAC master clock output.
XDAC_LRCK	83	DIO	I2S DAC Left/Right sample clock.
XDAC_BCLK	84	DIO	I2S DAC bit clock.
XDAC_SDOUT0	85	DO	I2S DAC channel 0,channel 1 serial data output.
XDAC_SDOUT1	86	DO	I2S DAC channel 2,channel 3 serial data output.
XDAC_SDOUT2	87	DO	I2S DAC channel 4,channel 5 serial data output.
XDAC_SDOUT3	88	DO	I2S DAC channel 6,channel 7 serial data output.
XADC1_MCLK	90	DO	I2S ADC 1 and I2S ADC 4 master clock output.
XADC1_LRCK	91	DIO	I2S ADC 1 Left/Right sample clock.
XADC1_BCLK	92	DIO	I2S ADC 1 bit clock.
XADC1_SDIN	93	DI, PU	I2S ADC 1 serial data input.
AC-Link Interface			
XAC97_BCLK	63	DI, PU	AC97 serial clock input8
XAC97_SDI0	62	DI, PD	AC97 serial data input 0
XAC97_SYNC	61	DO	AC97 frame synchronization.
XAC97_SDO0	64	DO	AC97 serial data output 0.
XAC97_RST0	60	DO	AC97 codec reset 0.
XAC97_MCLK	65	DO	AC97 master clock 24.5760M for AC97 codec.
Serial Port Interface			
XSPI_DIN/ XMSDA	73	DIO, PU	SPI data input. This pin is shared with 2-wire master serial data.
XSPI_CLK/ XMSCL	74	DIO, PU	SPI clock output. This pin is shared with 2-wire master serial clock.
XSPI_DOUT	75	DIO, PU	SPI data output.
XSPI_CEN0	77	DIO, PU	SPI chip enable, which select the codec #0 to be controlled.
XSPI_CEN1	78	DIO, PU	SPI chip enable, which select the codec #1 to be controlled (output).
XSPI_CEN2	79	DIO, PU	SPI chip enable, which select the codec #2 to be controlled (output).

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XSPI_CEN3	80	DIO, PU	SPI chip enable, which select the codec #3 to be controlled (output).
XSPI_CEN4/ XEESK	68	DO	SPI chip enable, which select the codec #4 to be controlled. It is shared with EEPROM serial clock.
XSPI_CEN5/ XEEDO	69	DO	SPI chip enable, which select the codec #5 to be controlled. It is shared with EEPROM serial data out.
2-Wire Master Serial Bus			
XMSDA/ XSPI_DIN	73	DIO, PU	2-wire serial bus data. This pin is shared with SPI data input.
XMSCL/ XSPI_CLK	74	DIO, PU	2-wire serial bus clock. This pin is shared with SPI clock output.
S/PDIF Interface			
XSPDIFI	107	DI	S/PDIF receiver.
XSPDIFO	116	DO	S/PDIF transmitter.
EEPROM Interface			
XEECS	67	DIO, PD	EEPROM chip enable (output). It is also used as power on EEPROM CS delay configuration (input, 0: no delay, 1: delay 1 clock) at the rising edge of XRST
XEESK/ XSPI_CEN4	68	DO	EEPROM serial clock. This pin is shared with SPI chip enable, which select the codec #4 to be controlled
XEEDI	66	DI, PU	EEPROM serial data in
XEEDO/ XSPI_CEN5	69	DO	EEPROM serial data out. This pin is shared with SPI chip enable, which select the codec #5 to be controlled
Jack Detect GPI Interface			
XGPI0	108	DI, PD	JACK A detection input
XGPI1	109	DI, PD	JACK B detection input
XGPI2	110	DI, PD	JACK C detection input
XGPI3	111	DI, PD	JACK D detection input
XGPI4	112	DI, PD	JACK E detection input
XGPI5	113	DI, PD	JACK F detection input
GPIO Interface			
XGPIO0	49	DIO, PD	GPIO0, default output Low.
XGPIO1	50	DIO, PD	GPIO1, default output Low.
XGPIO2	51	DIO, PD	GPIO2, default input.
XGPIO3	52	DIO, PU	GPIO3, default output Low.
XGPIO4	53	DIO, PU	GPIO4, default input.
XGPIO5	98	DIO, PD	GPIO5, default output Low.

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XGPIO6	99	DIO, PD	GPIO6, default input.
XGPIO7	100	DIO, PD	GPIO7, default output Low.
XGPIO8	101	DIO, PD	GPIO8, default input.
No Connection			
NC	57		
NC	58		
NC	59		
NC	94		
NC	95		
NC	96		
NC	97		
NC	103		
NC	104		
NC	105		
NC	106		
Miscellaneous			
XTAL1	46	DI	24.576Mhz OSC input
XTAL2	47	DO	OSC output
XRSTO	71	DO	External Codec reset, can be programmed as Active Low or High with Register 0x50-bit 2
XPWDN	115	DO	Power Down output pin, Active Low, default High
DVDD	6, 19, 32, 45, 56, 76, 89, 117		3.3V power input
DGND	12, 26, 39, 48, 70, 81, 102, 114		Ground

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6. Electrical Characteristics

6.1 Maximum Ratings

Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25oC

Parameter	Symbol	Min	Typ	Max	Units
Storge temperature	-	-55	-	150	°C
Operating ambient temperature	-	0	25	75	°C
DC supply voltage	-	3.0	3.3	3.6	V
I/O pin voltage	-	GND	-	V_{DD}	V
Power dissipation	-	-	0.15	-	W

6.2 Recommended Operation Conditions

Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25°C

Parameter	Symbol	Min	Typ	Max	Units
Input voltage range	-	V_{DD}-0.3	V_{DD}	V_{DD}+0.3	V
Output voltage range	-	0	-	V_{DD}	V

6.3 Power Consumption

Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25°C

Parameter	Symbol	Min	Typ	Max	Units
Supply current : power up	-	-	40	-	mA
Supply current : power down	-	-	10	-	uA

6.4 DC Characteristics

Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25oC

Parameter	Symbol	Min	Typ	Max	Units
Input voltage range	Vin	V_{DD}-0.3	V_{DD}	V_{DD}+0.3	V
Output voltage range	Vout	0	-	V_{DD}	V
High level input voltage	Vih	0.7V_{DD}	-	-	V
Low level input voltage	Vil	-	-	0.3V_{DD}	V
High level output voitage	Voh	2.4	-	-	V
Low level output voltage	Vol		-	0.4	V
Input leakage current	Iil	-10	-	10	uA
Output leakage current	Iol	-10	-	10	uA
Output buffer driver current	-	-	8	-	mA
SPDIF transmit output driver current	-	-	8	-	mA

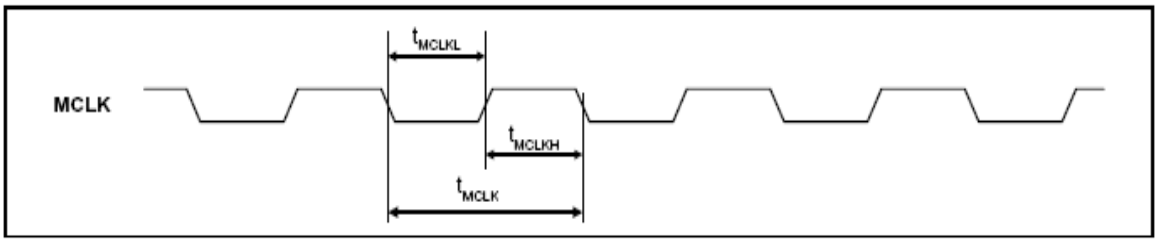
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6.5 AC Timing Characteristics

6.5.1 I2S Signal Timing

a. System Clock Timing

System Clock Timing Diagram



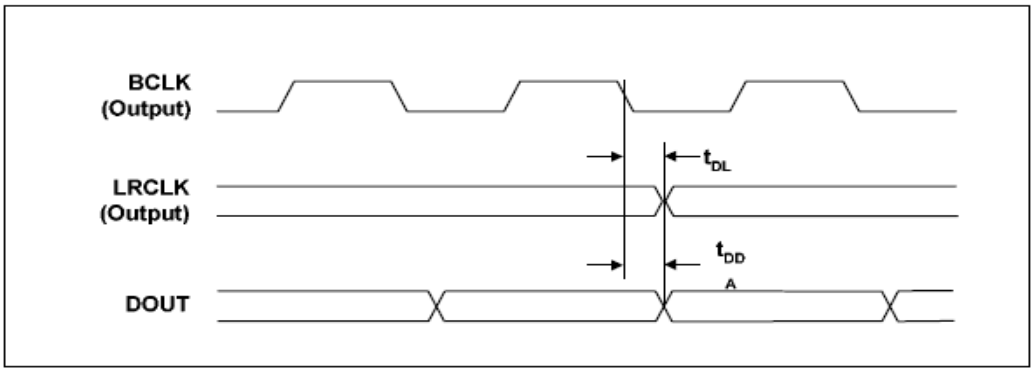
Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25oC,fs=96KHz,MCLK=512fs,24 bit data,unless otherwise stated

System Clock Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
MCLK clock cycle time	tmclk	20	-	-	ns
MCLK pulse width high	tmclkh	10	-	-	ns
MCLK pulse width high	tmclkl	10	-	-	ns
MCLK duty cycle		40	50	60	%

b. Audio Interface Timing

Audio Interface Timing Diagram



Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25oC,fs=96KHz,MCLK=512fs,24 bit data, unless otherwise stated

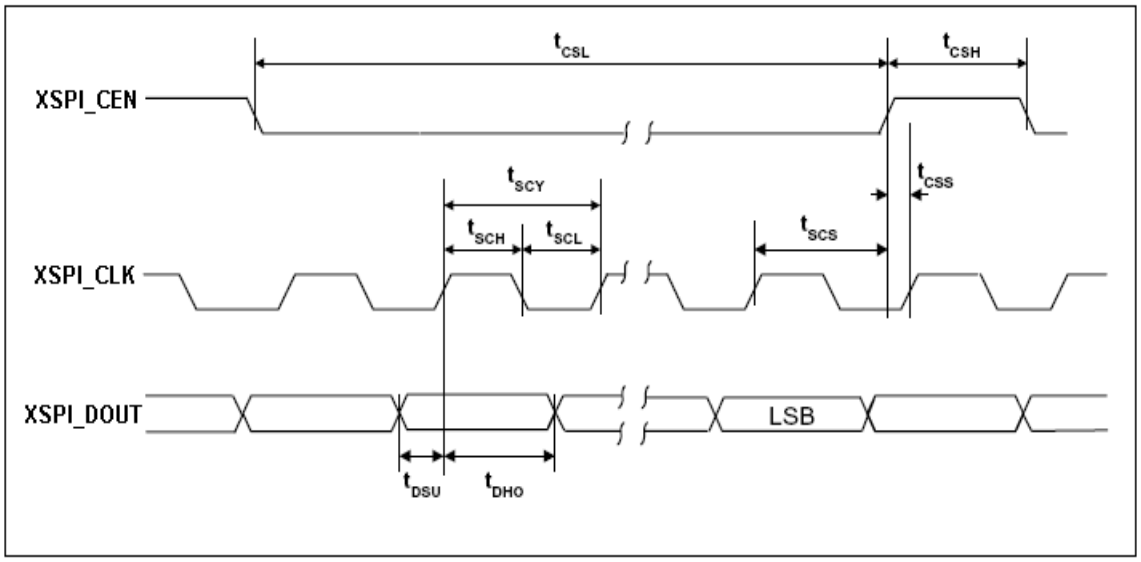
Audio Interface Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
LRCK propagation delay from BCLK falling edge	Tdl	5	-	-	ns
SDOUT propagation delay from BCLK falling edge	Tdd	5	-	-	ns

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6.5.2 Control Interface Timing - 3 - Wire Mode

Control Interface Timing -3- Wire Diagram



Note: latch data at XSPI_CEN clock low mode, XSPI_CEN clock can be low or high mode

Test Conditions

DVDD = 3.3V, DGND =0V, TA=+25°C, SPI clock 160 ns, unless otherwise stated

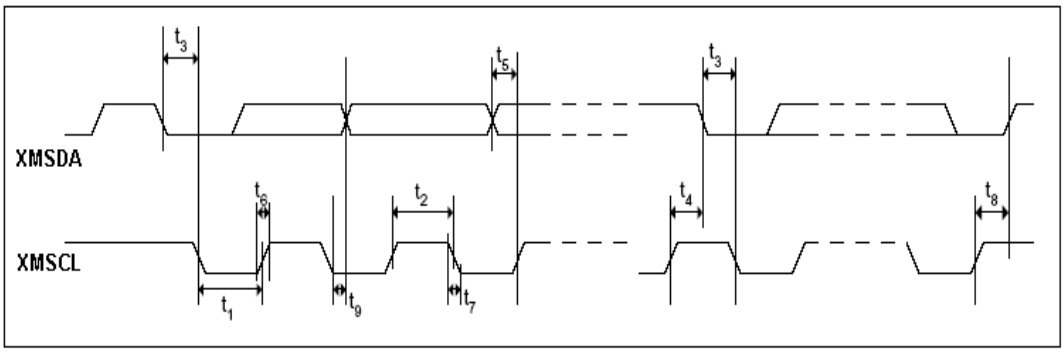
Control Interface Timing -3- Wire Parameters

Parameter	Symbol	Min	Typ	Max	Units
XSPI_CLK rising edge to XSPI_CEN rising edge	Tscs	120	-	-	ns
XSPI_CLK pulse cycle time	Tscy	160	-	-	ns
XSPI_CLK pulse width low	Tscl	80	-	-	ns
XSPI_CLK pulse width high	Tsch	80	-	-	ns
XSPI_DOUT to XSPI_CLK set-up time	Tdsu	40	-	-	ns
XSPI_DOUT to XSPI_CLK hold time	Tdho	40	-	-	ns
XSPI_CEN rising to SCLK rising	Tcss	40	-	-	ns

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6.5.3 Control Interface Timing - 2 - Wire Mode

Control Interface Timing -2- Wire Diagram



Test Conditions
DVDD = 3.3V, DGND =0V, TA=+25°C, 2 wire, Fast speed mode, unless otherwise stated

Control Interface Timing -2- Wire Parameters

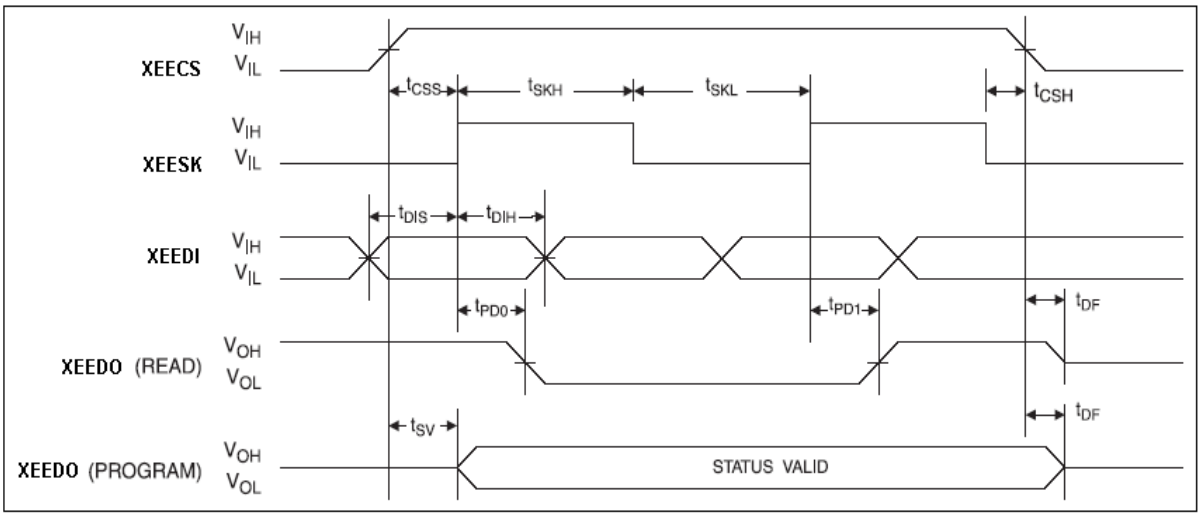
Parameter	Symbol	Min	Typ	Max	Units
XMSCL frequency		400	-	-	KHz
XMSCL pulse width low	t1	650	-	-	ns
XMSCL pulse width high	t2	1.3	-	-	us
Hold time (start condition)	t3	650	-	-	ns
Set-up time (start condition)	t4	650	-	-	ns
Data set-up time	t5	650	-	-	ns
XMSDI,XMSCL rise time	t6	100	-	-	ns
XMSDI,XMSCL fall time	t7	100	-	-	ns
Set-up time (stop condition)	t8	650	-	-	ns
Data hold time	t9	650	-	-	ns

Note: test parameters at 2 wire, Fast speed mode

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6.5.4 EEPROM Interface Timing

EEPROM Interface Timing Diagram



Test Conditions
DVDD = 3.3V, DGND =0V, TA=+25°C, unless otherwise stated

EEPROM Interface Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
XEESK clock frequency	tsk	555	-	-	KHz
XEESK high time	tskh	900	-	-	ns
XEESK low time	tskl	900	-	-	ns
XEECS setup time	tcss	900	-	-	ns
XEEDI setup time	tdis	900	-	-	ns
XEECS hold time	tcsh	900	-	-	ns
XEEDI hold time	tdih	2	-	-	ns
Output delay to “1”	tpd1	900	-	-	ns
Output delay to “0”	tpd0	30	-	-	ns
XEECS to status valid	tsv	30	-	-	ns
XEECS to XEEDO in high impedance	tdf	30	-	-	ns

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6.5.5 EEPROM AC Timing Characteristics

Symbol	Description	Min	Max	Units
fsk	SK Clock Frequency	0	0.5	MHz
tskh	SK High Time	500		ns
tskl	SK Low Time	500		ns
tcss	CS Setup Time	100		ns
tcsh	CS Hold Time	0		ns
tdis	DI Setup Time	200		ns
tdih	DI Hold Time	200		ns
tpd0	Output Delay to “0”		500	ns
tpd1	Output Delay to “1”		500	ns
tsv	CS to Status Valid		500	ns
tdf	CS to DO High Impedance		200	ns

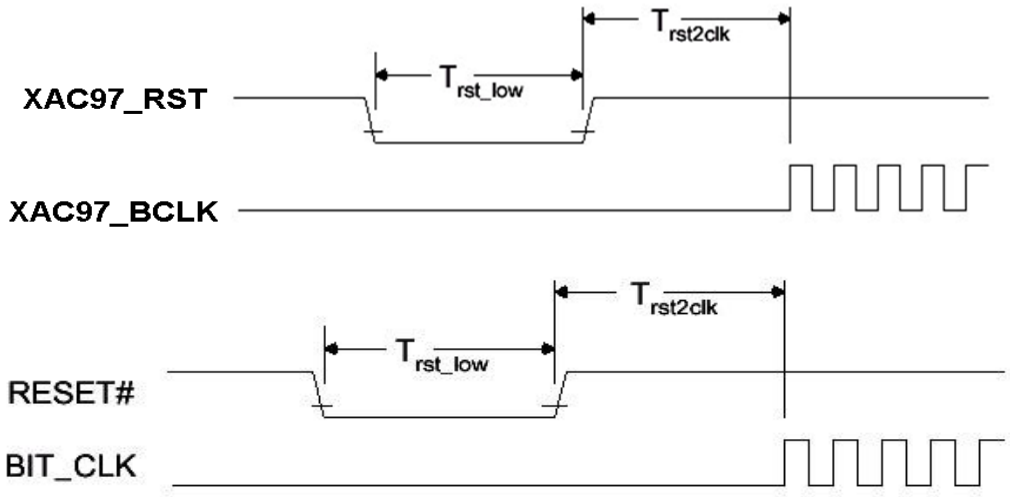
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6.5.6 AC-Link Timing Characteristics:

Test Conditions
DVDD = 3.3V, DGND =0V,TA=+25oC ,unless otherwise stated

1. Cold Rest

Cold Reset Timing Diagram



Cold Reset Timing Parameters

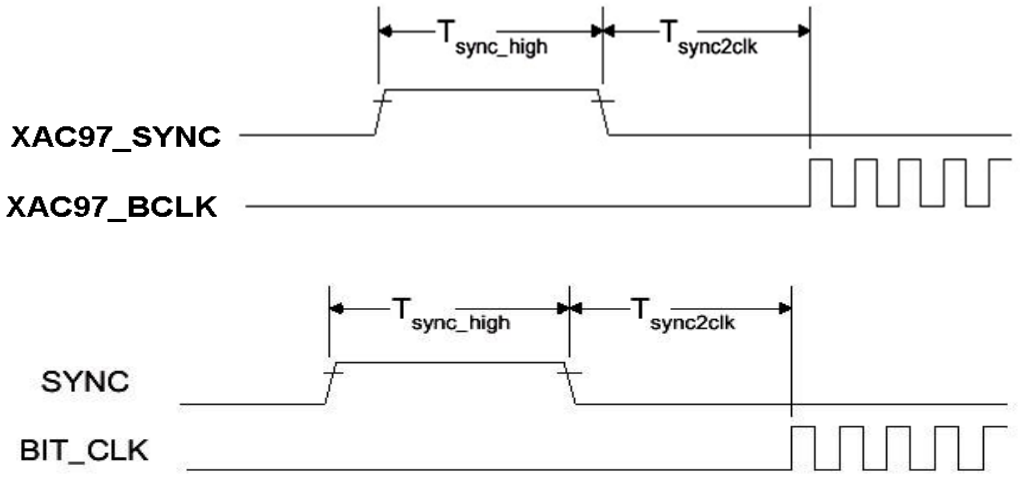
Parameter	Symbol	Min	Typ	Max	Units
XAC97_RST active low pulse width	Trst_low	1.7	-	-	us
XAC97_RST inactive to XAC97_BCLK startup delay	Trst2clk	168	-	-	ns

 # denotes active low.

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2. Warm Reset

Warm Reset Diagram

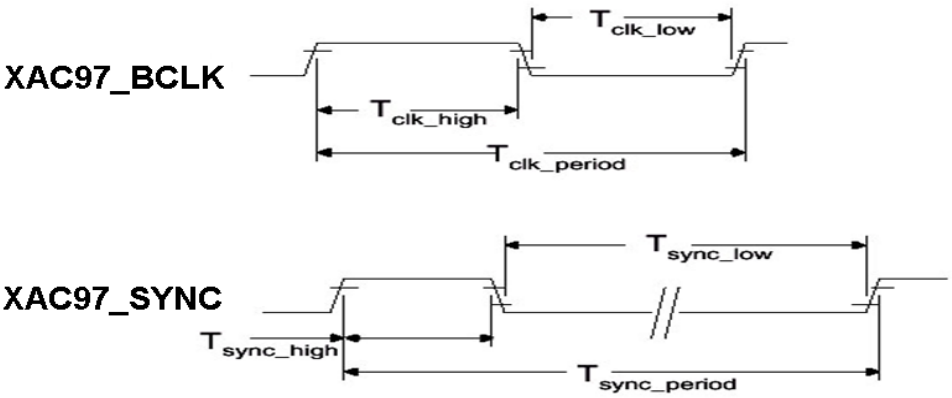


Warm Reset Parameters

Parameter	Symbol	Min	Typ	Max	Units
XAC97_SYNC active high pulse width	Tsync_high	1.2	-	-	us
XAC97_SYNC inactive to XAC97_BCLK startup delay	Tsync2clk	168	-	-	ns

3. AC-Link Clocks

BIT_CLK to SYNC Timing Diagram



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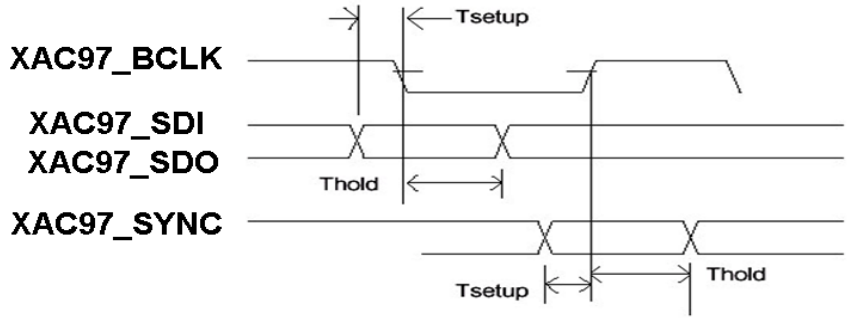
BIT_CLK to SYNC Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
XAC97_BCLK frequency		12.288	-	-	MHz
XAC97_BCLK period	Tclk_period	81.4	-	-	ns
XAC97_BCLK output jitter		750	-	-	ps
XAC97_BCLK high pulsewidth (note 1)	Tclk_high	40.7	-	-	ns
XAC97_BCLK low pulse width (note 1)	Tclk_low	40.7	-	-	ns
XAC97_SYNC frequency		48.0	-	-	kHz
XAC97_SYNC period	Tsync_period	20.8	-	-	us
XAC97_SYNC high pulse width	Tsync_high	1.3	-	-	us
XAC97_SYNC low_pulse width	Tsync_low	19.5	-	-	us

Note: Worst case duty cycle restricted to 45/55.

4. Data Setup and Hold

Data Setup and Hold diagram



Data Setup and Hold Parameters

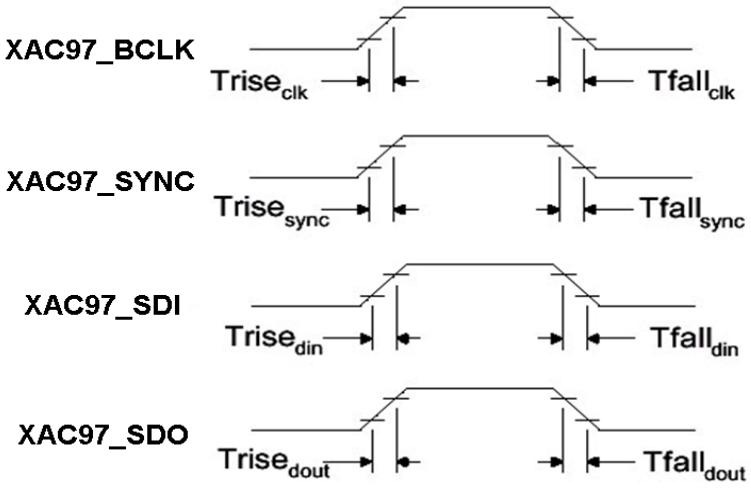
Parameter	Symbol	Min	Typ	Max	Units
Setup to falling edge of XAC97_BCLK	Tsetup	30	-	-	ns
Hold from falling edge of XAC97_BCLK	Thold	30	-	-	ns

Note: Setup and hold time parameters for SDATA_IN are with respect to the AC '97 Controller.

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5. Signal Rising and Falling Times

Signal Rising and Falling Times Diagram



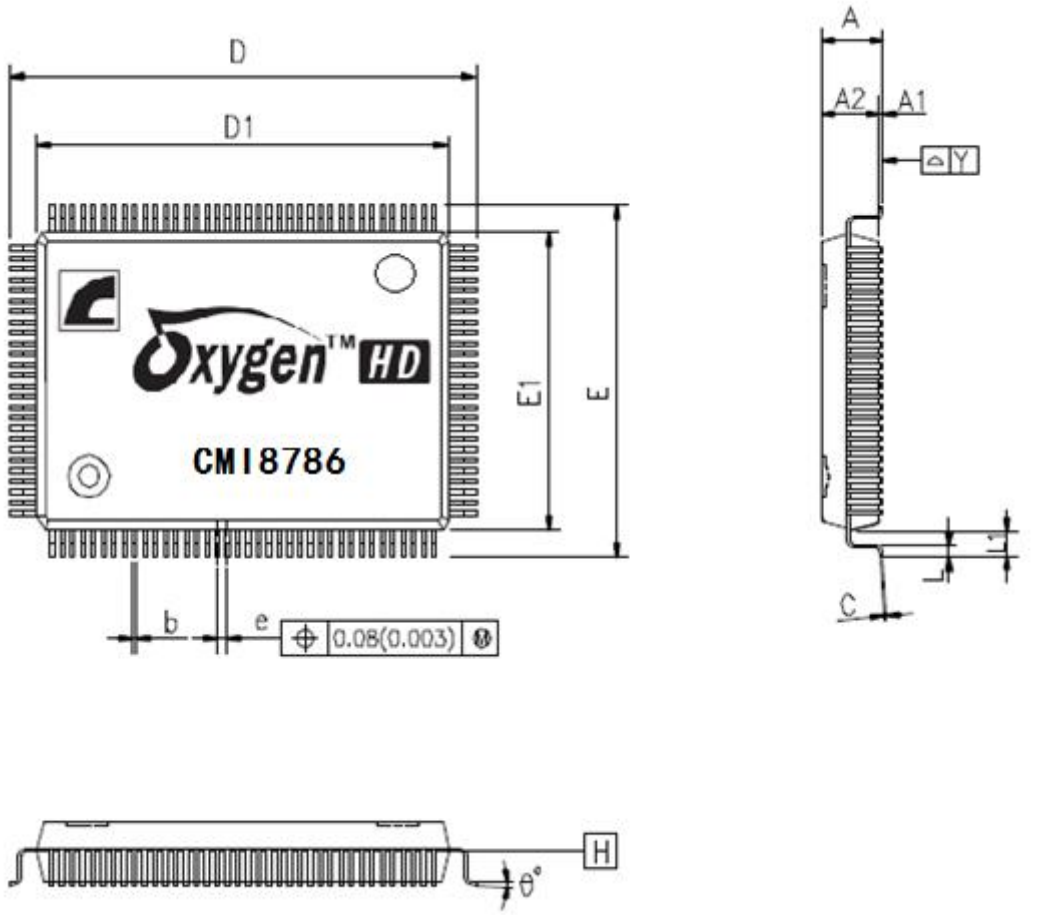
Signal Rising and Falling time Parameters

Parameter	Symbol	Min	Typ	Max	Units
XAC97_BCLK rising time	Triseclk	6	-	-	ns
XAC97_BCLK falling time	Tfallclk	6	-	-	ns
XAC97_SYNC rising time	Trisesync	6	-	-	ns
XAC97_SYNC falling time	Tfallsync	6	-	-	ns
XAC97_SDI rising time	Trisedin	6	-	-	ns
XAC97_SDI falling time	Tfalldin	6	-	-	ns
XAC97_SDO rising time	Trisedout	6	-	-	ns
XAC97_SDO falling time	Tfalldout	6	-	-	ns

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7. Mechanical Specification

7.1 Package Dimension



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
C	0.10	0.15	0.20
D1	–	20.00 BSC	–
E1	–	14.00 BSC	–
e	–	0.50 BSC	–
D	–	22.00 BSC	–
E	–	16.00 BSC	–
L	0.45	0.60	0.75
L1	–	1.00 REF	–
Y	–	–	0.08
θ°	0°	3.5°	7°

UNIT : mm

NOTES.

1. JEDEC OUTLINE.MS-026 BHB
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS E1 AND D1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS E AND E DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .

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—End of Specifications—

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