

100-Pin TQFP
Commercial Temp
Industrial Temp

512K x 18, 256K x 32, 256K x 36
8Mb Sync Burst SRAMs

100 MHz–66 MHz
3.3 V V_{DD}
3.3 V and 2.5 V I/O

Features

- $\overline{FT}$ pin for user-configurable flow through or pipelined operation
- Dual Cycle Deselect (DCD) operation
- 3.3 V +10%/–5% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{LBO}$ pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipeline mode
- Byte Write ($\overline{BW}$) and/or Global Write ($\overline{GW}$) operation
- Common data inputs and data outputs
- Clock Control, registered, address, data, and control
- Internal self-timed write cycle
- Automatic power-down for portable applications
- 100-lead TQFP package

		-11	-11.5	-100	-80	-66
Pipeline	tCycle	10 ns	10 ns	10 ns	12.5 ns	15 ns
3-1-1-1	t _{KQ}	4.0 ns	4.0 ns	4.0 ns	4.5 ns	5.0 ns
	I _{DD}	225 mA	225 mA	225 mA	200 mA	185 mA
Flow	t _{KQ}	11 ns	11.5 ns	12 ns	14 ns	18 ns
Through	tCycle	15 ns	15 ns	15 ns	15 ns	20 ns
	I _{DD}	180 mA	180 mA	180 mA	175 mA	165 mA

Functional Description

Applications

The GS880E18/32/36T is a 9,437,184-bit (8,388,608-bit for x32 version) high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enables ($\overline{E1}$, $\overline{E2}$, $\overline{E3}$), address burst control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$) and write control inputs ($\overline{Bx}$, $\overline{BW}$, $\overline{GW}$) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable ($\overline{G}$) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by $\overline{ADV}$. The burst address counter may be configured to count in either linear or

interleave order with the Linear Burst Order ($\overline{LBO}$) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through / Pipeline Reads

The function of the Data Output register can be controlled by the user via the $\overline{FT}$ mode pin (Pin 14). Holding the $\overline{FT}$ mode pin low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding $\overline{FT}$ high places the RAM in Pipeline mode, activating the rising-edge-triggered Data Output Register.

DCD Pipelined Reads

The GS880E18/32/36T is a DCD (Dual Cycle Deselect) pipelined synchronous SRAM. SCD (Single Cycle Deselect) versions are also available. DCD SRAMs pipeline disable commands to the same degree as read commands. DCD RAMs hold the deselect command for one full cycle and then begin turning off their outputs just after the second rising edge of clock.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable ($\overline{BW}$) input combined with one or more individual byte write signals ($\overline{Bx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the byte write control inputs.

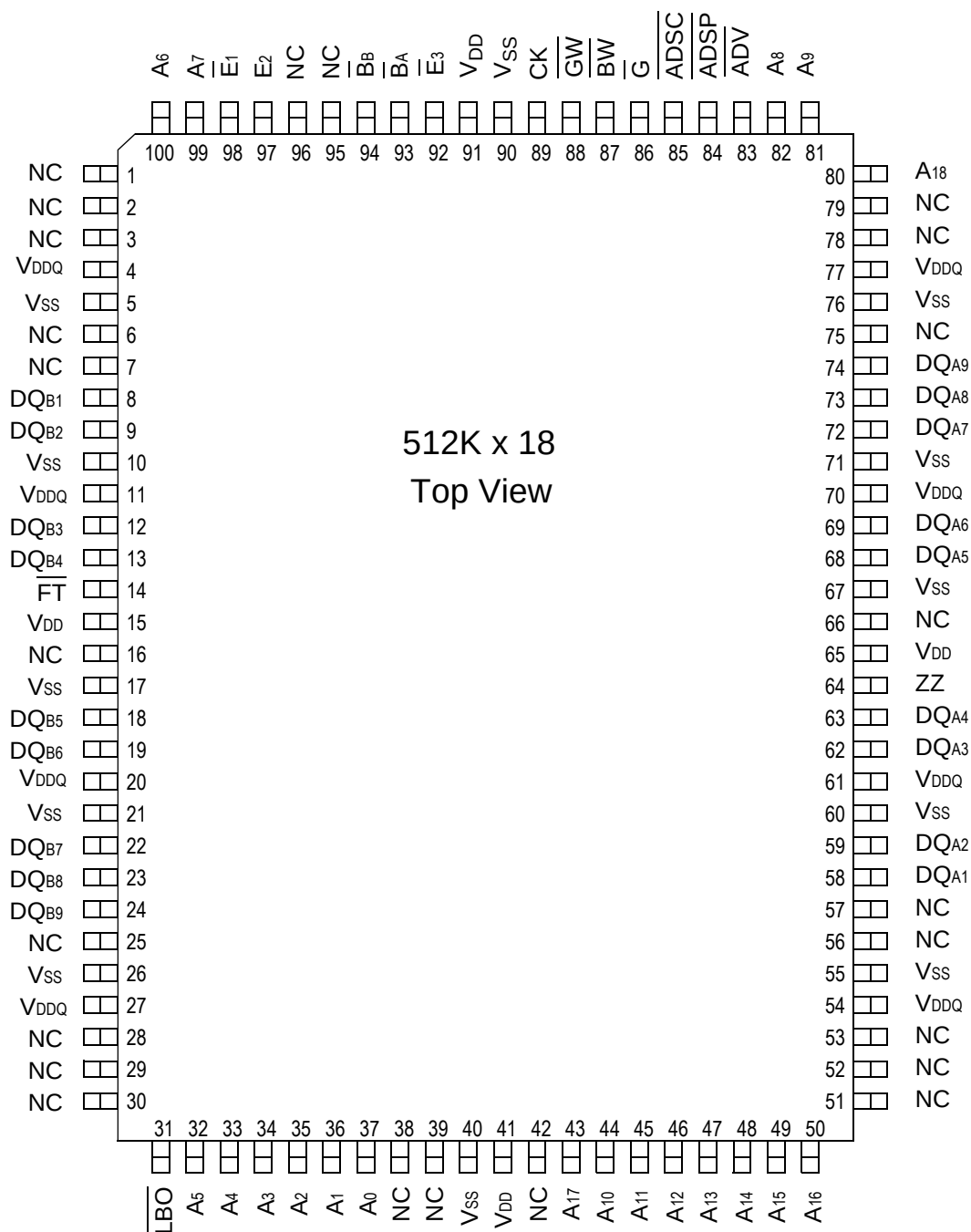
Sleep Mode

Low power (Sleep mode) is attained through the assertion (high) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

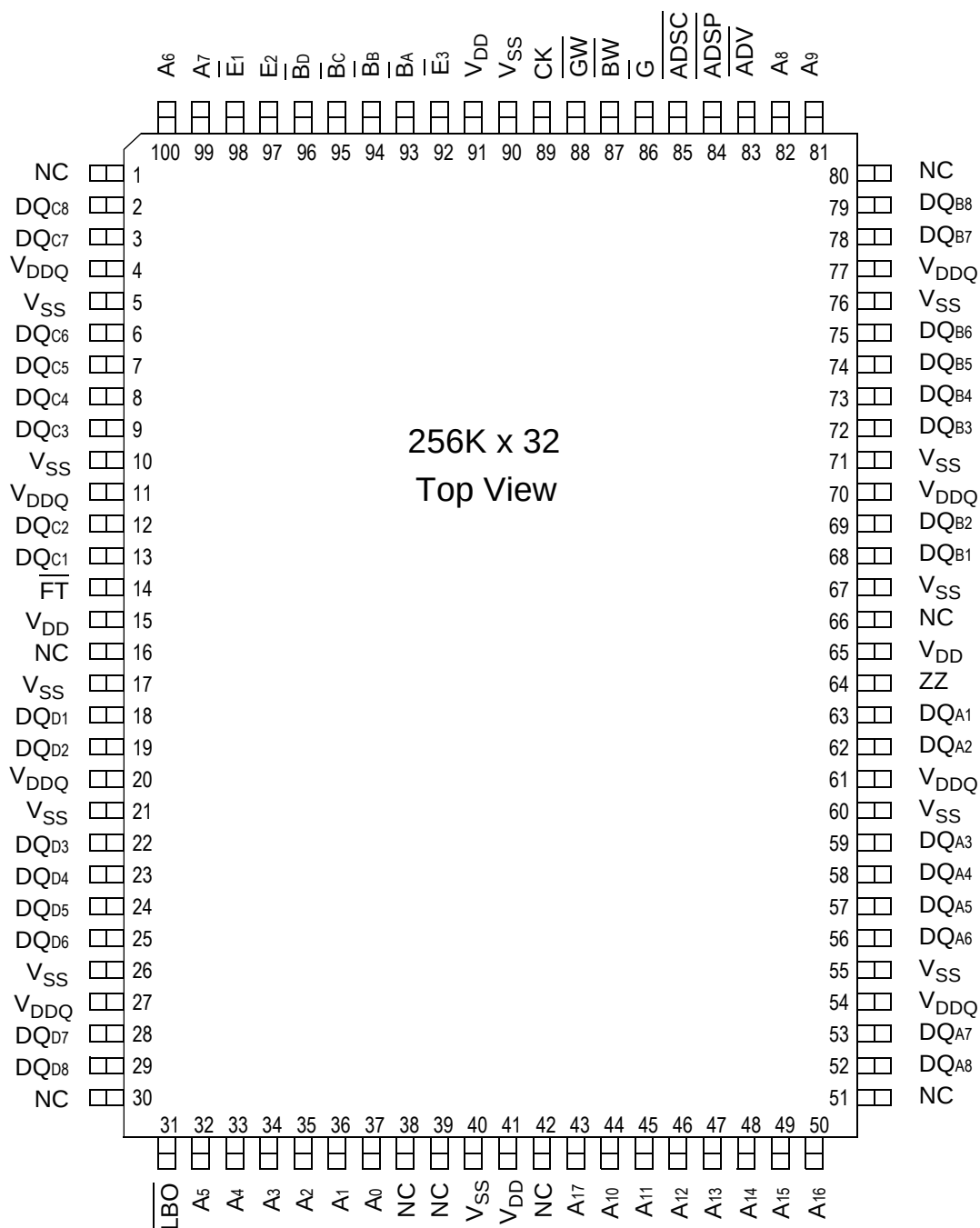
Core and Interface Voltages

The GS880E18/32/36T operates on a 3.3 V power supply, and all inputs/outputs are 3.3 V- and 2.5 V-compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuit.

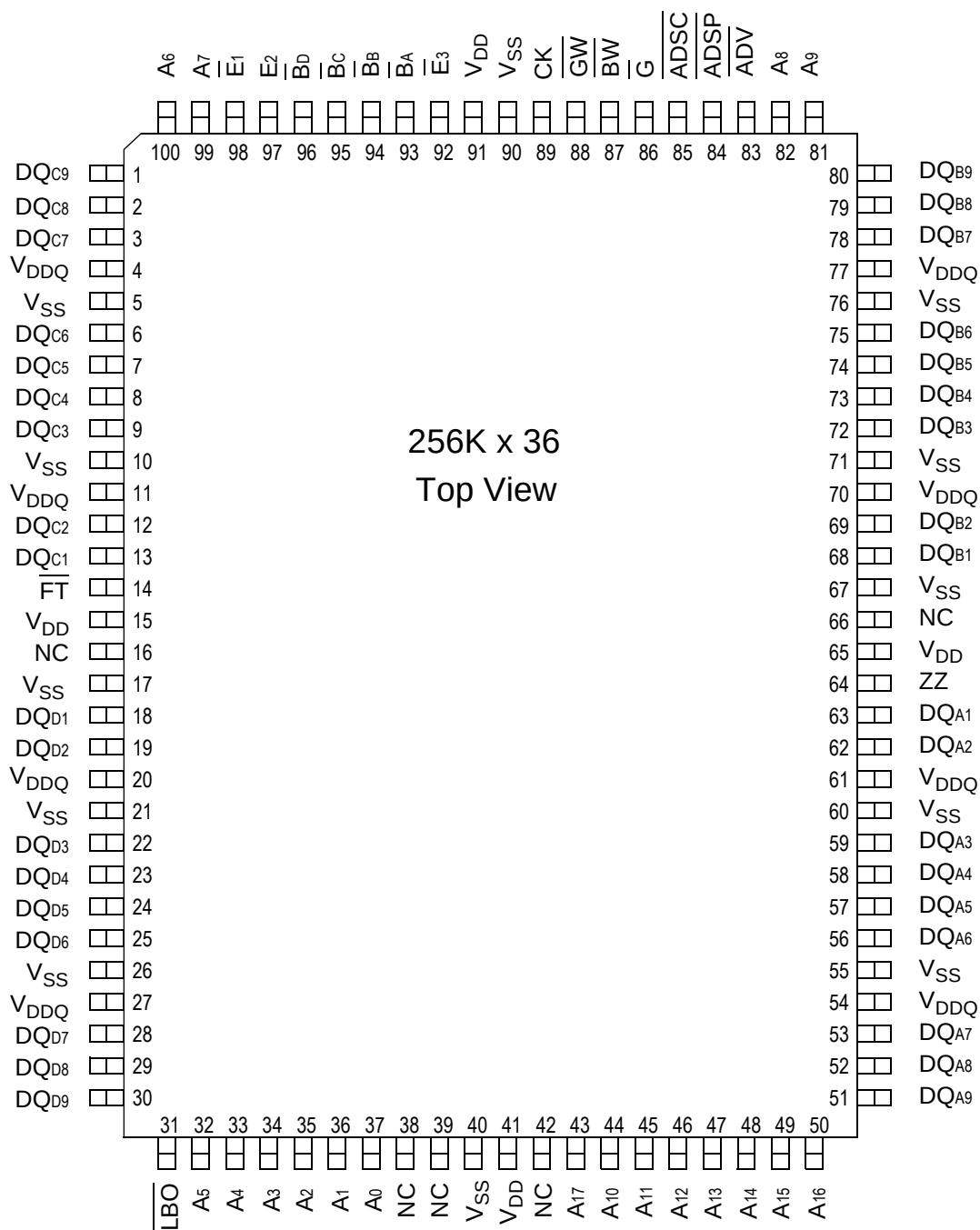
GS880E18 100-Pin TQFP Pinout



GS880E32 100-Pin TQFP Pinout



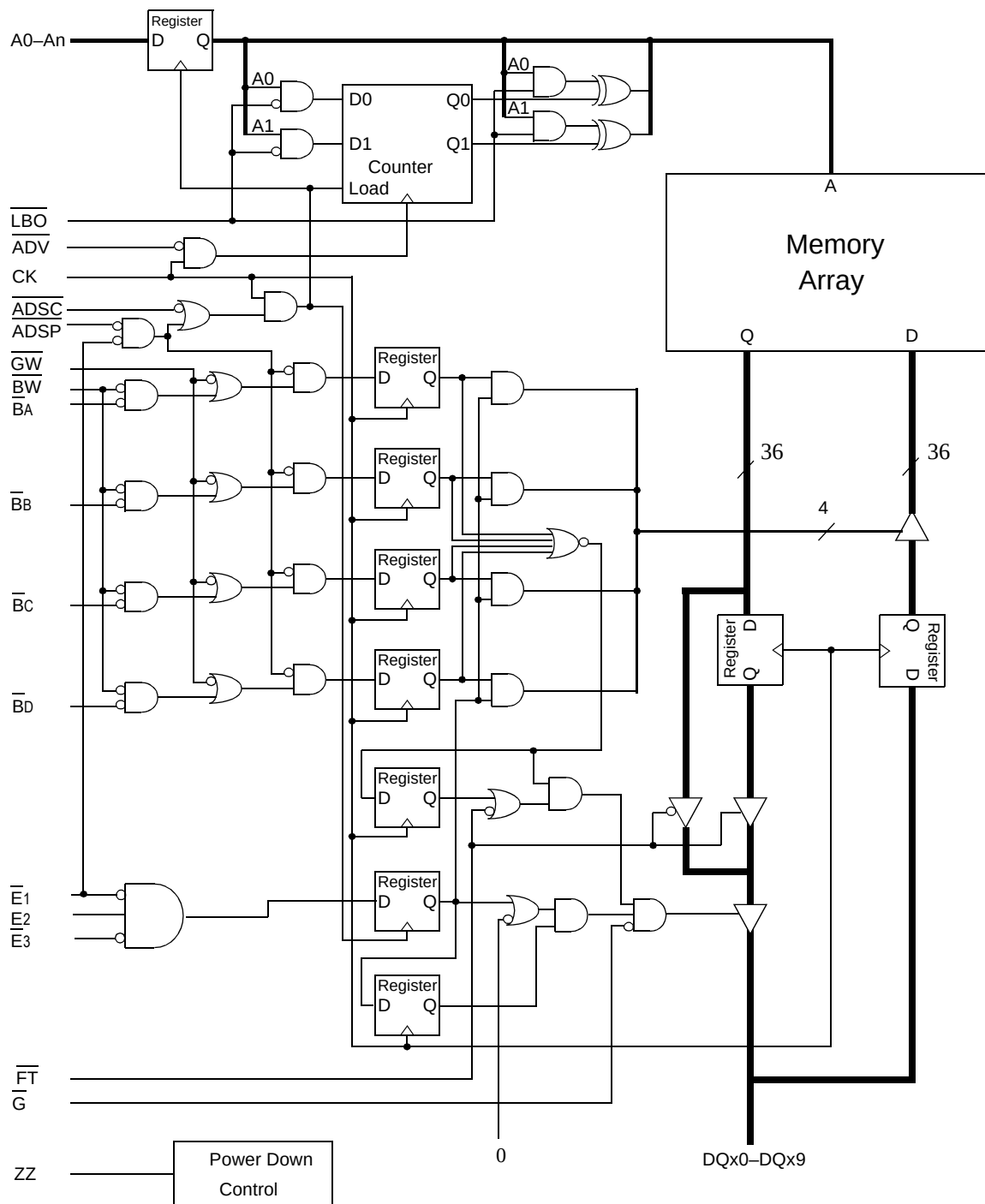
GS880E36 100-Pin TQFP Pinout



TQFP Pin Description

Pin Location	Symbol	Type	Description
37, 36	A ₀ , A ₁	I	Address field LSBs and Address Counter preset Inputs
35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 43	A ₂ –A ₁₇	I	Address Inputs
80	A ₁₈	I	Address Inputs
63, 62, 59, 58, 57, 56, 53, 52 68, 69, 72, 73, 74, 75, 78, 79 13, 12, 9, 8, 7, 6, 3, 2 18, 19, 22, 23, 24, 25, 28, 29	DQA ₁ –DQA ₈ DQB ₁ –DQB ₈ DQC ₁ –DQC ₈ DQD ₁ –DQD ₈	I/O	Data Input and Output pins (x32, x36 Version)
51, 80, 1, 30	DQA ₉ , DQB ₉ , DQC ₉ , DQD ₉	I/O	Data Input and Output pins
51, 80, 1, 30	NC	—	No Connect (x32 Version)
58, 59, 62, 63, 68, 69, 72, 73, 74 8, 9, 12, 13, 18, 19, 22, 23, 24	DQA ₁ –DQA ₉ DQB ₁ –DQB ₉	I/O	Data Input and Output pins
51, 52, 53, 56, 57 75, 78, 79, 1, 2, 3, 6, 7 25, 28, 29, 30	NC	—	No Connect
87	BW	I	Byte Write—Writes all enabled bytes; active low
93, 94	B _A , B _B	I	Byte Write Enable for DQA, DQB Data I/Os; active low
95, 96	B _C , B _D	I	Byte Write Enable for DQC, DQD Data I/Os; active low (x32, x36 Version)
95, 96	NC	—	No Connect (x18 Version)
89	CK	I	Clock Input Signal; active high
88	GW	I	Global Write Enable—Writes all bytes; active low
98, 92	E ₁ , E ₃	I	Chip Enable; active low
97	E ₂	I	Chip Enable; active high
86	G	I	Output Enable; active low
83	ADV	I	Burst address counter advance enable; active low
84, 85	ADSP, ADSC	I	Address Strobe (Processor, Cache Controller); active low
64	ZZ	I	Sleep mode control; active high
14	FT	I	Flow Through or Pipeline mode; active low
31	LBO	I	Linear Burst Order mode; active low
15, 41, 65, 91	V _{DD}	I	Core power supply
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V _{SS}	I	I/O and Core Ground
4, 11, 20, 27, 54, 61, 70, 77	V _{DDQ}	I	Output driver power supply
16, 38, 39, 42, 66	NC	—	No Connect.

GS880E32 Block Diagram



Note: Only x36 version shown for simplicity.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{\text{LBO}}$	L	Linear Burst
		H or NC	Interleaved Burst
Output Register Control	$\overline{\text{FT}}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:

There are pull-up devices on the $\overline{\text{LBO}}$ and $\overline{\text{FT}}$ pins and a pull down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above table.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note: The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note: The burst counter wraps to initial state on the 5th clock.

BPR 1999.05.18

Byte Write Truth Table

Function	$\overline{\text{GW}}$	$\overline{\text{BW}}$	$\overline{\text{B}}_A$	$\overline{\text{B}}_B$	$\overline{\text{B}}_C$	$\overline{\text{B}}_D$	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

Notes:

1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs $\overline{\text{B}}_A$, $\overline{\text{B}}_B$, $\overline{\text{B}}_C$, and/or $\overline{\text{B}}_D$ may be used in any combination with BW to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "c" and "d" are only available on the x32 and x36 versions.

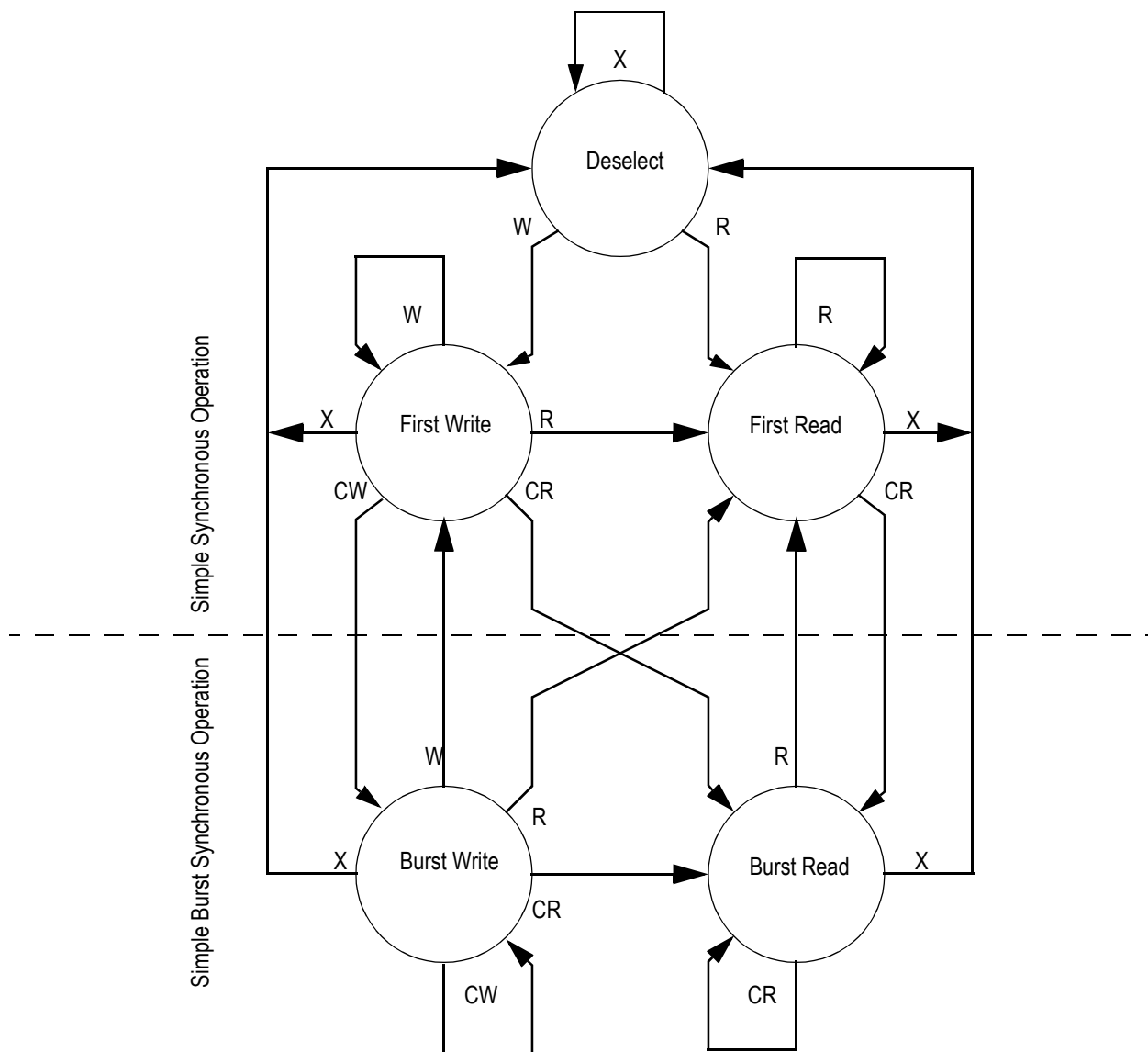
Synchronous Truth Table

Operation	Address Used	State Diagram Key ⁵	$\overline{E1}$	$E2^2$ (x36only)	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	W^3	DQ^4
Deselect Cycle, Power Down	None	X	H	X	X	L	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	F	L	X	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	F	H	L	X	X	High-Z
Read Cycle, Begin Burst	External	R	L	T	L	X	X	X	Q
Read Cycle, Begin Burst	External	R	L	T	H	L	X	F	Q
Write Cycle, Begin Burst	External	W	L	T	H	L	X	T	D
<i>Read Cycle, Continue Burst</i>	<i>Next</i>	<i>CR</i>	X	X	H	H	L	F	Q
Read Cycle, Continue Burst	Next	CR	H	X	X	H	L	F	Q
<i>Write Cycle, Continue Burst</i>	<i>Next</i>	<i>CW</i>	X	X	H	H	L	T	D
Write Cycle, Continue Burst	Next	CW	H	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	H	H	T	D

Notes:

1. X = Don't Care, H = High, L = Low.
2. For x36 Version, E = T (True) if $E2 = 1$ and $\overline{E3} = 0$; E = F (False) if $E2 = 0$ or $\overline{E3} = 1$.
3. $\overline{W} = T$ (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. $\overline{G}$ is an asynchronous input. $\overline{G}$ can be driven high at any time to disable active output drivers. $\overline{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying $\overline{ADSP}$ high and $\overline{ADSC}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying $\overline{ADSP}$ high and $\overline{ADV}$ low while using $\overline{ADSC}$ to load new addresses allows simple burst operations. See *ITALIC* items above.

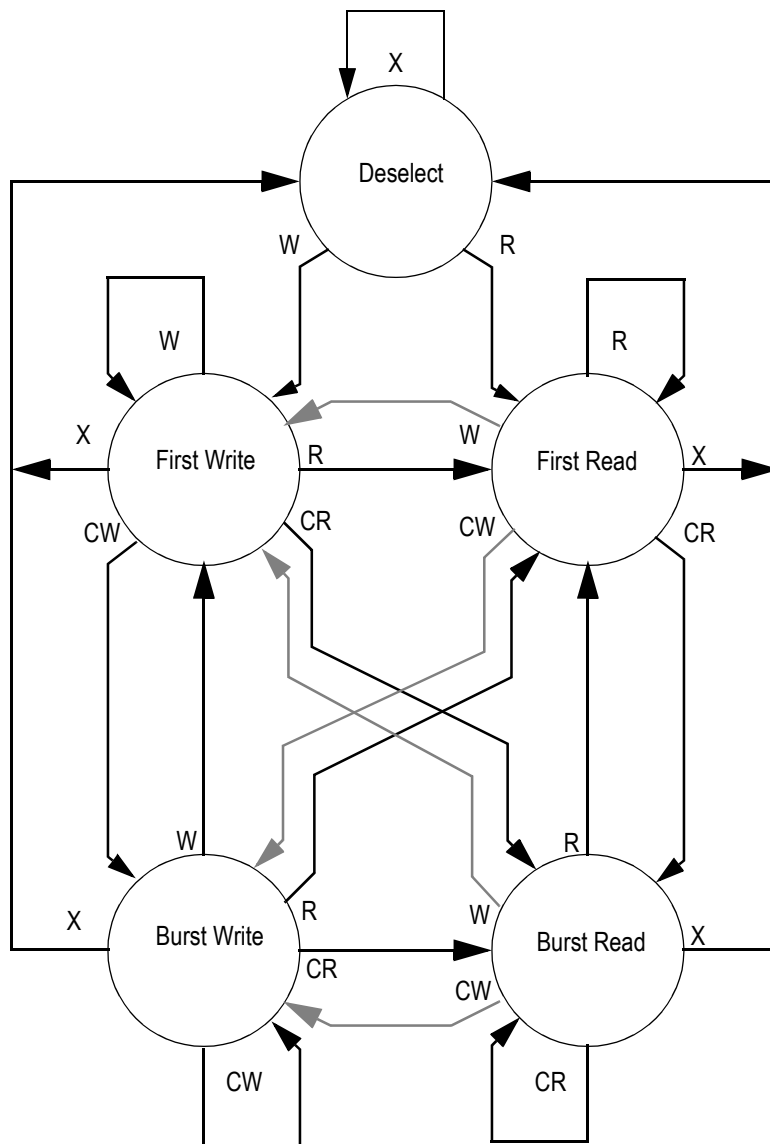
Simplified State Diagram



Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{E1}$, $\overline{E2}$, and $\overline{E3}$) and Write ($\overline{BA}$, $\overline{BB}$, $\overline{BC}$, $\overline{BD}$, $\overline{BW}$, and $\overline{GW}$) control inputs, and that $\overline{ADSP}$ is tied high and $\overline{ADSC}$ is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and $\overline{ADSC}$ control inputs, and assumes $\overline{ADSP}$ is tied high and $\overline{ADV}$ is tied low.

Simplified State Diagram with $\overline{G}$



Notes:

1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of "Dummy Reads" (Read Cycles with $\overline{G}$ High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal Read cycles.
3. Transitions shown in grey tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	-0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	-0.5 to V_{DD}	V
V_{CK}	Voltage on Clock Input Pin	-0.5 to 6	V
$V_{I/O}$	Voltage on I/O Pins	-0.5 to $V_{DDQ} + 0.5$ (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	-0.5 to $V_{DD} + 0.5$ (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/-20	mA
I_{OUT}	Output Current on Any I/O Pin	+/-20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	-55 to 125	°C
T_{BIAS}	Temperature Under Bias	-55 to 125	°C

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

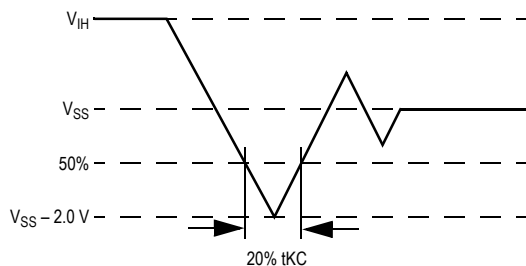
Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	3.135	3.3	3.6	V	
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V	1
Input High Voltage	V_{IH}	1.7	—	$V_{DD} + 0.3$	V	2
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	2
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	3
Ambient Temperature (Industrial Range Versions)	T_A	-40	25	85	°C	3

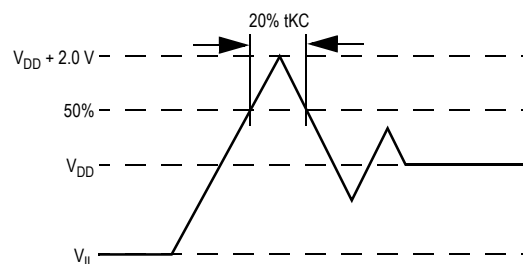
Notes:

- Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both $2.75 \text{ V} \leq V_{DDQ} \leq 2.375 \text{ V}$ (i.e., 2.5 V I/O) and $3.6 \text{ V} \leq V_{DDQ} \leq 3.135 \text{ V}$ (i.e., 3.3 V I/O), and quoted at whichever condition is worst case.
- This device features input buffers compatible with both 3.3 V and 2.5 V I/O drivers.
- Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
- Input Under/overshoot voltage must be $-2 \text{ V} > V_i < V_{DD} + 2 \text{ V}$ with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 3.3\text{ V}$)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0\text{ V}$	4	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0\text{ V}$	6	7	pF

Note: These parameters are sample tested.

Package Thermal Characteristics

Rating	Layer Board	Symbol	Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\theta JA}$	40	$^\circ\text{C/W}$	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\theta JA}$	24	$^\circ\text{C/W}$	1,2
Junction to Case (TOP)	—	$R_{\theta JC}$	9	$^\circ\text{C/W}$	3

Notes:

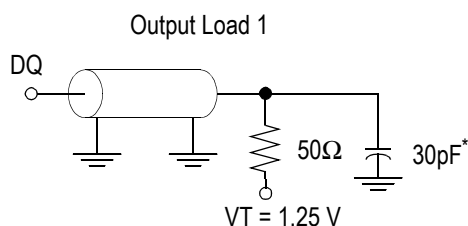
- Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
- SCMI G-38-87
- Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1

AC Test Conditions

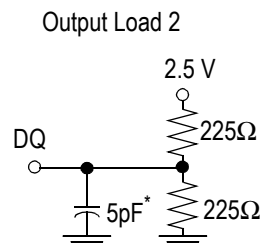
Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V
Output load	Fig. 1 & 2

Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
3. Output Load 2 for t_{LZ} , t_{HZ} , t_{OLZ} and t_{OHZ}
4. Device is deselected as defined by the Truth Table.



* Distributed Test Jig Capacitance



DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	$V_{IN} = 0 \text{ to } V_{DD}$	-1 μA	1 μA
ZZ Input Current	I_{INZZ}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0 \text{ V} \leq V_{IN} \leq V_{IH}$	-1 μA -1 μA	1 μA 300 μA
Mode Pin Input Current	I_{INM}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0 \text{ V} \leq V_{IN} \leq V_{IL}$	-300 μA -1 μA	1 μA 1 μA
Output Leakage Current	I_{OL}	Output Disable, $V_{OUT} = 0 \text{ to } V_{DD}$	-1 μA	1 μA
Output High Voltage	V_{OH}	$I_{OH} = -8 \text{ mA}$, $V_{DDQ} = 2.375 \text{ V}$	1.7 V	—
Output High Voltage	V_{OH}	$I_{OH} = -8 \text{ mA}$, $V_{DDQ} = 3.135 \text{ V}$	2.4 V	—
Output Low Voltage	V_{OL}	$I_{OL} = 8 \text{ mA}$	—	0.4 V

Operating Currents

Parameter	Test Conditions	Symbol	-11		-11.5		-100		-80		-66		Unit
			0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	
Operating Current	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	I_{DD} Pipeline	225	235	225	235	225	235	200	210	185	195	mA
		I_{DD} Flow-Thru	180	190	180	190	180	190	175	185	165	175	mA
Standby Current	$ZZ \geq V_{DD} - 0.2V$	I_{SB} Pipeline	30	40	30	40	30	40	30	40	30	40	mA
		I_{SB} Flow-Thru	30	40	30	40	30	40	30	40	30	40	mA
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	I_{DD} Pipeline	80	90	80	90	80	90	70	80	60	70	mA
		I_{DD} Flow-Thru	65	75	65	75	65	75	55	65	50	60	mA

AC Electrical Characteristics

	Parameter	Symbol	-11		-11.5		-100		-80		-66		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	t _{KC}	10	—	10	—	10	—	12.5	—	15	—	ns
	Clock to Output Valid	t _{KQ}	—	4.0	—	4.0	—	4.0	—	4.5	—	5	ns
	Clock to Output Invalid	t _{KQX}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	t _{LZ} ¹	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Flow-Thru	Clock Cycle Time	t _{KC}	15.0	—	15.0	—	15.0	—	15.0	—	20	—	ns
	Clock to Output Valid	t _{KQ}	—	11.0	—	11.5	—	12.0	—	14.0	—	18	ns
	Clock to Output Invalid	t _{KQX}	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	t _{LZ} ¹	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock HIGH Time	t _{KH}	1.7	—	1.7	—	2	—	2	—	2.3	—	ns
	Clock LOW Time	t _{KL}	2	—	2	—	2.2	—	2.2	—	2.5	—	ns
	Clock to Output in High-Z	t _{HZ} ¹	1.5	4.0	1.5	4.2	1.5	4.5	1.5	4.5	1.5	4.8	ns
	G to Output Valid	t _{OE}	—	4.0	—	4.2	—	4.5	—	4.5	—	4.8	ns
	G to output in Low-Z	t _{OLZ} ¹	0	—	0	—	0	—	0	—	0	—	ns
	G to output in High-Z	t _{OHZ} ¹	—	4.0	—	4.2	—	4.5	—	4.5	—	4.8	ns
	Setup time	t _S	1.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
	Hold time	t _H	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	ZZ setup time	t _{ZZS} ²	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	t _{ZZH} ²	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	t _{ZZR}	20	—	20	—	20	—	20	—	20	—	ns

Notes:

- These parameters are sampled and are not 100% tested.
- ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

The diagram illustrates the timing relationships between various signals during three operational phases: Single Write, Burst Write, and Deselected. The signals shown are CK (clock), ADSP, ADSC, ADV, A0–An (address), GW (write enable), BW (write enable), BA–BD (bank address), E1, E2, E3 (chip selects), G (global enable), and DQA–DQD (data bus).

Single Write Phase: Shows a single write operation. Key timing parameters include t_S (setup time) and t_H (hold time) for ADSP, ADSC, ADV, and the address signals (A0–An, BA–BD, E1, E2, E3). The data bus (DQA–DQD) is shown in a high-impedance (Hi-Z) state before the write.

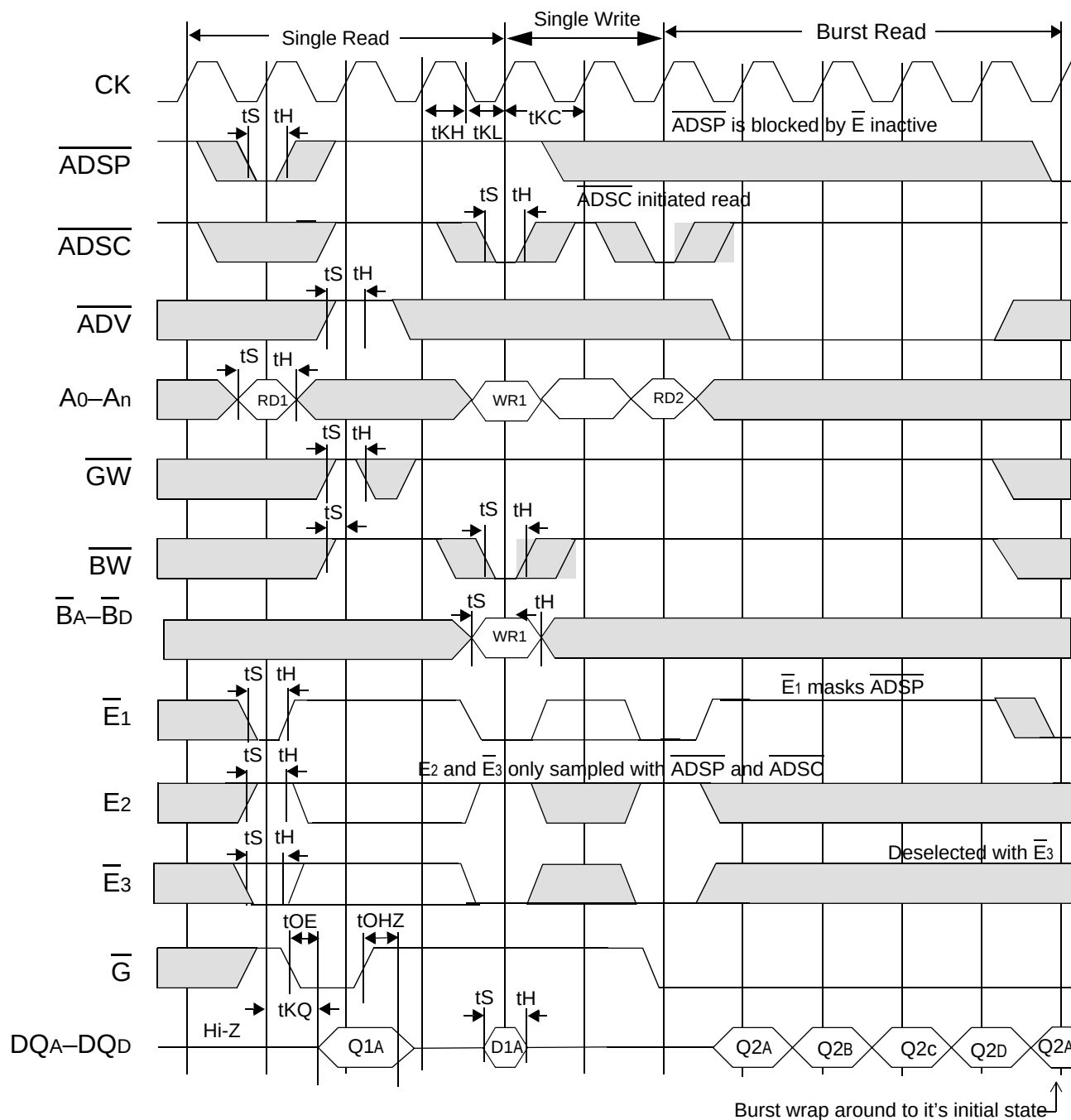
Burst Write Phase: Shows a burst of write operations. Key timing parameters include t_{KH} (clock-to-ADSP hold time), t_{KL} (ADSP-to-clock setup time), and t_{KC} (ADSP-to-clock setup time). The data bus is shown with multiple data bytes (D1A, D2A, D2B, D2C, D2D, D3A) being written.

Deselected Phase: Shows the state of the signals when the device is deselected. The data bus is shown in a high-impedance (Hi-Z) state.

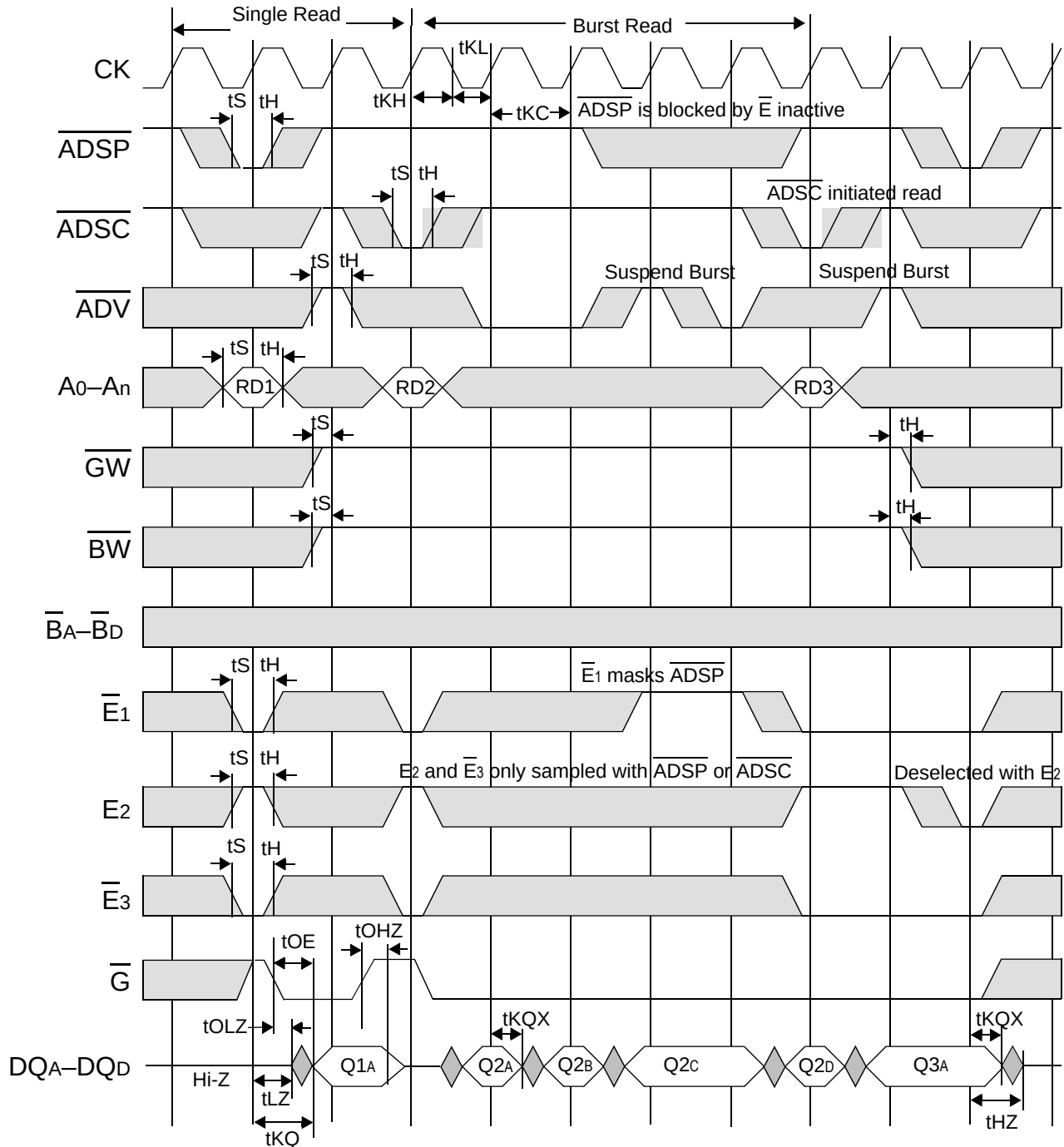
Annotations:

- ADSP is blocked by $\bar{E}$ inactive
- ADSC initiated write
- ADV must be inactive for ADSP Write
- $\bar{E}_1$ masks ADSP
- Deselected with E2
- E2 and $\bar{E}_3$ only sampled with ADSP or ADSC
- Write specified byte for 2A and all bytes for 2B, 2C & 2D

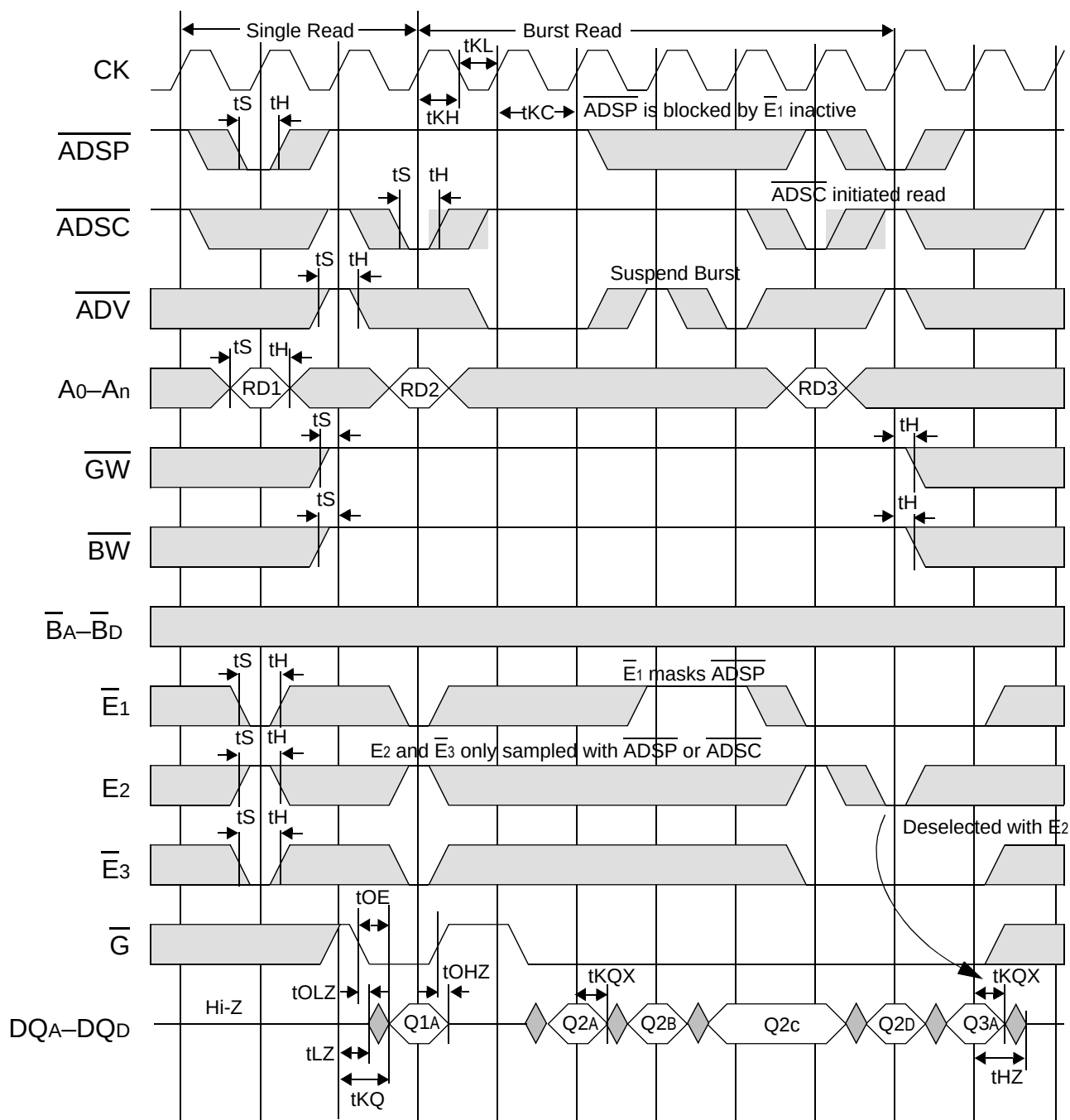
Flow Through Read-Write Cycle Timing



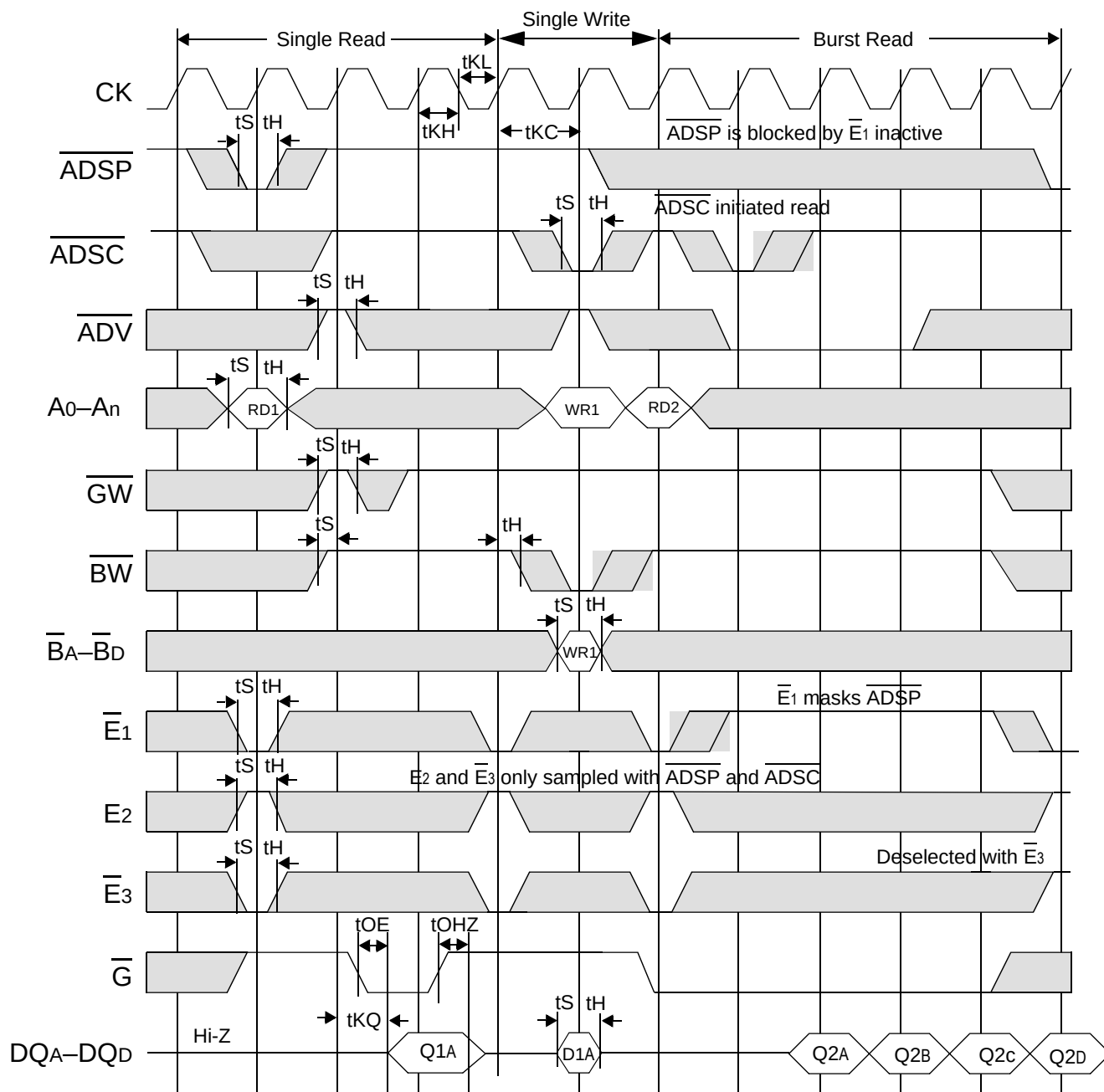
Flow Through Read Cycle Timing



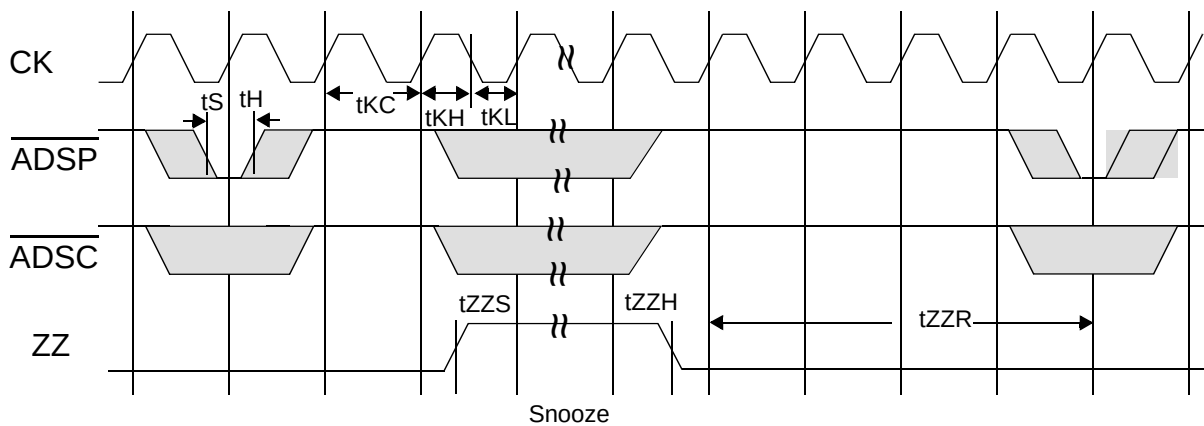
Pipelined DCD Read Cycle Timing



Pipelined DCD Read-Write Cycle Timing



Sleep Mode Timing Diagram

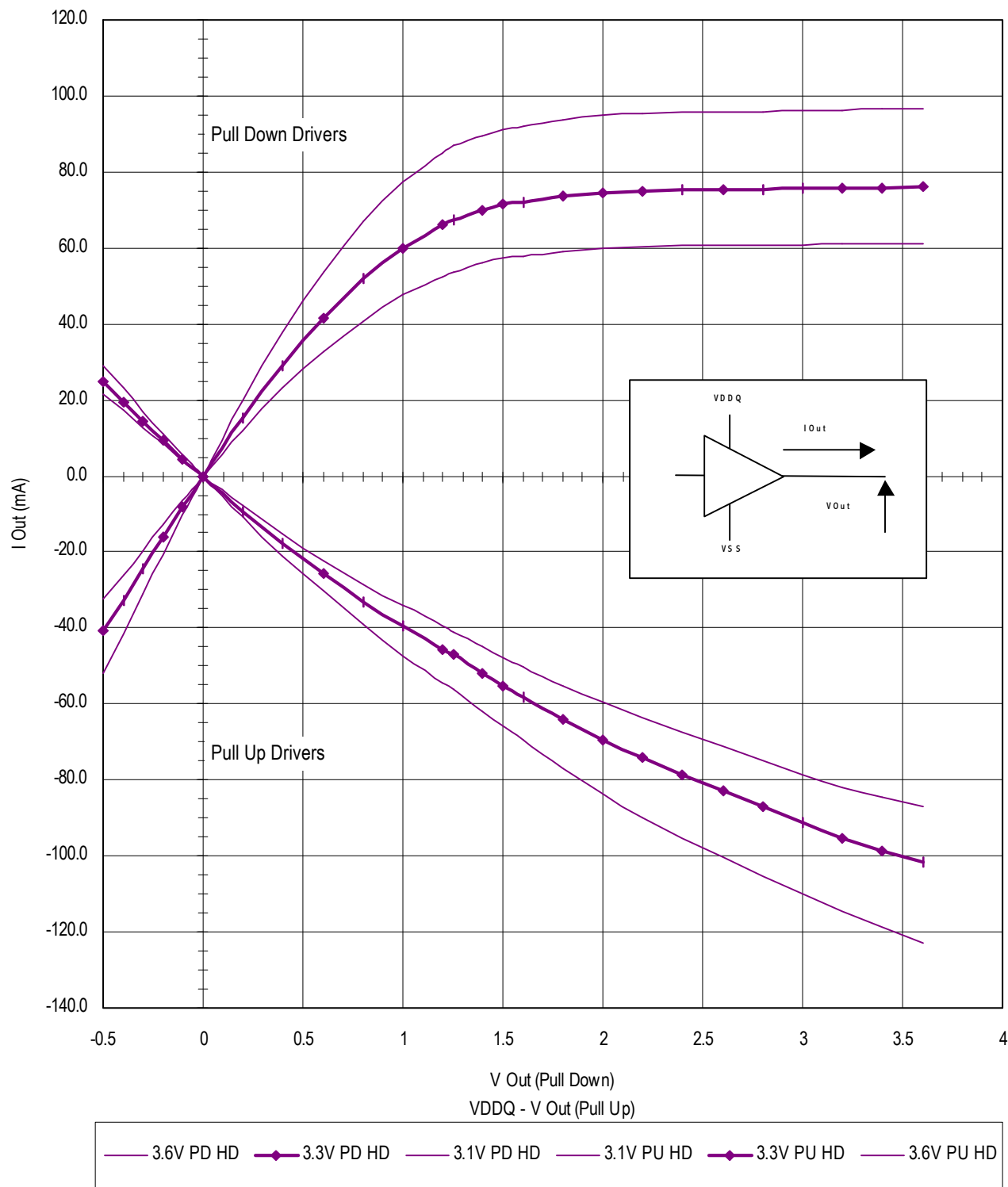


Application Tips

Single and Dual Cycle Deselect

SCD devices force the use of "dummy read cycles" (read cycles that are launched normally but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings) but greater care must be exercised to avoid excessive bus contention.

Output Driver Characteristics

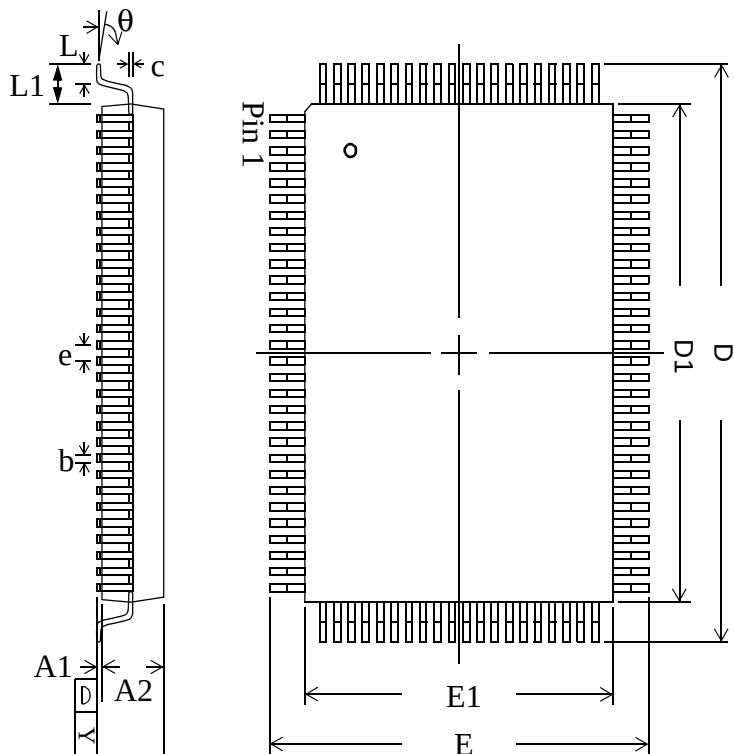


TQFP Package Drawing

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity	—	—	0.10
θ	Lead Angle	0°	—	7°

Notes:

1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.



BPR 1999.05.18

Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number ¹	Type	Package	Speed ² (MHz/ns)	T _A ³	Status
514K x 18	GS880E18T-11	DCD Pipeline/Flow Through	TQFP	100/11	C	
514K x 18	GS880E18T-11.5	DCD Pipeline/Flow Through	TQFP	100/11.5	C	
514K x 18	GS880E18T-100	DCD Pipeline/Flow Through	TQFP	100/12	C	
514K x 18	GS880E18T-80	DCD Pipeline/Flow Through	TQFP	80/14	C	
514K x 18	GS880E18T-66	DCD Pipeline/Flow Through	TQFP	66/18	C	
256K x 32	GS880E32T-11	DCD Pipeline/Flow Through	TQFP	100/11	C	
256K x 32	GS880E32T-11.5	DCD Pipeline/Flow Through	TQFP	100/11.5	C	
256K x 32	GS880E32T-100	DCD Pipeline/Flow Through	TQFP	100/12	C	
256K x 32	GS880E32T-80	DCD Pipeline/Flow Through	TQFP	80/14	C	
256K x 32	GS880E32T-66	DCD Pipeline/Flow Through	TQFP	66/18	C	
256K x 36	GS880E36T-11	DCD Pipeline/Flow Through	TQFP	100/11	C	
256K x 36	GS880E36T-11.5	DCD Pipeline/Flow Through	TQFP	100/11.5	C	
256K x 36	GS880E36T-100	DCD Pipeline/Flow Through	TQFP	100/12	C	
256K x 36	GS880E36T-80	DCD Pipeline/Flow Through	TQFP	80/14	C	
256K x 36	GS880E36T-66	DCD Pipeline/Flow Through	TQFP	66/18	C	
514K x 18	GS880E18T-11I	DCD Pipeline/Flow Through	TQFP	100/11	I	
514K x 18	GS880E18T-11.5I	DCD Pipeline/Flow Through	TQFP	100/11.5	I	
514K x 18	GS880E18T-100I	DCD Pipeline/Flow Through	TQFP	100/12	I	
514K x 18	GS880E18T-80I	DCD Pipeline/Flow Through	TQFP	80/14	I	
514K x 18	GS880E18T-66I	DCD Pipeline/Flow Through	TQFP	66/18	I	
256K x 32	GS880E32T-11I	DCD Pipeline/Flow Through	TQFP	100/11	I	
256K x 32	GS880E32T-11.5I	DCD Pipeline/Flow Through	TQFP	100/11.5	I	
256K x 32	GS880E32T-100I	DCD Pipeline/Flow Through	TQFP	100/12	I	
256K x 32	GS880E32T-80I	DCD Pipeline/Flow Through	TQFP	80/14	I	
256K x 32	GS880E32T-66I	DCD Pipeline/Flow Through	TQFP	66/18	I	
256K x 36	GS880E36T-11I	DCD Pipeline/Flow Through	TQFP	100/11	I	
256K x 36	GS880E36T-11.5I	DCD Pipeline/Flow Through	TQFP	100/11.5	I	
256K x 36	GS880E36T-100I	DCD Pipeline/Flow Through	TQFP	100/12	I	
256K x 36	GS880E36T-80I	DCD Pipeline/Flow Through	TQFP	80/14	I	
256K x 36	GS880E36T-66I	DCD Pipeline/Flow Through	TQFP	66/18	I	

Notes:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS880E18TT.
- The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
- T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
- GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsistechnology.com) for a complete listing of current offerings.

Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
GS880E18/32/36T Rev1.04h 5/1999; 1.05 9/1999I	Format/Typos	• Last Page/Fixed “GSGS..” in Ordering Information Note. • Formatted Pin Outs and Pin Description to new small caps. • Formatted Block diagrams to new small caps. • Formatted Timing Diagrams to new small caps. • Changed “Flow thru” to “Flow Through” in Timing Diagrams. • Package Diagram/Changed “Dimesion” to “Dimension”.
	Content	• 5/Fixed pin description table to match pinouts. • Pin Description/Changed chip enables to match pins. • Pin Description/Changed pin 80 from NC to Address Input. • Pin Description/Rearranged Address Inputs to match order of Pinout • Package Diagram/Changed Dimension D Max from 20.1 to 22.1
GS880E18/32/36T 1.05 11/ 1999K 880E18/32/36T 1.06 1/ 2000L	Content	• Changed Flow Through Read-Write Cycle Timing Diagram for accuracy. • Changed order of TQFP Address Inputs to match pinout. • Changed order of TQFP DATA Input and Output pins to match pinout. • New GSI Logo.
GS880E18/32/36T1.06 1/ 2000L; GS880E18/32/36T1.07 3/ 2000N;	Content	• Changed all speed bin information (headings, references, tables, ordering info..) to reflect 150 - 80Mhz
GS880E18/32/36T1.07 3/ 2000N; GS880E18/32/36T1.08 3/ 2000O;	Content	• Corrections to AC Electrical Characteristics Table -
GS880E18/32/36T1.08 3/ 2000O; 880E183236_r1_09	Content/Format	• Removed 150 MHz speed bin • Changed 133 MHz and 117 MHz speed bins to 11 ns and 11.5 ns (100 MHz) numbers • Updated format to comply with Technical Publications standards
880E18_r1_09; 880E18_r1_10	Content	• Updated Capitanace table—removed Input row and changed Output row to I/O
880E18_r1_10; 880E18_r1_11	Content	• Corrected typo in AC Electrical Characteristics table