# Intelligent Power Module (IPM)
# 1200 V, 10 A

*Advance Information*

# NFAM1012L5BT

The NFAM1012L5BT is a fully−integrated inverter power module consisting of an independent High side gate driver, LVIC, six IGBT's and a temperature sensor (TSU by LVIC and NTC Thermistor), suitable for driving permanent magnet synchronous (PMSM) motors, brushless DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a three−phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm.

The power stage has under−voltage lockout protection (UVP). Internal boost diodes are provided for high side gate boost drive.

### Features

- Three−phase 1200 V, 10 A IGBT Module with Independent Drivers
- Active Logic Interface
- Built−in Under−voltage Protection (UVP)
- Integrated Bootstrap Diodes and Resistors
- Separate Low−side IGBT Emitter Connections for Individual Current Sensing of Each Phase
- Temperature Sensor (TSU Output by LVIC or NTC Thermistor)
- UL Certification: E339285
- This is a Pb−Free Device

### Typical Application

- Industrial Drives
- Industrial Pumps
- Industrial Fans
- Industrial Automation

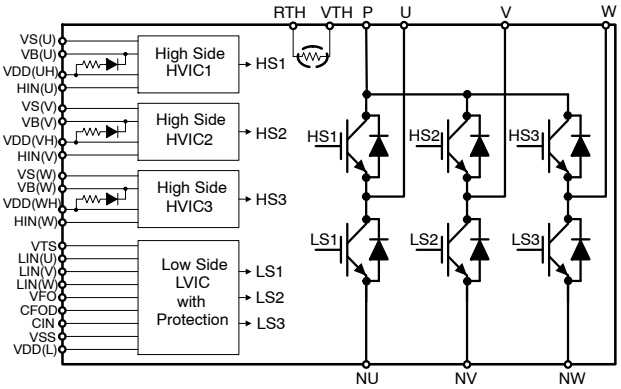
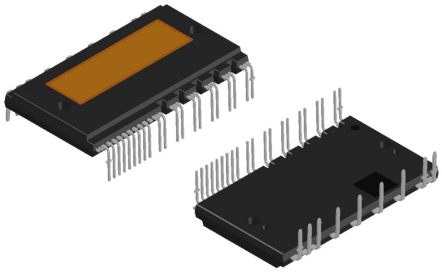



**Figure 1. Application Schematic**

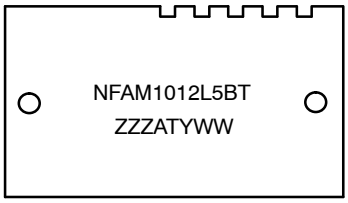
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**CASE MODGC**
**MINI DIP39, 31.0x54.5**

### MARKING DIAGRAM




NFAM1012L5BT = Specific Device Code
ZZZ = Assembly Lot Code
A = Assembly Location
T = Test Location
Y = Year
WW = Work Week
Device marking is on package top side

### ORDERING INFORMATION

| Device | Package | Shipping† (Qty / Packing) |
|---|---|---|
| NFAM1012L5BT | DIP39, 31.0x54.5 (Pb−Free) | 90 / BOX |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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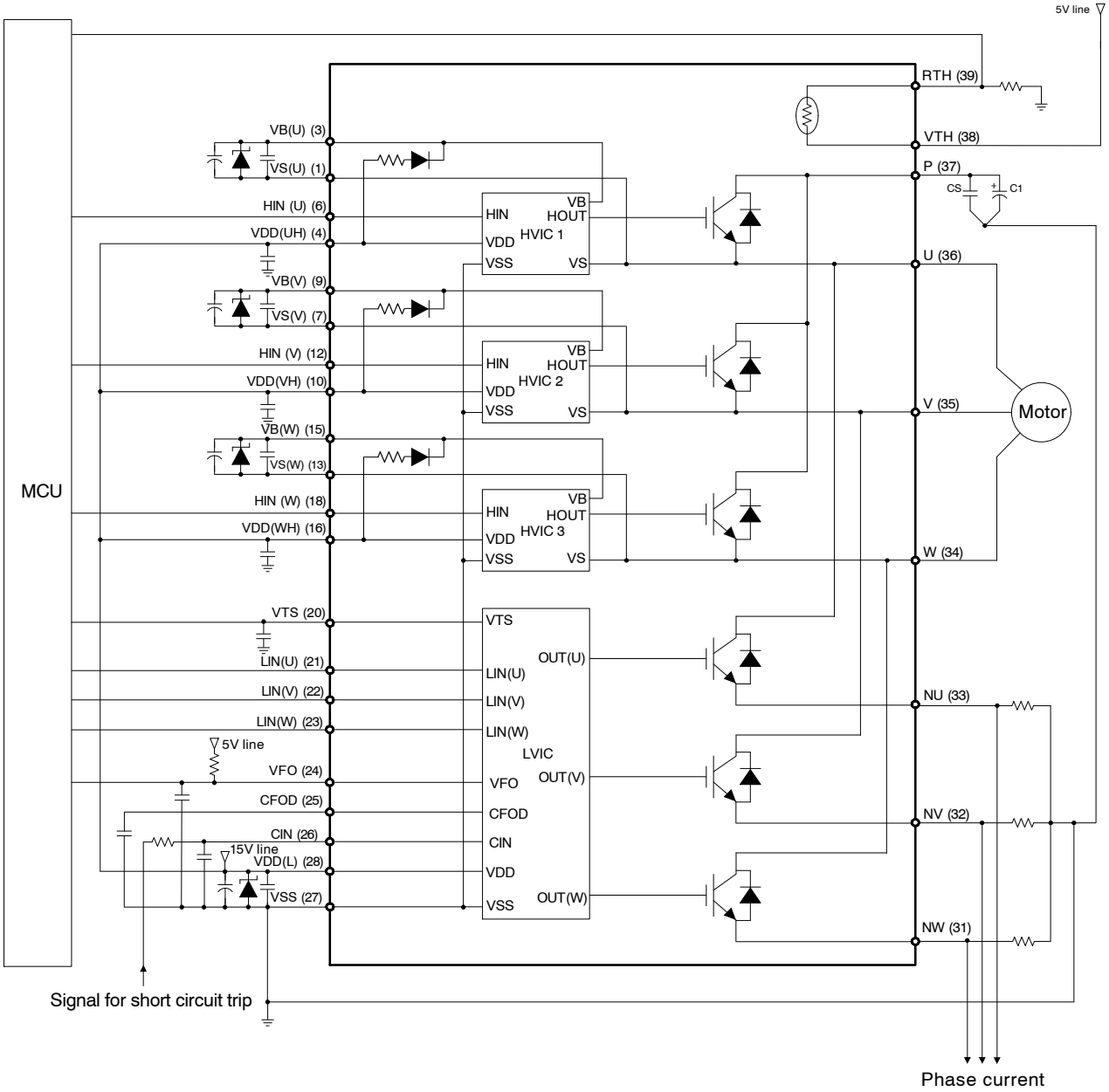



**Figure 2. Application Schematic – Adjustable Option**

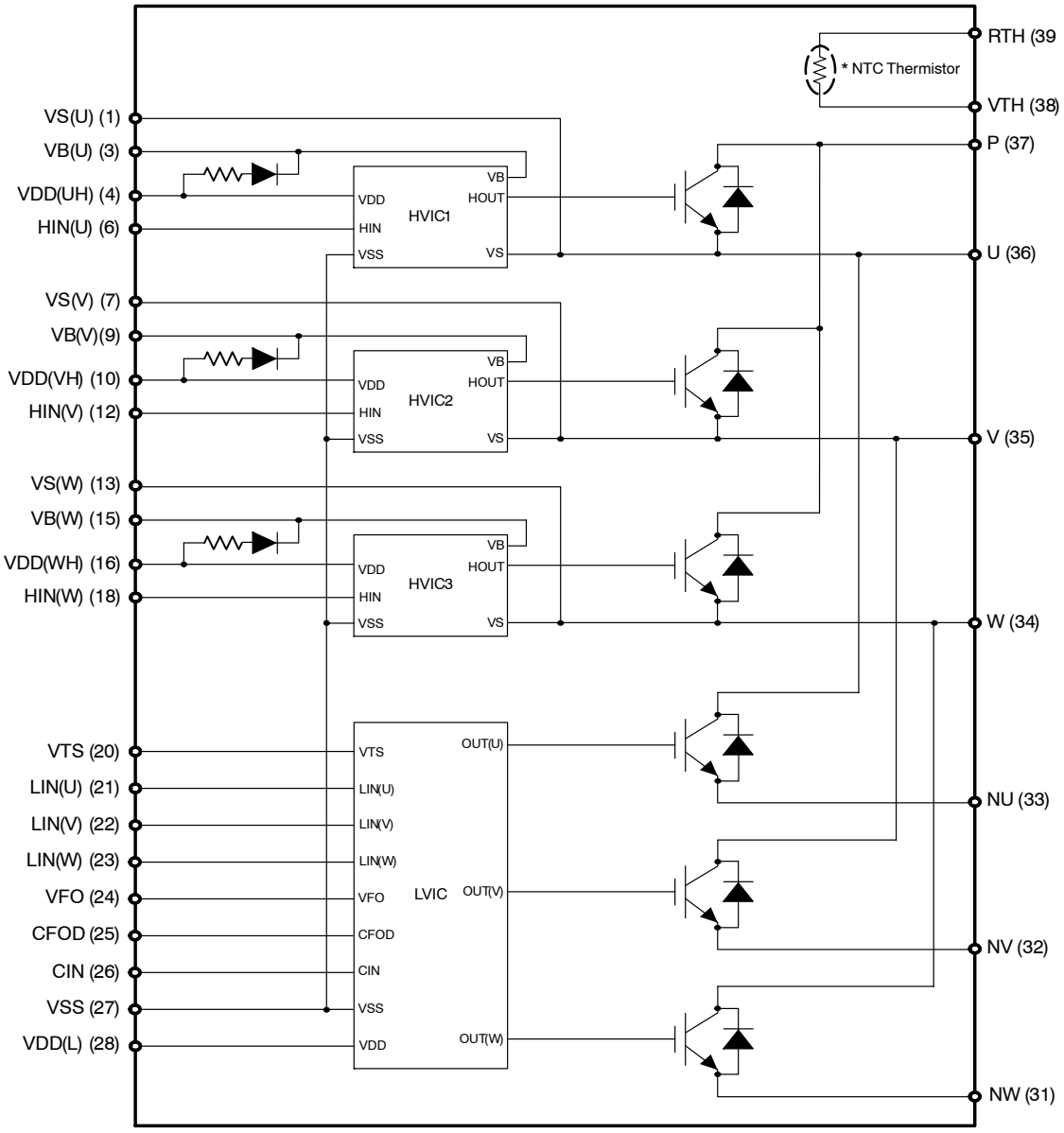



**Figure 3. Equivalent Block Diagram**

**Table 1. PIN FUNCTION DESCRIPTION**

| Pin | Name | Description |
|---|---|---|
| 1 | VS(U) | High−Side Bias Voltage GND for U Phase IGBT Driving |
| (2) | − | Dummy |
| 3 | VB(U) | High−Side Bias Voltage for U Phase IGBT Driving |
| 4 | VDD(UH) | High−Side Bias Voltage for U Phase IC |
| (5) | − | Dummy |
| 6 | HIN(U) | Signal Input for High−Side U Phase |
| 7 | VS(V) | High−Side Bias Voltage GND for V Phase IGBT Driving |
| (8) | − | Dummy |
| 9 | VB(V) | High−Side Bias Voltage for V Phase IGBT Driving |
| 10 | VDD(VH) | High−Side Bias Voltage for V Phase IC |
| (11) | − | Dummy |
| 12 | HIN(V) | Signal Input for High−Side V Phase |
| 13 | VS(W) | High−Side Bias Voltage GND for W Phase IGBT Driving |
| (14) | − | Dummy |
| 15 | VB(W) | High−Side Bias Voltage for W Phase IGBT Driving |
| 16 | VDD(WH) | High−Side Bias Voltage for W Phase IC |
| (17) | − | Dummy |
| 18 | HIN(W) | Signal Input for High−Side W Phase |
| (19) | − | Dummy |
| 20 | VTS | Voltage Output for LVIC Temperature Sensing Unit |
| 21 | LIN(U) | Signal Input for Low−Side U Phase |
| 22 | LIN(V) | Signal Input for Low−Side V Phase |
| 23 | LIN(W) | Signal Input for Low−Side W Phase |
| 24 | VFO | Fault Output |
| 25 | CFOD | Capacitor for Fault Output Duration Selection |
| 26 | CIN | Input for Current Protection |
| 27 | VSS | Low−Side Common Supply Ground |
| 28 | VDD(L) | Low−Side Bias Voltage for IC and IGBTs Driving |
| (29) | − | Dummy |
| (30) | − | Dummy |
| 31 | NW | Negative DC−Link Input for U Phase |
| 32 | NV | Negative DC−Link Input for V Phase |
| 33 | NU | Negative DC−Link Input for W Phase |
| 34 | W | Output for U Phase |
| 35 | V | Output for V Phase |
| 36 | U | Output for W Phase |
| 37 | P | Positive DC−Link Input |
| 38 | VTH | Thermistor Bias Voltage (T) / Not connection |
| 39 | RTH | Series Resister for Thermistor (Temperature Detection) *optional for T |

**Table 2. ABSOLUTE MAXIMUM RATINGS** $T_C$ = 25°C (Notes 1)

| Rating | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Supply Voltage | VPN | P – NU, NV, NW | 900 | V |
| Supply Voltage (Surge) | VPN(Surge) | P – NU, NV, NW, (Note 2) | 1000 | V |
| Self Protection Supply Voltage Limit (Short−Circuit Protection Capability | VPN(PROT) | VDD = VBS = 13.5 V ~ 16.5 V, Ti = 150°C, Vces < 1200 V, Non−Repetitive, < 2 μs | 800 | V |
| Collector−Emitter Voltage | Vces | | 1200 | V |
| Maximum Repetitive Revers Voltage | VRRM | | 1200 | V |
| Each IGBT Collector Current | ±Ic | | ±10 | A |
| Each IGBT Collector Current (Peak) | ±Icp | Under 1 ms Pulse Width | ±20 | A |
| Control Supply Voltage High−Side Control Bias Voltage | VDD | VDD(UH, VH, WH), VDD(L) – VSS | −0.3 to 20 | V |
| | VBS | VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W) | −0.3 to 20 | V |
| Input Signal Voltage | VIN | HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) – VSS | −0.3 to VDD | V |
| Fault Output Supply Voltage | VFO | VFO – VSS | −0.3 to VDD | V |
| Fault Output Current | IFO | Sink Current at VFO pin | 2 | mA |
| Current Sensing Input Voltage | VCIN | CIN – VSS | −0.3 to VDD | V |
| Corrector Dissipation | Pc | Per One Chip | 83 | W |
| Operating Junction Temperature | Tj | | −40 to +150 | °C |
| Storage Temperature | Tstg | | −40 to +125 | °C |
| Module Case Operation Temperature | Tc | | −40 to +125 | °C |
| Isolation Voltage | Viso | 60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate | 2500 | V rms |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This surge voltage developed by the switching operation due to the wiring inductance between P and NU, NV, NW terminal.

**Table 3. THERMAL CHARACTERISTICS**

| Rating | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Junction to Case Thermal Resistance | Rth(j−c)Q | Inverter IGBT Part (per 1/6 Module) | – | – | 1.5 | °C/W |
| | Rth(j−c)F | Inverter FRD Part (per 1/6 Module) | – | – | 1.8 | °C/W |

3. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

**Table 4. RECOMMENDED OPERATING RANGES** (Note 4)

| Rating | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | VPN | P – NU, NV, NW | – | 600 | 800 | V |
| Gate Driver Supply Voltages | VDD | VDD(UH, VH, WH), VDD(L) – VSS | 13.5 | 15 | 16.5 | V |
| | VBS | VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W) | 13.0 | 15 | 18.5 | V |
| Supply Voltage Variation | dVDD / dt dVBS / dt | | −1 | – | 1 | V/μs |
| PWM Frequency | fPWM | | 1 | | 20 | kHz |
| Dead Time | DT | Turn−off to Turn−on (external) | 3 | – | – | μs |

**Table 4. RECOMMENDED OPERATING RANGES** (Note 4) (continued)

| Rating | Symbol | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Allowable r.m.s. Current | Io | VPN = 600 V, VDD = VBS = 15 V, P.F. = 0.8, Tc ≤ 125°C, Tj ≤ 150°C, (Note 5) | $f_{PWM}$ = 5 kHz | – | – | 11.2 | A rms |
| | | | $f_{PWM}$ = 15 kHz | – | – | 6.3 | |
| Allowable Input Pulse Width | PWIN (on) | 400 V ≤ VPN ≤ 800 V, 13.5 V ≤ VDD ≤ 16.5 V, 13.0 V ≤ VBS ≤ 18.5 V, −40°C ≤ Tc ≤ 150°C | | 2.0 | – | – | μs |
| | PWIN (off) | | | 2.5 | – | – | |
| Package Mounting Torque | | M3 Type Screw | | 0.6 | 0.7 | 0.9 | Nm |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Allowable r.m.s Current depends on the actual conditions.
5. Flatness tolerance of the heatsink should be within −50 μm to +100 μm.

**Table 5. ELECTRICAL CHARACTERISTICS** (Tc = 25°C, VD = 15 V, unless otherwise noted) (Note 6)

| Parameter | | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **INVERTER SECTION** | | | | | | | |
| Collector−Emitter Leakage Current | | Vce = Vces, Tj = 25°C | Ices | – | – | 1 | mA |
| | | Vce = Vces, Tj = 150°C | | – | – | 10 | mA |
| Collector−Emitter Saturation Voltage | | VDD = VBS = 15 V, IN = 5 V Ic = 10 A, Tj = 25°C | VCE(sat) | – | 1.85 | 2.5 | V |
| | | VDD = VBS = 15 V, IN = 5 V Ic = 10 A, Tj = 150°C | | – | 2.00 | – | V |
| FWDi Forward Voltage | | IN = 0 V, If = 10 A, Tj = 25°C | VF | – | 1.80 | 2.6 | V |
| | | IN = 0 V, If = 10 A, Tj = 150°C | | – | 1.70 | – | V |
| High Side | Switching Times | VPN = 600 V, VDD(H) = VDD(L) = 15 V Ic = 10 A, Tj = 25°C, IN = 0 ⇔ 5 V Inductive Load | ton | 0.80 | 1.40 | 2.00 | μs |
| | | | tc (on) | – | 0.30 | 0.60 | μs |
| | | | toff | – | 1.70 | 2.50 | μs |
| | | | tc (off) | – | 0.20 | 0.60 | μs |
| | | | trr | – | 0.40 | – | μs |
| Low Side | Switching Times | VPN = 600 V, VDD(H) = VDD(L) = 15 V Ic = 10 A, Tj = 25°C, IN = 0 ⇔ 5 V Inductive Load | ton | 0.90 | 1.50 | 2.10 | μs |
| | | | tc (on) | – | 0.30 | 0.60 | μs |
| | | | toff | – | 1.70 | 2.50 | μs |
| | | | tc (off) | – | 0.20 | 0.60 | μs |
| | | | trr | – | 0.40 | – | μs |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **DRIVER SECTION** | | | | | | | |
| Quiescent VDD Supply Current | VDD(UH,VH,WH) = 15 V, HIN(U,V,W) = 0 V | VDD(UH) − VSS VDD(VH) − VSS VDD(WH) − VSS | IQDDH | – | – | 0.30 | mA |
| | VDD(L) = 15 V, LIN(U, V, W) = 0 V | VDD(L) − VSS | IQDDL | – | – | 3.50 | mA |
| Operating VDD Supply Current | VDD(UH, VH, WH) = 15 V, $f_{PWM}$ = 20 kHz, Duty = 50%, Applied to one PWM Signal Input for High−Side | VDD(UH) − VSS VDD(VH) − VSS VDD(WH) − VSS | IPDDH | – | – | 0.40 | mA |
| | VDD(L) = 15 V, $f_{PWM}$ = 20 kHz, Duty = 50%, Applied to one PWM Signal Input for Low−Side | VDD(L) − VSS | IPDDL | – | – | 7.00 | mA |

**Table 5. ELECTRICAL CHARACTERISTICS** (Tc = 25°C, VD = 15 V, unless otherwise noted) (Note 6) (continued)

| Parameter | Test Conditions | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **DRIVER SECTION** | | | | | | | |
| Quiescent VBS Supply Current | VBS = 15 V<br>HIN(U, V, W) = 0 V | VB(U) – VS(U)<br>VB(V) – VS(V)<br>VB(W) – VS(W) | IQBS | – | – | 0.30 | mA |
| Operating VBS Supply Current | VDD = VBS = 15 V,<br>$f_{PWM}$ = 20 kHz, Duty = 50%,<br>Applied to one PWM Signal Input for High–Side | VB(U) – VS(U)<br>VB(V) – VS(V)<br>VB(W) – VS(W) | IPBS | – | – | 6.00 | mA |
| ON Threshold Voltage | HIN(U, V, W) – VSS, LIN(U, V, W) – VSS | | VIN(ON) | – | – | 2.6 | V |
| OFF Threshold Voltage | | | VIN(OFF) | 0.8 | – | – | V |
| Short Circuit Trip Level | VDD = 15 V, CIN–VSS | | VCIN(ref) | 0.46 | 0.48 | 0.50 | V |
| Supply Circuit Under–Voltage Protection | Detection Level | | UVDDD | 10.3 | – | 12.5 | V |
| | Reset Level | | UVDDR | 10.8 | – | 13.0 | V |
| | Detection Level | | UVBSD | 10.0 | – | 12.0 | V |
| | Reset Level | | UVBSR | 10.5 | – | 12.5 | V |
| Voltage Output for LVIC Temperature Sensing Unit | VTS–VSS = 10 nF, Temp. = 25°C | | VTS | (0.905) | (1.030) | (1.155) | V |
| Fault Output Voltage | VDD = 0 V, CIN = 0 V,<br>VFO Circuit: 10 kΩ to 5 V Pull–up | | VFOH | 4.9 | – | – | V |
| | VDD = 0 V, CIN = 1 V,<br>VFO Circuit: 10 kΩ to 5 V Pull–up | | VFOL | – | – | 0.95 | V |
| Fault–Output Pulse Width | CFOD = 22 nF | | tFOD | 1.6 | 2.4 | – | ms |
| **BOOTSTRAP SECTION** | | | | | | | |
| Bootstrap Diode Forward Current | If = 0.1 A | | VF | 3.4 | 4.6 | 5.8 | V |
| Built–in Limiting Resistance | | | RBOOT | 30 | 38 | 46 | Ω |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A = 25°C$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
7. The fault–out pulse width tFOD depends on the capacitance value of CFOD according to the following approximate equation: tFOD = (TBD) x $10^6$ x CFOD (s).
8. Values based on design and/or characterization.

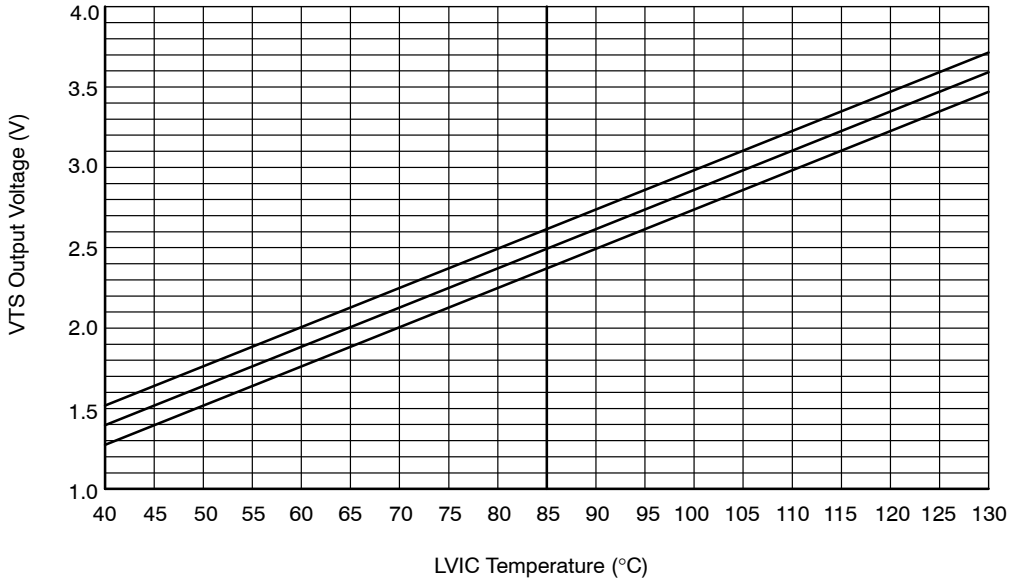



**Figure 4. Temperature of LVIC versus VOT Characteristics**

**Table 6. THERMISTOR CHARACTERISTIC**

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Resistance | $R_{25}$ | Tc = 25°C | 46.530 | 47 | 47.47 | kΩ |
| Resistance | $R_{125}$ | Tc = 125°C | 1.344 | 1.406 | 1.471 | kΩ |
| B−Constant (25−50°C) | − | B | 4009.5 | 4050 | 4090.5 | K |
| Temperature Range | − | − | −40 | − | +125 | °C |

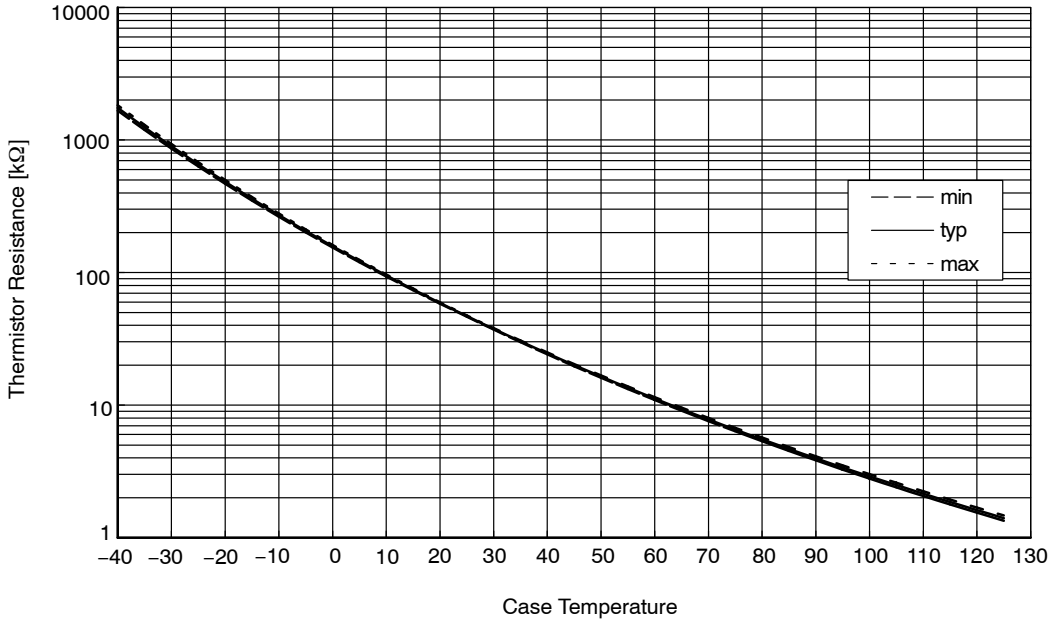



**Figure 5. Thermistor Resistance versus Case Temperature**

# NFAM1012L5BT

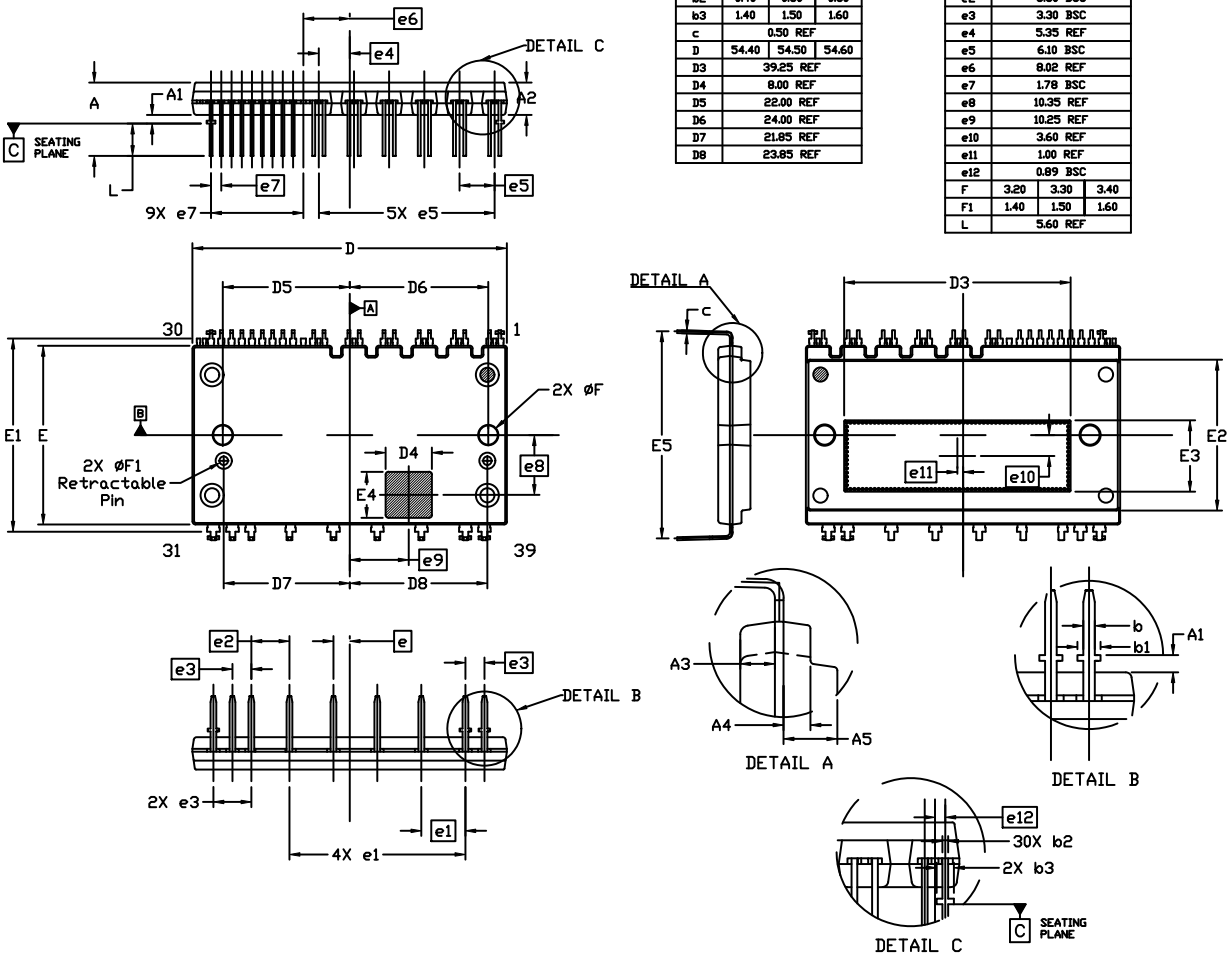
## PACKAGE DIMENSIONS

**MINI DIP39, 31.0x54.5**
CASE MODGC
ISSUE A

NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEAD IS DETERMINED AT THE ROOT OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.
5. SHORTENED/CUT PINS ARE 2,5,8,11,14,17,19,29 AND 30.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 12.20 | 12.7 | 13.2 |
| A1 | 1.00 | 1.50 | 2.00 |
| A2 | 5.50 | 5.60 | 5.70 |
| A3 | | 2.00 REF | |
| A4 | | 1.55 REF | |
| A5 | | 3.10 REF | |
| b | 0.90 | 1.00 | 1.10 |
| b1 | 1.90 | 2.00 | 2.10 |
| b2 | 0.40 | 0.50 | 0.60 |
| b3 | 1.40 | 1.50 | 1.60 |
| c | | 0.50 REF | |
| D | 54.40 | 54.50 | 54.60 |
| D3 | | 39.25 REF | |
| D4 | | 8.00 REF | |
| D5 | | 22.00 REF | |
| D6 | | 24.00 REF | |
| D7 | | 21.85 REF | |
| D8 | | 23.85 REF | |

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| E | 30.90 | 31.00 | 31.10 |
| E1 | | 33.50 REF | |
| E2 | | 26.14 REF | |
| E3 | | 12.35 REF | |
| E4 | | 8.00 REF | |
| E5 | 35.40 | 35.90 | 36.40 |
| e | | 2.81 REF | |
| e1 | | 7.62 BSC | |
| e2 | | 6.60 BSC | |
| e3 | | 3.30 BSC | |
| e4 | | 5.35 REF | |
| e5 | | 6.10 BSC | |
| e6 | | 8.02 REF | |
| e7 | | 1.78 BSC | |
| e8 | | 10.35 REF | |
| e9 | | 10.25 REF | |
| e10 | | 3.60 REF | |
| e11 | | 1.00 REF | |
| e12 | | 0.89 BSC | |
| F | 3.20 | 3.30 | 3.40 |
| F1 | 1.40 | 1.50 | 1.60 |
| L | | 5.60 REF | |




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