Dual UV/OV Voltage Monitor

FEATURES

- **Monitors Two Voltages Simultaneously**
- **Adjustable UV and OV Trip Values**
- **Guaranteed Threshold Accuracy: ±1.5%**
- **Input Glitch Rejection**
- Adjustable Reset Timeout with Disable
- 44µA Quiescent Current
- Open-Drain $\overline{OV}$ and $\overline{UV}$ Outputs
- Guaranteed $\overline{OV}$ and $\overline{UV}$ for $V_{CC} \geq 1V$
- Available in 10-Lead MSOP and (3mm × 3mm) DFN Packages

APPLICATIONS

- Desktop and Notebook Computers
- Network Servers
- Core, I/O Voltage Monitors

DESCRIPTION

The LTC®2913 is a dual input voltage monitor intended for multiple voltages in a variety of applications. Dual inputs for each voltage allow monitoring two separate undervoltage (UV) conditions and two separate overvoltage (OV) conditions. All monitors share a common undervoltage output and a common overvoltage output. The LTC2913-1 has latching capability for the overvoltage output. The LTC2913-2 has functionality to disable both the overvoltage and undervoltage outputs.

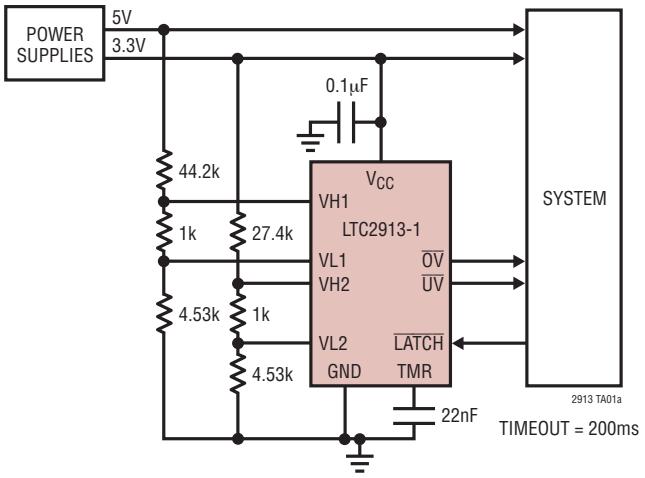
Glitch filtering ensures reliable reset operation without false or noisy triggering.

The LTC2913 provides a precise, versatile, space-conscious, micropower solution for voltage monitoring.

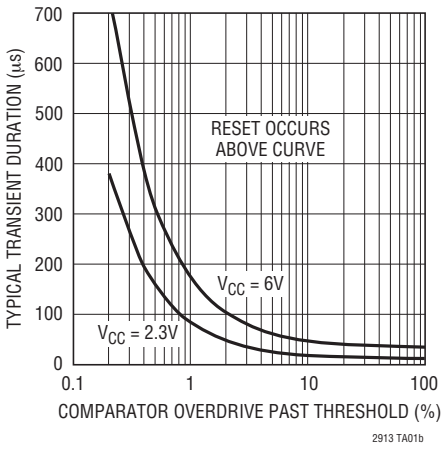
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All other trademarks are the property of their respective owners.

TYPICAL APPLICATION

Dual OV/UV Supply Monitor



Typical Transient Duration vs Comparator Overdrive



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Terminal Voltages
- V_{CC} (Note 3) ..... –0.3V to 6V
- $\overline{OV}$, $\overline{UV}$ ..... –0.3V to 16V
- TMR ..... –0.3V to (V_{CC} + 0.3V)
- VHn, VLn, $\overline{LATCH}$, DIS ..... –0.3V to 7.5V

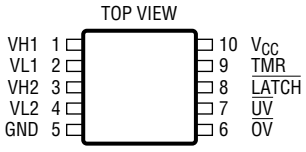
Terminal Currents
- I_{VCC} ..... +10mA
- $I_{\overline{UV}}$, $I_{\overline{OV}}$ 10mA

Operating Temperature Range
- LTC2913C ..... 0°C to 70°C
- LTC2913I ..... –40°C to 85°C
- LTC2913H ..... –40°C to 125°C

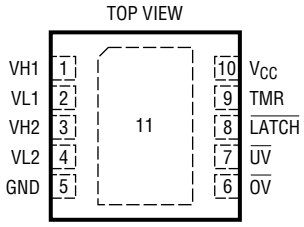
Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)
- MSOP ..... 300°C

PACKAGE/ORDER INFORMATION

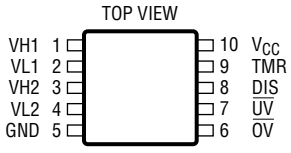


MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 120°C/W

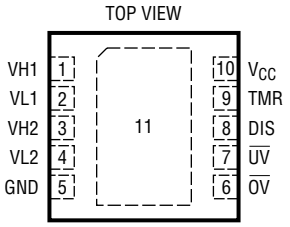


DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) PCB GND CONNECTION OPTIONAL

ORDER PART NUMBER	MS PART MARKING*	ORDER PART NUMBER	DD PART MARKING*
LTC2913CMS-1 LTC2913IMS-1 LTC2913HMS-1	LTCKK LTCKK LTCKK	LTC2913CDD-1 LTC2913IDD-1 LTC2913HDD-1	LCKN LCKN LCKN



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 120°C/W



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) PCB GND CONNECTION OPTIONAL

ORDER PART NUMBER	MS PART MARKING*	ORDER PART NUMBER	DD PART MARKING*
LTC2913CMS-2 LTC2913IMS-2 LTC2913HMS-2	LTCKM LTCKM LTCKM	LTC2913CDD-2 LTC2913IDD-2 LTC2913HDD-2	LCKP LCKP LCKP

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

*The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, VLn = 0.45V, VHn = 0.55V, $\overline{LATCH}$ = V_{CC}, DIS = Open unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SHUNT}	V_{CC} Shunt Regulator Voltage	I_{CC} = 5mA	●	6.2	6.6	6.9	V
		–40°C < T_A < 125°C	●	6.2	6.6	7.0	V
ΔV_{SHUNT}	V_{CC} Shunt Regulator Load Regulation	I_{CC} = 2mA to 10mA	●		200	300	mV
V_{CC}	Supply Voltage (Note 3)		●	2.3		V_{SHUNT}	V
$V_{CCR(MIN)}$	Minimum V_{CC} Output Valid	DIS = 0V	●			1	V
$V_{CC(UVLO)}$	Supply Undervoltage Lockout	DIS = 0V, V_{CC} Rising	●	1.9	2	2.1	V
$\Delta V_{CC(UVHYST)}$	Supply Undervoltage Lockout Hysteresis	DIS = 0V	●	5	25	50	mV
I_{CC}	Supply Current	V_{CC} = 2.3V to 6V	●		44	80	µA
V_{UOT}	Undervoltage/Overvoltage Threshold		●	492	500	508	mV
t_{UOD}	Undervoltage/Overvoltage Threshold to Output Delay	VHn = V_{UOT} – 5mV or VLn = V_{UOT} + 5mV	●	50	125	500	µs
I_{VHL}	VHn, VLn Input Current		●			±15	nA
		–40°C < T_A < 125°C	●			±30	nA
t_{UOTO}	$\overline{UV}/\overline{OV}$ Time-Out Period	C_{TMR} = 1nF	●	6	8.5	12.5	mS
		–40°C < T_A < 125°C	●	6	8.5	14	mS
$V_{\overline{LATCH}(VIH)}$	$\overline{OV}$ Latch Clear Input High		●	1.2			V
$V_{\overline{LATCH}(VIL)}$	$\overline{OV}$ Latch Clear Input Low		●			0.8	V
$I_{\overline{LATCH}}$	$\overline{LATCH}$ Input Current	$V_{\overline{LATCH}}$ > 0.5V	●			±1	µA
$V_{DIS(VIH)}$	DIS Input High		●	1.2			V
$V_{DIS(VIL)}$	DIS Input Low		●			0.8	V
I_{DIS}	DIS Input Current	V_{DIS} > 0.5V	●	1	2	3	µA
$I_{TMR(UP)}$	TMR Pull-Up Current	V_{TMR} = 0V	●	–1.3	–2.1	–2.8	µA
		–40°C < T_A < 125°C	●	–1.2	–2.1	–2.8	µA
$I_{TMR(DOWN)}$	TMR Pull-Down Current	V_{TMR} = 1.6V	●	1.3	2.1	2.8	µA
		–40°C < T_A < 125°C	●	1.2	2.1	2.8	µA
$V_{TMR(DIS)}$	Timer Disable Voltage	Referenced to V_{CC}	●	–180	–270		mV
V_{OH}	Output Voltage High $\overline{UV}/\overline{OV}$	V_{CC} = 2.3V, $I_{\overline{UV}/\overline{OV}}$ = –1µA	●	1			V
V_{OL}	Output Voltage Low $\overline{UV}/\overline{OV}$	V_{CC} = 2.3V, $I_{\overline{UV}/\overline{OV}}$ = 2.5mA V_{CC} = 1V, I_{UV} = 100µA	● ●		0.1 0.01	0.3 0.15	V V

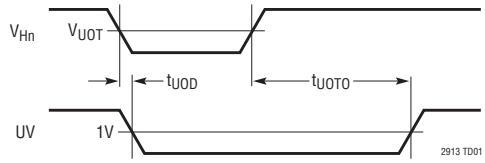
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

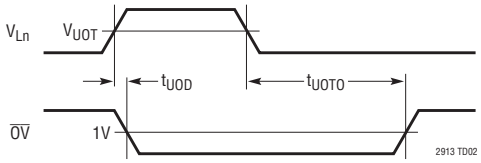
Note 3: V_{CC} maximum pin voltage is limited by input current. Since the V_{CC} pin has an internal 6.5V shunt regulator, a low impedance supply that exceeds 6V may exceed the rated terminal current. Operation from higher voltage supplies requires a series dropping resistor. See Applications Information.

TIMING DIAGRAMS

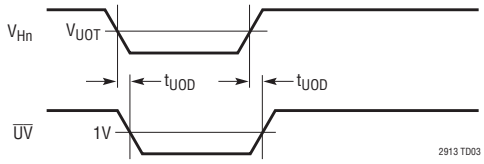
V_{Hn} Monitor Timing



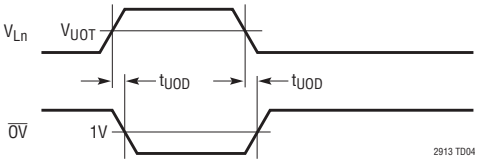
V_{Ln} Monitor Timing



V_{Hn} Monitor Timing (TMR Pin Strapped to V_{CC})



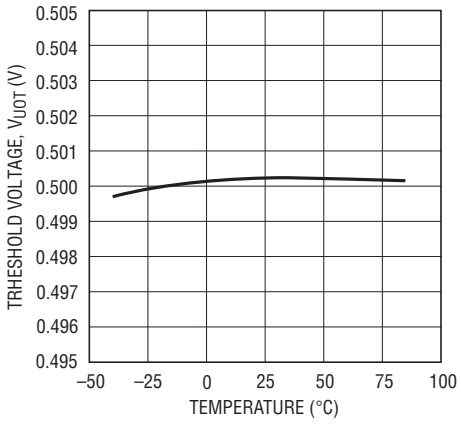
V_{Ln} Monitor Timing (TMR Pin Strapped to V_{CC})



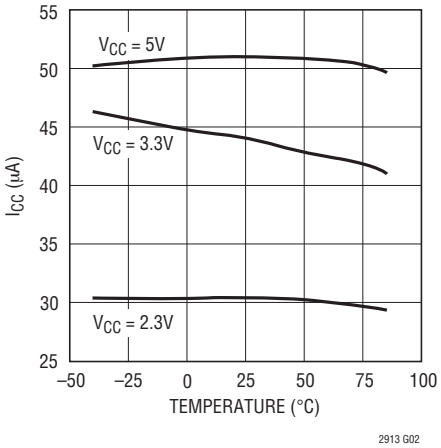
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C, V_{CC} = 3.3V unless otherwise noted.

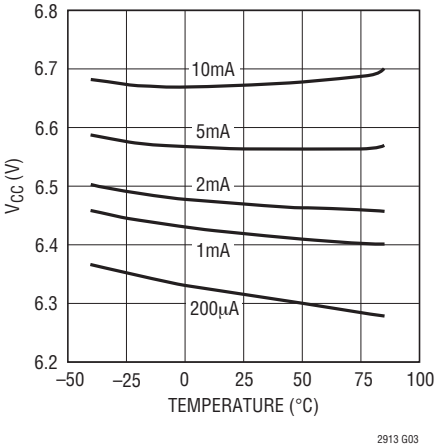
Input Threshold Voltage vs Temperature



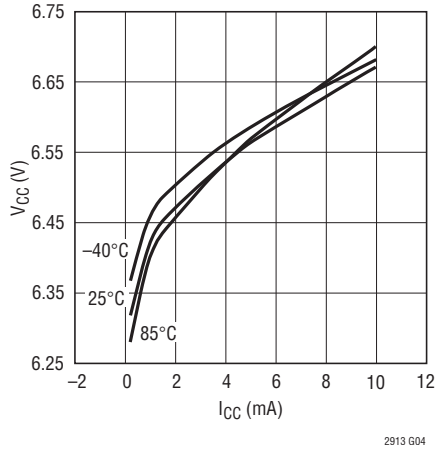
Supply Current vs Temperature



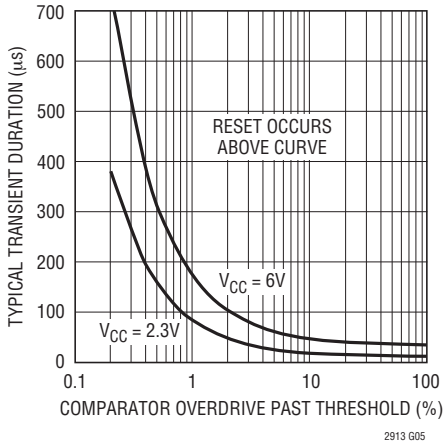
V_{CC} Shunt Voltage vs Temperature



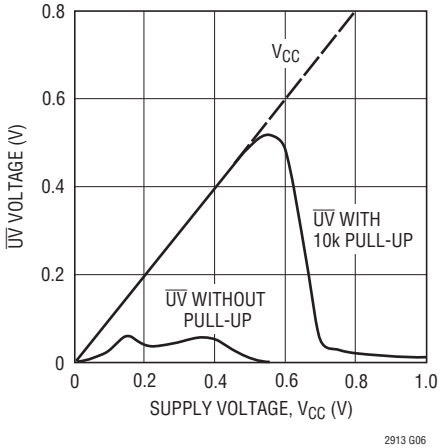
V_{CC} Shunt Voltage vs I_{CC}



Typical Transient Duration vs Comparator Overdrive



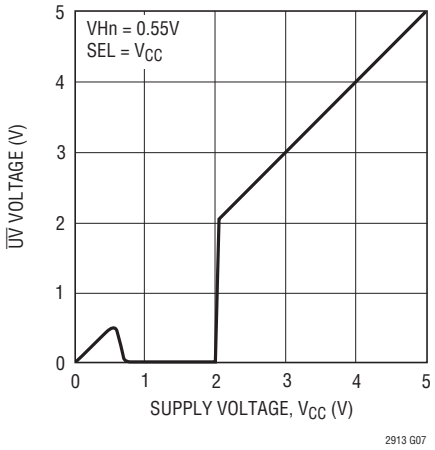
$\overline{UV}$ Output Voltage vs V_{CC}



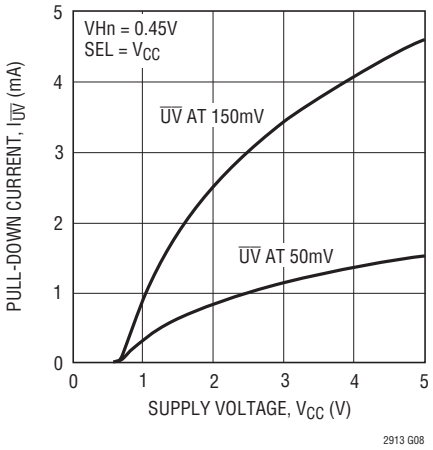
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C, V_{CC} = 3.3V unless otherwise noted.

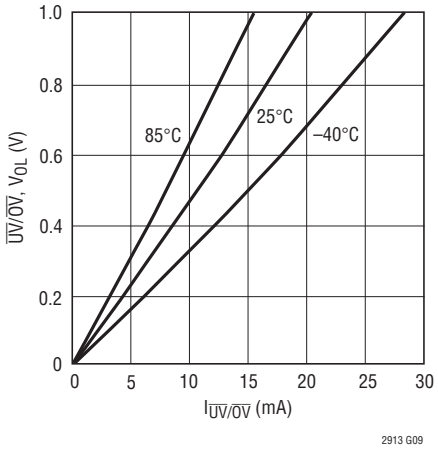
$\overline{UV}$ Output Voltage vs V_{CC}



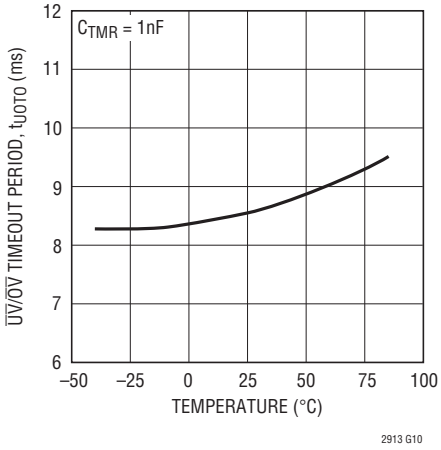
$\overline{UV}$, I_{SINK} vs V_{CC}



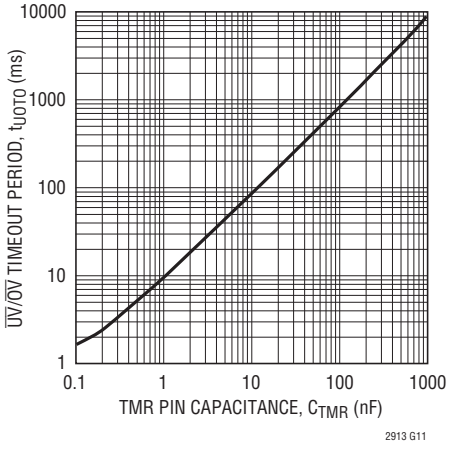
$\overline{UV}$/$\overline{OV}$ Voltage Output Low vs Output Sink Current



Reset Timeout Period vs Temperature



Reset Timeout Period vs Capacitance



PIN FUNCTIONS

DIS (Pin 8, LTC2913-2): Output Disable Input. Disables the $\overline{OV}$ and $\overline{UV}$ output pins. When DIS is pulled high, the $\overline{OV}$ and $\overline{UV}$ pins are not asserted except during a UVLO condition. DIS has a weak (2µA) internal pull-down to GND. Leave DIS open if unused.

Exposed Pad (Pin 11, DFN Package): Exposed Pad may be left open or connected to device ground.

GND (Pin 5): Device Ground.

$\overline{LATCH}$ (Pin 8, LTC2913-1): $\overline{OV}$ Latch Clear/Bypass Input. When pin is pulled low, $\overline{OV}$ is latched when asserted. When pulled high, $\overline{OV}$ latch is cleared. While held high, $\overline{OV}$ has the same delay and output characteristics as $\overline{UV}$.

$\overline{OV}$ (Pin 6): Overvoltage Logic Output. Asserts low when either VL input voltage is above threshold. Latched low (LTC2913-1). Held low for programmed delay time after both VL inputs are valid (LTC2913-2). $\overline{OV}$ has a weak pull-up to V_{CC} and may be pulled above V_{CC} using an external pull-up. Leave $\overline{OV}$ open if unused.

PIN FUNCTIONS

TMR (Pin 9): Reset Delay Timer. Attach an external capacitor (C_{TMR}) of at least 10pF to GND to set a reset delay time of 9ms/nF. A 1nF capacitor will generate an 8.5ms reset delay time. Tie TMR to V_{CC} to bypass timer.

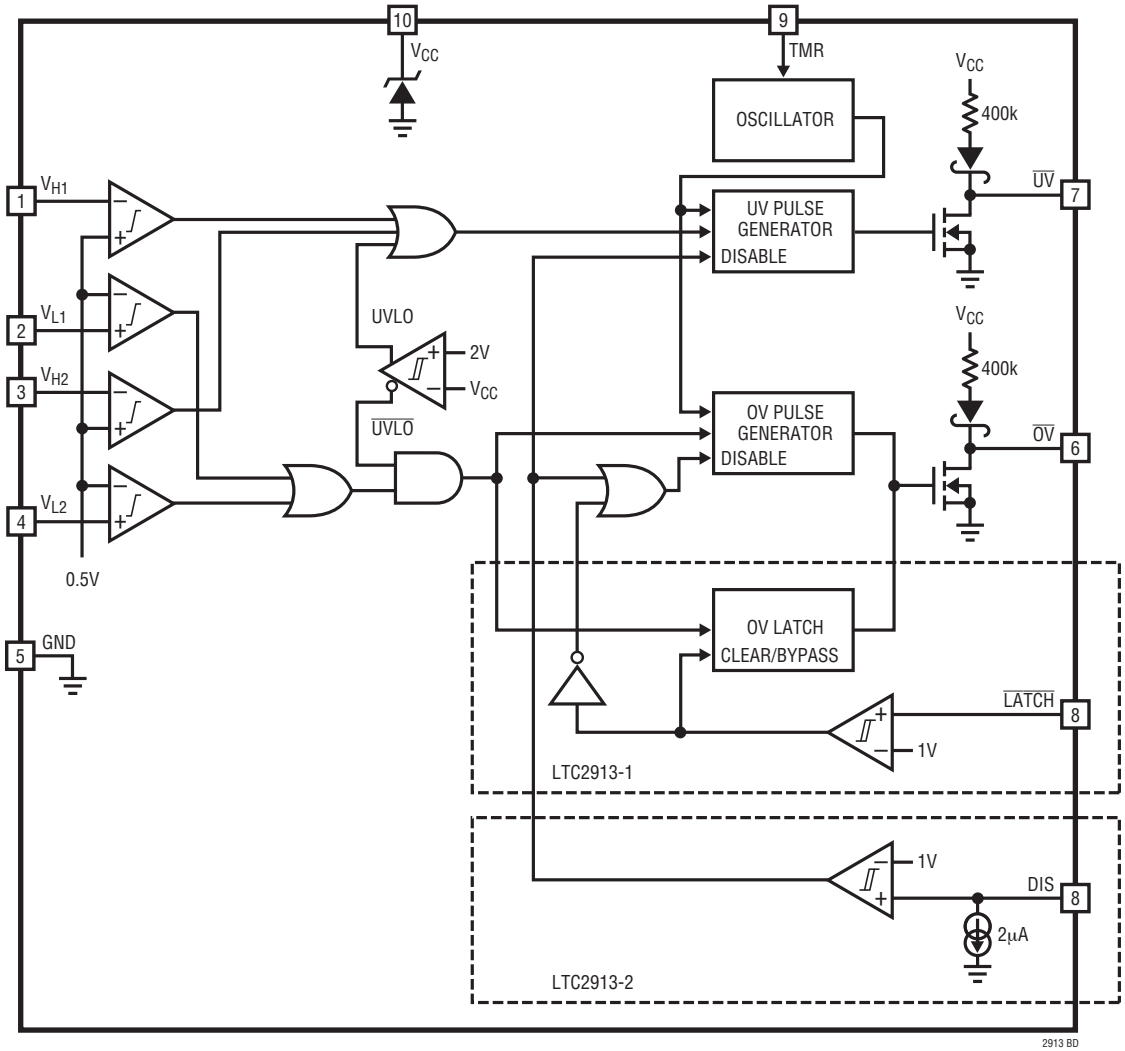
$\overline{UV}$ (Pin 7): Undervoltage Logic Output. Asserts low when either VH input voltage is below threshold. Held low for a programmed delay time after both VH inputs are valid. $\overline{UV}$ has a weak pull-up to V_{CC} and may be pulled above V_{CC} using an external pull-up. Leave $\overline{UV}$ open if unused.

V_{CC} (Pin 10): Supply Voltage. Bypass this pin to GND with a 0.1µF (or greater) capacitor. Operates as a direct supply input for voltages up to 6V. Operates as a shunt regulator for supply voltages greater than 6V and must have a resistance between the pin and the supply to limit input current to no greater than 10mA. When used without a current-limiting resistance, V_{CC} voltage must not exceed 6V.

VH1/VH2 (Pin 1/Pin 3): Voltage High Inputs 1 and 2. When the voltage on this pin is below 0.5V, an undervoltage condition is triggered. Tie pin to V_{CC} if unused.

VL1/VL2 (Pin 2/Pin 4): Voltage Low Inputs 1 and 2. When the voltage on this pin is above 0.5V, an overvoltage condition is triggered. Tie pin to GND if unused.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Voltage Monitoring

The LTC2913 is a low power dual voltage monitoring circuit with two undervoltage and two overvoltage inputs. A timeout period that holds $\overline{OV}$ and $\overline{UV}$ asserted after all faults have cleared is adjustable using an external capacitor and is externally disabled.

Each voltage monitor has two inputs (VHn and VLn) for detecting undervoltage and overvoltage conditions. When configured to monitor a positive voltage V_n using the 3-resistor circuit configuration shown in Figure 1, VHn is connected to the high side tap of the resistive divider and VLn is connected to the low side tap of the resistive divider.

3-Step Design Procedure

The following 3-step design procedure determines appropriate resistances to obtain the desired UV and OV trip points for the voltage monitor circuit in Figure 1.

For supply monitoring, V_n is the desired nominal operating voltage, I_n is the desired nominal current through the resistive divider, V_{OV} is the desired overvoltage trip point and V_{UV} is the desired undervoltage trip point.

1. Choose R_A to obtain the desired OV trip point

R_A is chosen to set the desired trip point for the overvoltage monitor.

$$R_A = \left| \frac{0.5V}{I_n} \bullet \frac{V_n}{V_{OV}} \right| \quad (1)$$

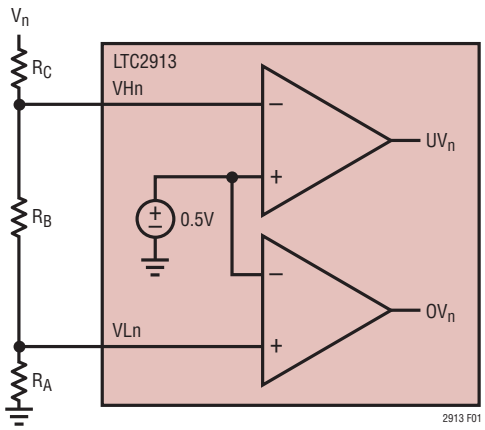


Figure 1. 3-Resistor Positive UV/OV Monitoring Configuration

2. Choose R_B to obtain the desired UV trip point

Once R_A is known, R_B is chosen to set the desired trip point for the undervoltage monitor.

$$R_B = \left| \frac{0.5V}{I_n} \bullet \frac{V_n}{V_{UV}} \right| - R_A \quad (2)$$

3. Choose R_C to complete the design

Once, R_A and R_B are known, R_C is determined by:

$$R_C = \left| \frac{V_n}{I_n} \right| - R_A - R_B \quad (3)$$

If any of the variables V_n, I_n, V_{UV} or V_{OV} change, then each step must be recalculated.

Voltage Monitor Example

A typical voltage monitor application is shown in Figure 2. The monitored voltage is a 5V ±10% supply. Nominal current in the resistive divider is 10µA.

1. Find R_A to set the OV trip point of the monitor.

$$R_A = \left| \frac{0.5V}{10\mu A} \bullet \frac{5V}{5.5V} \right| \approx 45.3k$$

2. Find R_B to set the UV trip point of the monitor.

$$R_B = \left| \frac{0.5V}{10\mu A} \bullet \frac{5V}{4.5V} \right| - 45.3k \cong 10.2k$$

3. Determine R_C to complete the design.

$$R_C = \left| \frac{5V}{10\mu A} \right| - 45.3k - 10.2k \approx 442k$$

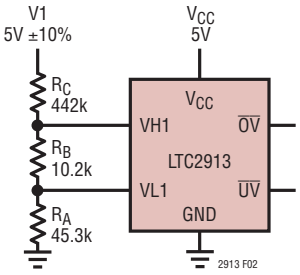


Figure 2. Typical Supply Monitor

APPLICATIONS INFORMATION

Power-Up/Power-Down

As soon as V_{CC} reaches 1V during power-up, the $\overline{UV}$ output asserts low and the $\overline{OV}$ output weakly pulls to V_{CC}.

The LTC2913 is guaranteed to assert $\overline{UV}$ low and $\overline{OV}$ high under conditions of low V_{CC}, down to V_{CC} = 1V. Above V_{CC} = 2V (2.1V maximum), the VH and VL inputs take control.

Once both VH inputs and V_{CC} are valid, an internal timer is started. After an adjustable delay time, $\overline{UV}$ weakly pulls high.

Threshold Accuracy

Reset threshold accuracy is important in a supply-sensitive system. Ideally, such a system resets only if supply voltages fall outside the exact thresholds for a specified margin. All LTC2913 inputs have a relative threshold accuracy of ±1.5% over the full operating temperature range.

For example, when the LTC2913 is programmed to monitor a 5V input with a 10% tolerance, the desired UV trip point is 4.5V. Because of the ±1.5% relative accuracy of the LTC2913, the UV trip point is between 4.433V and 4.567V which is 4.5V ±1.5%.

Likewise, the accuracy of the resistances chosen for R_A, R_B and R_C can affect the UV and OV trip points as well. Using the example just given, if the resistances used to set the UV trip point have 1% accuracy, the UV trip range is between 4.354V and 4.650V. This is illustrated in the following calculations.

The UV trip point is given as:

$$V_{UV} = 0.5V\left(1+\frac{R_C}{R_A+R_B}\right)$$

The two extreme conditions, with a relative accuracy of 1.5% and resistance accuracy of 1%, result in:

$$V_{UV(MIN)} = 0.5V \bullet 0.985 \bullet \left(1+\frac{R_C \bullet 0.99}{(R_A+R_B)\bullet 1.01}\right)$$

and

$$V_{UV(MAX)} = 0.5V \bullet 1.015 \bullet \left(1+\frac{R_C \bullet 1.01}{(R_A+R_B)\bullet 0.99}\right)$$

For a desired trip point of 4.5V, $\frac{R_C}{R_A+R_B} = 8$

Therefore,

$$V_{UV(MIN)} = 0.5V \bullet 0.985 \bullet \left(1+8\frac{0.99}{1.01}\right) = 4.354V$$

and

$$V_{UV(MAX)} = 0.5V \bullet 1.015 \bullet \left(1+8\frac{1.01}{0.99}\right) = 4.650V$$

Glitch Immunity

In any supervisory application, noise riding on the monitored DC voltage causes spurious resets. To solve this problem without adding hysteresis, which causes a new error term in the trip voltage, the LTC2913 lowpass filters the output of the first stage comparator at each input. This filter integrates the output of the comparator before asserting the UV or OV logic. A transient at the input of the comparator of sufficient magnitude and duration triggers the output logic. The Typical Performance Characteristics show a graph of the Transient Duration vs. Comparator Overdrive.

APPLICATIONS INFORMATION

UV/OV Timing

The LTC2913 has an adjustable timeout period (t_{UOTO}) that holds $\overline{OV}$ or $\overline{UV}$ asserted after all faults have cleared. This assures a minimum reset pulse width allowing a settling time delay for the monitored voltage after it has entered the valid region of operation.

When any VH input drops below its designed threshold, the $\overline{UV}$ pin asserts low. When all inputs recover above their designed thresholds, the UV output timer starts. If all inputs remain above their designed thresholds when the timer finishes, the $\overline{UV}$ pin weakly pulls high. However, if any input falls below its designed threshold during this timeout period, the timer resets and restarts when all inputs are above the designed thresholds. The $\overline{OV}$ output behaves as the $\overline{UV}$ output when $\overline{LATCH}$ is high (LTC2913-1).

Selecting the UV/OV Timing Capacitor

The UV and OV timeout period (t_{UOTO}) for the LTC2913 is adjustable to accommodate a variety of applications. Connecting a capacitor, C_{TMR}, between the TMR pin and ground sets the timeout period. The value of capacitor needed for a particular timeout period is:

$$C_{TMR} = t_{UOTO} \bullet 115 \bullet 10^{-9} \ [F/s]$$

The Reset Timeout Period vs Capacitance graph found in the Typical Performance Characteristics shows the desired delay time as a function of the value of the timer capacitor that must be used. The TMR pin must have a minimum 10pF load or be tied to V_{CC}. For long timeout periods, the only limitation is the availability of a large value capacitor with low leakage. Capacitor leakage current must not exceed the minimum TMR charging current of 1.3µA. Tying the TMR pin to V_{CC} will bypass the timeout period.

Undervoltage Lockout

When V_{CC} falls below 2V, the LTC2913 asserts an undervoltage lockout (UVLO) condition. During UVLO, $\overline{UV}$ is asserted and pulled low while $\overline{OV}$ is cleared and blocked from asserting. When V_{CC} rises above 2V, $\overline{UV}$ follows the same timing procedure as an undervoltage condition on any input.

Shunt Regulator

The LTC2913 has an internal shunt regulator. The V_{CC} pin operates as a direct supply input for voltages up to 6V. Under this condition, the quiescent current of the device remains below a maximum of 80µA. For V_{CC} voltages higher than 6V, the device operates as a shunt regulator and must have a resistance R_Z between the supply and the V_{CC} pin to limit the current to no greater than 10mA.

When choosing this resistance value, select an appropriate location on the I-V curve shown in the Typical Performance Characteristics to accommodate any variations in V_{CC} due to changes in current through R_Z.

$\overline{UV}$ and $\overline{OV}$ Output Characteristics

The DC characteristics of the $\overline{UV}$ and $\overline{OV}$ pull-down strength are shown in the Typical Performance Characteristics. Each pin has a weak internal pull-up to V_{CC} and a strong pull-down to ground. This arrangement allows these pins to have open-drain behavior while possessing several other beneficial characteristics. The weak pull-up eliminates the need for an external pull-up resistor when the rise time on the pin is not critical. On the other hand, the open-drain configuration allows for wired-OR connections, and is useful when more than one signal needs to pull down on the output. V_{CC} of 1V guarantees a maximum V_{OL} = 0.15V at $\overline{UV}$.

At V_{CC} = 1V, the weak pull-up current on $\overline{OV}$ is barely turned on. Therefore, an external pull-up resistor of no more than 100k is recommended on the $\overline{OV}$ pin if the state and pull-up strength of the $\overline{OV}$ pin is crucial at very low V_{CC}.

Note however, by adding an external pull-up resistor, the pull-up strength on the $\overline{OV}$ pin is increased. Therefore, if it is connected in a wired-OR connection, the pull-down strength of any single device must accommodate this additional pull-up strength.

Output Rise and Fall Time Estimation

The $\overline{UV}$ and $\overline{OV}$ outputs have strong pull-down capability. The following formula estimates the output fall time (90% to 10%) for a particular external load capacitance (C_{LOAD}):

$$t_{FALL} \approx 2.2 \bullet R_{PD} \bullet C_{LOAD}$$

APPLICATIONS INFORMATION

where R_{PD} is the on-resistance of the internal pull-down transistor, typically 50Ω at V_{CC} > 1V and at room temperature (25°C). C_{LOAD} is the external load capacitance on the pin. Assuming a 150pF load capacitance, the fall time is 16.5ns.

The rise time on the $\overline{UV}$ and $\overline{OV}$ pins is limited by a 400k pull-up resistance to V_{CC}. A similar formula estimates the output rise time (10% to 90%) at the $\overline{UV}$ and $\overline{OV}$ pins:

$$t_{RISE} \approx 2.2 \bullet R_{PU} \bullet C_{LOAD}$$

where R_{PU} is the pull-up resistance.

$\overline{OV}$ Latch (LTC2913-1)

With the $\overline{LATCH}$ pin held low, the $\overline{OV}$ pin latches low when an OV condition is detected. The latch is cleared by raising the $\overline{LATCH}$ pin high. If an OV condition clears while $\overline{LATCH}$ is held high, the latch is bypassed and the $\overline{OV}$ pin behaves the same as the $\overline{UV}$ pin with a similar timeout period at the output. If $\overline{LATCH}$ is pulled low while the timeout period is active, the $\overline{OV}$ pin latches as before.

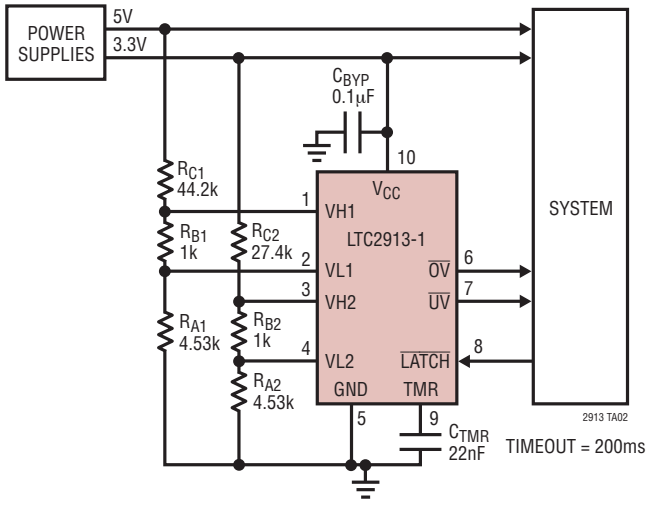
Disable (LTC2913-2)

The LTC2913-2 allows disabling the $\overline{UV}$ and $\overline{OV}$ outputs via the DIS pin. Pulling DIS high will force both outputs to remain weakly pulled high, regardless of any faults that occur on the inputs. However, if a UVLO condition occurs, $\overline{UV}$ asserts and pulls low, but the timeout function is bypassed. $\overline{UV}$ pulls high as soon as the UVLO condition is cleared.

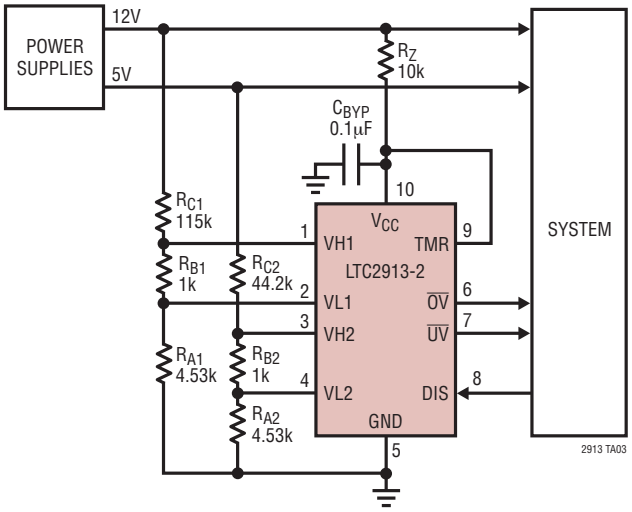
DIS has a weak 2µA (typical) internal pull-down current guaranteeing normal operation with the pin left open.

TYPICAL APPLICATIONS

Dual UV/OV Supply Monitor, 10% Tolerance, 5V, 3.3V

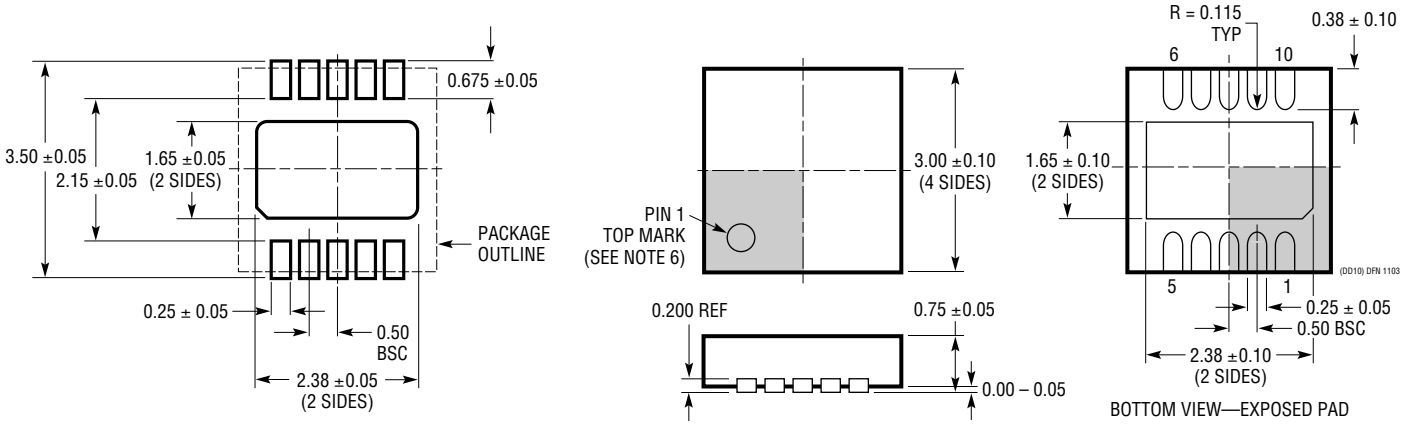


Supply Monitor Powered from 12V, 10% Tolerance, 12V, 5V



PACKAGE DESCRIPTION

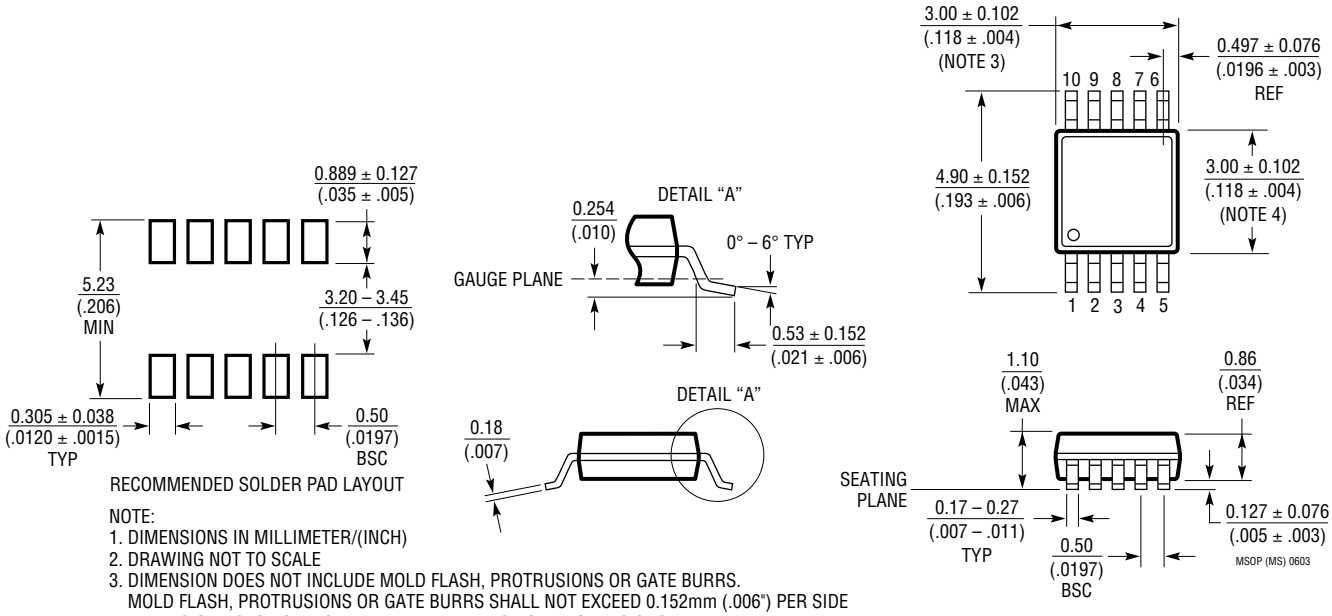
DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)

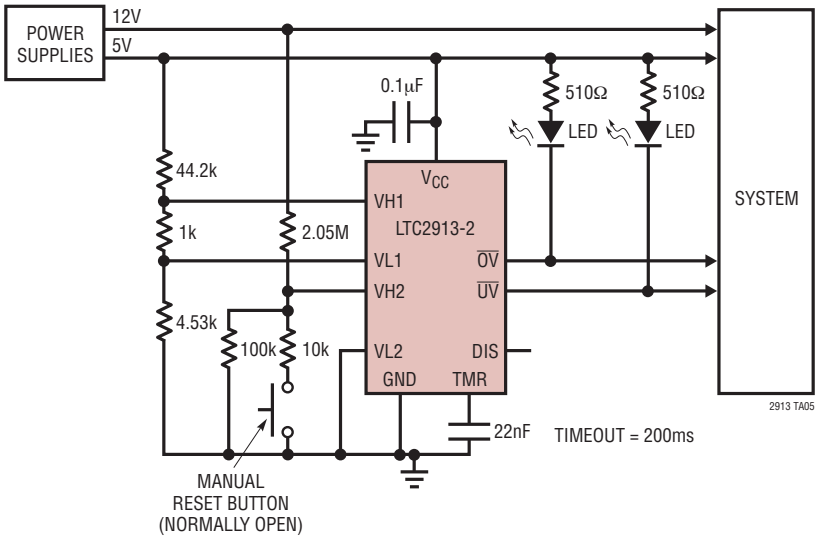


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Dual UV/OV Supply Monitor with LED Undervoltage and Overvoltage Indicator and Manual Undervoltage Reset Button, 10% Tolerance, 12V, 5V



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1326/ LTC1326-2.5	Micropower Precision Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ	4.725V, 3.118V, 1V Threshold (±0.75%)
LTC1726-2.5/ LTC1726-5	Micropower Triple Supply Monitor for 2.5V/5V, 3.3V and ADJ	Adjustable RESET and Watchdog Time-Outs
LTC1727-2.5/ LTC1727-5	Micropower Triple Supply Monitor with Open-Drain Reset	Individual Monitor Outputs in MSOP
LTC1728-1.8/ LTC1728-3.3	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1728-2.5/ LTC1728-5	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1985-1.8	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC2900	Programmable Quad Supply Monitor	Adjustable RESET, 10-Lead MSOP and 3mm × 3mm 10-Lead DFN Package
LTC2901	Programmable Quad Supply Monitor	Adjustable RESET and Watchdog Timer, 16-Lead SSOP Package
LTC2902	Programmable Quad Supply Monitor	Adjustable RESET and Tolerance, 16-Lead SSOP Package, Margining Functions
LTC2903	Precision Quad Supply Monitor	6-Lead SOT-23 Package, Ultralow Voltage Reset
LTC2904	3-State Programmable Precision Dual Supply Monitor	Adjustable Tolerance, 8-Lead SOT-23 Package
LTC2905	3-State Programmable Precision Dual Supply Monitor	Adjustable RESET and Tolerance, 8-Lead SOT-23 Package
LTC2906	Precision Dual Supply Monitor 1-Selectable and 1 Adjustable	Separate V_{CC} Pin, RST/$\overline{RST}$ Outputs
LTC2907	Precision Dual Supply Monitor 1-Selectable and 1 Adjustable	Separate V_{CC}, Adjustable Reset Timer
LTC2908	Precision Six Supply Monitor (Four Fixed & 2 Adjustable)	8-Lead SOT-23 and DFN Packages
LTC2909	Prevision Dual Input UV, OV and Negative Voltage Monitor	Separate V_{CC} Pin, Adjustable Reset Timer, 8-Lead TSOT-23 and DFN Packages
LTC2910	Octal Positive/Negative Voltage Monitor	Separate V_{CC} Pin, Eight Inputs, Up to Two Negative Monitors Adjustable Reset Timer, 16-Lead SSOP and DFN Packages
LTC2914	Quad UV/OV Positive/Negative Voltage Monitor	Separate V_{CC} Pin, Four inputs, Up To Two Negative Monitors, Adjustable Reset Timer, 16-Lead SSOP and DFN Packages

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