TPS63070 具有 3.6A 开关电流的 2V 至 16V 降压-升压转换器

1 特性

- 输入电压范围：2.0V 至 16V
- 输出电压范围：2.5V 至 9V
- 效率高达 95%
- 脉宽调制 (PWM) 模式下的直流精度为 +/-1%
- 脉频调制 (PFM) 模式下的直流精度为 +3%/-1%
- 降压模式下的输出电流为 2A
- 升压模式下的输出电流为 2A（VIN = 4V；Vout = 5V）
- 精密使能输入可实现
  - 用户定义的欠压闭锁
  - 准确排序
- 在降压和升压模式之间实现自动转换
- 器件静态电流典型值：50μA
- 具有固定和可调输出电压选项
- 具有输出放电选项
- 省电模式可提高低输出功率时的效率
- 2.4MHz 强制固定运行频率和同步选项
- 电源正常输出
- 可通过 VSEL 轻松更改输出电压
- 关断期间负载断开
- 过热保护
- 输入/输出过压保护
- 采用四方扁平无引线 (QFN) 封装

2 应用

- 双节锂离子 应用
- 工业计量设备
- 数码相机 (DSC) 和便携式摄像机
- 笔记本电脑
- 超便携移动个人计算机和移动互联网器件
- 个人医疗产品

3 说明

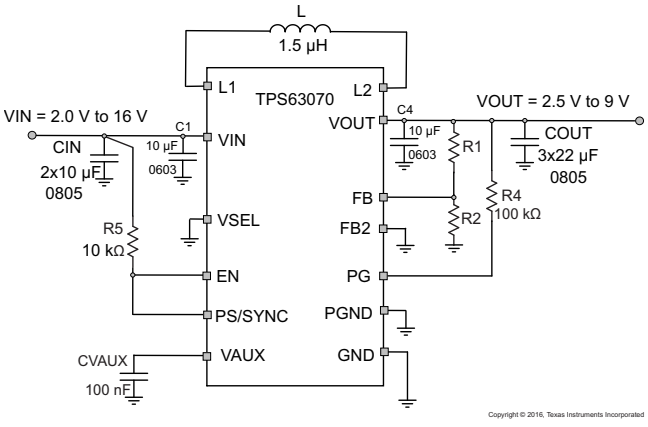
TPS6307x 是一款具有低静态电流的高效降压-升压转换器，适用于 那些 输入电压可能高于或低于输出电压的应用。在升压或降压模式下,输出电流可高达 2A。此降压-升压转换器基于一个固定频率、脉宽调制 (PWM) 控制器，此控制器通过使用同步整流来获得最高效率。在低负载电流情况下，此转换器进入省电模式以在宽负载电流范围内保持高效率。转换器可被禁用以最大限度地减少电池消耗。在关断期间，负载从电池上断开。此器件采用 2.5mm x 3mm QFN 封装。

器件信息(1)

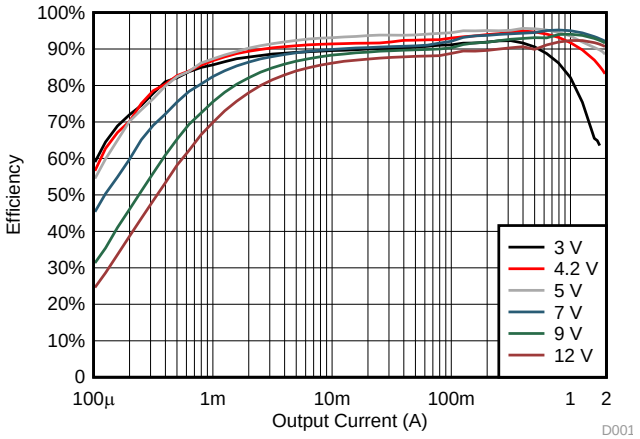
器件号	封装	封装尺寸（标称值）
TPS63070	VQFN	2.5mm x 3mm
TPS630701	VQFN	2.5mm x 3mm
TPS630702	VQFN	2.5mm x 3mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



效率与输出电流间的关系；Vo = 5V



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (August 2016) to Revision B **Page**

- 已添加 添加了多处微小的编辑更新和更正 ... 1
- 已添加 添加了“TPS630702 型号” ... 1
- Added TPS630702 Variant with "output discharge=on" option ... 3
- Added TPS630702 VOUT info ... 7
- Added TPS630702 VFB info at 3 instances ... 7
- Added Parameter Name ROD to output discharge resistance row ... 7
- Added Link to TechNote SLVAE62 ... 13
- Added more descriptive text for better understanding ... 15
- Changed Description of Discharge Feature, reflecting TPS630702 ... 15
- Changed description of output voltage programming to match EC table ... 17
- Added table of content for application curves ... 20
- 已添加 添加了“TPS630702 型号” ... 33

Changes from Original (June 2016) to Revision A **Page**

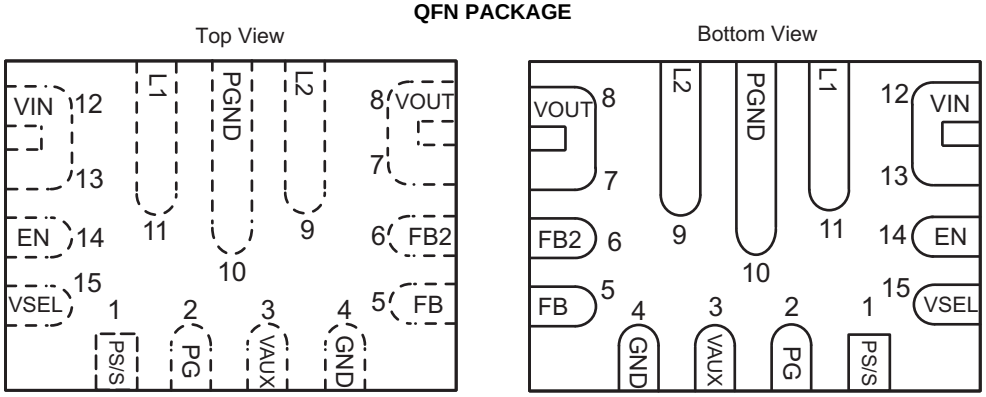
- 已添加 完整版量产数据数据表 ... 1

5 Device Comparison Table

Device Number	Features	Output Voltage	Marking
TPS63070	output discharge = off	adjustable	3070
TPS630701	output discharge = off	fixed 5 V	0701
TPS630702	output discharge = on	adjustable	0702

6 Pin Configuration and Functions

QFN PACKAGE



Pin Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
EN	14	I	Enable input. Pull high to enable the device, pull low to disable the device.
FB	5	I	Voltage feedback of adjustable versions, must be connected to VOUT on fixed output voltage versions
GND	4		Control / logic ground
L1	11	I	Connection for Inductor
L2	9	I	Connection for Inductor
PS/SYNC	1	I	Pull to low for forced PWM, pull high for PWM/PFM (power save) mode. Apply a clock signal to synchronize to an external frequency.
PG	2	O	Open drain power good output
PGND	10		Power ground
VIN	12, 13	I	Supply voltage for power stage
VOUT	7,8	O	Buck-boost converter output
VAUX	3	O	Connection for Capacitor of internal voltage regulator. This pin must not be loaded externally.
VSEL	15	I	Voltage scaling input. A high level on this pin enables a transistor which pulls pin FB2 to GND.
FB2	6	O	Voltage scaling output. Connect a resistor from FB to FB2 to change the voltage divider ratio on the feedback pin. A logic high level on VSEL will change the output voltage to a higher value. Leave the pin open or connect to GND if not used.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage range	VIN, PS/SYNC, EN, VSEL	–0.3	20	V
	L1	–0.3	20	V
	L1 (transient for t<10ns) (2)	–3	25	V
	L2, PG, VOUT, FB	–0.3	12	V
	L2 (transient for t<10ns) (2)	–3	15	V
	AUX	–0.3	7	V
	FB2	–0.3	3	V
Operating junction temperature, T_j		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) While switching

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage at VIN	2.0		16	V
Output Voltage	2.5		9	V
Effective Inductance	0.7	1.5	2.8	µH
Capacitance connected to VIN pin	4.7	10		µF
Capacitance connected to VAUX pin		100		nF
Total capacitance connected to VOUT pin (1)	15	47	470	µF
duty cycle in buck mode over recommended operating conditions	30			%
duty cycle in buck mode over recommended operating conditions but effective output capacitance Cout,eff ≥ 40uF; effective inductance L,eff = 0.7µH to 1.8uH	20			%
Operating junction temperature range, T_J	–40		125	°C

(1) Due to the dc bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. This is why the capacitance is specified to allow the selection of the minimal capacitor required with the dc bias effect for this type of capacitor in mind. The capacitance range given above is for the nominal inductance of 1.5 µH. Please also see the detailed design procedure in the application section about the ratio of inductance and minimum output capacitance.

7.4 Thermal Information

THERMAL METRIC(1)		TPS63070x VQFN 13 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over VIN = 2V to 16V; Tj = -40°C to 125°C; typical values are at Tj = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
VIN	Input voltage range	once started; Vout ≥ 3.0 V	2.0		16	V
VIN	Input voltage range	for start-up; Vout < 3.0 V	3.0		16	V
IOUT	Output current	during operation with either VIN ≥ 4.5 V or VOUT ≥ 4.5 V and the boost factor (VOUT/VIN) ≤ 1			2	A
I_Q	Quiescent current	into VIN; IOUT= 0 mA, V_{EN} = VIN = 6 V, PFM VOUT = 5 V; Tj = -40°C to 85°C		54	103	µA
I_Q	Quiescent current	into VIN; IOUT= 0 mA, V_{EN} = VIN = 6 V, PFM VOUT = 5 V; Tj = -40°C to 125°C			133	µA
I_Q	Quiescent current	into VOUT; IOUT= 0 mA, V_{EN} = VIN = 6 V, VOUT = 5 V, PFM Tj = -40°C to 85°C		5	9	µA
I_Q	Quiescent current	into VOUT; IOUT= 0 mA, V_{EN} = VIN = 6 V, VOUT = 5 V, PFM Tj = -40°C to 125°C			17	µA
I_{SD}	Shutdown current	V_{EN} = 0 V; Tj = -40°C to 85°C; VIN = 5V		2	12	µA
I_{SD}	Shutdown current	V_{EN} = 0 V; Tj = -40°C to 85°C			26	µA
V_{UVLO}	Undervoltage lockout threshold	VIN voltage falling	1.7	1.85	1.95	V
$V_{UVLO,TH}$	Undervoltage lockout hysteresis	VIN voltage rising	525	850		mV
T_{SD}	Thermal shutdown			160		°C
T_{SD}	Thermal shutdown hysteresis			20		°C
LOGIC SIGNALS: EN, PS/SYNC, PG, VSEL						
V_{THR}	Threshold Voltage rising edge for EN pin and PS/SYNC used for PWM/PFM mode change		0.77	0.8	0.83	V
V_{THF}	Threshold Voltage falling edge for EN pin and PS/SYNC used for PWM/PFM mode change		0.67	0.7	0.73	V
V_{IL}	VSEL low level input voltage; PS/SYNC low level input voltage when used for synchronization				0.3	V
V_{IH}	VSEL high level input voltage; PS/SYNC high level input voltage when used for synchronization		1.1			V
	EN, PS/SYNC, VSEL input current				0.2	µA
V_{OL}	PG output low voltage	I_{PG} = -1 mA			0.4	V
I_{LKG}	PG output leakage current	PG pin high impedance; V_{PG} = 5 V			0.2	µA
I_{PG}	PG sink current				1	mA
V_{TH_PG}	Power Good Threshold Voltage, rising Vout		94.5	96	98.5	%
V_{TH_PG}	Power Good Threshold Voltage, falling Vout		90	92	94.5	%

Electrical Characteristics (continued)

over VIN = 2V to 16V; Tj = -40°C to 125°C; typical values are at Tj = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
VOUT	TPS63070/TPS630702 output voltage range (1)		2.5		9	V
VOUT	TPS630701 output voltage			5.0		V
V_{FB}	TPS63070/TPS630702 feedback voltage	PS/SYNC = VIN		800		mV
	feedback impedance	for fixed voltage versions		1.5		MΩ
	feedback leakage	for adjustable version; VFB = 0.8V			100	nA
V_{FB}	TPS63070/TPS630702 feedback voltage accuracy	PS/SYNC = GND (PWM mode)	-1		1	%
VOUT	TPS630701 output voltage accuracy	PS/SYNC = GND (PWM mode)	-1		1	%
V_{FB}	TPS63070/TPS630702 feedback voltage accuracy	PS/SYNC = VIN (PFM mode); VIN ≥ 3V	-1		3	%
VOUT	TPS630701 output voltage accuracy	PS/SYNC = VIN (PFM mode); VIN ≥ 3V	-1		3	%
f_{SW}	Oscillator frequency		2100	2400	2700	kHz
	Frequency range for synchronization		2100		2800	kHz
IIN,max	Average, positive input current limit	VIN = 5.0V; VOUT = 6.5V; Tj = 0°C to 125°C	3050	3600	4150	mA
IIN,max	Average, negative input current limit	VIN = 5.0V; VOUT = 6.5V; Tj = 0°C to 125°C	1100	1800		mA
$R_{DS(ON)-BUCK}$	High side switch on resistance	VIN = 5 V		50	80	mΩ
	Low side switch on resistance	VIN = 5 V		100	160	mΩ
$R_{DS(ON)-BOOST}$	High side switch on resistance	VIN = 5 V		40	70	mΩ
	Low side switch on resistance	VIN = 5 V		80	125	mΩ
$R_{DS(ON)-FB2}$	FB2 resistance to GND with VSEL = high			25	100	Ω
I_{LKG}	Input leakage current into FB2 with VSEL=low	VFB = VFB2 = 0.8V			100	nA
	FB2 sink current				100	µA
	Line regulation	Power Save Mode disabled		0.07		%/V
	Load regulation	Power Save Mode disabled		0.2		%/A
V_{AUX}	Maximum bias voltage	VIN ≥ VOUT; VIN < 6V	VIN - 0.3		7	V
		VIN < VOUT	VOUT - 0.3		7	V
R_{OD}	Output discharge resistance (only in TPS630702)	VIN = 5 V; VOUT = 5V		200		Ω
t_{delay}	Start-up delay	time from EN = V_{IH} to device starts switching		70		µs
t_{SS}	soft-start time	time to ramp from 5% to 95% of Vout; buck mode; VIN = 7.2 V, Vout = 3.3 V, Iout = 500 mA		400		µs
		time to ramp from 5% to 95% of Vout; boost mode; VIN = 3.0 V, Vout = 3.3 V, Iout = 250 mA		850		µs

(1) Please observe the minimum duty cycle in buck mode

7.6 Typical Characteristics

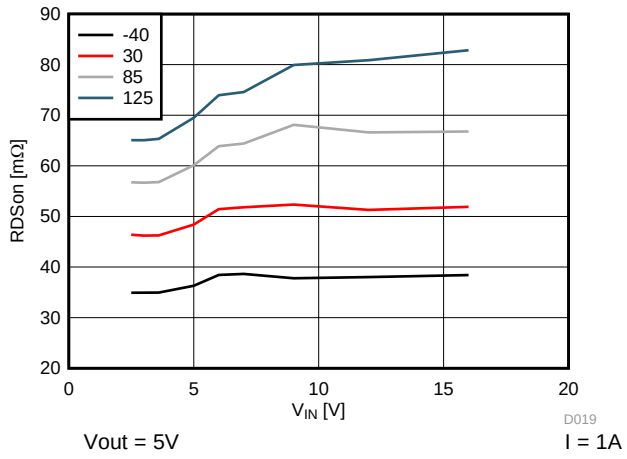


Figure 1. Rds(on) of High-side Buck Switch

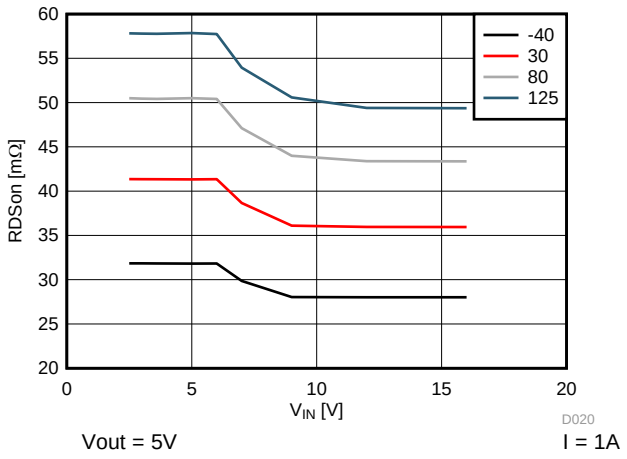


Figure 2. Rds(on) of High-side Boost Switch

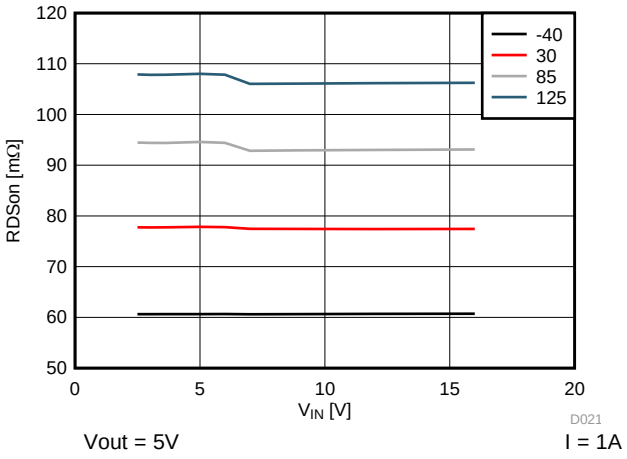


Figure 3. Rds(on) of Low-side Boost Switch

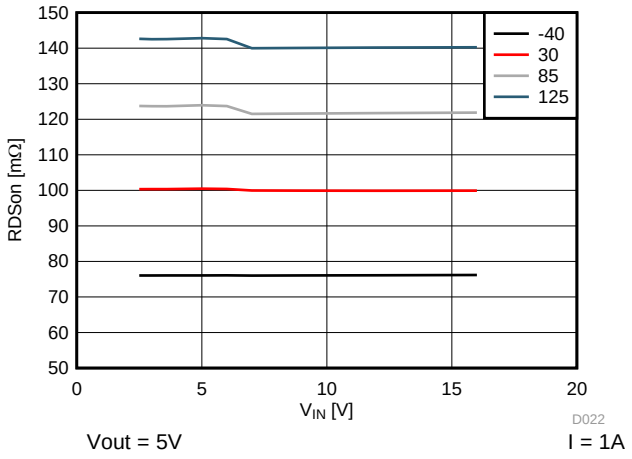


Figure 4. Rds(on) of Low-side Buck Switch

8 Detailed Description

8.1 Overview

The TPS6307x use 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range. To regulate the output voltage at all possible input voltage conditions, the device automatically switches from buck operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch on, and one switch held off. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are switching. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. For the remaining 2 switches, one is kept on and the other is kept off, thus causing no switching losses. Controlling the switches this way allows the converter to always keep high efficiency over the complete input voltage range. The device provides a seamless transition from buck to boost or from boost to buck operation.

8.2 Functional Block Diagram TPS63070

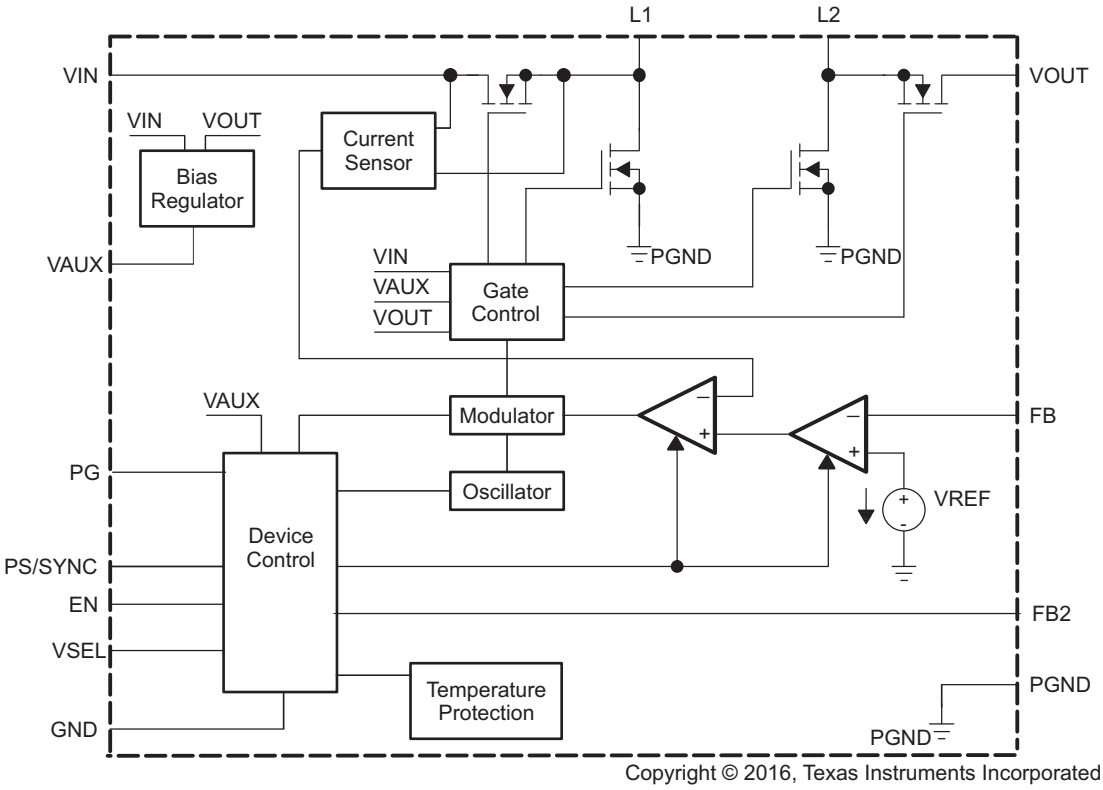


Figure 5. Functional Block Diagram

8.3 Functional Block Diagram TPS630701

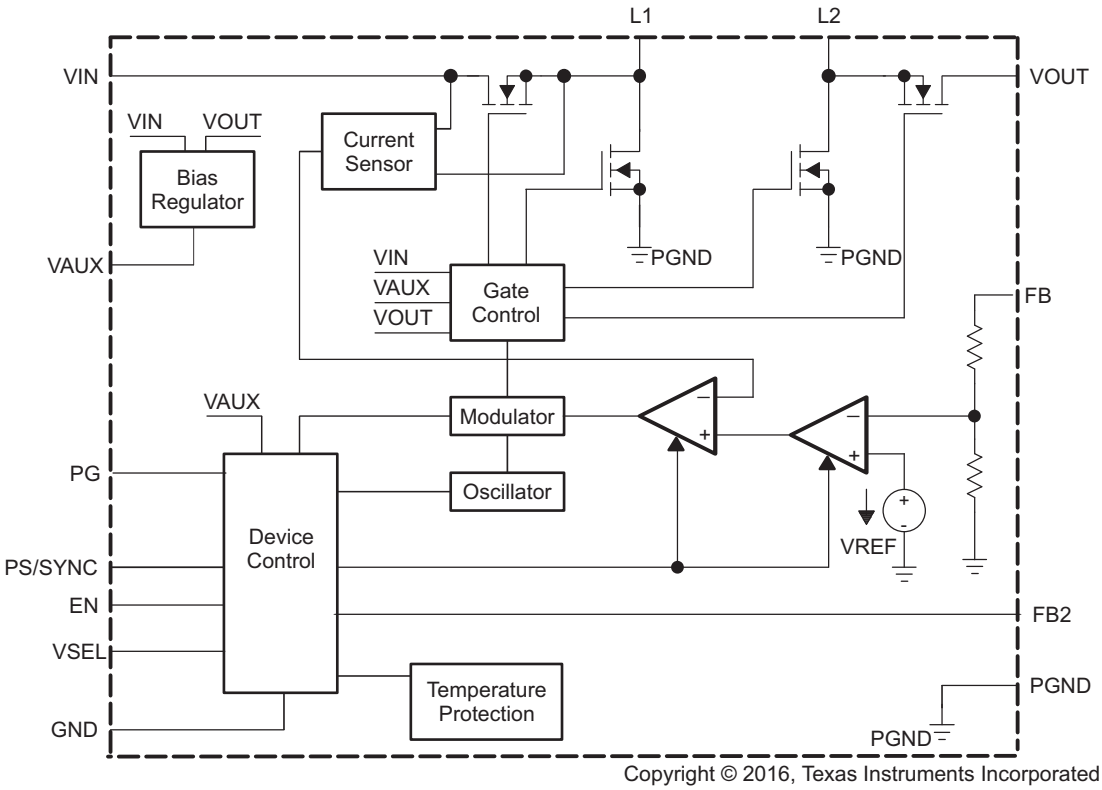


Figure 6. Functional Block Diagram

8.4 Feature Description

8.4.1 Control Loop Description

The controller circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop.

The non inverting input of the transconductance amplifier gmv can be assumed to be constant. The output of gmv defines the average inductor current. The inductor current is reconstructed by measuring the current through the high side buck MOSFET. This current corresponds exactly to the inductor current in boost mode. In buck mode, the current is measured during the on-time of the same MOSFET. During the off-time, the current is reconstructed internally starting from the peak value reached at the end of the on-time cycle. The average current is then compared to the desired value and the difference, or current error, is amplified and compared to the sawtooth ramp of either the Buck or the Boost. Depending on which of the two ramps is crossed by the signal, either the Buck MOSFETs or the Boost MOSFETs are activated. When the input voltage is close to the output voltage, one buck cycle is followed by a boost cycle. In this condition, not more than three cycle in a row of the same mode are allowed. This control method in the buck-boost region ensures a robust control and the highest efficiency.

For an input voltage above 9 V, and Vout below 2.2 V, the switching frequency is reduced by a factor of 2 to keep the minimum on-time at a reasonable value. For short circuit protection, at an output voltage below 1.2V, the low side input FET and the high side output FET are not actively switched but their back-gate diode used for conduction.

TPS6307x also contains a negative current limit. This allows the inductor current to reverse and flow from the output to the input. This is required for forced PWM operation at low output current but also for applications that require a fairly high current from the output to the input like TEC (thermo electric cooling) applications where the TEC cell is placed between input and output of the converter,

Feature Description (continued)

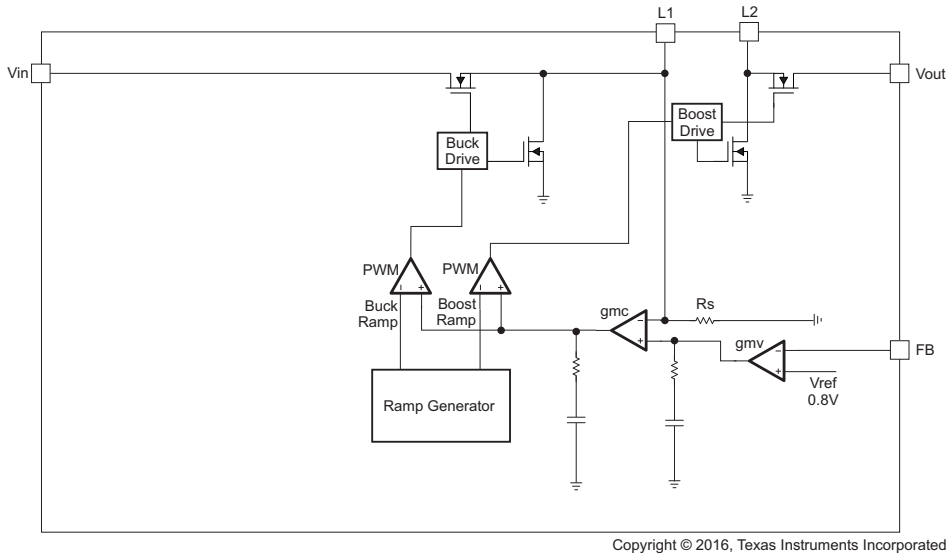


Figure 7. Average Current Mode Control

8.4.2 Precise Enable

The enable pin of the TPS63070 is not just a simple digital input but compares the voltage applied to a fixed threshold of 0.8V for a rising voltage. This allows to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a precise power-up delay. The enable input threshold for a falling edge is typically 100mV lower than the rising edge threshold. The TPS63070 starts operation when the rising threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown. In this mode, the internal high side and low side MOSFETs are turned off and the entire internal-control circuitry is switched off. The enable pin can also be used with an external voltage divider to set a user-defined minimum supply voltage.

It is recommended to not connect EN directly to VIN but use a resistor in series in the range of 1kΩ to 1MΩ. If several inputs like EN and PS/SYNC are connected to VIN, the resistor can be shared. No resistor is required if the pin is driven from an analog or digital signal rather than a supply voltage.

8.4.3 Power Good

The device has a built in power good output that indicates whether the output voltage has reached its nominal value. The PG signal is generated based on the status of the output voltage monitor. The power good circuit operates as long as the converter is enabled and VIN is above the undervoltage lockout threshold.

If the output voltage has not reached the regulated condition, the PG pin is held low. When the regulated condition is reached, PG is high impedance.

The PG output needs an external pull-up resistor. This resistor can be pulled to any voltage up to the maximum output voltage rating.

Table 1. Power Good Status

EN	output voltage status	PG
low	output off	low
high	output voltage above power good threshold	high impedance
high	output voltage below power good threshold, in thermal shutdown or input / output overvoltage protection active	low

8.4.4 Soft Start

To minimize inrush current during start up, the device has a soft start. When the EN pin is set high, after a thermal shutdown or after the undervoltage lockout threshold is exceeded, a soft-start cycle is started and the input current is ramped until the output voltage reaches regulation. The device ramps up the output voltage in a controlled manner, even if a large capacitor is connected at the output. During soft-start, as long as the output voltage is below the power good threshold, the input current limit is reduced to typically 1A. The soft-start time is defined by the current limit during the soft-start phase along with the load current, output capacitance and the input to output voltage ratio.

8.4.5 PS/SYNC

The PS/SYNC pin has two functions:

- switching between forced PWM mode and power save mode
- synchronizing to an external clock applied at pin PS/SYNC

When PS/SYNC is set high, the device operates in power save mode at low output current. For an average inductor current above a certain threshold the device switches to forced PWM mode. The automatic switch-over from PFM to PWM and vice versa is done such that the efficiency is kept at the maximum possible level. It is not based on a fixed threshold but at a current that depends on input voltage and output voltage to keep the efficiency at the maximum possible level.

The power save mode is disabled when PS/SYNC is set low. The device then operates in forced fixed frequency PWM mode independent of the output current.

TPS6307x can be synchronized to an external clock applied at pin PS/SYNC. Details about the voltage level and frequency range can be found in the electrical characteristics. When an external clock is detected, TPS6307x switches from internal clock or power save mode to fixed frequency operation based on the external clock frequency. When the external clock is removed, TPS6307x switches back to internal clock or power save mode depending on the average inductor current and status of the PS/SYNC pin. The PS/SYNC pin has two parallel input stages, a slow one with the precise threshold for PWM/PFM mode change and a fast digital input stage for an external clock signal for synchronization.

It is recommended to not connect PS/SYNC directly to VIN but use a resistor in series in the range of 1kΩ to 1MΩ. If several inputs like EN and PS/SYNC are connected to VIN, the resistor can be shared. No resistor is required if the pin is driven from an analog or digital signal rather than a supply voltage.

8.4.6 Short Circuit Protection

The TPS6307x provides short circuit protection to protect itself and the application. When the output voltage is below 1.2 V, the back-gate diodes of the low side input FET and high side output FET are used for rectification. For an input voltage above 9 V and an output voltage below 2.2 V, the switching frequency is scaled to ½ of its nominal value.

8.4.7 VSEL and FB2 pins

The VSEL pin allows to dynamically select between two different output voltages on the adjustable version. The voltage is set by a resistor that is connected between the FB and the FB2 pin. FB2 is connected to GND if VSEL = high. FB2 is high impedance if VSEL= low. The transition speed during a voltage change is defined by the loop bandwidth of the device and can be adjusted by adding a feed-forward capacitor in parallel to R1.

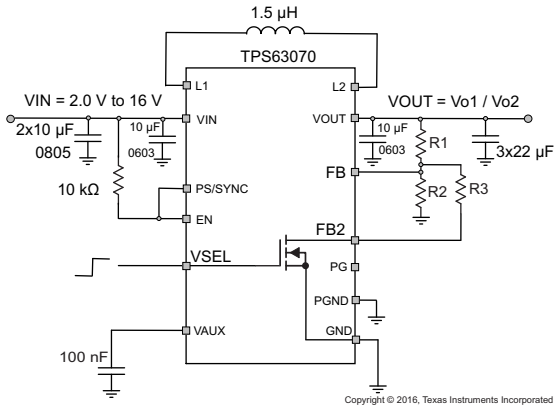


Figure 8. Typical Application using VSEL

The resistor values for the feedback divider and FB2 are in the 50-500kΩ range. R3 is calculated as follows:

$$R3 = \frac{Vo1 \times R1 \times R2^2}{(Vo2 - Vo1)(R1 \times R2 + R2^2)} \quad for\ Vo2 > Vo1 \tag{1}$$

For more details on how to use VSEL see Technote SLVAE62.

8.4.8 Overvoltage Protection

TPS6307x has a built in over-voltage protection which limits the output voltage. The voltage is internally sensed on the VOUT pin. In case the voltage on the feedback pin is not set correctly or the connection is open, this limits the output voltage to a value that protects the output stage from a too high voltage by limiting it to a internally set value.

Input over-voltage protection forces PFM mode to make sure the device is protected against boosting from the output to the input. This may happen if there is a large capacitor charged above the nominal voltage on the output and the supply on the input is removed. In PWM mode, the device is able to provide current from the output to the input causing a rise in the input voltage. In PFM mode, the current to the input is blocked so the input voltage can not rise. The input over-voltage protection does not protect the device from a too high voltage applied to the input but just from operating such that the device itself causes a rise of the input voltage above critical levels. Both over-voltage sensors are de-glitched by approximately 1µs.

8.4.9 Undervoltage Lockout

When the input voltage drops, the undervoltage lockout prevents mis-operation by switching off the device. The converter starts operation when the input voltage exceeds the threshold by a hysteresis of typically 850 mV. This relatively large hysteresis is needed to allow operation down to 2-V of supply voltage for the case when the output voltage is up at 3-V or above but restrict start-up for the case when the output voltage is zero. For start-up when the output voltage has not yet ramped, the rising UVLO threshold was set to a level that allows to start TPS63070 at a supply voltage where the load does not demand much load current.

8.4.10 Overtemperature Protection

The junction temperature (Tj) of the device is monitored by an internal temperature sensor. When Tj exceeds the thermal shutdown temperature, the device goes into thermal shutdown. The power stage is turned off and PG goes low. When Tj decreases below the hysteresis amount, the converter resumes normal operation, beginning with a Soft Start cycle. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shutdown temperature. In addition, the thermal shutdown is debounced by approximately 10 µs.

8.5 Device Functional Modes

8.5.1 Power Save Mode

Depending on the load current, in order to provide the best efficiency over the complete load range, the device works in PWM mode at an inductor current of approximately 650 mA or higher. At lighter load, the device switches automatically in to Power Save Mode to reduce power consumption and extend battery life. The PFM/PWM pin can be used to select between the two different operation modes. To enable Power Save Mode, the PFM/PWM pin must be set high.

During Power Save Mode, the part operates with a reduced switching frequency and supply current to maintain high efficiency. The output voltage is monitored by a comparator for the threshold "comp low" and "comp high" at every clock cycle. When the device enters Power Save Mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the output capacitance. When the output voltage reaches the comp low threshold, at the next clock cycle the device ramps up the output voltage again by starting operation. Operation can last for one or several pulses until the "comp high" threshold is reached. At the next PFM cycle, if the inductor current is still lower than about 650 mA, the device switches off again and the same operation is repeated. Instead, if at the next PFM cycle, the inductor current is above approximately 650 mA , the device automatically switches to PWM mode.

In order to keep high efficiency in PFM mode, there is only a comparator active to keep the output voltage regulated. The AC ripple in this condition is increased, compared to the voltage in PWM mode. The amplitude of this voltage ripple typically is 50 mV pk-pk, with 22 µF effective capacitance. In order to avoid a critical voltage drop when switching from 0 A to full load, the output voltage in PFM is typically 1 % above the nominal value in PWM. This allows the converter to operate with a small output capacitor and still have a low absolute voltage drop during heavy load transients.

Power Save Mode can be disabled by programming the PFM/PWM pin low.

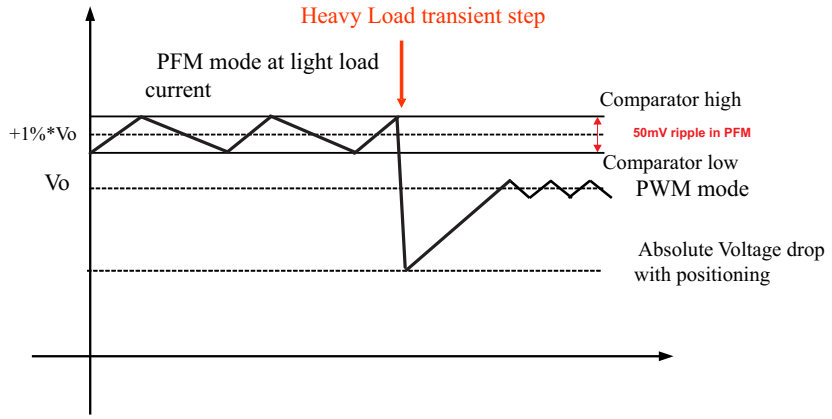


Figure 9. Dynamic Voltage Positioning

8.5.2 Current Limit

it is possible to calculate the output current in the different conditions in boost mode using Equation 2 and Equation 3 and in buck mode using Equation 4 and Equation 5.

Duty Cycle Boost $$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (2)$$

Output Current Boost $$I_{OUT} = \eta \times I_{IN} (1-D) \quad (3)$$

Duty Cycle Buck $$D = \frac{V_{OUT}}{V_{IN}} \quad (4)$$

Output Current Buck $$I_{OUT} = (\eta \times I_{IN}) / D \quad (5)$$

Device Functional Modes (continued)

With,

η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)
I_{IN} = Minimum average input current
The maximum output current TPS63070 can provide, can directly be seen from the graphs "Maximum Load Current vs Input Voltage" for different output voltages at (Figure 43, Figure 20 and Figure 22). The start-up current is lower because the current limit is set to typically 1A to limit the inrush current at start-up as long as the power good signal is low. Please see the typical start-up current graphs at Figure 42, Figure 19 and Figure 21. Once the power good comparator indicates "power good", the current limit is set to its nominal value as given in the electrical characteristics.

8.5.3 Output Discharge Function (TPS630702 only)

To make sure the load applied at TPS630702 is powered up from 0 V once TPS630702 is enabled, the device features an internal discharge resistor for the output capacitor. The discharge function is enabled as soon as the device is disabled, in thermal shutdown or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active when enabled is approximately 2 V. The discharge function is only active after the device has been enabled at least once after supply voltage was applied. This feature is only enabled in TPS630702 and it is the only difference between TPS63070 and TPS630702.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6307x is a high efficiency, low quiescent current buck-boost converter suitable for applications where the input voltage can be higher or lower than the output voltage. The TPS63070 is internally supplied from the higher of the input voltage or output voltage. For proper operation either one or both need to have a voltage of 3.0 V or above but must not exceed their maximum rating.

9.2 Typical Application for adjustable version

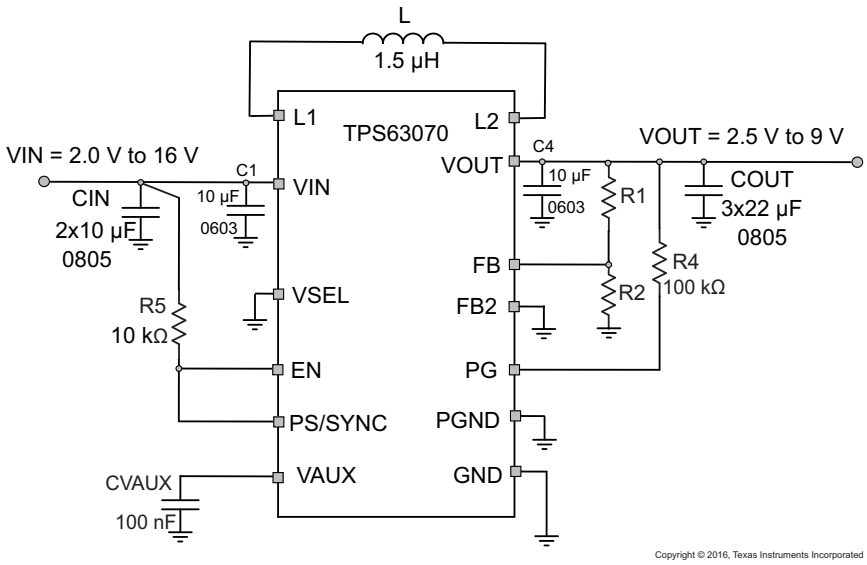


Figure 10. Typical Application For Adjustable Version

9.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions. The input and output capacitors have been split into a small 0603 size capacitor close to the device pins and 0805 size capacitors to get the required capacitance.

Table 2. Bill of Materials

REFERENCE	DESCRIPTION	VALUE	MANUFACTURER
IC	TPS63070RNM		Texas Instruments
L	XFL4020-152ME	1.5 µH	Coilcraft
CIN	GRM21BC71E106ME11L	2 x 10 µF / 25 V / X7S / 0805	Murata
C1	TMK107BBJ106MA-T	10 µF / 25 V / X5R / 0603	Taiyo Yuden
COUT	GRM21BC81C226ME44L	3 x 22 µF / 16 V / X6S / 0805	Murata
C4	TMK107BBJ106MA-T	10 µF / 25 V / X5R / 0603	Taiyo Yuden

Table 2. Bill of Materials (continued)

REFERENCE	DESCRIPTION	VALUE	MANUFACTURER
CVAUX	TMK105B7104MV-FR	100 nF / 25V / X7R / 0402	Taiyo Yuden
R1, R2	Metal Film Resistor ; 1%	depending on desired output voltage	
R4	Metal Film Resistor ; 1%	100 kΩ	

9.2.2 Detailed Design Procedure

The TPS6307x series of buck-boost converter has internal loop compensation. Therefore, the external L-C filter has to be selected according to the internal compensation. It's important to consider that the effective inductance, due to inductor tolerance and current derating can vary between 20% and -30%. The same for the capacitance of the output filter: the effective capacitance can vary between +20% and -80% of the specified datasheet value, due to capacitor tolerance and bias voltage. For this reason, *Output Filter Selection* shows the nominal capacitance and inductance value allowed. The effective capacitance of the adjustable version TPS63070 on the output (in µF) needs to be at least 10 times higher than the effective inductance (in µH) to ensure a good transient response and stable operation.

Table 3. Output Filter Selection

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)			
	22	47	68	100
1.0		√	√	√
1.5		√(3)	√	√
2.2			√	√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating of +20% and -50% is anticipated. For capacitors with larger dc bias effect, a larger nominal value needs to be selected.
(3) Typical application. Other check marks indicates recommended filter combinations

9.2.2.1 Programming The Output Voltage

While the output voltage of the TPS63070 is adjustable, the TPS630701 is set to a fixed voltage. For fixed output versions, the FB pin must be connected to the output directly. The adjustable version can be programmed for output voltages from 2.5V to 9V by using a resistive divider from VOUT to GND. The voltage at the FB pin (V_{REF})is regulated to 800mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6 . It is recommended to choose resistor values which allow a current of at least 2uA, meaning the value of R2 shouldn't exceed 400kΩ. Lower resistor values are recommended for highest accuracy and most robust design.

$$R_1 = R_2\left(\frac{V_{OUT}}{0.8V} - 1\right) \tag{6}$$

Table 4. Typical Resistor Values

Output Voltage	R1	R2
3.3 V	470 kΩ	150 kΩ
5.0 V	680 kΩ	130 kΩ
5.3 V	560 kΩ	100 kΩ
5.5 V	300 kΩ	51 kΩ
6.5 V	360 kΩ	51 kΩ
9 V	402 kΩ	39 kΩ

9.2.2.2 Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using Equation 8. Only the equation which defines the switch current in boost mode is shown, because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{7}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{8}$$

Where,

D =Duty Cycle in Boost mode

f = Converter switching frequency (typical 2.4MHz)

L = Selected inductor value

η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)

Note: The calculation must be done for the minimum input voltage which is possible to have in boost mode

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to choose an inductor with a saturation current 20% higher than the value calculated from Equation 8. The following inductors are recommended for use:

Table 5. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER(1)	SIZE (LxWxH /mm)	Isat/DCR
1.2 µH	Coilcraft, XFL4015-122ME	4 x 4 x 1.5	4.5 A / 18.8 mΩ
1.5 µH	Coilcraft, XFL4020-152ME	4 x 4 x 2.1	4.6 A / 14.4 mΩ
1.0 µH	Coilcraft, XFL4020-102ME	4 x 4 x 2.1	5.4 A / 10.8 mΩ
1 µH	Murata, 1277AS-H-1R0M	3.2 x 2.5 x 1.2	3.7 A / 45 mΩ

(1) See *Third-party Products Disclaimer*

The inductor value also affects the stability of the feedback loop. In particular the boost transfer function exhibits a right half-plane zero. The frequency of the right half plane zero is inverse proportional to the inductor value and the load current. This means the higher the value of the inductance and load current, the more the right half plane zero is moved to a lower frequency. This degrades the phase margin of the feedback loop. It is recommended to choose the inductor's value in order to have the frequency of the right half plane zero >400 kHz. The frequency of the RHPZ is calculated using Equation 9.

$$f_{RHPZ} = \frac{(1 - D)^2 \times Vout}{2\pi \times Iout \times L} \tag{9}$$

With,

D =Duty Cycle in Boost mode

Note: The calculation must be done for the minimum input voltage which is possible to have in boost mode

If the operating conditions results in a frequency of the RHPZ of less than 400kHz, more output capacitance should be added to reduce the cross over frequency. The RHPZ moves to lowest frequency at lowest input voltage (highest boost factor) and largest output current. Device stability should therefore be observed mainly under these worst case operating conditions.

9.2.2.3 Capacitor Selection

9.2.2.3.1 Input Capacitor

It is recommended to use a combination of capacitors on the input. A small size ceramic capacitor as close as possible from the VIN pin to GND to block high frequency noise and a larger one in parallel for the required capacitance on for good transient behavior of the regulator. X5R or X7R ceramic capacitor are recommended. The input capacitor needs to be large enough to avoid supply voltage dips shorter than 5us as the undervoltage lockout circuitry needs time to react.

9.2.2.3.2 Output Capacitor

Same as the input, the output capacitor should be a combination of capacitors optimized for suppressing high frequency noise and a larger capacitor for low output voltage ripple and stable operation. The use of small X5R or X7R ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC is recommended. A 0603 size capacitor close to the pins of the IC and as many 0805 capacitors as required to get the capacitance given the output voltage and dc bias effect of the ceramic capacitors is best. The recommended typical output capacitor values are outlined in *Output Filter Selection*. Please also see the *Recommended Operating Conditions* for the minimum and maximum capacitance at the output.

Larger capacitors will cause lower output voltage ripple as well as lower output voltage drop during load transients.

Table 6. Typical Capacitors

VALUE	PART NUMBER	COMPONENT SUPPLIER(1)	COMMENT	SIZE (LxWxH mm)
22 µF	EMK212BBJ226MG-T	Taiyo Yuden	input capacitor for Vin ≤ 8 V	2 x 1.25 x 1.25
22 µF	TMK316BBJ226ML	Taiyo Yuden	input capacitor	3.2 x 1.6 x 1.6
10 µF	TMK107BBJ106MA-T	Taiyo Yuden	bypass capacitor directly at device pins on VIN to GND and VOUT to GND	1.6 x 0.8 x 0.8
10 µF	GRM21BC71E106ME11	Murata	small body size; 2 parts required if used at VIN > 6V	2 x 1.25 x 1.25
22 µF	GRM21BC81C226ME44	Murata	small body size; 3 parts required if used at Vo > 5V; otherwise 2 parts	2 x 1.25 x 1.25

(1) See *Third-party Products Disclaimer*

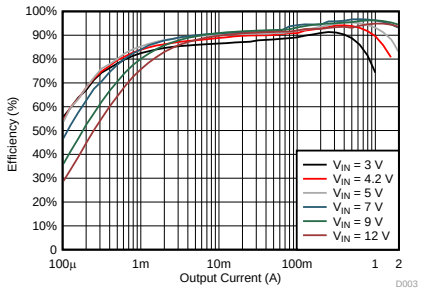
9.2.3 Application Curves

Table 7. Typical Application Curves for Adjustable Version

Parameter	Conditions	Figure
Efficiency		
Efficiency vs Output Current (PFM/PWM)	V_{IN} = 3 V, 4.2 V, 5 V, 7 V, 9 V, 12 V, V_{OUT} = 7 V , PS/SYNC = Low	Figure 11
Efficiency vs Output Current (PWM only)	V_{IN} = 3 V, 4.2 V, 5 V, 7 V, 9 V, 12 V, V_{OUT} = 7 V , PS/SYNC = High	Figure 12
Efficiency vs Output Current (PFM/PWM)	V_{IN} = 3 V, 4.2 V, 5 V, 7 V, 9 V, 12 V, V_{OUT} = 9 V , PS/SYNC = Low	Figure 13
Efficiency vs Output Current (PWM only)	V_{IN} = 3 V, 4.2 V, 5 V, 7 V, 9 V, 12 V, V_{OUT} = 9 V , PS/SYNC = High	Figure 14
Load Regulation		
Load Regulation, PFM/PWM Operation	V_{IN} = 3 V, 4.2 V, 5 V, 7 V, 9 V, 12 V, V_{OUT} = 7 V , PS/SYNC = Low	Figure 15
Load Regulation, PWM Operation	V_{IN} = 3 V, 4.2 V, 5 V, 7 V, 9 V, 12 V, V_{OUT} = 7 V , PS/SYNC = High	Figure 16
Load Regulation, PFM/PWM Operation	V_{IN} = 3 V, 4.2 V, 5 V, 7 V, 9 V, 12 V, V_{OUT} = 9 V , PS/SYNC = Low	Figure 17
Load Regulation, PWM Operation	V_{IN} = 3 V, 4.2 V, 5 V, 7 V, 9 V, 12 V, V_{OUT} = 9 V , PS/SYNC = High	Figure 18
Output Current		
Typical Start-up Current vs Input Voltage	V_{OUT} = 7 V, T_J = -40 °C, 25 °C, 85 °C, 125 °C	Figure 19
Maximum Load Current vs Input Voltage	V_{OUT} = 7 V, T_J = -40 °C, 25 °C, 85 °C, 125 °C, PG = high	Figure 20
Typical Start-up Current vs Input Voltage	V_{OUT} = 9 V, T_J = -40 °C, 25 °C, 85 °C, 125 °C	Figure 21
Maximum Load Current vs Input Voltage	V_{OUT} = 9V, T_J = -40 °C, 25 °C, 85 °C, 125 °C, PG = high	Figure 22
Regulation Accuracy		
Load Transient, PFM/PWM Boost Operation	V_{IN} = 4.2 V, V_{OUT} = 7 V, Load = 100 mA to 1 A, PS/SYNC = Low	Figure 23
Load Transient, PFM/PWM Buck Operation	V_{IN} = 12 V, V_{OUT} = 7 V, Load = 200 mA to 1.8 A, PS/SYNC = Low	Figure 24
Load Transient, PFM/PWM Boost Operation	V_{IN} = 4.2 V, V_{OUT} = 9 V, Load = 100 mA to 1 A, PS/SYNC = Low	Figure 25
Load Transient, PFM/PWM Buck Operation	V_{IN} = 12 V, V_{OUT} = 9 V, Load = 200 mA to 1.8 A, PS/SYNC = Low	Figure 26
Line Transient, PFM/PWM Operation	V_{IN} = 5 V to 9 V, V_{OUT} = 7 V, Load = 1 A, PS/SYNC = Low	Figure 27
Line Transient, PFM/PWM Operation	V_{IN} = 8 V to 12 V, V_{OUT} = 9 V, Load = 1 A, PS/SYNC = Low	Figure 28
Output Voltage Ripple		
Output Voltage Ripple, PFM/PWM Operation	V_{IN} = 5 V, V_{OUT} = 7 V, Load = 0.3 A, PS/SYNC = Low	Figure 29
Output Voltage Ripple, PWM Operation	V_{IN} = 5 V, V_{OUT} = 7 V, Load = 1 A, PS/SYNC = high	Figure 30
Output Voltage Ripple, PFM/PWM Operation	V_{IN} = 12 V, V_{OUT} = 7 V, Load = 0.3 A, PS/SYNC = Low	Figure 31
Output Voltage Ripple, PFM/PWM Operation	V_{IN} = 5 V, V_{OUT} = 9 V, Load = 0.1 A, PS/SYNC = Low	Figure 32
Output Voltage Ripple, PWM Operation	V_{IN} = 5 V, V_{OUT} = 9 V, Load = 0.5 A, PS/SYNC = high	Figure 33
Output Voltage Ripple, PFM/PWM Operation	V_{IN} = 12 V, V_{OUT} = 9 V, Load = 0.1 A, PS/SYNC = Low	Figure 34

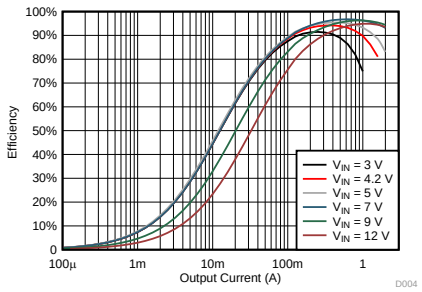
Table 7. Typical Application Curves for Adjustable Version (continued)

Parameter	Conditions	Figure
Startup		
Start-up Behavior from Rising Enable, PFM/PWM Operation	V_{IN} = 4.5 V, V_{OUT} = 7 V, Load = 0.5 A, PS/SYNC = Low	Figure 35
Start-up Behavior from Rising Enable, PFM/PWM Operation	V_{IN} = 7 V, V_{OUT} = 9 V, Load = 0.5 A, PS/SYNC = Low	Figure 36



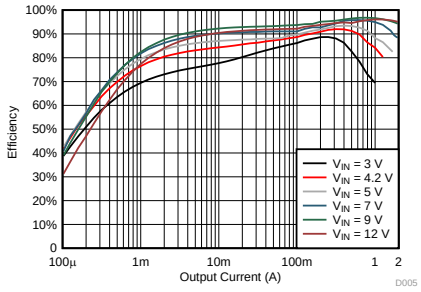
Vout = 7 V PFM T = 25 °C

Figure 11. Efficiency vs Output Current



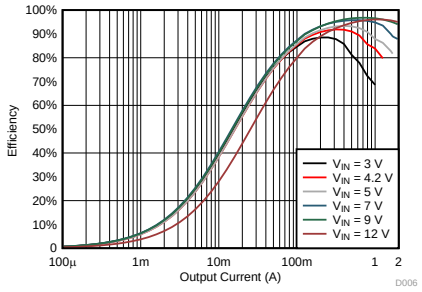
Vout = 7 V PWM T = 25 °C

Figure 12. Efficiency vs Output Current



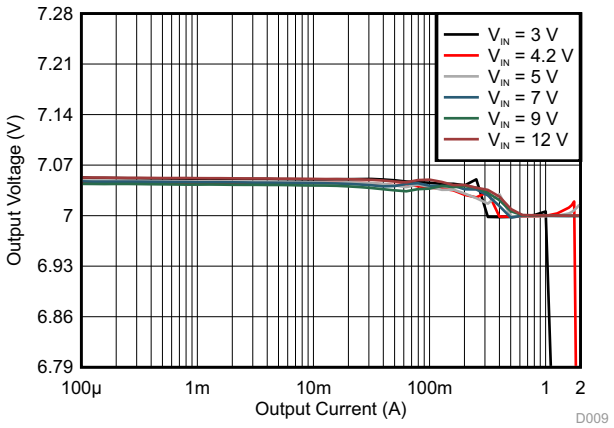
Vout = 9 V PFM T = 25 °C

Figure 13. Efficiency vs Output Current



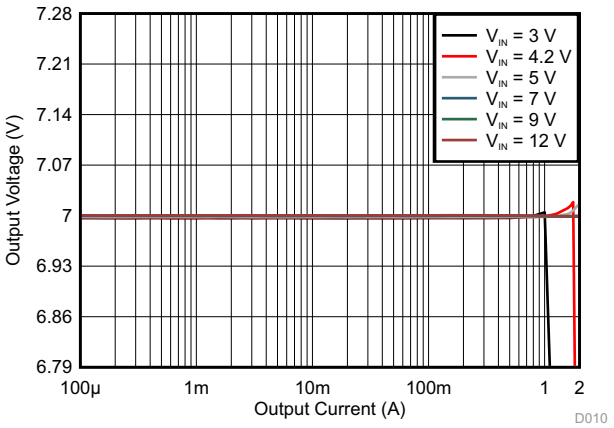
Vout = 9 V PWM T = 25 °C

Figure 14. Efficiency vs Output Current



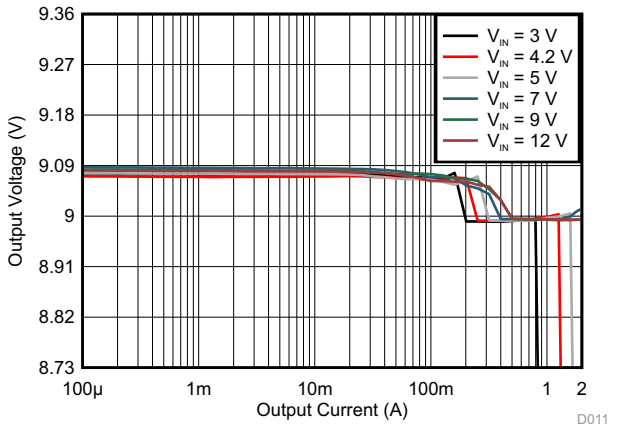
Vout = 7 V PFM T = 25 °C

Figure 15. Output Voltage vs Output Current



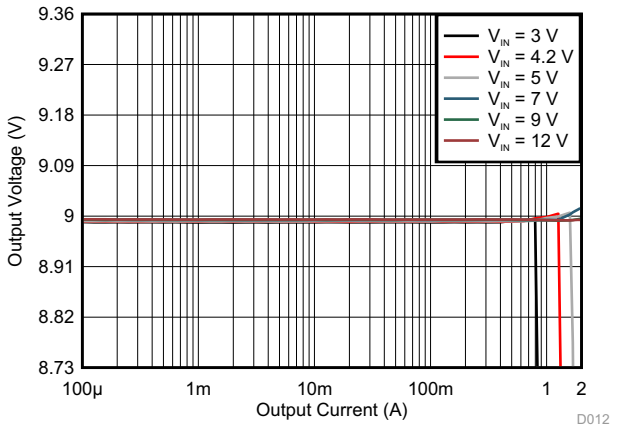
Vout = 7 V PWM T = 25 °C

Figure 16. Output Voltage vs Output Current



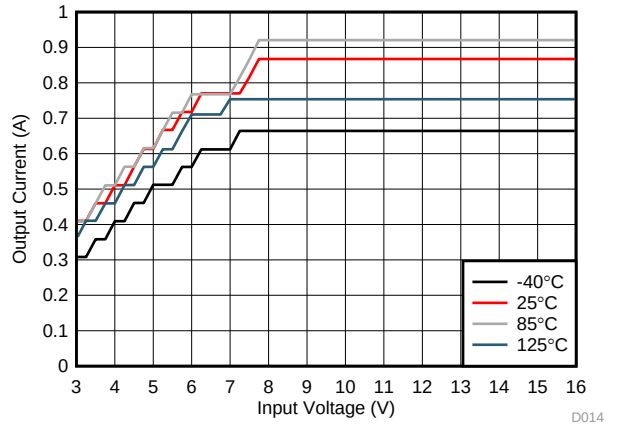
Vout = 9 V PFM T = 25 °C

Figure 17. Output Voltage vs Output Current



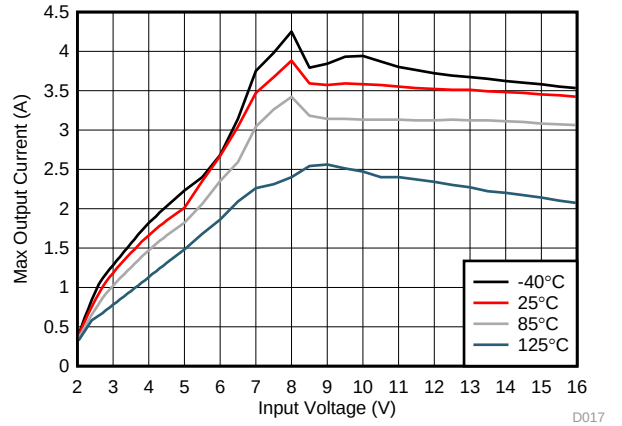
Vout = 9 V PWM T = 25 °C

Figure 18. Output Voltage vs Output Current



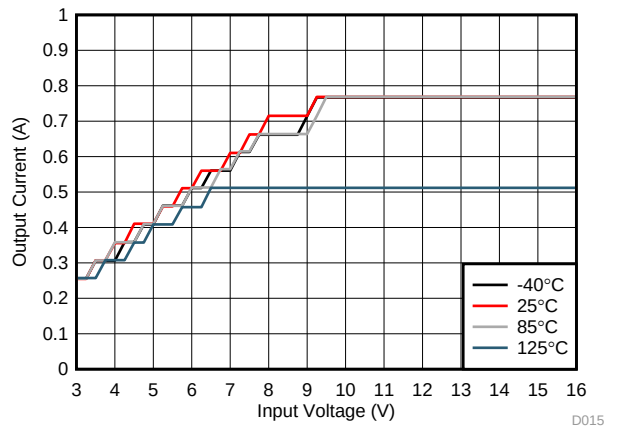
Vout = 7 V resistive load

Figure 19. Typical Start-up Current



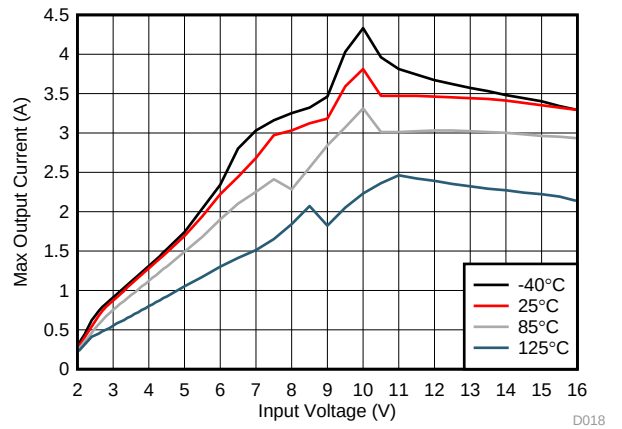
Vout = 7 V after start-up with PG = high

Figure 20. Maximum Load Current vs Input Voltage



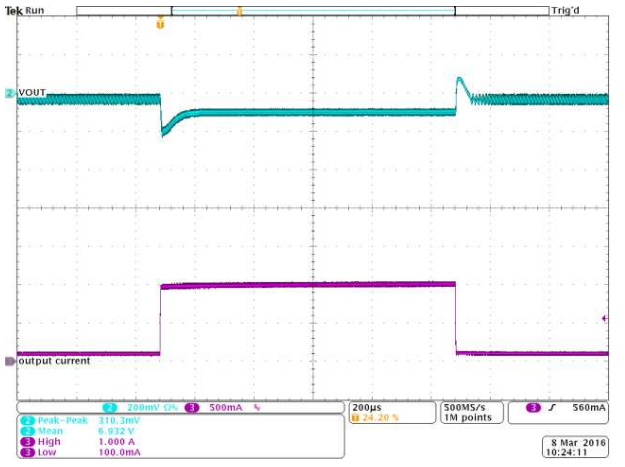
Vout = 9 V resistive load

Figure 21. Typical Start-up Current



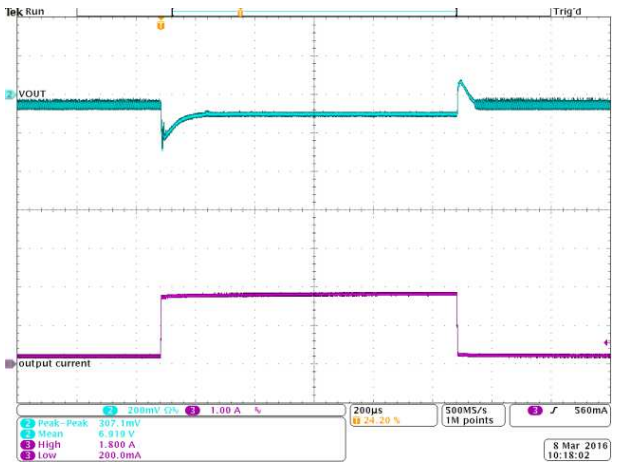
Vout = 9 V after start-up with PG = high

Figure 22. Maximum Load Current vs Input Voltage



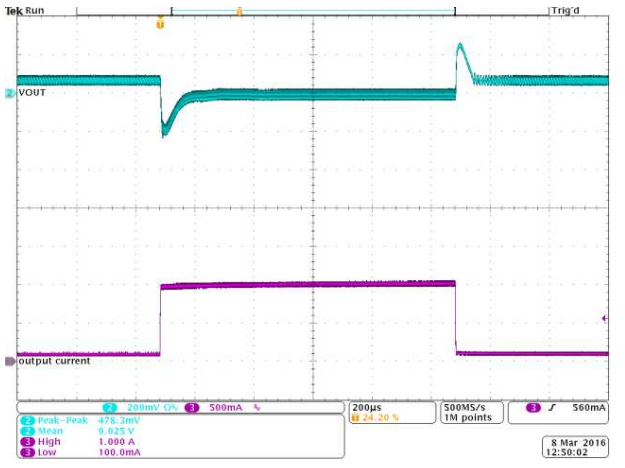
Vout = 7 V PFM Vin = 4.2V

Figure 23. Load Transient Response



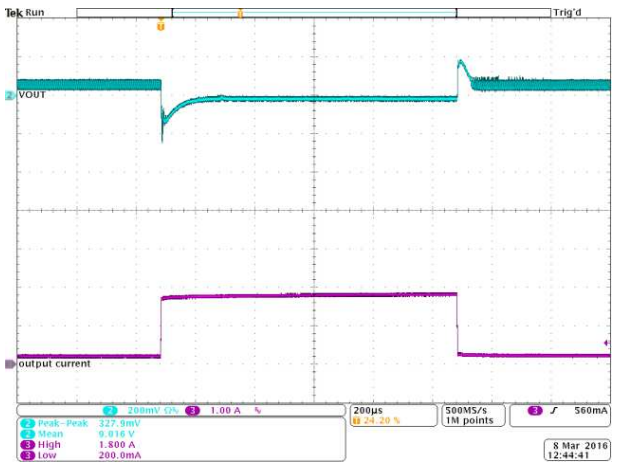
Vout = 7 V PFM Vin = 12V

Figure 24. Load Transient Response



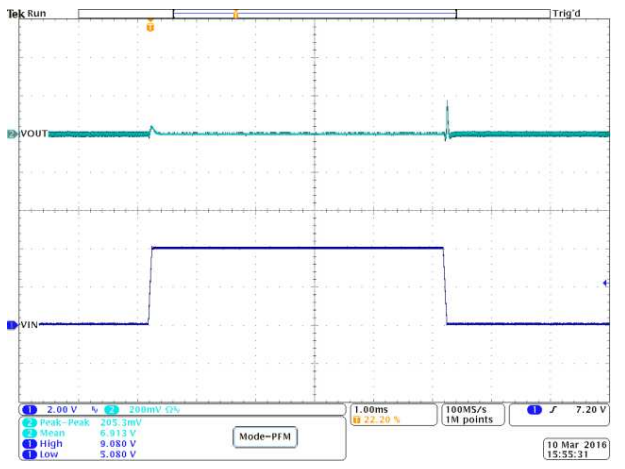
Vout = 9 V PFM Vin = 4.2V

Figure 25. Load Transient Response



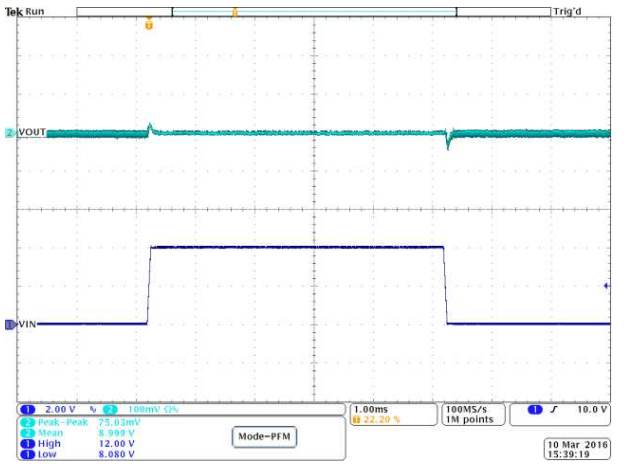
Vout = 9 V PFM Vin = 12V

Figure 26. Load Transient Response



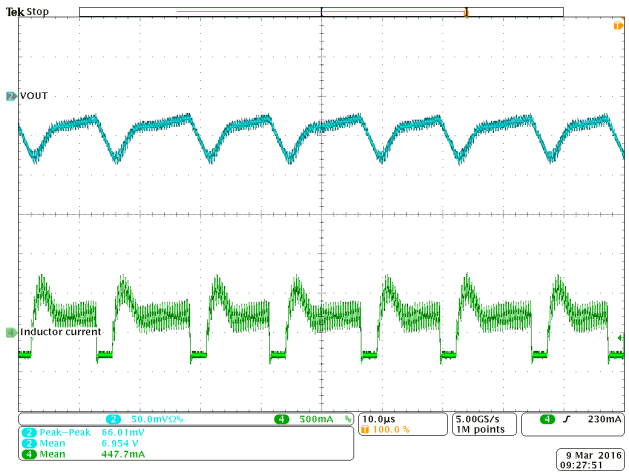
Vout = 7 V PFM Io = 1A

Figure 27. Line Transient Response



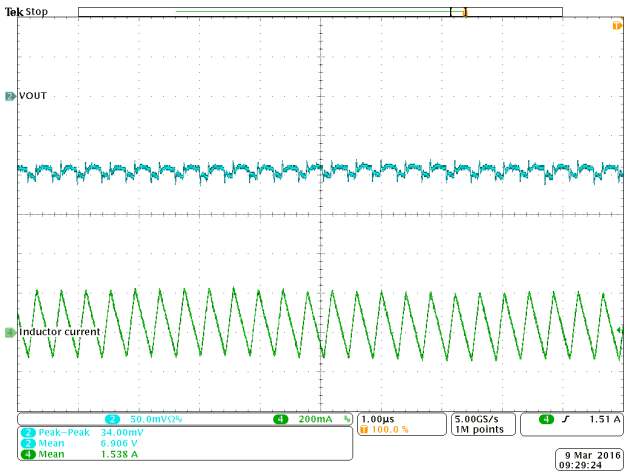
Vout = 9 V PFM Io = 1A

Figure 28. Line Transient Response



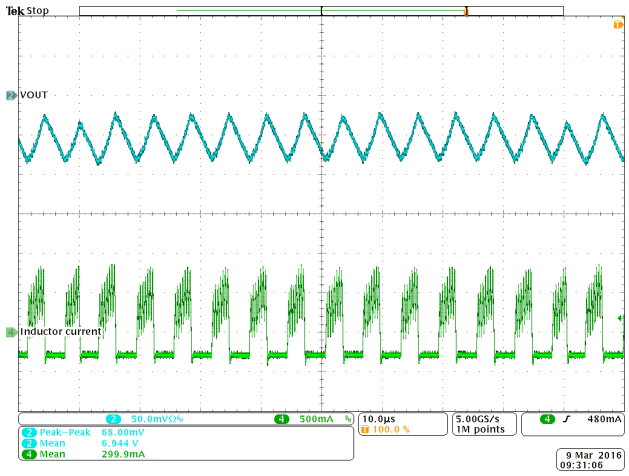
Vin = 5V; Vout = 7 V PFM Io = 0.3A

Figure 29. Output Voltage Ripple



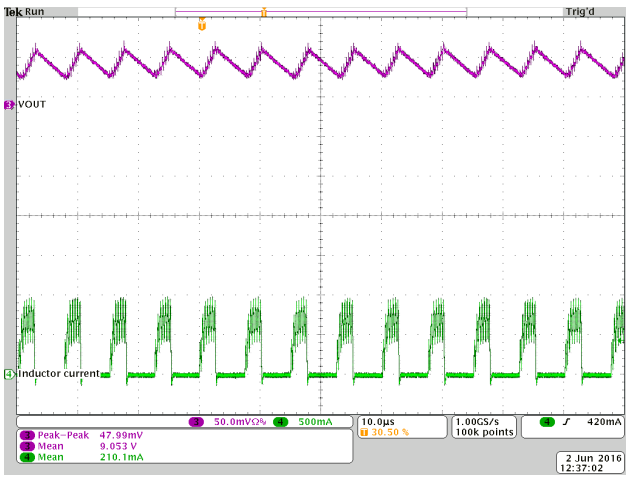
Vin = 5V; Vout = 7 V PWM Io = 1A

Figure 30. Output Voltage Ripple



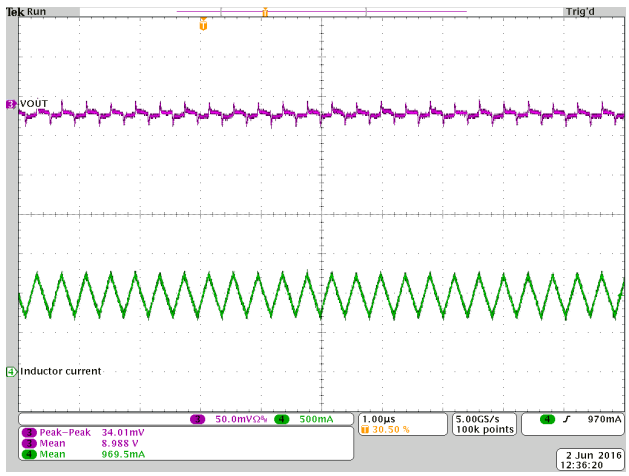
Vin = 12V; Vout = 7 V PFM Io = 0.3A

Figure 31. Output Voltage Ripple



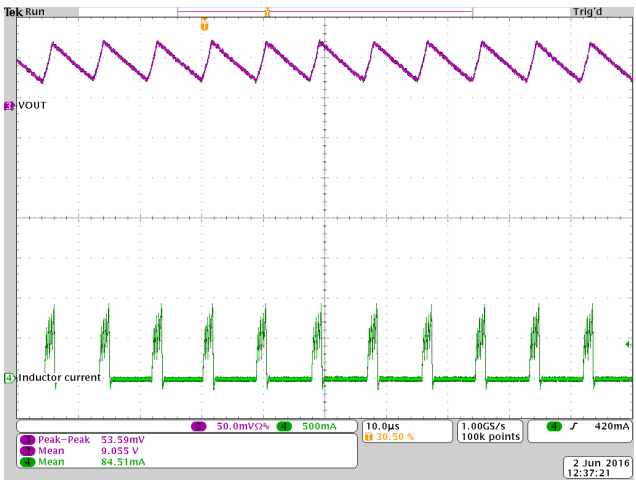
Vin = 5V; Vout = 9 V PFM Io = 0.1A

Figure 32. Output Voltage Ripple



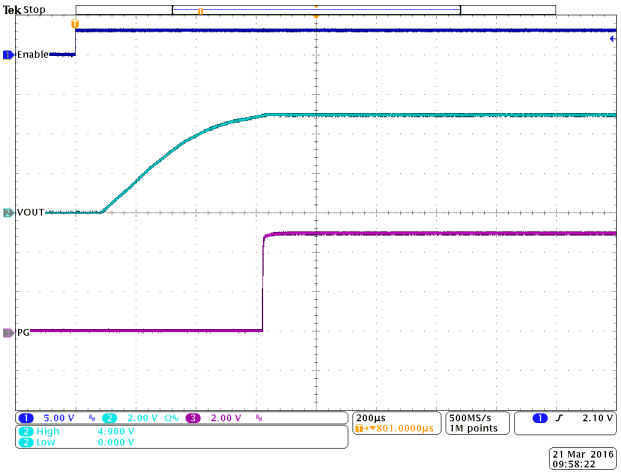
Vin = 5V; Vout = 9 V PWM Io = 0.5A

Figure 33. Output Voltage Ripple



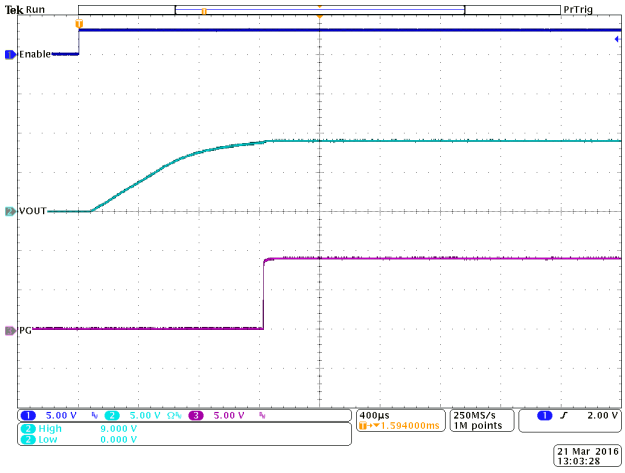
Vin = 12V; Vout = 9 V PFM Io = 0.1A

Figure 34. Output Voltage Ripple



Vin = 4.5V; Vout = 7 V PFM Io = 0.5A

Figure 35. Start-up Timing



Vin = 7V; Vout = 9 V PFM Io = 0.5A

Figure 36. Start-up Timing

9.3 Typical Application for Fixed Voltage Version

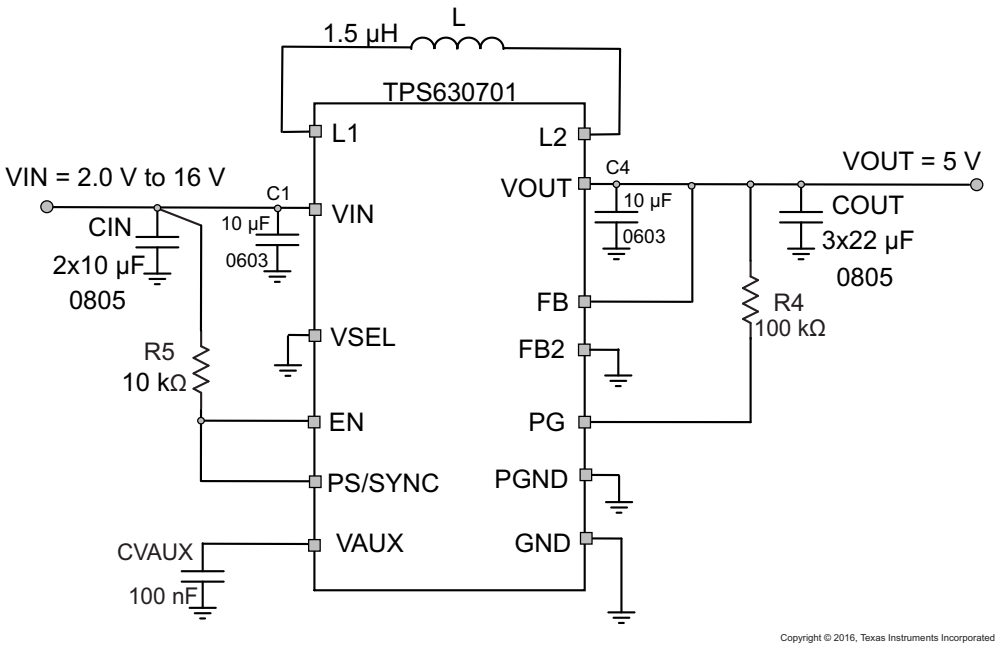


Figure 37. Typical Application For Fixed Voltage Version With Minimum External Part Count And Minimum Soft Start Time

9.3.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions. The input and output capacitors have been split into a small 0603 size capacitor close to the device pins and 0805 size capacitors to get the required capacitance.

Table 8. Bill of Materials

REFERENCE	DESCRIPTION	VALUE	MANUFACTURER
IC	TPS630701RNM		Texas Instruments
L	XFL4020-1.5µH	1.5 µH	Coilcraft
CIN	GRM21BC71E106ME11L	2 x 10 µF / 25 V / X7S / 0805	Murata
C1	TMK107BBJ106MA-T	10 µF / 25 V / X5R / 0603	Taiyo Yuden
COUT	GRM21BC81C226ME44L	3 x 22 µF / 16 V / X6S / 0805	Murata
C4	TMK107BBJ106MA-T	10 µF / 25 V / X5R / 0603	Taiyo Yuden
CVAUX	TMK105B7104MV-FR	100 nF / 25V / X7R / 0402	Taiyo Yuden
R4	Metal Film Resistor ; 1%	100 kΩ	-

9.3.2 Detailed Design Procedure

The TPS6307x series of buck-boost converter has internal loop compensation. Therefore, the external L-C filter has to be selected according to the internal compensation. It's important to consider that the effective inductance, due to inductor tolerance and current derating can vary between 20% and -30%. The same for the capacitance of the output filter: the effective capacitance can vary between +20% and -80% of the specified datasheet value, due to capacitor tolerance and bias voltage. For this reason, *Output Filter Selection* shows the nominal capacitance and inductance value allowed. For the fixed voltage version TPS630701, the effective capacitance on the output (in µF) needs to be at least 15 times higher than the effective inductance (in µH) to ensure a good transient response and stable operation.

9.3.3 Application Curves

Table 9. Typical Application Curves for Fixed Voltage Version

Parameter	Conditions	Figure
Efficiency		
Efficiency vs Output Current (PFM/PWM)	V_{IN} = 3 V, 4.2 V, 5 V, 7 V, 9 V, 12 V, V_{OUT} = 5 V , PS/SYNC = Low	Figure 38
Efficiency vs Output Current (PWM only)	V_{IN} = 3 V, 4.2 V, 5 V, 7 V, 9 V, 12 V, V_{OUT} = 5 V , PS/SYNC = High	Figure 39
Load Regulation		
Load Regulation, PFM/PWM Operation	V_{IN} = 3 V, 4.2 V, 5 V, 7 V, 9 V, 12 V, V_{OUT} = 5 V , PS/SYNC = Low	Figure 40
Load Regulation, PWM Operation	V_{IN} = 3 V, 4.2 V, 5 V, 7 V, 9 V, 12 V, V_{OUT} = 5 V , PS/SYNC = High	Figure 41
Output Current		
Typical Start-up Current vs Input Voltage	V_{OUT} = 5 V, T_J = -40 °C, 25 °C, 85 °C, 125 °C	Figure 42
Maximum Load Current vs Input Voltage	V_{OUT} = 5 V, T_J = -40 °C, 25 °C, 85 °C, 125 °C, PG = high	Figure 43
Regulation Accuracy		
Load Transient, PFM/PWM Boost Operation	V_{IN} = 4.2 V, V_{OUT} = 5 V, Load = 100 mA to 1 A, PS/SYNC = Low	Figure 44
Load Transient, PFM/PWM Buck Operation	V_{IN} = 12 V, V_{OUT} = 5 V, Load = 200 mA to 1.8 A, PS/SYNC = Low	Figure 45
Line Transient, PFM/PWM Operation	V_{IN} = 4.2 V to 7 V, V_{OUT} = 5 V, Load = 1 A, PS/SYNC = Low	Figure 46
Output Voltage Ripple		
Output Voltage Ripple, PFM/PWM Operation	V_{IN} = 4.2 V, V_{OUT} = 5 V, Load = 0.3 A, PS/SYNC = Low	Figure 47
Output Voltage Ripple, PWM Operation	V_{IN} = 4.2 V, V_{OUT} = 5 V, Load = 1 A, PS/SYNC = high	Figure 48
Output Voltage Ripple, PFM/PWM Operation	V_{IN} = 7.2 V, V_{OUT} = 5 V, Load = 0.3 A, PS/SYNC = Low	Figure 49
Startup		
Start-up Behavior from Rising Enable, PFM/PWM Operation	V_{IN} = 4.5 V, V_{OUT} = 5 V, Load = 0.5 A, PS/SYNC = Low	Figure 50

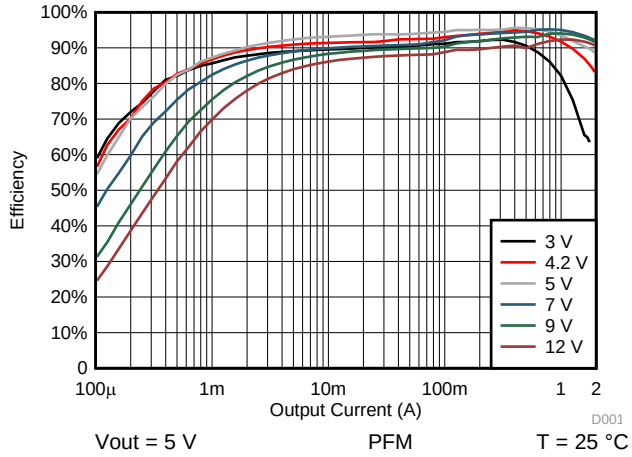


Figure 38. Efficiency vs Output Current

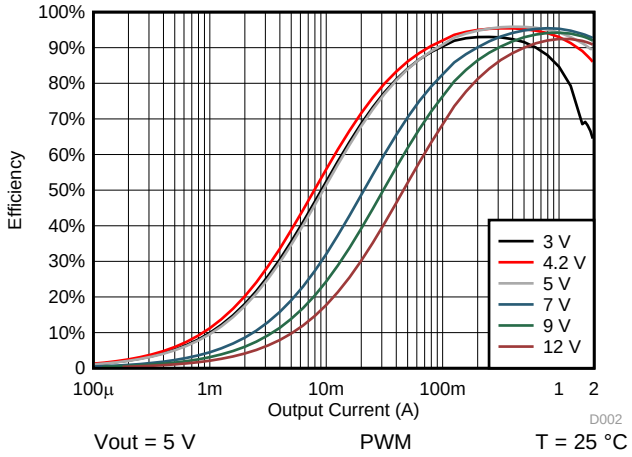


Figure 39. Efficiency vs Output Current

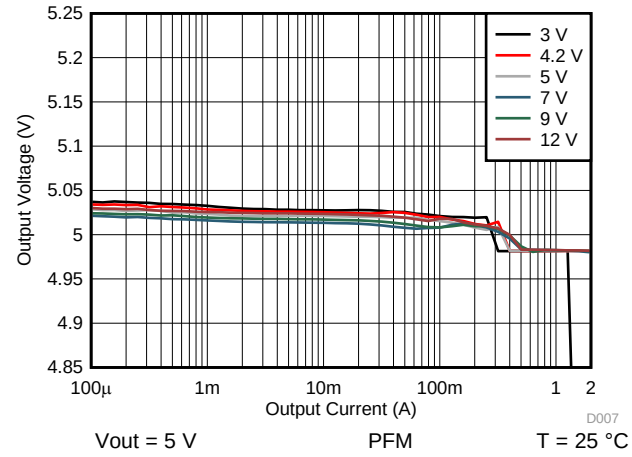


Figure 40. Output Voltage vs Output Current

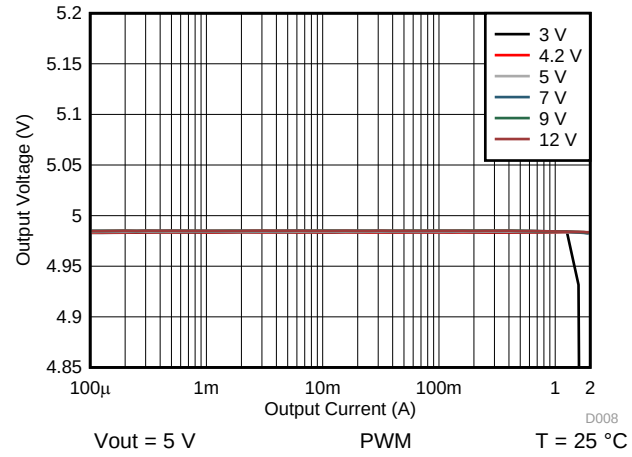


Figure 41. Output Voltage vs Output Current

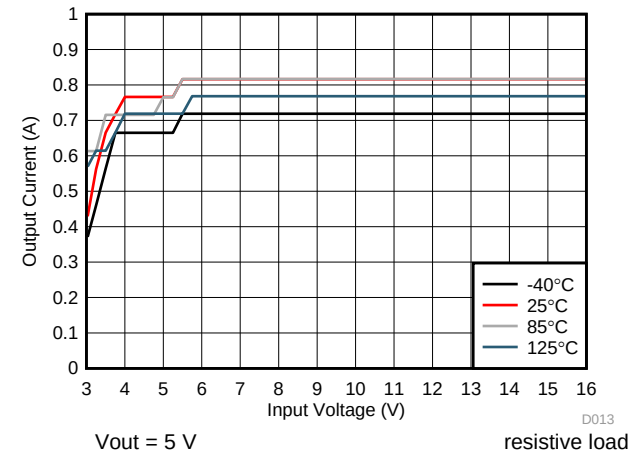


Figure 42. Typical Start-up Current

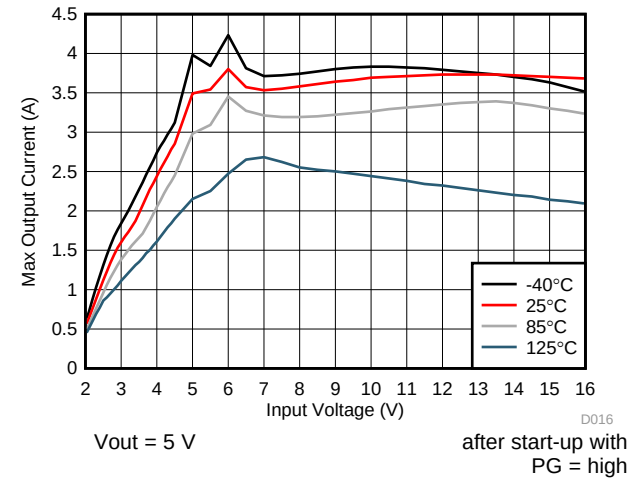
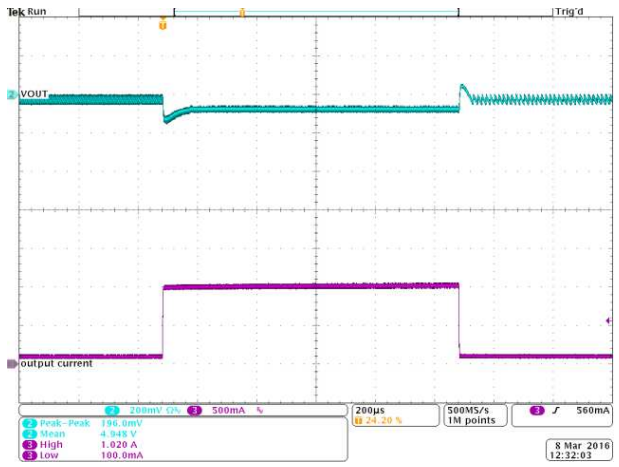
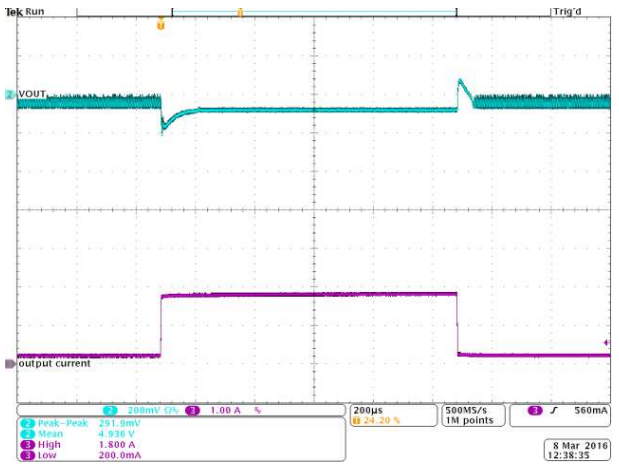


Figure 43. Maximum Load Current vs Input Voltage



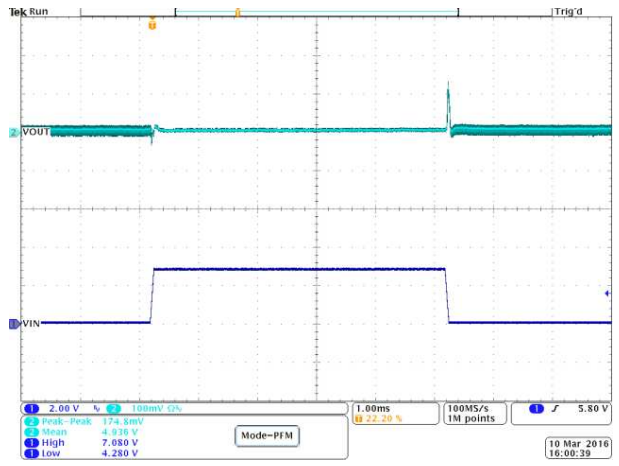
Vout = 5 V PFM Vin = 4.2V

Figure 44. Load Transient Response



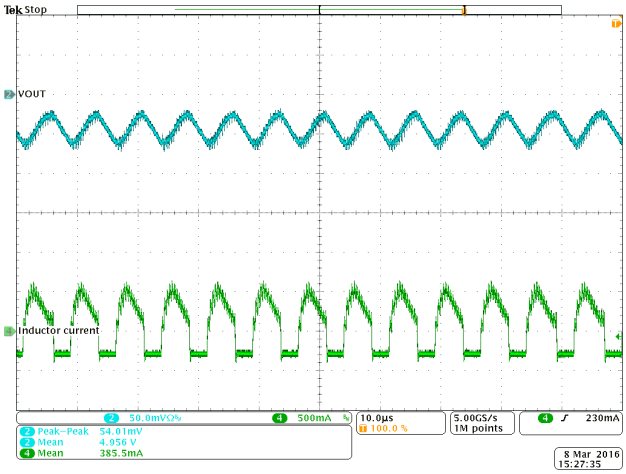
Vout = 5 V PFM Vin = 12V

Figure 45. Load Transient Response



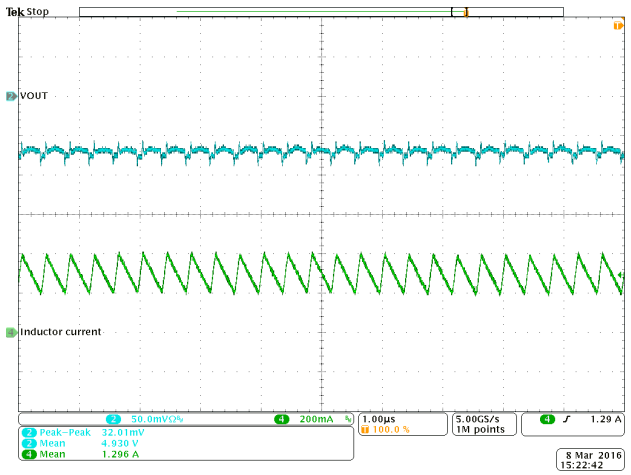
Vout = 5 V PFM Io = 1A

Figure 46. Line Transient Response



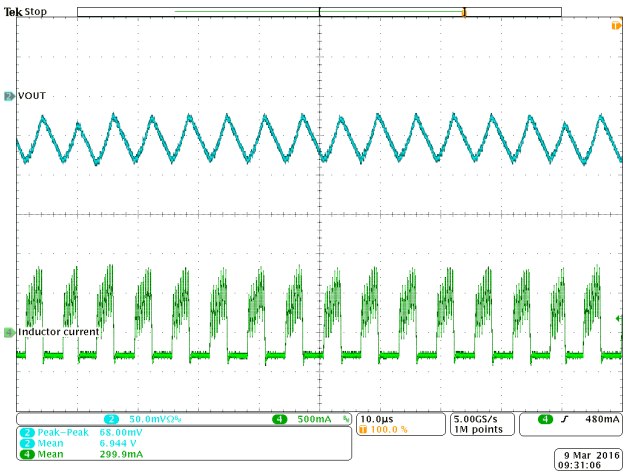
Vin = 4.2V; Vout = 5 V PFM Io = 0.3A

Figure 47. Output Voltage Ripple



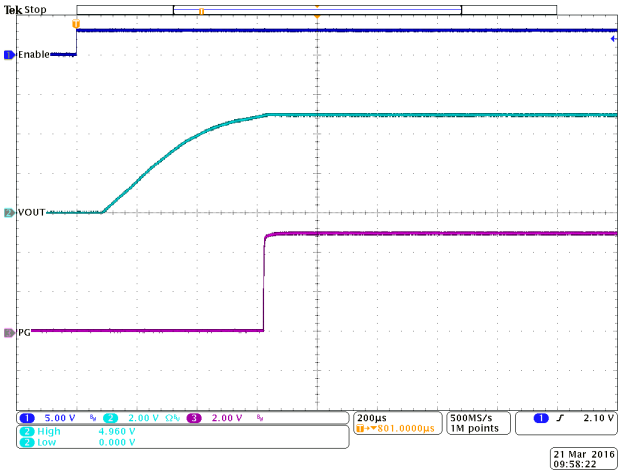
Vin = 4.2V; Vout = 5 V PWM Io = 1A

Figure 48. Output Voltage Ripple



Vin = 7.2V; Vout = 5 V PFM Io = 0.3A

Figure 49. Output Voltage Ripple



Vin = 4.5V; Vout = 5 V PFM Io = 0.5A

Figure 50. Start-up Timing

10 Power Supply Recommendations

The TPS63070 device family has no special requirements for its power supply. The power supply output current needs to be rated according to the supply voltage, output voltage and output current of TPS63070. Please see the layout guidelines about the placement of the external components.

10.1 Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the PowerPAD™
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table please check the Thermal Characteristics Application Note (SZZA017) and the IC Package Thermal Metrics Application Note (SPRA953).

11 Layout

11.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground connection. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pin of the IC.

A ceramic capacitor each, as close as possible from the VIN pin to GND and one from the VOUT pin to GND, shown as C1 and C4 in the layout proposal are used to suppress high frequency noise. The case size should be 0603 or smaller for good high frequency performance. Additional 0805 size input and output capacitors are used to get the required capacitance on the input and output depending on the supply voltage range and the output voltage.

The feedback divider should be placed as close as possible to the feedback pin of the IC. To lay out the control ground, short traces are recommended as well, separation from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

In case any of the digital inputs EN, VSEL or PS/SYNC need to be tied to the input supply voltage VIN, a 10k resistor must be used in series. One common resistor for all digital inputs that are tied to VIN is sufficient.

11.2 Layout Example

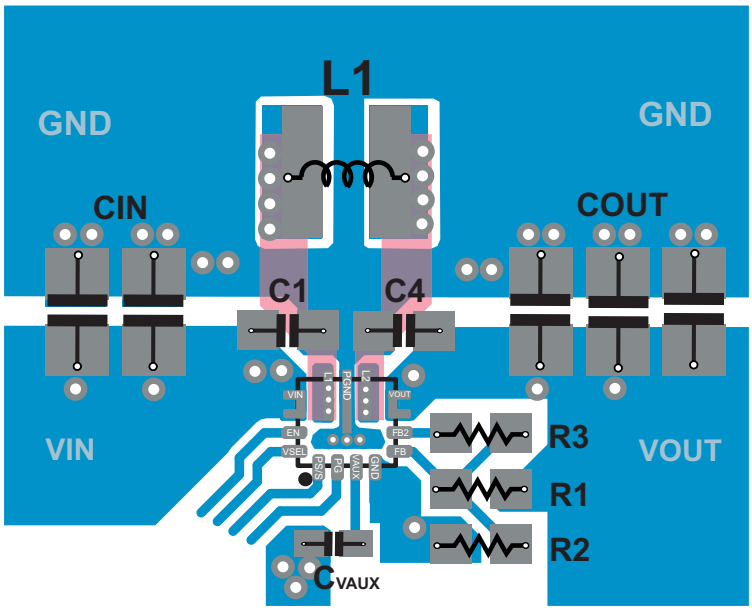


Figure 51. EVM Layout

12 器件和文档支持

12.1 器件支持

12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **10.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TPS63070	单击此处	单击此处	单击此处	单击此处	单击此处
TPS630701	单击此处	单击此处	单击此处	单击此处	单击此处
TPS630702	单击此处	单击此处	单击此处	单击此处	单击此处

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

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All other trademarks are the property of their respective owners.

12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS630701RNMR	ACTIVE	VQFN-HR	RNM	15	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	0701	Samples
TPS630701RNMT	ACTIVE	VQFN-HR	RNM	15	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	0701	Samples
TPS630702RNMR	ACTIVE	VQFN-HR	RNM	15	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	0702	Samples
TPS630702RNMT	ACTIVE	VQFN-HR	RNM	15	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	0702	Samples
TPS63070RNMR	ACTIVE	VQFN-HR	RNM	15	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3070	Samples
TPS63070RNMT	ACTIVE	VQFN-HR	RNM	15	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3070	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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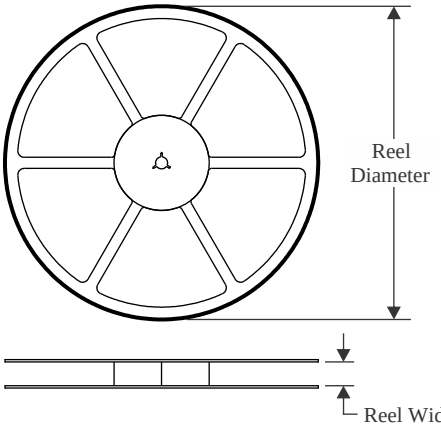
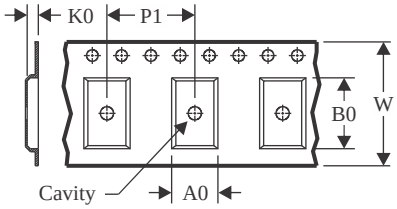
TAPE AND REEL INFORMATION

REEL DIMENSIONS

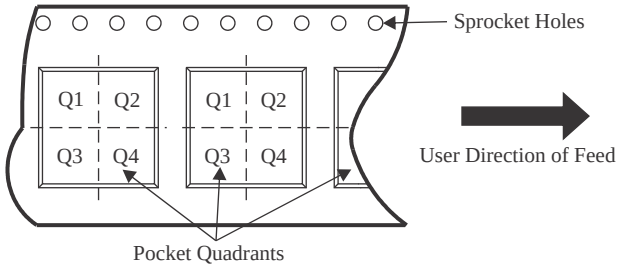


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

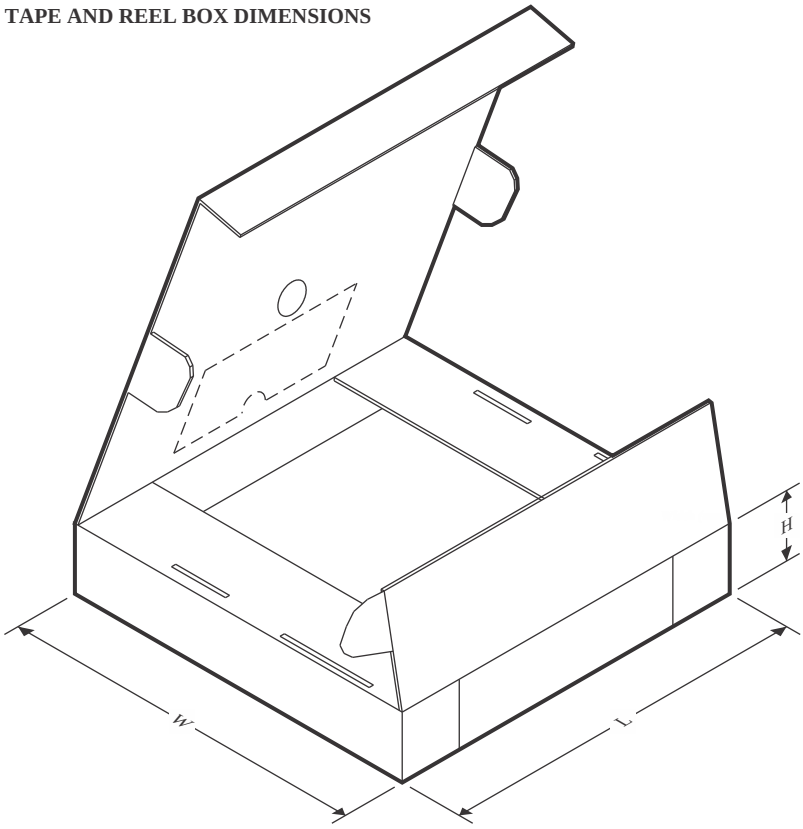
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS630701RNMR	VQFN-HR	RNM	15	3000	330.0	12.4	2.8	3.3	1.2	8.0	12.0	Q1
TPS630701RNMT	VQFN-HR	RNM	15	250	180.0	12.4	2.8	3.3	1.2	8.0	12.0	Q1
TPS630702RNMR	VQFN-HR	RNM	15	3000	330.0	12.4	2.8	3.3	1.2	8.0	12.0	Q1
TPS630702RNMT	VQFN-HR	RNM	15	250	180.0	12.4	2.8	3.3	1.2	8.0	12.0	Q1
TPS63070RNMR	VQFN-HR	RNM	15	3000	330.0	12.4	2.8	3.3	1.2	8.0	12.0	Q1
TPS63070RNMR	VQFN-HR	RNM	15	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
TPS63070RNMT	VQFN-HR	RNM	15	250	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
TPS63070RNMT	VQFN-HR	RNM	15	250	180.0	12.4	2.8	3.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

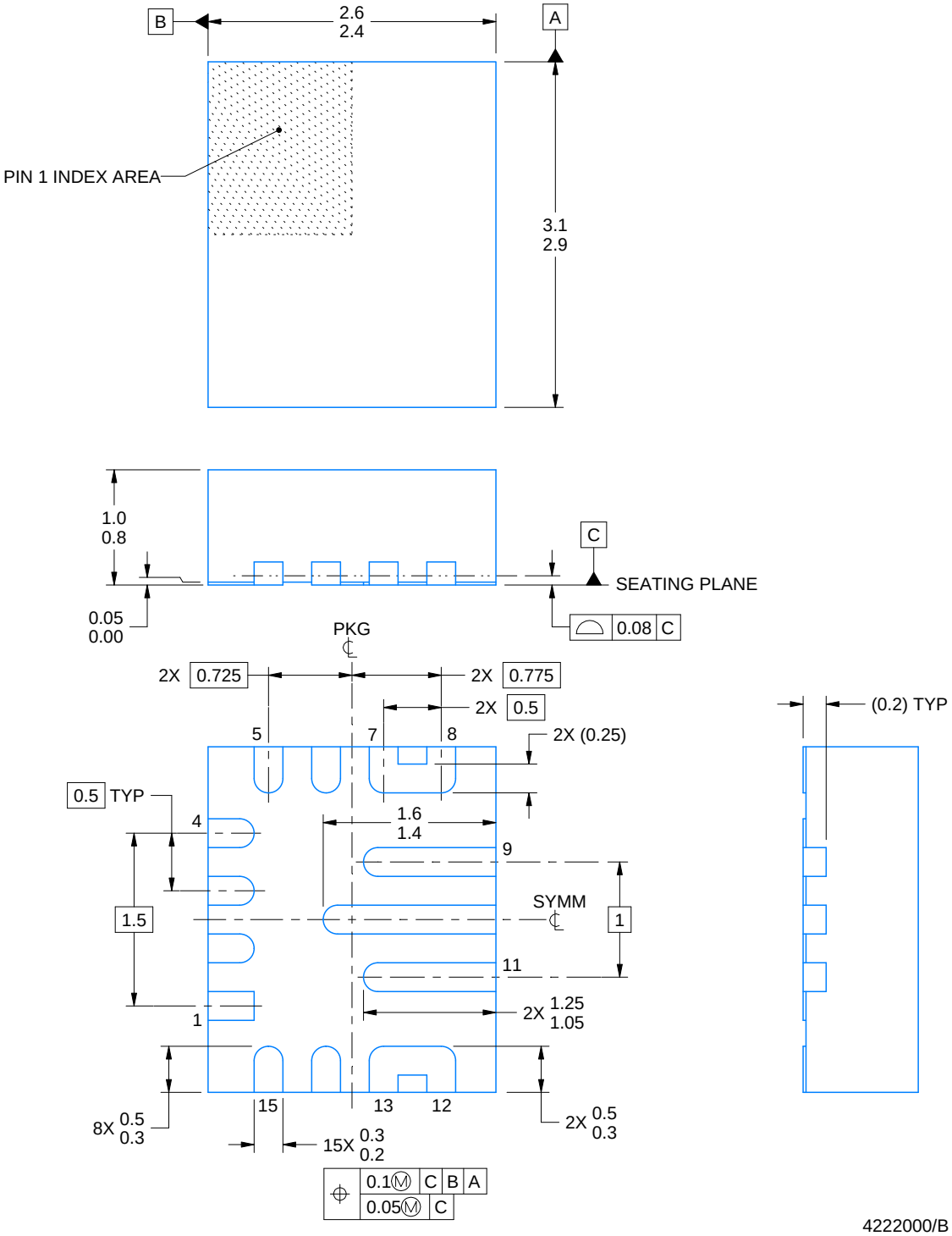
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS630701RNMR	VQFN-HR	RNM	15	3000	367.0	367.0	35.0
TPS630701RNMT	VQFN-HR	RNM	15	250	182.0	182.0	20.0
TPS630702RNMR	VQFN-HR	RNM	15	3000	367.0	367.0	35.0
TPS630702RNMT	VQFN-HR	RNM	15	250	182.0	182.0	20.0
TPS63070RNMR	VQFN-HR	RNM	15	3000	367.0	367.0	35.0
TPS63070RNMR	VQFN-HR	RNM	15	3000	210.0	185.0	35.0
TPS63070RNMT	VQFN-HR	RNM	15	250	210.0	185.0	35.0
TPS63070RNMT	VQFN-HR	RNM	15	250	182.0	182.0	20.0

PACKAGE OUTLINE

RNM0015A

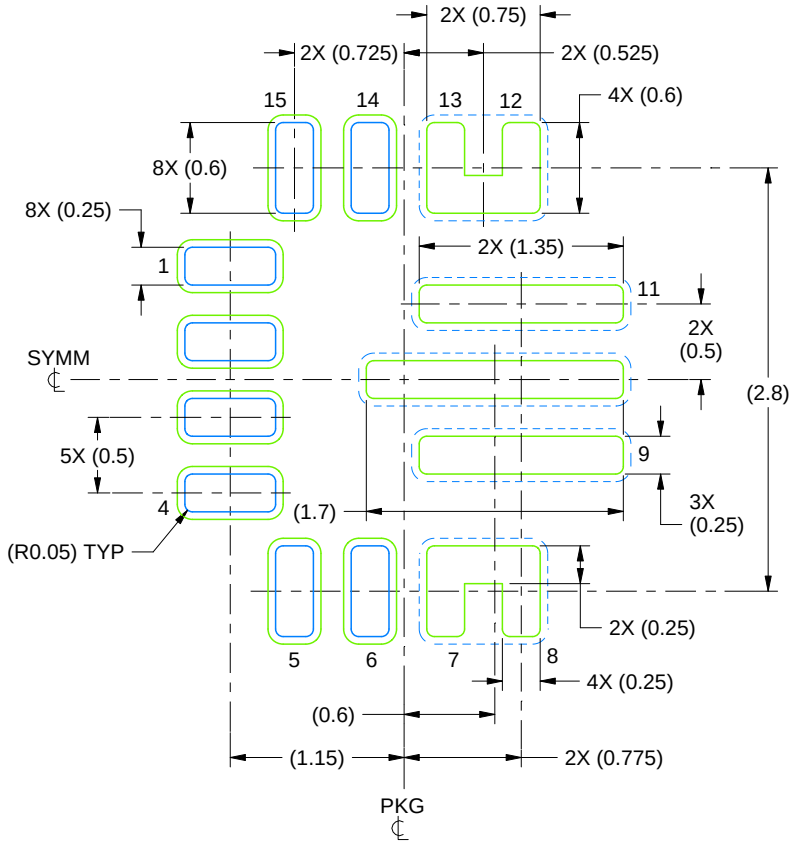
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

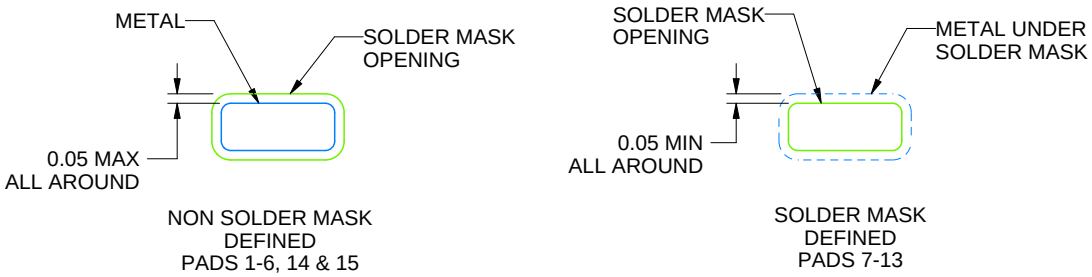


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:20X

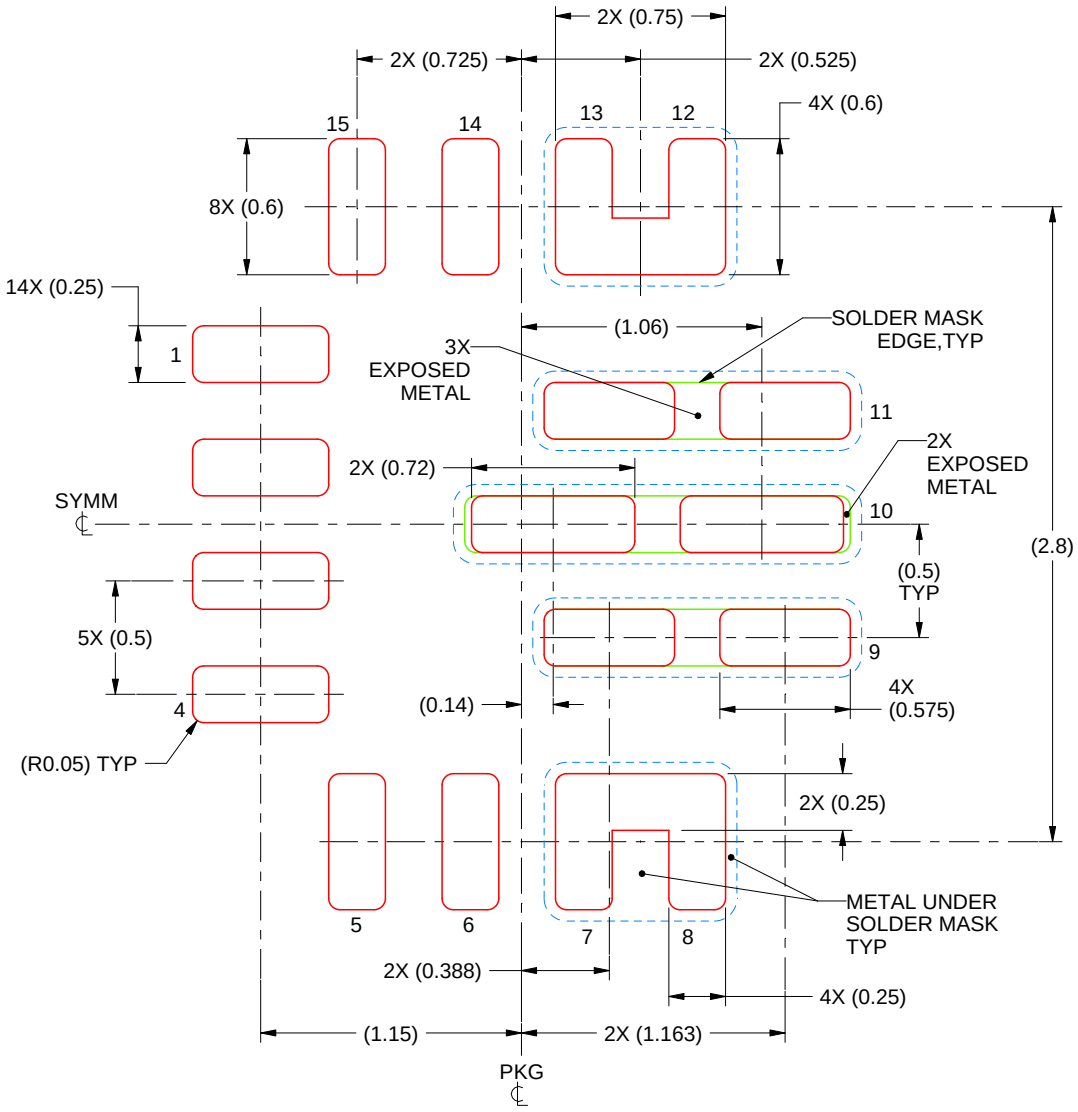


SOLDER MASK DETAILS

4222000/B 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR EXPOSED PADS 9-11
85% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

4222000/B 03/2020

NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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