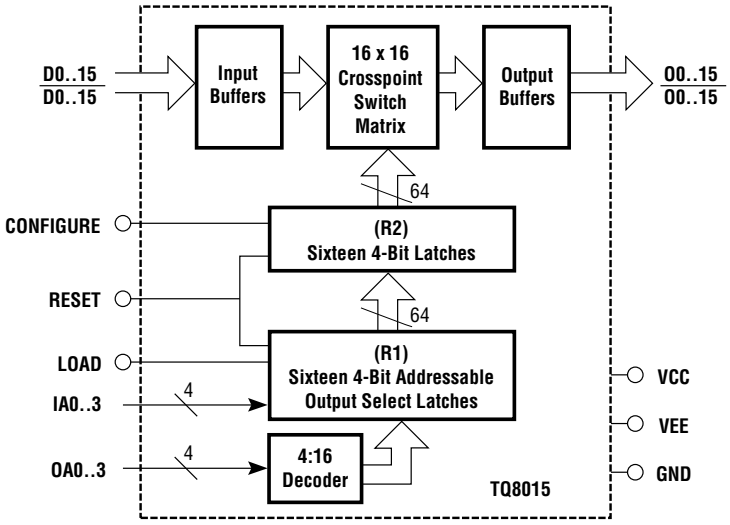
TQ8015

1.25 Gigabit/sec 16x16 Digital ECL Crosspoint Switch

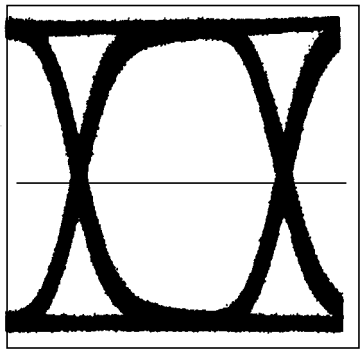


The TQ8015 is a non-blocking 16 x 16 digital crosspoint switch capable of data rates greater than 1.25 Gigabits per second per port. Utilizing a fully differential internal data path and ECL I/O, the TQ8015 offers a high data rate with exceptional signal fidelity. The symmetrical switching and noise rejection characteristics inherent in differential logic result in low jitter and signal skew. The TQ8015 is ideally suited for digital video, data communications and telecommunication switching applications.

The non-blocking architecture uses 16 fully independent 16:1 multiplexers (see diagram on page 2), allowing each output port to be independently programmed to any input port. The switch is configured by sequentially loading each multiplexer's 4-bit program latch (OA0:3) with the desired input port address (IA0:3) and enabling the LOAD pin. When complete, the CONFIGURE pin is strobed and all new configurations are simultaneously transferred into the switch multiplexers. Data integrity is maintained on all unchanged data paths.

Electrical Characteristics

	Min	*Max*	*Units*
Data Rate/Port	1.25		Gb/s
Jitter		150	ps peak-peak
Channel Propagation Delay		2000	ps
Ch-to-Ch Propagation Delay Skew		500	ps



Typical output waveform with all channels driven

Features

- *>20 Gb/s aggregate BW*
- *1.25 Gb/s/port NRZ data rate*
- *Non-blocking architecture*
- *500 ps delay match*
- *Differential ECL-level data I/O; CMOS-level control inputs*
- *Low jitter and signal skew*
- *Fully differential data path*
- *Double buffered configuration latches*
- *132-pin MQFP package*

Applications

Telecom/Datacom Switching

Hubs and Routers

Video Switching

Figure 1. TQ8015 architecture.

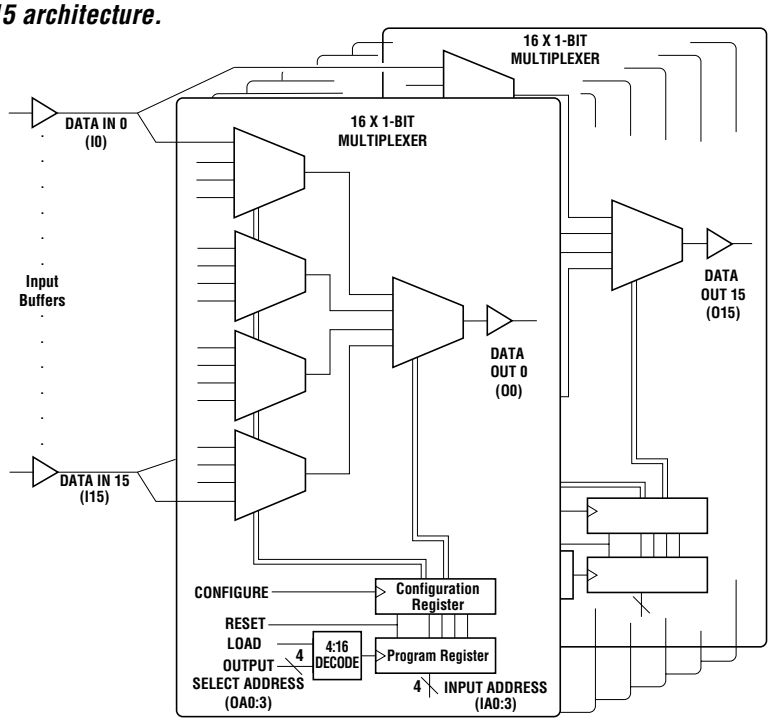


Table 1. Absolute Maximum Ratings[5]

Symbol	*Parameter*	*Absolute Max. Rating*	*Notes*
T_{STOR}	Storage Temperature	–65° C to +150° C	
T_{CH}	Junction (Channel) Temperature	–65° C to +150° C	1
T_C	Case Temperature Under Bias	–65° C to +125° C	2
V_{CC}	Supply Voltage	0 V to +7 V	3
V_{EE}	Supply Voltage	–7 V to 0 V	3
V_{TT}	Load Termination Supply Voltage	V_{EE} to 0 V	4
V_{IN}	Voltage Applied to Any ECL Input; Continuous	V_{EE} –0.5 V to +0.5 V	
I_{IN}	Current Into Any ECL Input; Continuous	–1.0 mA to +1.0 mA	
V_{IN}	Voltage Applied to Any CMOS Input; Continuous	–0.5 V to V_{CC} +0.5 V	
I_{IN}	Current Into Any CMOS Input; Continuous	–1.0 mA to +1.0 mA	
V_{OUT}	Voltage Applied to Any ECL Output	V_{EE} –0.5 V to +0.5 V	4
I_{OUT}	Current From Any ECL Output; Continuous	–40 mA	
P_D	Power Dissipation per Output $P_{OUT} = (GND – V_{OUT}) \times I_{OUT}$	50 mW	

Notes: 1. For die applications.
2. T_C is measured at case top.
3. All voltages specified with respect to GND, defined as 0V.
4. Subject to I_{OUT} and power dissipation limitations.
5. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur.

Table 2. Recommended Operating Conditions[3]

Symbol	Parameter	Min	Typ	Max	Units	Notes
T_C	Case Operating Temperature	0		85	°C	1
V_{CC}	Supply Voltage	4.5		5.5	V	
V_{EE}	Supply Voltage	–5.5		–4.5	V	
V_{TT}	Load Termination Supply Voltage		–2.0		V	2
R_{LOAD}	Output Termination Load Resistance		50		Ω	2
Θ_{JC}	Thermal Resistance Junction to Case			7	°C/W	

Notes: 1. T_C measured at case top. Use of adequate heatsink is required.
2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions.
3. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified.

SWITCHING PRODUCTS

Table 3. Pin Descriptions

Signal	Name/Level	Description
I0 to I15, NI0 to NI15	Data input true and complement. Differential ECL	Differential data input ports.
O0 to O15, NO0 to NO15	Data output true and complement. Differential ECL	Differential data output ports.
IA0:3	Input address, CMOS	Input port selection address that is written into the selected output port program latches (OA0:3).
OA0:3	Output select address, CMOS	Output port selection address. Selects the output port program latches to which the input port selection address (IA0:3) is written.
LOAD	CMOS	Enables the selected output port program latches while set 'high'. Latches the data when set to a 'low' level.
CONFIGURE	CMOS	Transfers the program latches data to the configuration latches and implements the switch changes while set 'high'. Latches the data when set to a 'low' level.
RESET	CMOS	Sets the switch into broadcast or pass-through configuration, overwriting existing configurations. *Broadcast mode:* All output ports are connected to data input port 0. This mode is selected by applying a RESET "high" pulse with CONFIGURE held "low".

IA3	IA2	IA1	IA0	Input port
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
:	:	:	:	:
1	1	1	1	15

OA3	OA2	OA1	OA0	Output port
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
:	:	:	:	:
1	1	1	1	15

Table 4. DC Characteristics[1] – *Within recommended operating conditions, unless otherwise indicated.*

Symbol	Parameter	Min	Max	Units	Test Cond.	Notes
V_{IH}	ECL Input Voltage High	–1100	–500	mV		
V_{IL}	ECL Input Voltage Low	V_{TT}	–1500	mV		
I_{IH}	ECL Input Current High		+30	µA	V_{IH} = –0.7 V	
I_{IL}	ECL Input Current Low	–30		µA	V_{IL} = –2.0 V	
V_{ICM}	ECL Input Common Mode Voltage	–1500	–1100	mV		
V_{IDIF}	ECL Input Differential Voltage (pk-pk)	400	1200	mV		
V_{IH}	CMOS Input Voltage High	3.5	V_{CC}	V		
V_{IL}	CMOS Input Voltage Low	0	1.5	V		
I_{IH}	CMOS Input Current High		+100	µA	$V_{IH} = V_{CC}$	
I_{IL}	CMOS Input Current Low		–100	µA	V_{IL} = 0 V	
V_{OCM}	ECL Output Common Mode	–1500	–1100	mV		
V_{ODIF}	ECL Output Differential Voltage	600		mV		
V_{OH}	ECL Output Voltage High	–1000	–600	mV		
V_{OL}	ECL Output Voltage Low	V_{TT}	–1600	mV		
I_{OH}	ECL Output Current High	20	27	mA		
I_{OL}	ECL Output Current Low	0	8	mA		
I_{CC}	Power Supply Current (+)		20	mA		
I_{EE}	Power Supply Current (–)		–950	mA		

Notes: 1. Test conditions unless otherwise indicated: V_{TT} = –2.0 V, R_{LOAD} = 50 W to V_{TT}.

Table 5. AC Characteristics[1] – *Within recommended operating conditions, unless otherwise indicated.*

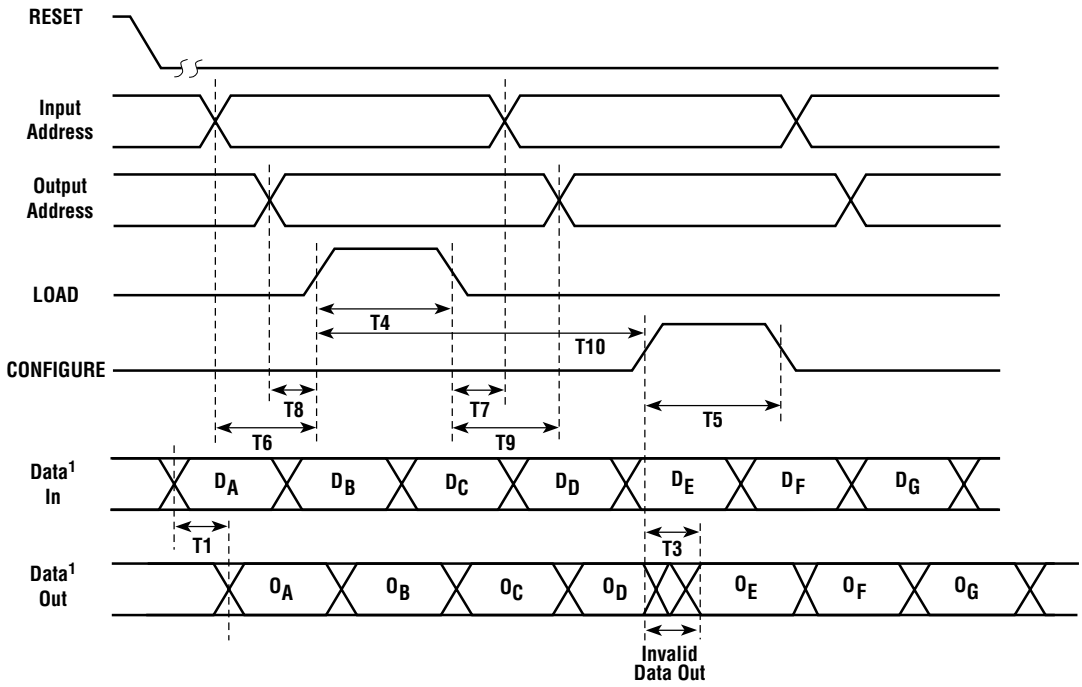
Symbol	Parameter	Min	Typ	Max	Units	Notes
	Maximum Data Rate/Port			1.25	Gb/s	1,2
	Jitter			150	ps pk-pk	1
T_1	Channel Propagation Delay			2000	ps	
T_2	Ch-to-Ch Propagation Delay Skew			500	ps	
T_3	CONFIG to Data Out (Oi) Delay			5	ns	
T_4	LOAD Pulse Width	7			ns	
T_5	CONFIG Pulse Width	7			ns	
T_6	IAi to LOAD High Setup Time	0			ns	
T_7	LOAD to IAi Low Hold Time	3			ns	
T_8	OAi to LOAD High Setup Time	0			ns	
T_9	LOAD to OAi Low Hold Time	3			ns	
T_{10}	Load ↑ to CONFIG ↑	0			ns	
T_{11}	RESET Pulse Width	10			ns	
$T_{R,F}$	Output Rise or Fall Time		250	400	ps	3

Notes: 1. Test conditions: V_{TT} = –2.0 V, R_{LOAD} = 50 W to V_{TT}; ECL inputs: V_{IH} = –1.1 V; V_{IL} = –1.5 V; CMOS inputs: V_{IH} = 3.5 V, V_{IL} = 1.5 V; ECL outputs: $V_{OH} \geq$ –1.0 V, $V_{OL} \leq$ –1.6 V; ECL inputs rise and fall times ≤ 1 ns; CMOS inputs rise and fall times ≤ 20 ns. A bit error rate of 1E–13 BER or better for 2^{23}–1PRBS pattern, jitter and rise/fall times are guaranteed through characterization.

2. 1.2 Gb/s Non-Return-Zero (NRZ) data equivalent to 600 MHz clock signal.

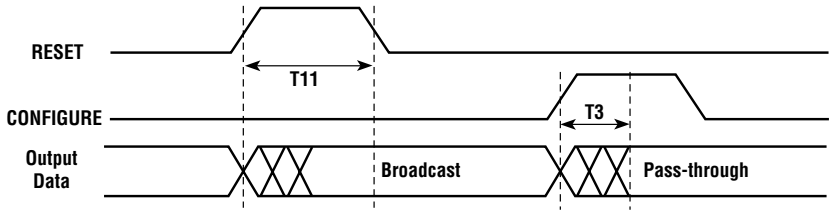
3. Rise and fall times are measured at the 20% and 80% points of the transition from V_{OL} max to V_{OL} min.

Figure 2. Switch Configuration Timing



Notes: 1. No data loss on unchanged paths.

Figure 5. Reset Timing



Notes: 1. LOAD input must remain LOW to insure correct programming of the switch.
2. "Broadcast" is defined as data input 0 to all data outputs (0…15).
3. "Pass-through" is defined as data input 0 to data output 0, data input 1 to data output 1, and so on.

Typical Performance Data

Figure 4. Data Eye Closure

Percent RMS vs. Data Rate (typical)

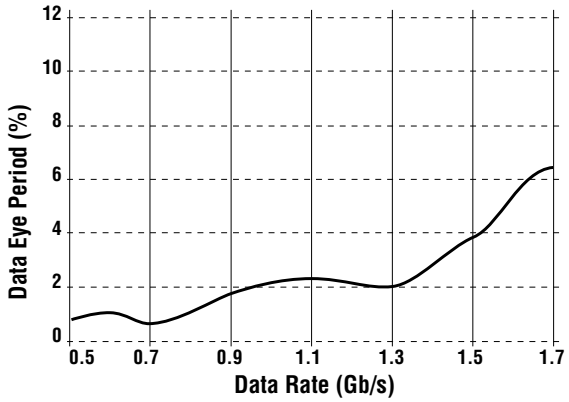


Figure 5. Data Eye Closure

Time & Amplitude vs Data Rate (typical)

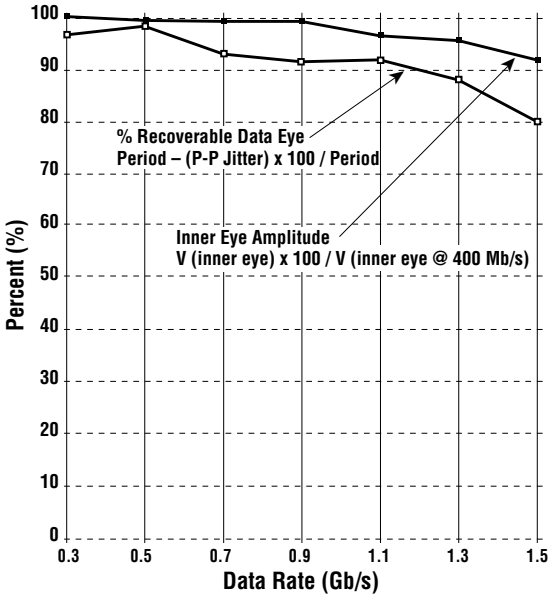


Figure 6. RMS Jitter vs. Data Rate *(typical)*

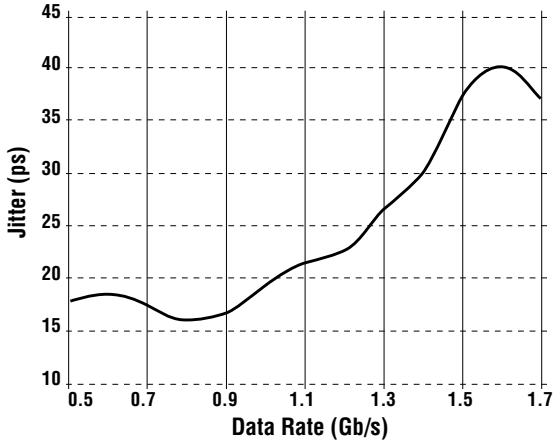
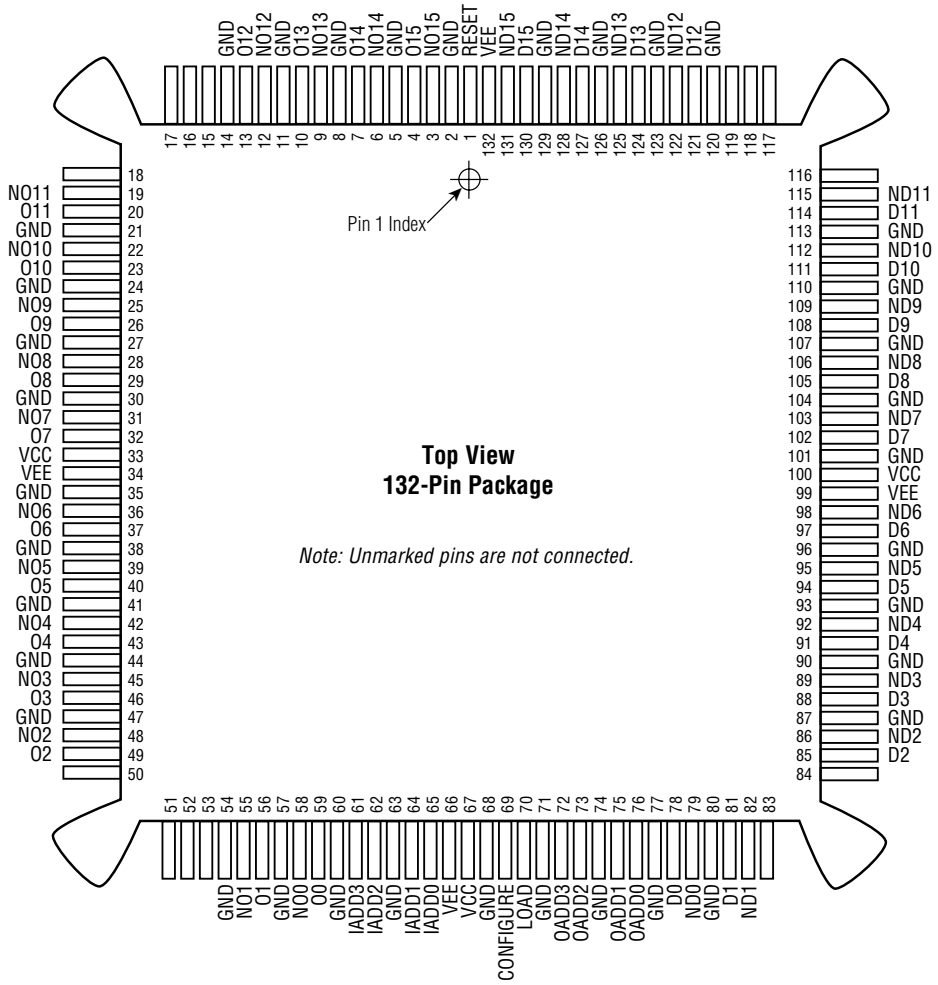


Figure 7. Package Pinout

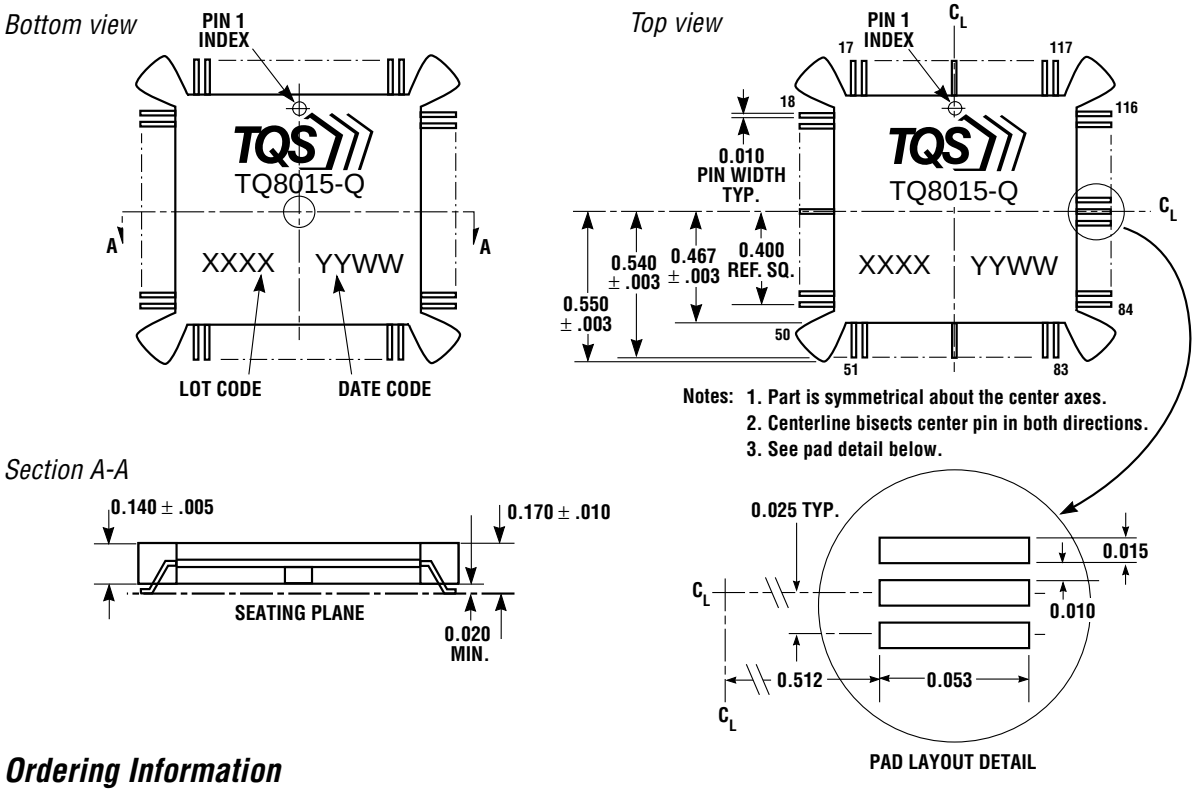


Top View
132-Pin Package

Note: Unmarked pins are not connected.

SWITCHING PRODUCTS

Figure 8. Mechanical Dimensions *(in inches)*



Ordering Information

TQ8015-Q *1.25 16x16 Gb/s ECL Crosspoint Switch*

Additional Information

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