Si51210

TWO OUTPUTS FACTORY PROGRAMMABLE CLOCK GENERATOR

Features

- Generates up to 2 CMOS clock outputs from 3 to 200 MHz
- Accepts crystal or reference clock input
  - 3 to 166 MHz reference clock input
  - 8 to 48 MHz crystal input
- Programmable FSEL, SSEL, SSON, PD, and OE input functions
- Low power dissipation
- 2.5 to 3.3 V voltage supply range
- 0.25% to 1.0% spread spectrum (center spread)
- Low cycle-cycle jitter
- Programmable output rise and fall times
- Ultra small 6-pin TDFN package (1.2 mm x 1.4 mm)

Ordering Information:
See page 9.

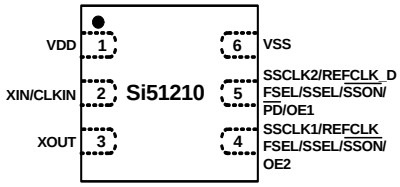
Applications

- Crystal/XO replacement
- EMI reduction
- Portable devices
- Digital still camera
- IP phone
- Smart meter

Description

The factory programmable Si51210 is industry's lowest power, smallest footprint and frequency flexible programmable clock generator targeting low power, low cost and high volume consumer and embedded applications. The device operates from a single crystal or an external clock source and generates 1 to 2 outputs up to 200 MHz. They are factory programmed to provide customized output frequencies, control inputs and ac parameter tuning like output drive strength that are optimized for customer board condition and application requirements.

Pin Assignments



Patents pending

Functional Block Diagram

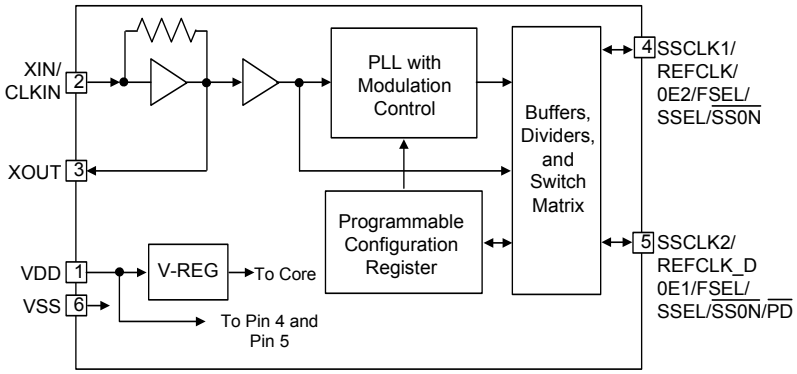


TABLE OF CONTENTS

1. Electrical Specifications

Table 1. DC Electrical Specifications

(V_{DD} = 2.5 V ±5%, or V_{DD} = 3.3 V ± 10%, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	V_{DD}=3.3 V ± 10%	2.97	3.3	3.63	V
		V_{DD}=2.5 V ± 5%	2.375	2.5	2.625	V
Output High Voltage	V_{OH}	I_{OH}=–4 mA	V_{DD} – 0.5	—	—	V
Output Low Voltage	V_{OL}	I_{OL}=4 mA	—	—	0.3	V
Input High Voltage	V_{IH}	CMOS Level	0.7 V_{DD}	—	—	V
Input Low Voltage	V_{IL}	CMOS Level	0	—	0.3 V_{DD}	V
Operating Supply Current	I_{DD}	F_{IN}=12 MHz, SSCLK1 =12 MHz, SSCLK2 =24 MHz, C_L=0, V_{DD}=3.3 V	—	4.5	—	mA
Nominal Output Impedance	Z_O		—	30	—	Ω
Internal Pull-up/Pull-down Resistor	R_{PUP}/R_{PD}	Pin 5	—	150k	—	Ω
Input Pin Capacitance	C_{IN}	Input pin capacitance	—	3	5	pF
Load Capacitance	C_L	Clock outputs < 166 MHz	—	—	15	pF
		Clock outputs > 166 MHz	—	—	10	pF

Table 2. AC Electrical Specifications

(V_{DD} = 2.5 V ±5%, or V_{DD} = 3.3 V ± 10%, T_A = 0 to 70 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	F_{IN1}	Crystal input	8	—	48	MHz
Input Frequency Range	F_{IN2}	Reference clock Input	3	—	166	MHz
Output Frequency Range	F_{OUT}	SSCLK1/2, CL=15 pF	3	—	200	MHz
Frequency Accuracy	F_{ACC}	Configuration dependent	—	0	—	ppm
Output Duty Cycle	DC_{OUT}	Measured at $V_{DD}/2$	45	50	55	%
Input Duty Cycle	DC_{IN}	CLKIN, CLKOUT through PLL	30	50	70	%
Output Rise Time	t_r	C_L=15 pF, 20 to 80%	—	1	3.0	ns
Output Fall Time	t_f	C_L=15 pF, 20 to 80%	—	1	3.0	ns
Period Jitter	PJ_1	SSCLK1/2, two clocks running, V_{DD}=3.3 V, C_L=15 pF	—	150*	—	ps
Cycle-to-Cycle Jitter	CCJ_1	SSCLK1/2, two clocks running, V_{DD}=3.3 V, C_L=15 pF	—	100*	—	ps
Power-up Time	t_{PU}	Time from 0.9 V_{DD} to valid frequencies at all clock outputs	—	1.2	5.0	ms
Output Enable Time	t_{OE}	Time from OE raising edge to active at output SSCLK (asynchronous)	—	15	—	ns
Output Disable Time	t_{OD}	Time from OE falling edge to active at output SSCLK (asynchronous)	—	15	—	ns

***Note:** Jitter performance depends on configuration and programming parameters.

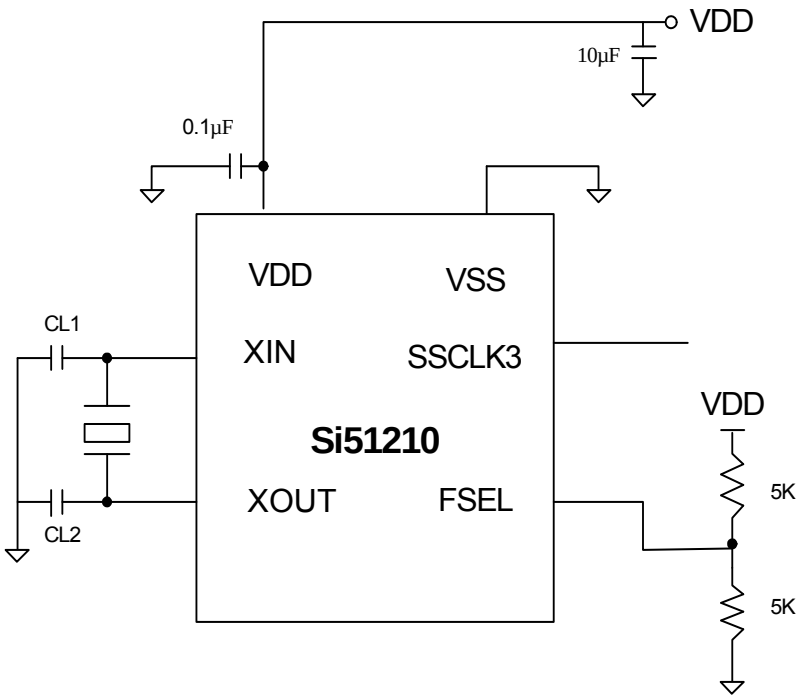
Table 3. Absolute Maximum Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Main Supply Voltage	V_{DD}		–0.5	—	4.2	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5	—	V_{DD}+0.5	V
Temperature,	T_S	Non-functional	–65	—	150	°C
Temperature, Operating Ambient	T_A	Functional, C-Grade	0	—	70	°C
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22-A114)	–4000	—	4000	V
ESD Protection (Charge Device Model)	ESD_{CDM}	JEDEC (JESD 22-C101)	–1500	—	1500	V
ESD Protection (Machine Model)	ESD_{MM}	JEDEC (JESD 22-A115)	–200	—	200	V
Moisture Sensitivity Level	MSL	JEDEC (J-STD-020)	1			

Note: While using multiple power supplies, the Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

2. Design Considerations

2.1. Typical Application Schematic



2.2. Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1 µF must be used between VDD and VSS on pin 1. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin. In addition, a 10 µF capacitor should be placed between VDD and VSS.

Series Termination Resistor: A series termination resistor is recommended if the distance between the outputs (SSCLK or REFCLK pins) and the load is over 1 ½ inches. The nominal impedance of the SSCLK output is about 30 Ω. Use a 20 Ω resistor in series with the output to terminate a 50 Ω trace impedance and place a 20 Ω resistor as close to the SSCLK output as possible.

Crystal and Crystal Load: Only use a parallel resonant fundamental AT cut crystal. **Do not use higher overtone crystals.** To meet the crystal initial accuracy specification (in ppm) make sure that external crystal load capacitor is matched to crystal load specification. To determine the value of CL1 and CL2, use the following formula:

$$C1 = C2 = 2CL – (Cpin + Cp)$$

Where: CL is load capacitance stated by crystal manufacturer

Cpin is the Si51210 pin capacitance (4 pF).

Cp is the parasitic capacitance of the PCB traces.

Example: If a crystal with CL = 12 pF specification is used and Cp = 1 pF (parasitic PCB capacitance on PCB), 19 or 20 pF external capacitors from pins XIN (pin 2) and XOUT (Pin 3) to VSS are required. Users must verify Cp value.

3. Functional Description

3.1. Input Frequency Range

The input frequency range is from 8.0 to 48.0 MHz for crystals and ceramic resonators. If an external clock is used, the input frequency range is from 8.0 to 166.0 MHz.

3.2. Output Frequency Range and Outputs

Up to two outputs can be programmed as SSCLK or REFCLK. SSCLK output can be synthesized to any value from 3 to 200 MHz with spread based on valid input frequency. The spread at SSCLK pins can be stopped by the $\overline{\text{SSON}}$ input control pin. If $\overline{\text{SSON}}$ pin is high (VDD), the frequency at SSCLK pin is synthesized to the nominal value of the input frequency and there is no spread.

REFCLK is the buffered output of the oscillator and is the same frequency as the input frequency without spread. However, REFCLK_D output is divided by output dividers from 2 to 32. By using only low cost, fundamental mode crystals, the Si51210 can synthesize output frequency up to 200 MHz, eliminating the need for higher order crystals (Xtals) and crystal oscillators (XOs). This reduces the cost while improving the system clock accuracy, performance, and reliability

3.3. Programmable Modulation Frequency

The spread spectrum clock (SSC) modulation default value is 31.5 kHz. The higher values of up to 62 kHz can also be programmed. Less than 30 kHz modulation frequency is not recommended to stay out of the range audio frequency bandwidth since this frequency could be detected as a noise by the audio receivers within the vicinity.

3.4. Programmable Spread Percent (%)

The spread percent (%) value is programmable from ±0.25% to ±1% (center spread) for all SSCLK frequencies. It is possible to program smaller or larger non-standard values of spread percentage. Contact Silicon Labs if these non-standard spread percent values are required in the application.

3.5. $\overline{\text{SSON}}$ or Frequency Select (FSEL)

The Si51210 pin 4 and 5 can be programmed as either $\overline{\text{SSON}}$ to enable or disable the programmed spread percent value or as frequency select (FSEL). If $\overline{\text{SSON}}$ is used, when this pin is pulled high (VDD), the spread is stopped and the frequency is the nominal value without spread. If low (GND), the frequency is the nominal value with the spread.

If FSEL function is used, the output pin can be programmed for different set of frequencies as selected by FSEL. SSCLK value can be any frequency from 3 to 200 MHz, but the spread % is the same percent value. REFCLK is the same frequency as the input reference clock and the REFCLK_D is input clock divided by 2 to 32 without spread. The set of frequencies in Table 4 is given as an example, using a 48 MHz crystal.

Table 4. Example Frequencies

FSEL (Pin 4)	SSCLK1 (Pin 5)
0	66 MHz, ±1%
1	33 MHz, ±1%

3.6. Power Down ($\overline{\text{PD}}$) or Output Enable (OE)

The Si51210 pin 5 can be programmed as $\overline{\text{PD}}$ input. Pin 4 and pin 5 can be programmed as OE input. $\overline{\text{PD}}$ turns off both PLL and output buffers whereas OE only disables the output buffers to Hi-Z.

4. Pin Descriptions: 6-Pin TDFN

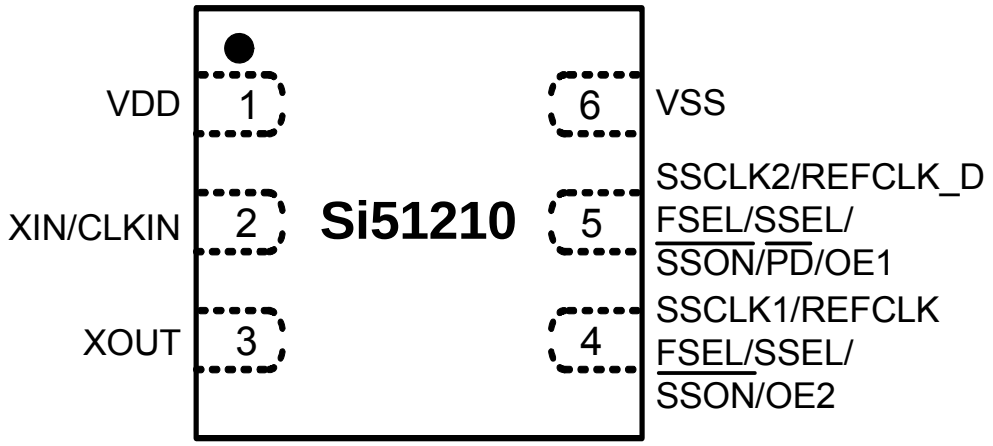
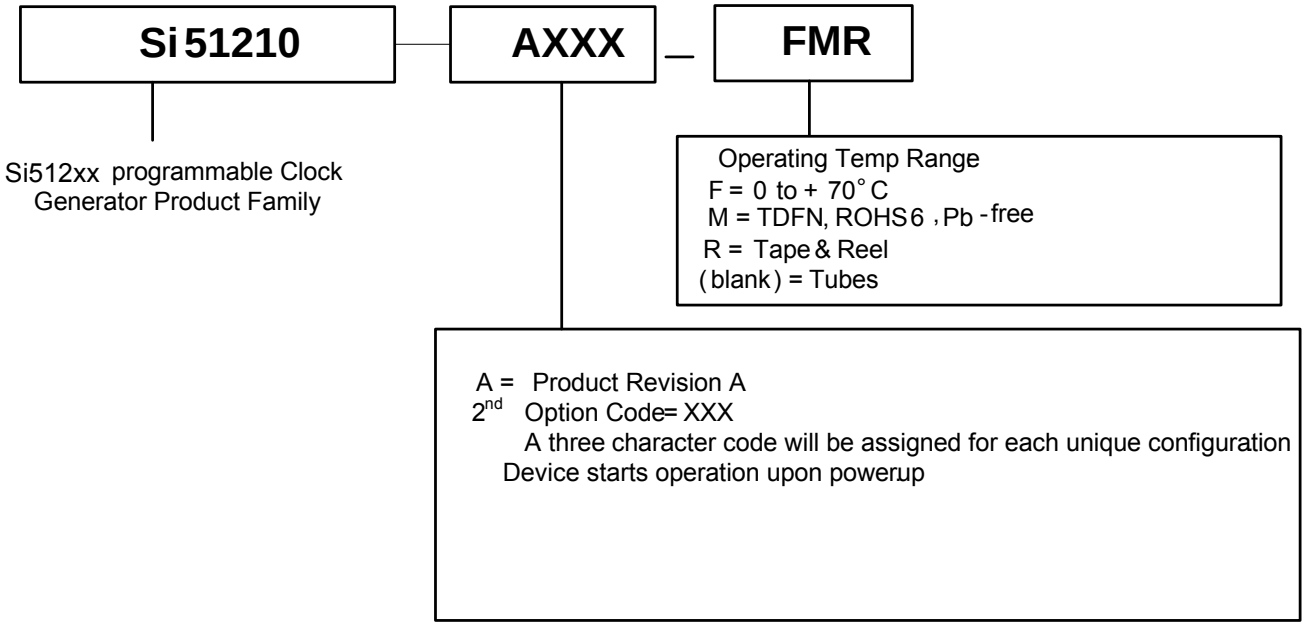


Table 5. Si51210 6-Pin Descriptions

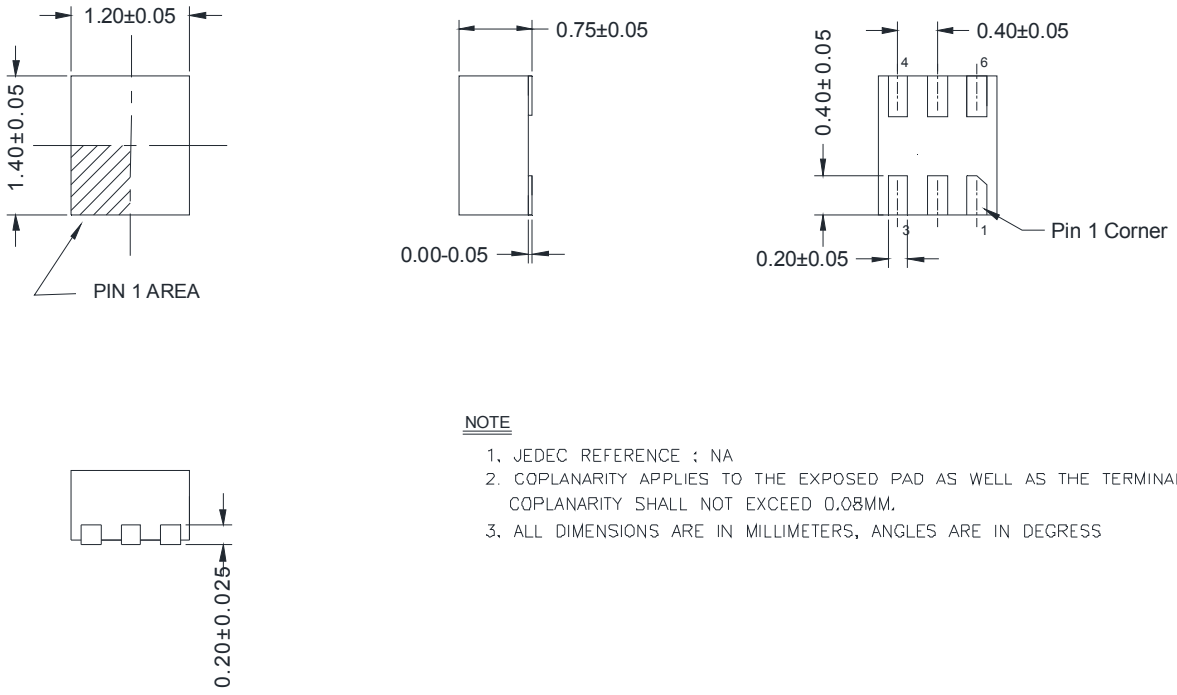
Pin #	Name	Type	Description
1	VDD	PWR	2.5 to 3.3 V power supply.
2	XIN/CLKIN	I	External crystal and clock input.
3	XOUT	O	Crystal output. Leave this pin unconnected (floating) if an external clock input is used.
4	SSCLK1/REFCLK/ FSEL/SSEL/SSON/ OE2	I/O	Programmable SSCLK1 or REFCLK output or MultiFunction control input. The frequency at this pin is synthesized by internal PLL if programmed as SSCLK1 with or without spread. If programmed as REFCLK, output clock is buffered output of crystal or reference clock input. If programmed as MultiFunction control input, it can be OE, FSEL, SSEL and SSON.
5	SSCLK2/REFCLK_D/ OE1/FSEL/SSEL/ SSON/PD	I/O	Programmable SSCLK2 or REFCLK_D output or MultiFunction control input. The frequency at this pin is synthesized by internal PLL if programmed as SSCLK2 with or without spread. If programmed as REFCLK_D, output clock is buffered output of crystal or reference clock input divided by 2 to 32. If programmed as MultiFunction control input, it can be OE, PD, FSEL, SSEL and SSON.
6	VSS	GND	Ground.

5. Ordering Information

Part Number	Package Type	Temperature
Si51210-AxxxFM	6-pin TDFN	Commercial, 0 to 70 °C
Si51210-AxxxFMR	6-pin TDFN—Tape and Reel	Commercial, 0 to 70 °C



6. Package Outline: 6-pin TDFN



NOTE

1. JEDEC REFERENCE : NA
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08MM.
3. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGRESS

NOTES:

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
https://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.