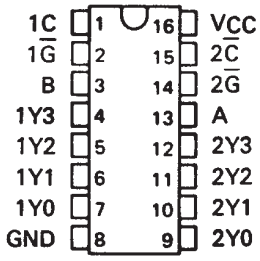
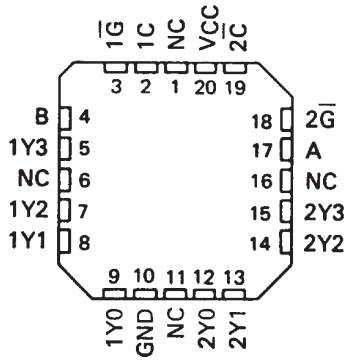
- **Applications:**
  - **Dual 2-to 4-Line Decoder**
  - **Dual 1-to 4-Line Demultiplexer**
  - **3-to 8-Line Decoder**
  - **1-to 8-Line Demultiplexer**
- **Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words**
- **Input Clamping Diodes Simplify System Design**
- **Choice of Outputs:**
  - **Totem Pole ('155, 'LS155A)**
  - **Open-Collector ('156, 'LS156)**

| TYPES | TYPICAL AVERAGE PROPAGATION DELAY 3 GATE LEVELS | TYPICAL POWER DISSIPATION |
|---|---|---|
| '155, '156 | 21 ns | 125 mW |
| 'LS155A | 18 ns | 31 mW |
| 'LS156 | 32 ns | 31 mW |

SN54155, SN54156, SN54LS155A,
SN54LS156 . . . J OR W PACKAGE
SN74155, SN74156 . . . N PACKAGE
SN74LS155A, SN74LS156 . . . D OR N PACKAGE
(TOP VIEW)




SN54LS155A, SN54LS156 . . . FK PACKAGE
(TOP VIEW)



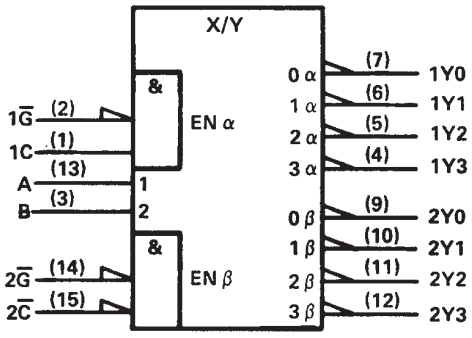

NC - No internal connection

## description

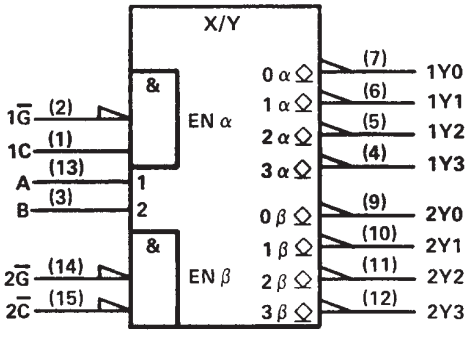
These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at $\overline{2C}$ is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

## logic symbols (2-line to 4-line decoder)†

'155, 'LS155A




'156, 'LS156




†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. For alternative symbols for other applications, see the following page.

Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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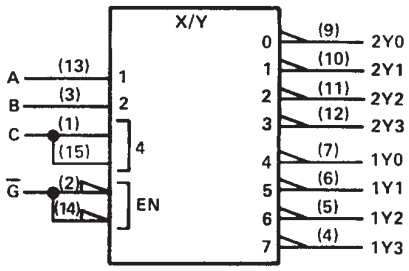
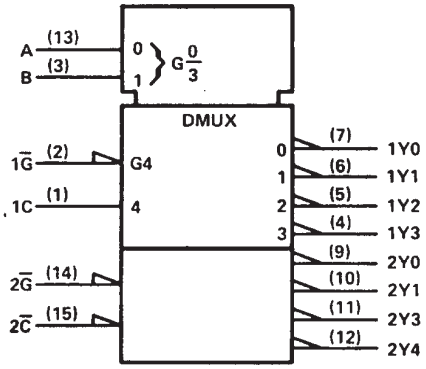
### additional logic symbols (alternatives)†

'155, 'LS155A

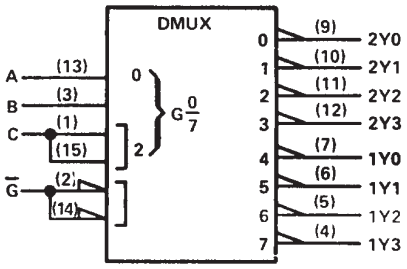
3-line to 8-line Decoder




1-line to 4-line DMUX

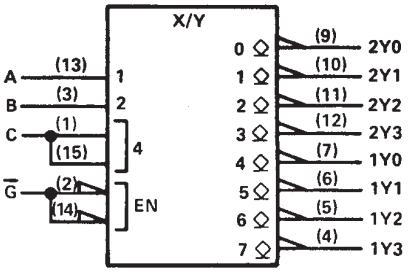



1-line to 8-line DMUX

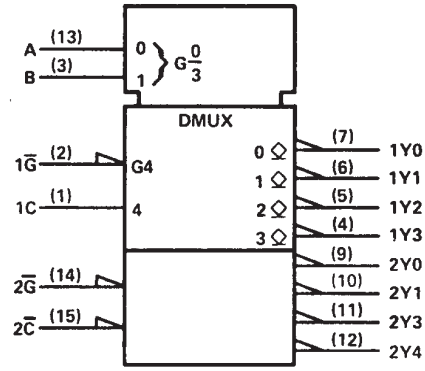



'156, 'LS156

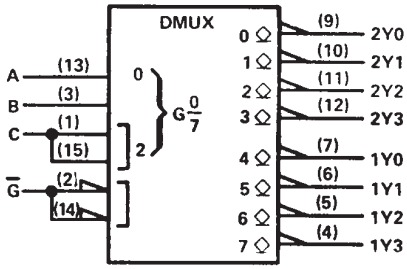
3-line to 8-line Decoder




1-line to 4-line DMUX




1-line to 8-line DMUX

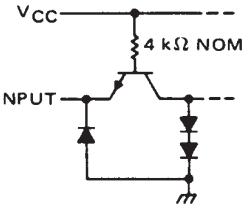



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

### schematics of inputs and outputs

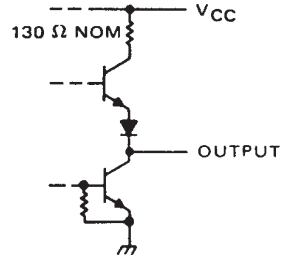
'155, '156

EQUIVALENT OF EACH INPUT



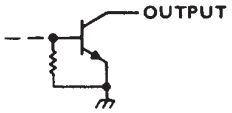

'155

TYPICAL OF ALL OUTPUTS




'156

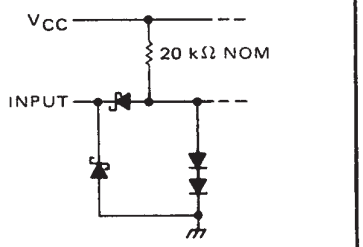
TYPICAL OF ALL OUTPUTS



## schematics of inputs and outputs (continued)

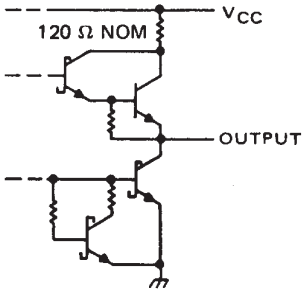
'LS155A, 'LS156

EQUIVALENT OF EACH INPUT



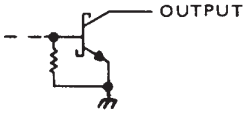

'LS155A

TYPICAL OF ALL OUTPUTS

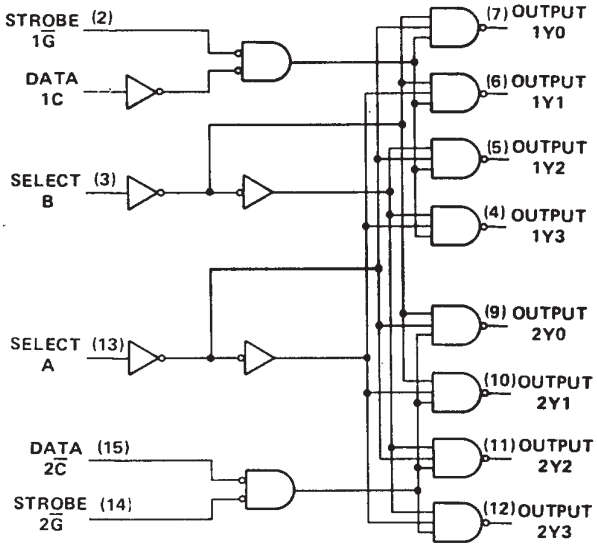



'LS156

TYPICAL OF ALL OUTPUTS




## logic diagram (positive logic)




FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

| INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| SELECT | | STROBE | DATA | | | | |
| B | A | $1\overline{G}$ | 1C | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| X | X | H | X | H | H | H | H |
| L | L | L | H | L | H | H | H |
| L | H | L | H | H | L | H | H |
| H | L | L | H | H | H | L | H |
| H | H | L | H | H | H | H | L |
| X | X | X | L | H | H | H | H |

| INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| SELECT | | STROBE | DATA | | | | |
| B | A | $2\overline{G}$ | 2C | 2Y0 | 2Y1 | 2Y2 | 2Y3 |
| X | X | H | X | H | H | H | H |
| L | L | L | L | L | H | H | H |
| L | H | L | L | H | L | H | H |
| H | L | L | L | H | H | L | H |
| H | H | L | L | H | H | H | L |
| X | X | X | H | H | H | H | H |

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

| INPUTS | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SELECT | | | STROBE OR DATA | (0) | (1) | (2) | (3) | (4) | (5) | (6) | (7) |
| C† | B | A | $\overline{G}$‡ | 2Y0 | 2Y1 | 2Y2 | 2Y3 | 1Y0 | 1Y1 | 1Y2 | 1Y3 |
| X | X | X | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H |
| L | H | L | L | H | H | L | H | H | H | H | H |
| L | H | H | L | H | H | H | L | H | H | H | H |
| H | L | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | L | H | H |
| H | H | L | L | H | H | H | H | H | H | L | H |
| H | H | H | L | H | H | H | H | H | H | H | L |

†C = inputs 1C and $2\overline{C}$ connected together
‡$\overline{G}$ = inputs $1\overline{G}$ and $2\overline{G}$ connected together
H = high level, L = low level, X = irrelevant

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage: '155, '156 . . . . . 5.5 V
'LS155A, 'LS156 . . . . . 7 V
Off-state output voltage: '156 . . . . . 5.5 V
'LS156 . . . . . 7 V
Operating free-air temperature range: SN54', SN54LS' Circuits . . . . . −55°C to 125°C
SN74', SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

| | SN54155 | | | SN74155 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | −800 | | | −800 | μA |
| Low-level output current, $I_{OL}$ | | | 16 | | | 16 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54155 SN74155 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −8 mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.2 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −1.6 | mA |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | SN54155 | −20 | | −55 | mA |
| | | | SN74155 | −18 | | −57 | |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | SN54155 | | 25 | 35 | mA |
| | | | SN74155 | | 25 | 40 | |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: $I_{CC}$ is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

### switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LEVELS OF LOGIC | TEST CONDITIONS | SN54155 SN74155 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$ | Y | 2 | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Note 3 | | 13 | 20 | ns |
| $t_{PHL}$ | A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$ | Y | 2 | | | 18 | 27 | ns |
| $t_{PLH}$ | A or B | Y | 3 | | | 21 | 32 | ns |
| $t_{PHL}$ | A or B | Y | 3 | | | 21 | 32 | ns |
| $t_{PLH}$ | 1C | Y | 3 | | | 16 | 24 | ns |
| $t_{PHL}$ | 1C | Y | 3 | | | 20 | 30 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## recommended operating conditions

| | SN54156 | | | SN74156 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output voltage, $V_{OH}$ | | | 5.5 | | | 5.5 | V |
| Low-level output current, $I_{OL}$ | | | 16 | | | 16 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54156 SN74156 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −8 mA | | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $V_{OH}$ = 5.5 V | | | | 250 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | | 0.2 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −1.6 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | SN54156 | | 25 | 35 | mA |
| | | | SN74156 | | 25 | 40 | |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
NOTE 2: $I_{CC}$ is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER§ | FROM (INPUT) | TO (OUTPUT) | LEVELS OF LOGIC | TEST CONDITIONS | SN54156 SN74156 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$ | Y | 2 | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Note 3 | | 15 | 23 | ns |
| $t_{PHL}$ | A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$ | Y | 2 | | | 20 | 30 | ns |
| $t_{PLH}$ | A or B | Y | 3 | | | 23 | 34 | ns |
| $t_{PHL}$ | A or B | Y | 3 | | | 23 | 34 | ns |
| $t_{PLH}$ | 1C | Y | 3 | | | 18 | 27 | ns |
| $t_{PHL}$ | 1C | Y | 3 | | | 22 | 33 | ns |

§$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## recommended operating conditions

| | SN54LS155A | | | SN74LS155A | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | −400 | | | −400 | μA |
| Low-level output current, $I_{OL}$ | | | 4 | | | 8 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS155A | | | SN74LS155A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL\ max}$, $I_{OH}$ = −400 μA | | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL\ max}$ | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | | | 6.1 | 10 | | 6.1 | 10 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: $I_{CC}$ is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | LEVELS OF LOGIC | TEST CONDITIONS | SN54LS155A SN74LS155A | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | A, B, 2$\overline{C}$, 1$\overline{G}$, or 2$\overline{G}$ | Y | 2 | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Note 3 | | 10 | 15 | ns |
| $t_{PHL}$ | A, B, 2$\overline{C}$, 1$\overline{G}$, or 2$\overline{G}$ | Y | 2 | | | 19 | 30 | ns |
| $t_{PLH}$ | A or B | Y | 3 | | | 17 | 26 | ns |
| $t_{PHL}$ | A or B | Y | 3 | | | 19 | 30 | ns |
| $t_{PLH}$ | 1C | Y | 3 | | | 18 | 27 | ns |
| $t_{PHL}$ | 1C | Y | 3 | | | 18 | 27 | ns |

¶$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## recommended operating conditions

| | SN54LS156 | | | SN74LS156 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output voltage, $V_{OH}$ | | | 5.5 | | | 5.5 | V |
| Low-level output current, $I_{OL}$ | | | 4 | | | 8 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS156 | | | SN74LS156 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max, $V_{OH}$ = 5.5 V | | | | 100 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | | | 6.1 | 10 | | 6.1 | 10 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
NOTE 2: $I_{CC}$ is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER§ | FROM (INPUT) | TO (OUTPUT) | LEVELS OF LOGIC | TEST CONDITIONS | SN54LS156 SN74LS156 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | A, B, $2\overline{C}$ $1\overline{G}$, or $2\overline{G}$ | Y | 2 | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Note 3 | | 25 | 40 | ns |
| $t_{PHL}$ | A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$ | Y | 2 | | | 34 | 51 | ns |
| $t_{PLH}$ | A or B | Y | 3 | | | 31 | 46 | ns |
| $t_{PHL}$ | A or B | Y | 3 | | | 34 | 51 | ns |
| $t_{PLH}$ | 1C | Y | 3 | | | 32 | 48 | ns |
| $t_{PHL}$ | 1C | Y | 3 | | | 32 | 48 | ns |

§$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9750801QEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9750801QE A SNJ54LS155AJ | Samples |
| 5962-9750801QFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9750801QF A SNJ54LS155AW | Samples |
| 5962-9750801QFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9750801QF A SNJ54LS155AW | Samples |
| SN54155J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |
| SN54155J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |
| SN54LS155AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS155AJ | Samples |
| SN54LS155AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS155AJ | Samples |
| SN54LS156J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS156J | Samples |
| SN54LS156J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS156J | Samples |
| SN74155N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74155N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74155N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74155N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74156N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74156N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74LS155AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS155A | Samples |
| SN74LS155AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS155A | Samples |
| SN74LS155ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS155A | Samples |
| SN74LS155ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS155A | Samples |
| SN74LS155ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS155A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS155ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS155A | Samples |
| SN74LS155ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS155A | Samples |
| SN74LS155ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS155A | Samples |
| SN74LS155AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS155AN | Samples |
| SN74LS155AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS155AN | Samples |
| SN74LS155ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS155AN | Samples |
| SN74LS155ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS155AN | Samples |
| SN74LS155ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS155A | Samples |
| SN74LS155ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS155A | Samples |
| SN74LS156D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 | Samples |
| SN74LS156D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 | Samples |
| SN74LS156DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 | Samples |
| SN74LS156DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 | Samples |
| SN74LS156DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 | Samples |
| SN74LS156DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 | Samples |
| SN74LS156DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 | Samples |
| SN74LS156DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 | Samples |
| SN74LS156DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS156DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 | Samples |
| SN74LS156DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 | Samples |
| SN74LS156DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS156 | Samples |
| SN74LS156N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS156N | Samples |
| SN74LS156N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS156N | Samples |
| SN74LS156N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74LS156N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74LS156NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS156N | Samples |
| SN74LS156NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS156N | Samples |
| SN74LS156NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS156 | Samples |
| SN74LS156NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS156 | Samples |
| SNJ54155J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |
| SNJ54155J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |
| SNJ54155W | OBSOLETE | CFP | W | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |
| SNJ54155W | OBSOLETE | CFP | W | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |
| SNJ54LS155AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9750801QEA SNJ54LS155AJ | Samples |
| SNJ54LS155AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9750801QEA SNJ54LS155AJ | Samples |
| SNJ54LS155AW | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9750801QFA SNJ54LS155AW | Samples |
| SNJ54LS155AW | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9750801QFA SNJ54LS155AW | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SNJ54LS156FK | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI | -55 to 125 | | |
| SNJ54LS156FK | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI | -55 to 125 | | |
| SNJ54LS156J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS156J | Samples |
| SNJ54LS156J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS156J | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54155, SN54LS155A, SN54LS156, SN74155, SN74LS155A, SN74LS156 :**

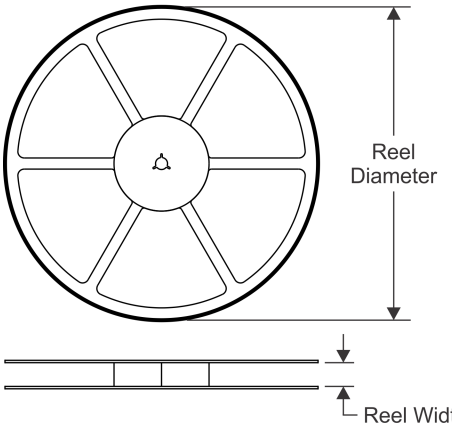
- Catalog: SN74155, SN74LS155A, SN74LS156
- Military: SN54155, SN54LS155A, SN54LS156

NOTE: Qualified Version Definitions:

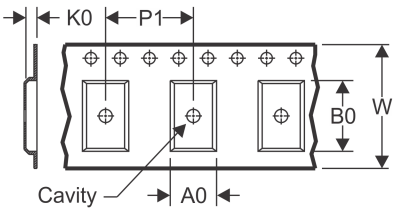
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

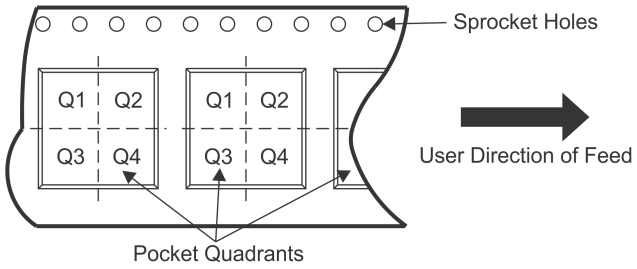



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

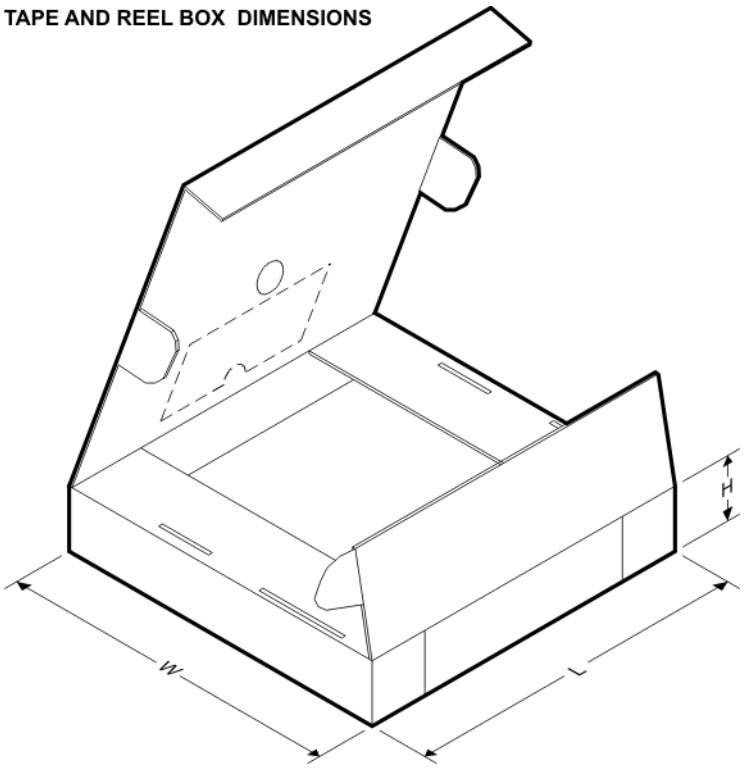
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS155ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS156DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS156NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



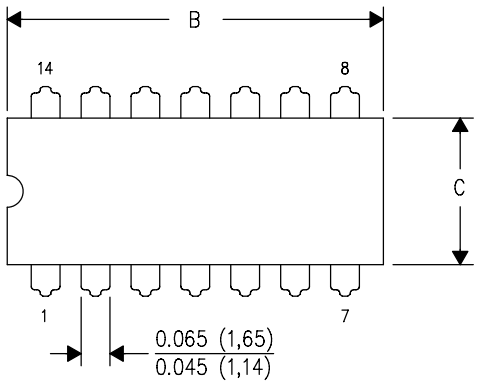

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LS155ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LS156DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LS156NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |

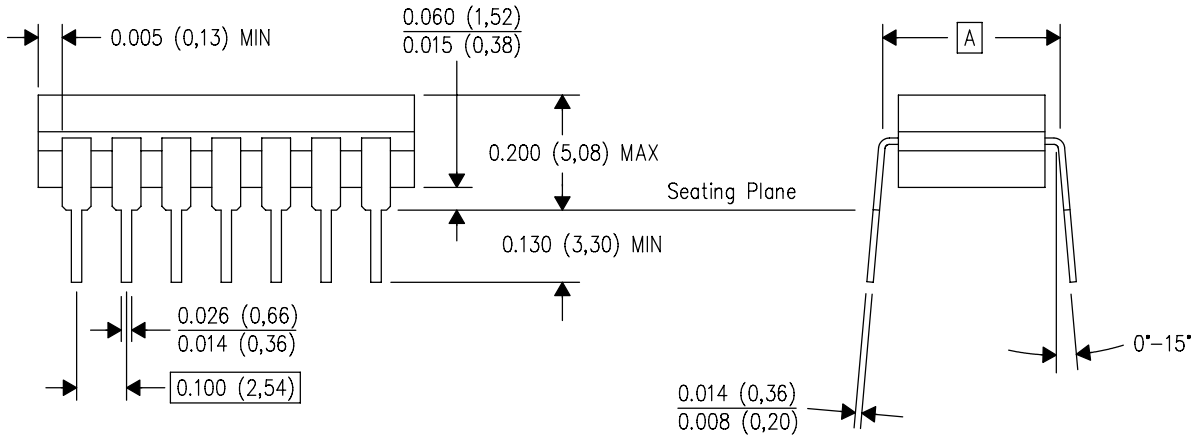
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE



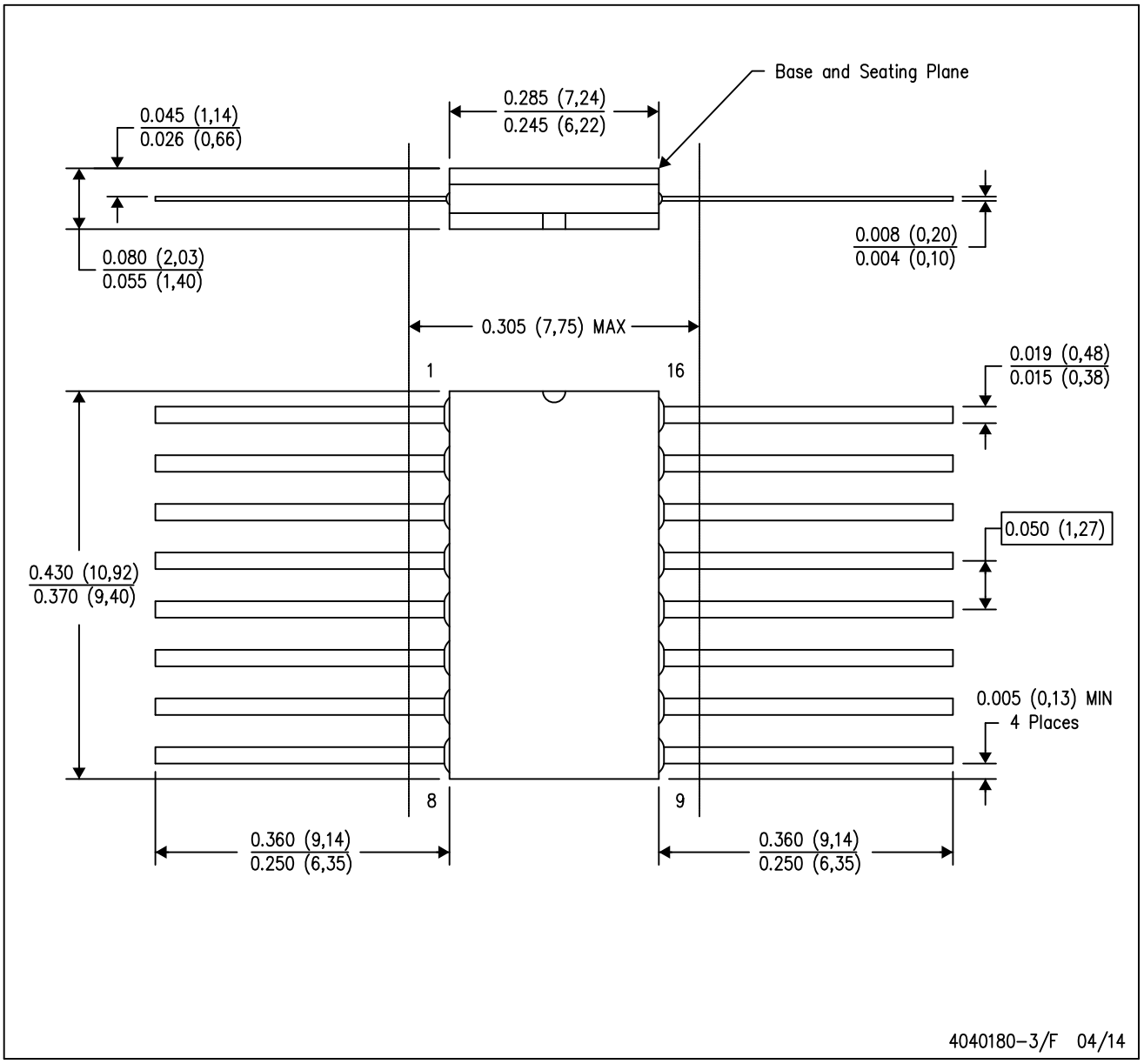

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

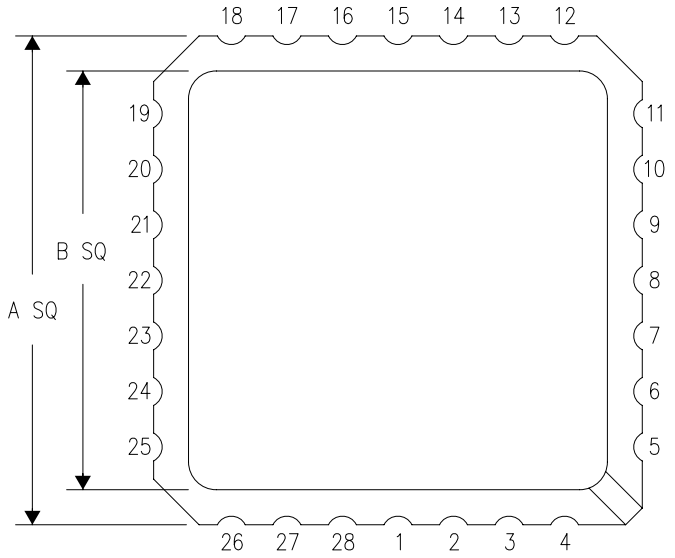
W (R–GDFP–F16) CERAMIC DUAL FLATPACK



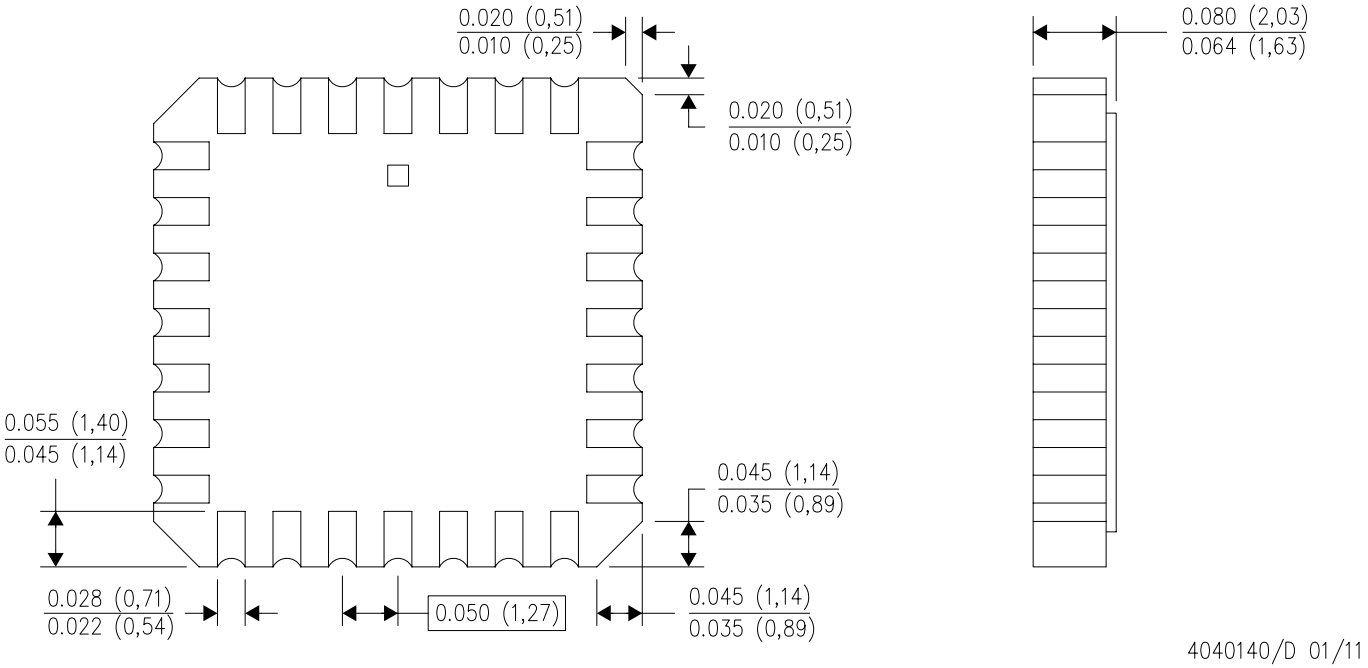

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



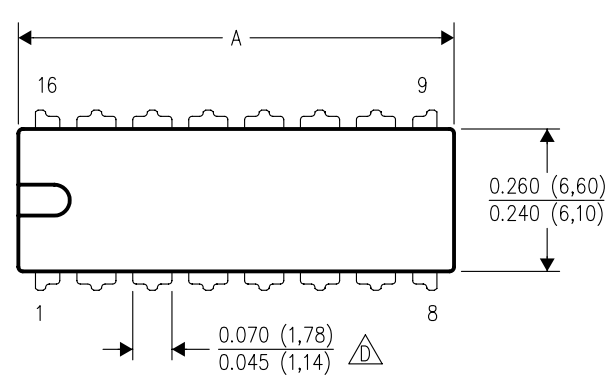

4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

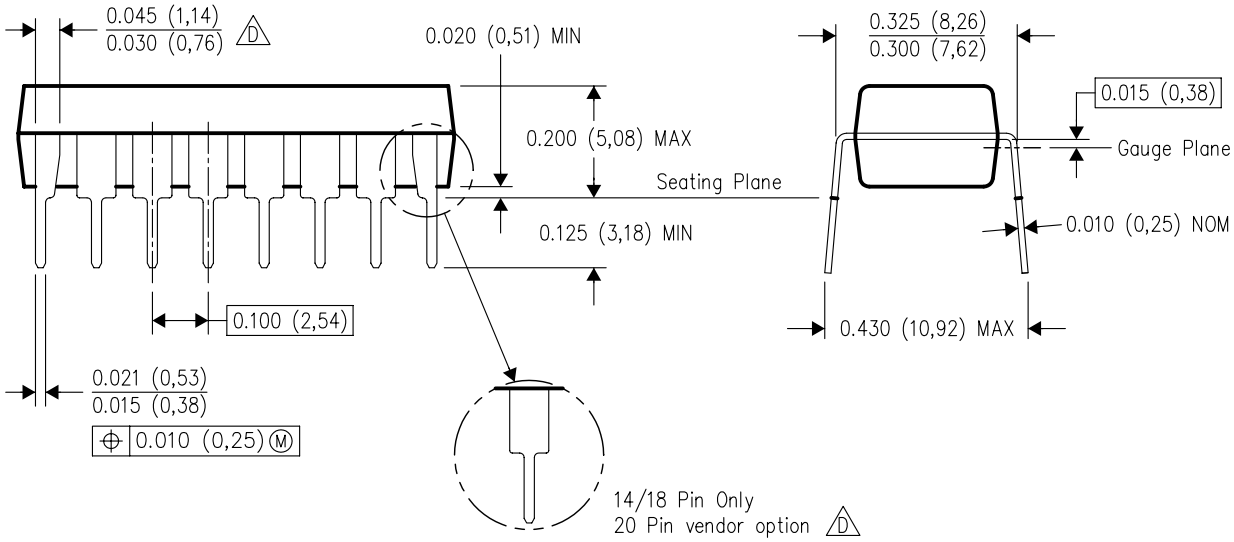
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



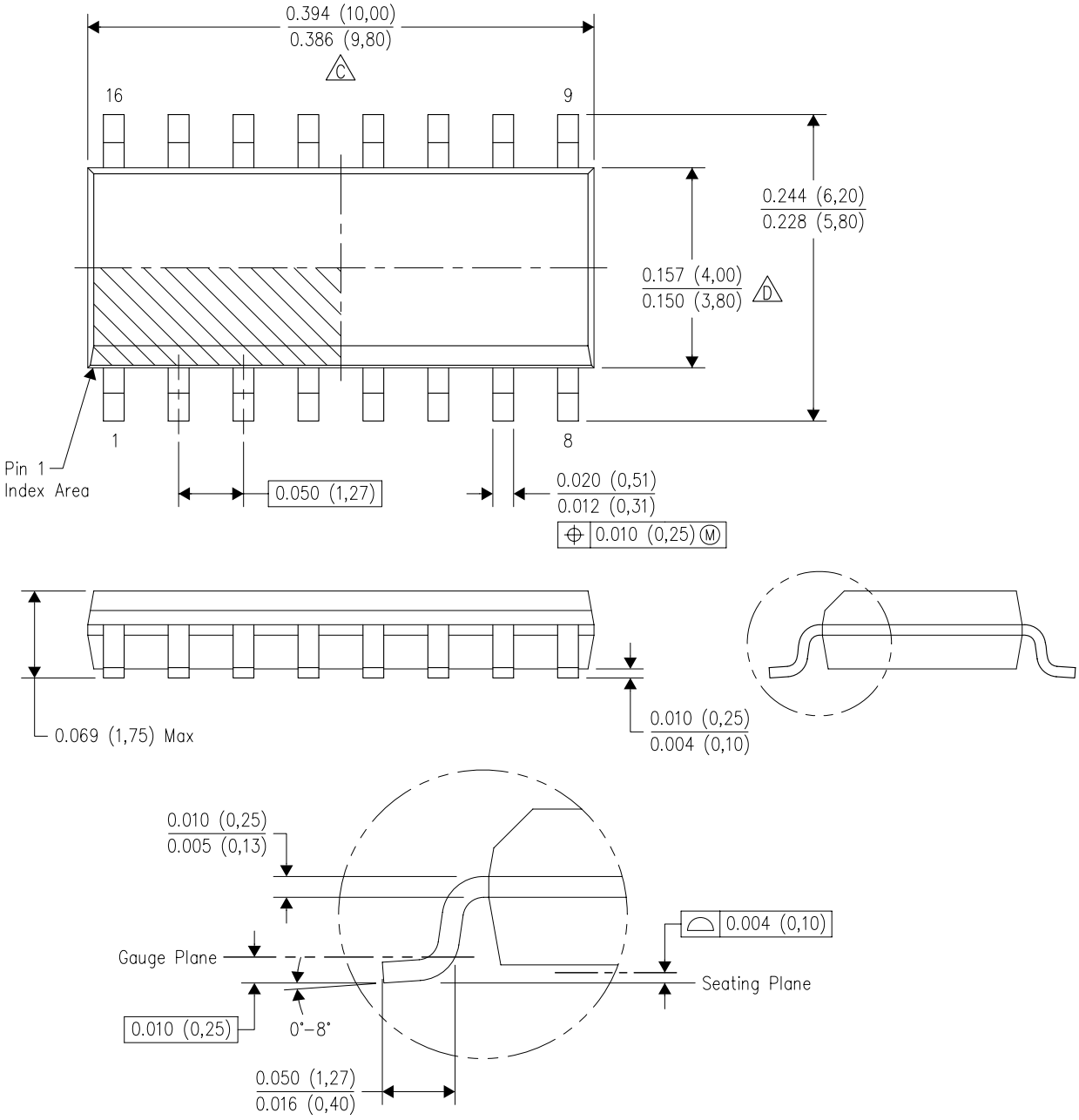

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

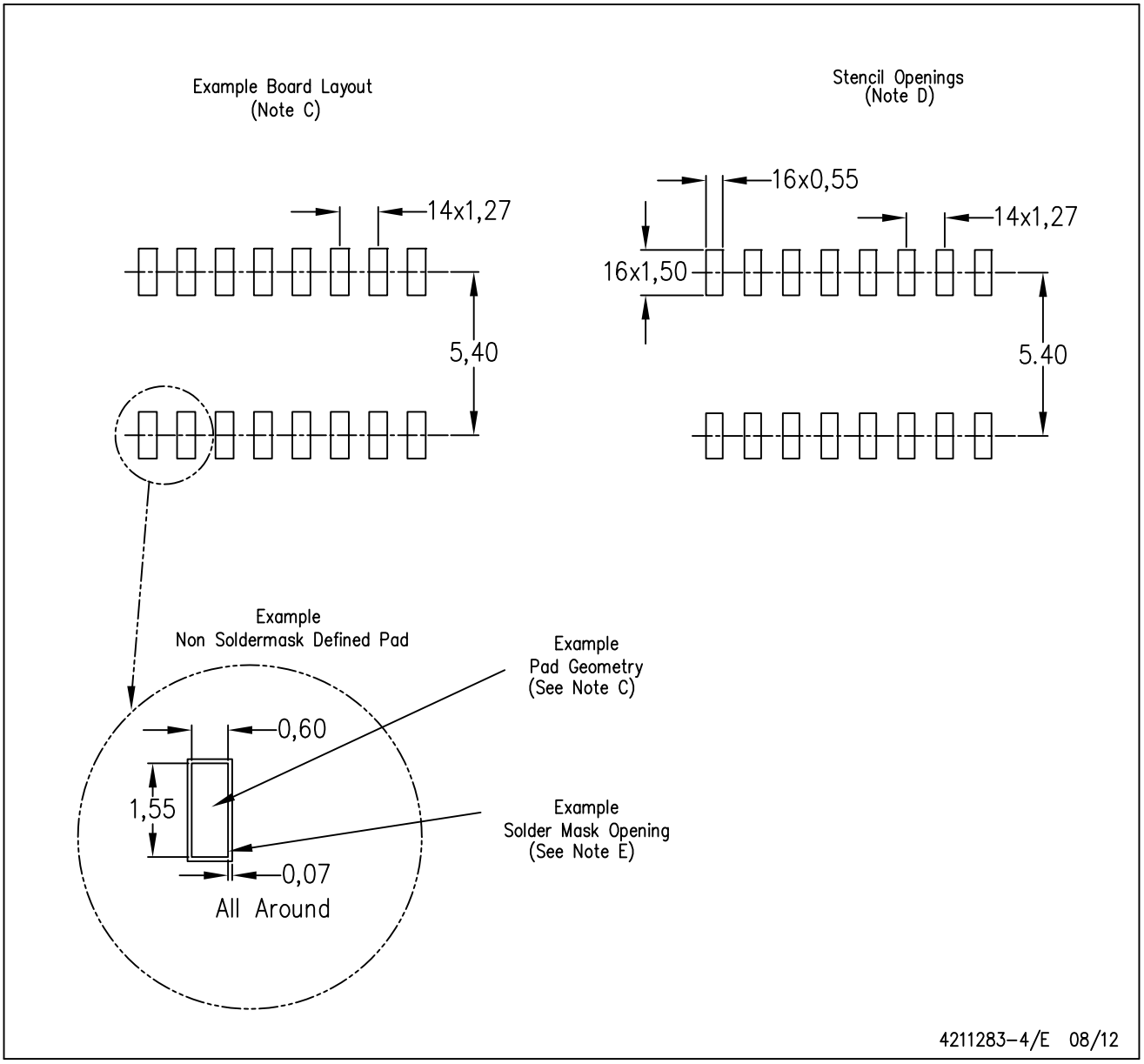
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

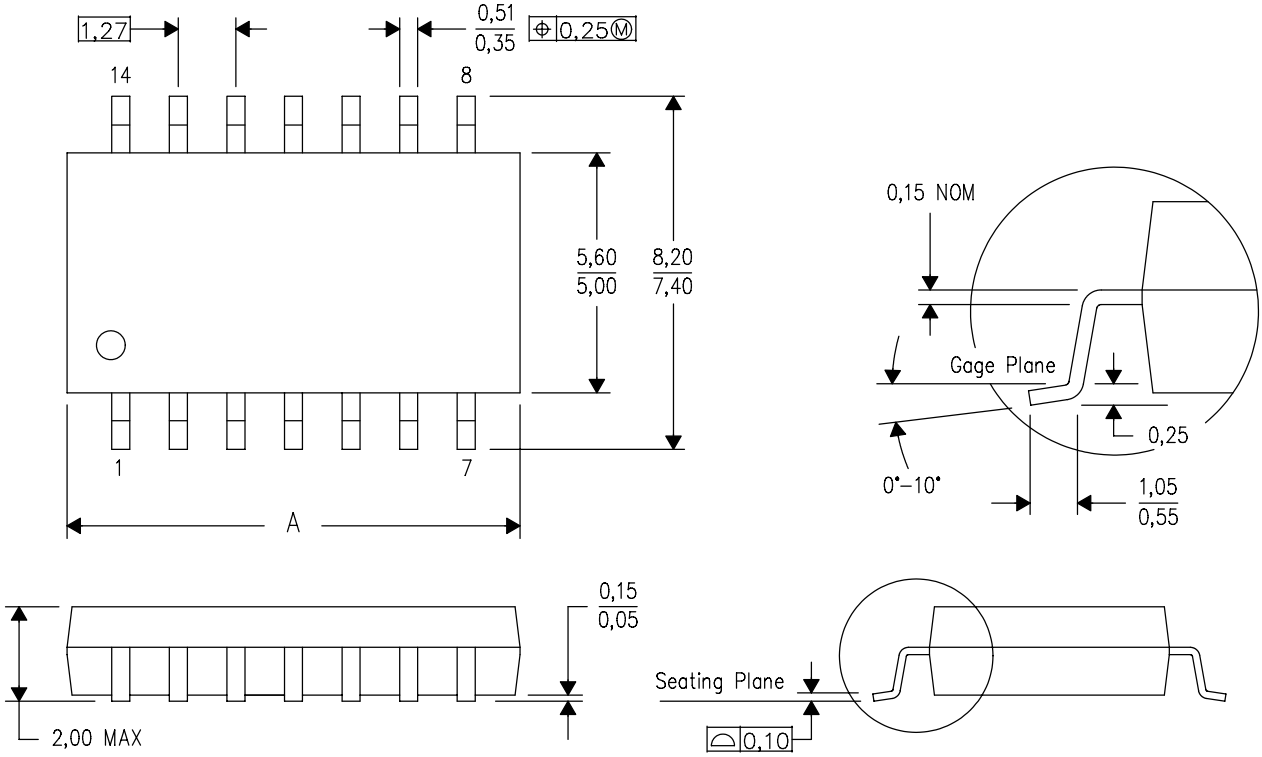



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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