R2A20124AFP/R2A20124ASP

Synchronous Phase Shift Full-Bridge Control IC Series

REJ03D0928-0200
Rev.2.00
Aug 03, 2010

Description

The R2A20124AFP/R2A20124ASP controls a full-bridge phase shift circuit and secondary synchronous rectification. The R2A20124AFP/R2A20124ASP has adjustable delay time functions which make ZVS of primary side and make loss of body diode of primary switching device minimal.

The R2A20124AFP/R2A20124ASP is based on HA16163/R2A20121. And RAMP slope compensation circuit is built-in as an additional function. Also its output driver circuits are improved to enlarge gate drive output voltage swing from VREF to VCC.

In addition R2A20124AFP has ON/OFF function of synchronous rectification and includes amplifier which detect input current signal.

Features

- Maximum ratings
  - Supply voltage Vcc: 20 V
  - Operating junction temperature Tj-opr: –40 to +125°C
- Electrical characteristics
  - VFB feedback voltage VFB(–): 1.25 V ± 2.0%
  - UVLO (Under Voltage Lockout) operation start voltage VH: 8.4 V ± 0.7 V
  - UVLO operation shutdown voltage VL: 8.0 V ± 0.6 V
  - UVLO hysteresis voltage dVUVL: 0.4 V ± 0.1 V
  - Output voltage swing of OUT-A, B, C, D, and E for gate drive: GND to VCC
- Functions

  R2A20124AFP/R2A20124ASP
  - Full-bridge phase-shift switching circuit with adjustable delay times
  - Pulse by pulse current limit
  - Synchronization I/O for the oscillator
  - Ramp sloping adjustor
  - Error amplifier built-in
  - Soft start function

  R2A20124AFP
  - Synchronous rectification on/off control
  - Remote on/off control
  - Amplified output of current sense input voltage: CS
- Package lineup
  - Pb-free LQFP-40: R2A20124AFP
  - Pb-free SOP-20: R2A20124ASP

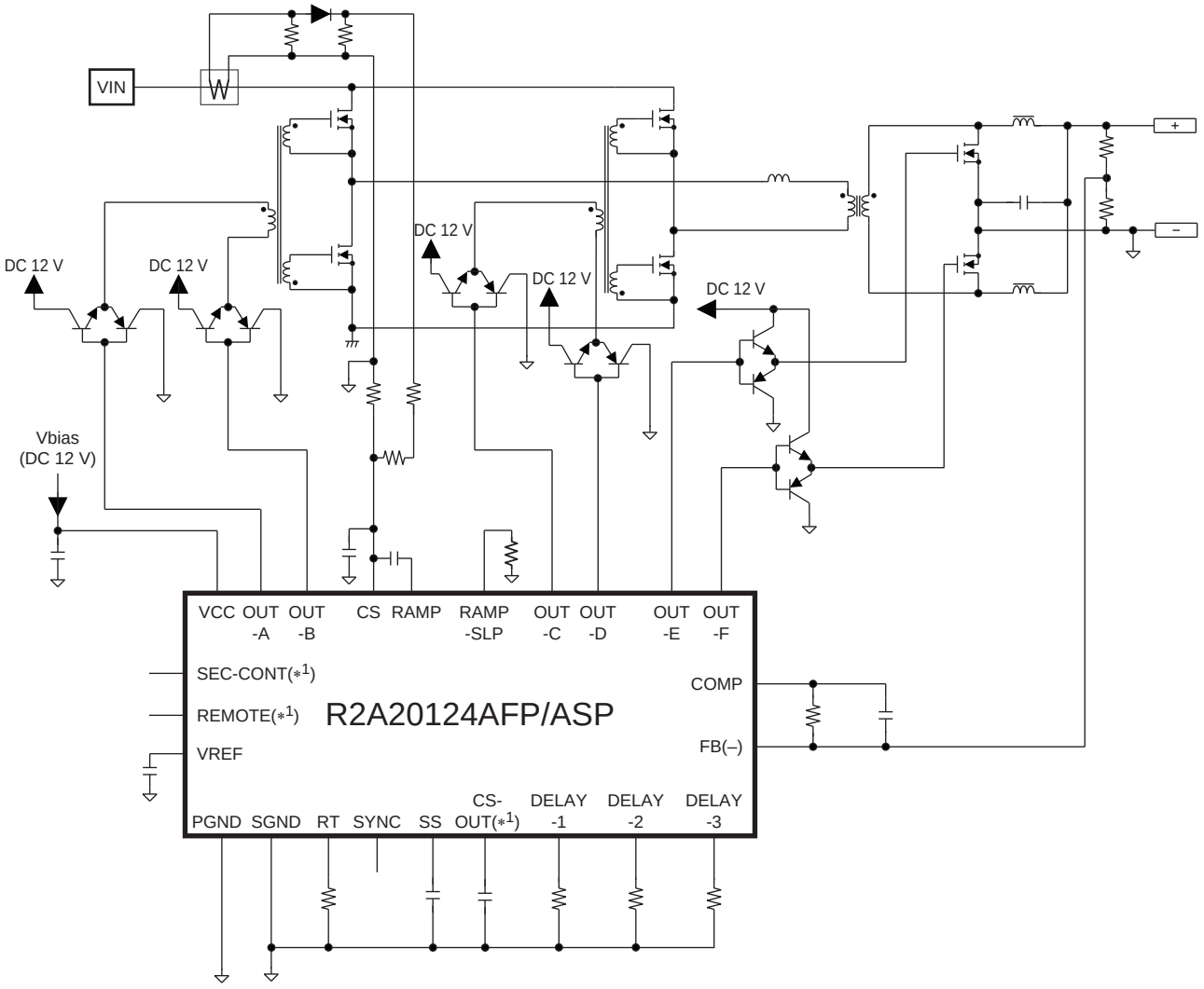
Ordering Information

Part No.	Package Name	Package Code	Taping Spec.
R2A20124AFP-W0	FP-40EV	PLQP0040JB-C	2000 pcs./one taping product
R2A20124AFP-W5			2000 pcs./one taping product
R2A20124AFP-U0			—
R2A20124AFP-U5			—
R2A20124ASP-W0	FP-20DAV	PRSP0020DD-B	2000 pcs./one taping product
R2A20124ASP-W5			2000 pcs./one taping product
R2A20124ASP-U0			—
R2A20124ASP-U5			—

Modified Points from R2A20121SP

- The swing level of the maximum output voltage is changed from VREF to VCC.
- Ramp sloping compensation circuit is added.
- Synchronous rectification control is possible to turned off at light load. (only R2A20124AFP)
- On/off control terminal for Remote is added. (only R2A20124AFP)

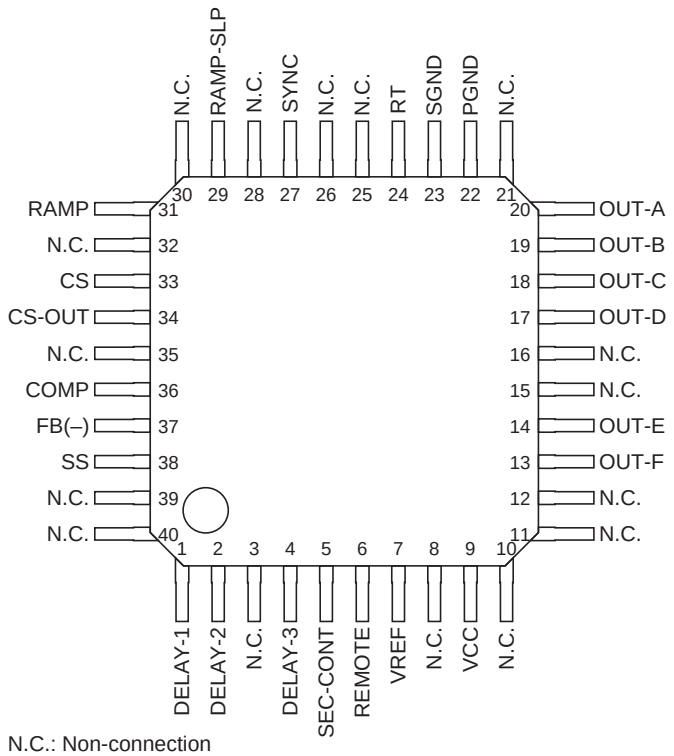
Illustrative Circuit



Note: ∗1. Only R2A20124AFP

Pin Arrangement

R2A20124AFP

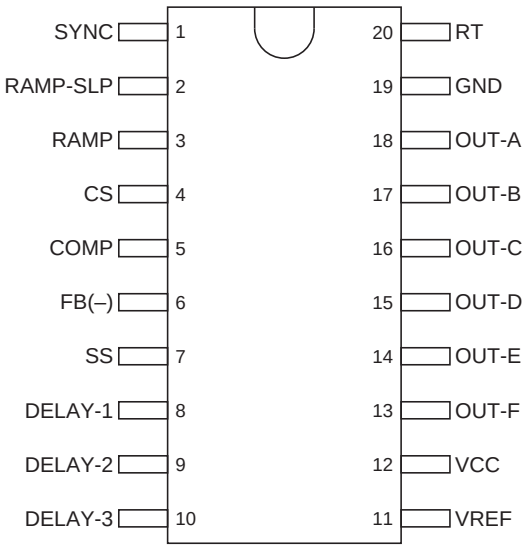


N.C.: Non-connection

(Top view)

Outline: LQFP-40 (PLQP0040JB-C)

R2A20124ASP



(Top view)

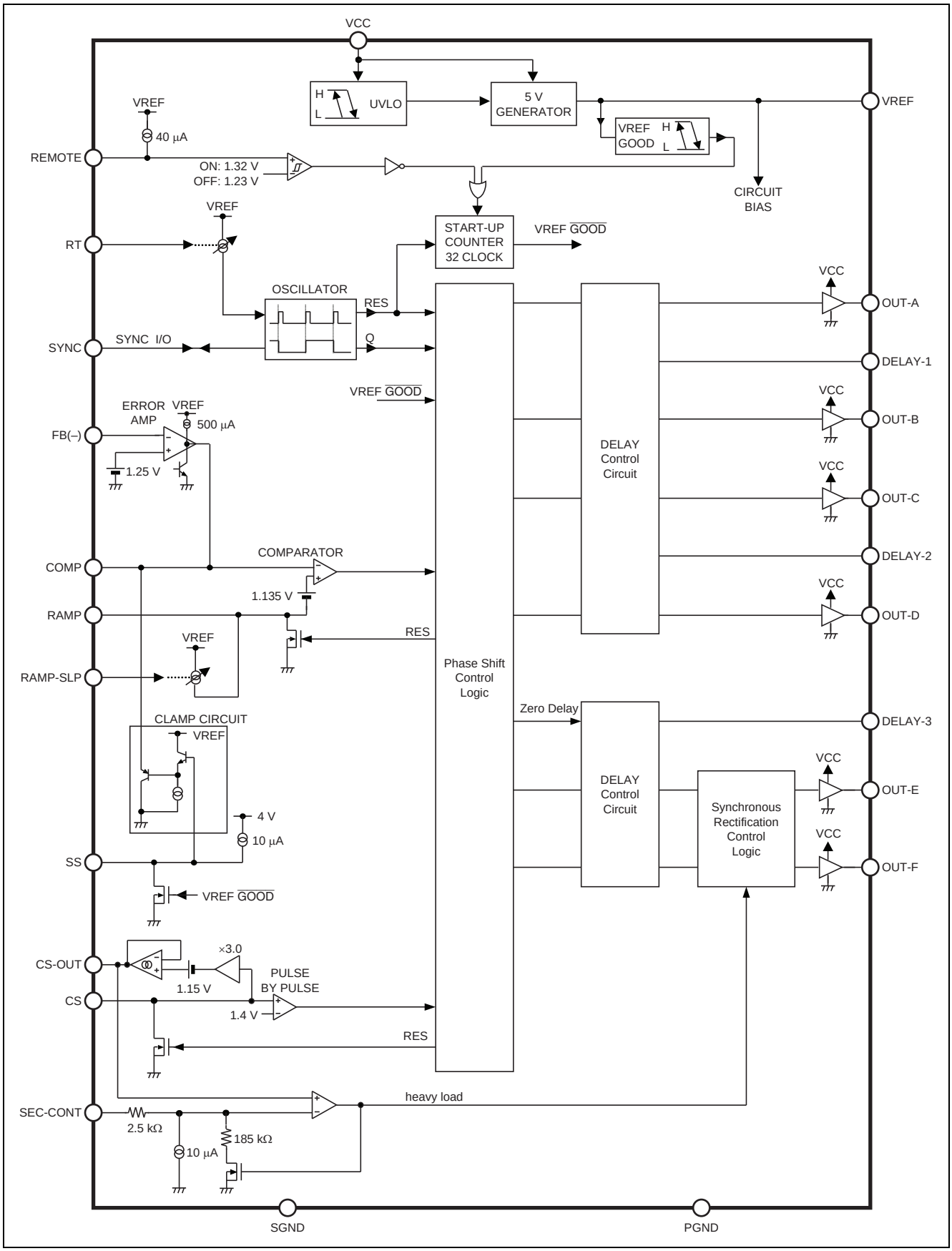
Outline: SOP-20 (PRSP0020DD-B)

Pin Functions

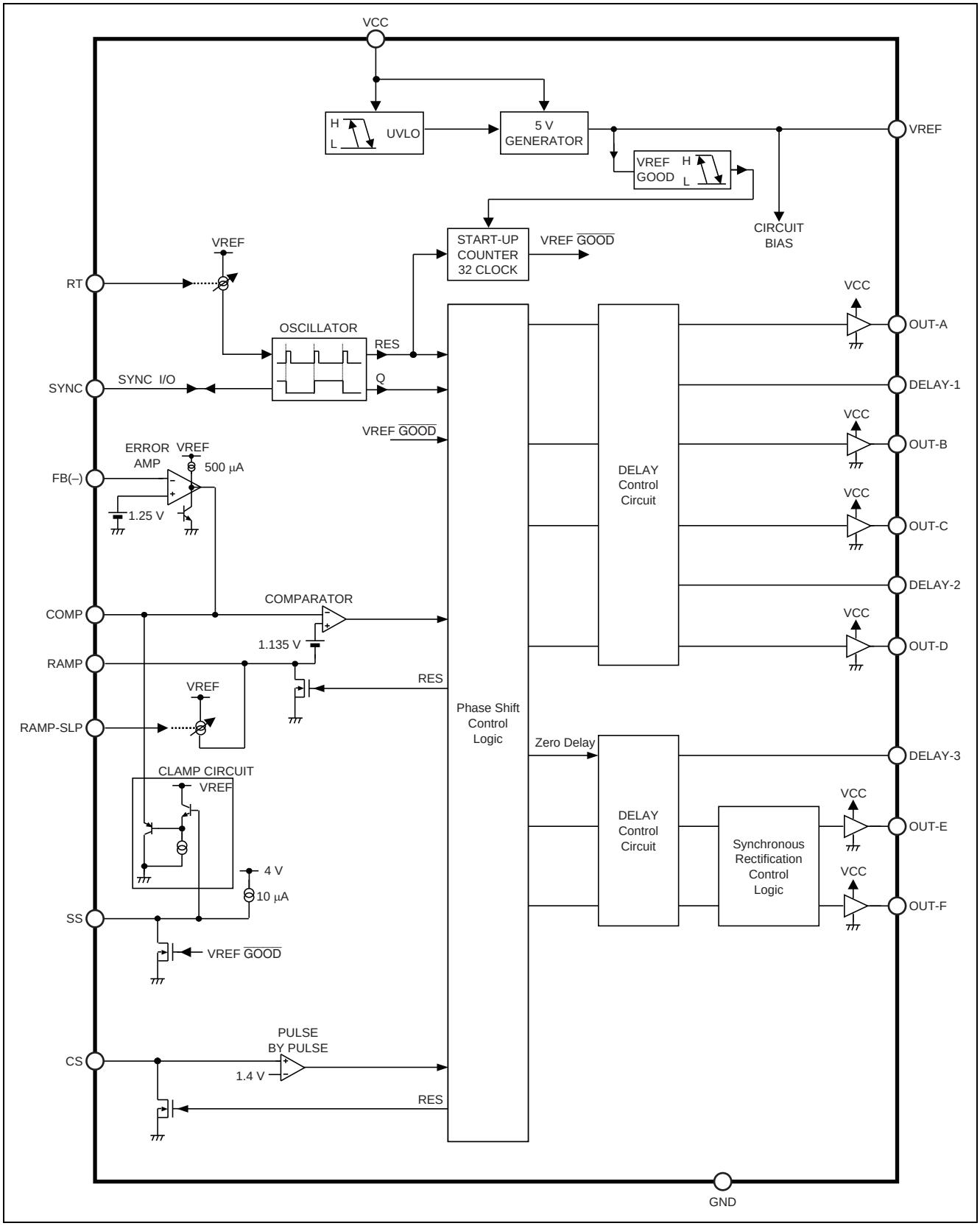
LQFP-40 Pin No.	SOP-20 Pin No.	Pin Name	Input/Output	Pin Function
1	8	DELAY-1	Input/Output	Delay time adjustor for the full-bridge control signal (OUT-A and B)
2	9	DELAY-2	Input/Output	Delay time adjustor for the full-bridge control signal (OUT-C and D)
4	10	DELAY-3	Input/Output	Delay time adjustor for the secondary control signal (OUT-E and F)
5	—	SEC-CONT	Input	Synchronous rectification on/off control
6	—	REMOTE	Input	Remote on/off control
7	11	VREF	Output	5 V/20 mA output
9	12	VCC	Input	IC power supply input
13	13	OUT-F	Output	Secondary control signal
14	14	OUT-E	Output	Secondary control signal
17	15	OUT-D	Output	Full-bridge control signal
18	16	OUT-C	Output	Full-bridge control signal
19	17	OUT-B	Output	Full-bridge control signal
20	18	OUT-A	Output	Full-bridge control signal
22	—	PGND	—	Ground level for the output signal
23	—	SGND	—	Ground level for the small signal
—	19	GND	—	Ground
24	20	RT	Input/Output	Timing resistor for the oscillator
27	1	SYNC	Input/Output	Synchronization I/O for the oscillator
29	2	RAMP-SLP	Input/Output	Ramp sloping adjustor
31	3	RAMP	Input	Ramp waveform set
33	4	CS	Input	Current sense signal input for OCP
34	—	CS-OUT	Output	Current sense information amplifier output
36	5	COMP	Output	Error amplifier output
37	6	FB(–)	Input	Error amplifier negative input
38	7	SS	Output	Timing capacitor for soft start
3, 8, 10 to 12, 15, 16, 21, 25, 26, 28, 30, 32, 35, 39, 40	—	N.C.	—	Open

Block Diagram

R2A20124AFP



R2A20124ASP



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Power supply voltage	Vcc	20	V	1
Peak output current	Ipk-out	±200	mA	2, 3
DC output current	Idc-out	±50	mA	3, 4
VREF output current	Iref-out	–20	mA	3
COMP sink current	Isink-comp	2	mA	3
DELAY set current	Iset-delay	0.3	mA	3
RT set current	Iset-rt	0.3	mA	3
RAMP-SLP set current	Iset-ramp-slp	0.3	mA	3
VREF terminal voltage	Vter-ref	–0.3 to +6	V	1, 5
Terminal group 1 voltage	Vter-1	–0.3 to (Vref + 0.3)	V	1, 6
Operating junction temperature	Tj-opr	–40 to +125	°C	7
Storage temperature	Tstg	–55 to +150	°C	

Notes: 1. Rated voltages are with reference to the GND or SGND pin.
2. The Rating shows the transient current when driving a capacitive load.
3. For rated currents, inflow to the IC is indicated by (+), and outflow by (–).
4. Total current of OUT-A, Out-B, OUT-C, OUT-D, OUT-E, and OUT-F must be not exceed ±90 mA.
5. VREF pin voltage must not exceed VCC pin voltage.
6. Terminal group 1 is defined the pins;
REMOTE, RAMP-SLP, SEC-CONT, CS, RAMP, COMP, CS-OUT, FB(–), SS, RT, SYNC, and DELAY-1 to 3
7. Theramal resistance θja
R2A20124AFP (40-pin); 85.3°C/W Board condition; Glass epoxy 50 mm × 50 mm × 1.6 mm, 10% wiring density.
R2A20124ASP (20-pin); 120°C/W Board condition; Glass epoxy 40 mm × 40 mm × 1.6 mm, 10% wiring density.

Electrical Characteristics

(Ta = 25°C, Vcc = 12 V, RT = 180 kΩ, Rdelay = 51 kΩ, Ramp-slp = 27 kΩ, unless otherwise specified.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY: R2A20124AFP/ASP						
Start threshold	VH	7.7	8.4	9.1	V	
Shutdown threshold	VL	7.4	8.0	8.6	V	
UVLO hysteresis	dVUVL	0.3	0.4	0.5	V	
Start-up current	Is	—	90	150	μA	Vcc = 7.5 V
Operating current	Icc	—	8	11.5	mA	No load on VREF pin
VREF: R2A20124AFP/ASP						
Output voltage	Vref	4.9	5.0	5.1	V	
Line regulation	Vref-line	—	0	10	mV	Vcc= 10 V to 16 V
Load regulation	Vref-load	—	6	20	mV	Iref= –1 mA to –20 mA
Temperature stability	dVref/dTa	—	±80*[1]	—	ppm/°C	Ta = –40°C to 105°C
OSCILLATOR: R2A20124AFP/ASP						
Oscillator frequency	fosc	—	200*[1]	—	kHz	
Switching frequency	fsw	85	100	115	kHz	Measured on OUT-A, -B
Line stability	fsw-line	–1.5	0	1.5	%	Vcc = 10 V to 16 V
Temperature stability	dfsw/dTa	—	±0.1*[1]	—	%/°C	Ta = –40°C to 105°C
RT voltage	V_{RT}	2.5	2.7	2.9	V	
SYNC: R2A20124AFP/ASP						
Input threshold	$V_{TH-SYNC}$	2.5	2.85	3.2	V	
Output high	$V_{OH-SYNC}$	3.5	4.0	—	V	RSYNC = 33 kΩ to GND *[2]
Output low	$V_{OL-SYNC}$	—	0.05	0.15	V	RSYNC = 33 kΩ to VREF
Minimum input pulse	T_{I-MIN}	50	—	—	ns	
Output pulse width	T_{O-SYNC}	—	3.0*[1]	—	μs	
REMOTE: R2A20124AFP						
On threshold voltage	$V_{ON-REMOTE}$	1.12	1.32	1.52	V	
Off threshold voltage	$V_{OFF-REMOTE}$	1.04	1.23	1.42	V	
REMOTE hysteresis	dVREMOTE	60	90	120	mV	
Input bias current	I_{REMOTE}	–100	–50	—	μA	REMOTE = 2 V
ERROR AMPLIFIER: R2A20124AFP/ASP						
FB(–) input voltage	$V_{FB(-)}$	1.225	1.250	1.275	V	FB(–) and COMP are shorted
FB(–) input current	$I_{FB(-)}$	–2.0	0	2.0	μA	FB(–) = 1.25 V
Open-loop DC gain	Av	—	80*[1]	—	dB	
Unity gain bandwidth	BW	—	2*[1]	—	MHz	
Output source current	I_{SOURCE}	–650	–500	–390	μA	FB(–) = 0.75 V, COMP = 2 V
Output sink current	I_{SINK}	2.0	6.5	—	mA	FB(–) = 1.75 V, COMP = 2 V
Output high voltage	V_{OH-EO}	3.7	3.9	—	V	FB(–) = 0.75 V, COMP; open
Output low voltage	V_{OL-EO}	—	0.1	0.4	V	FB(–) = 1.75 V, COMP; open
Output clamp voltage *[3]	$V_{CLAMP-EO}$	–0.16	–0.07	0.0	V	FB(–) = 0.75 V, COMP; open, SS = 1 V

Notes: 1. Design specification (reference data)
2. R2A20124AFP: SGND and PGND
3. $V_{CLAMP-EO} = V_{COMP}$ – SS voltage (1 V)

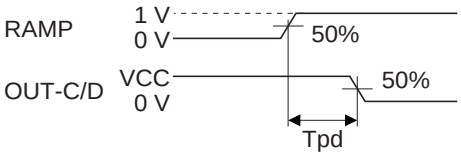
Electrical Characteristics (cont.)

(Ta = 25°C, Vcc = 12 V, RT = 180 kΩ, Rdelay = 51 kΩ, Rramp-slp = 27 kΩ, unless otherwise specified.)

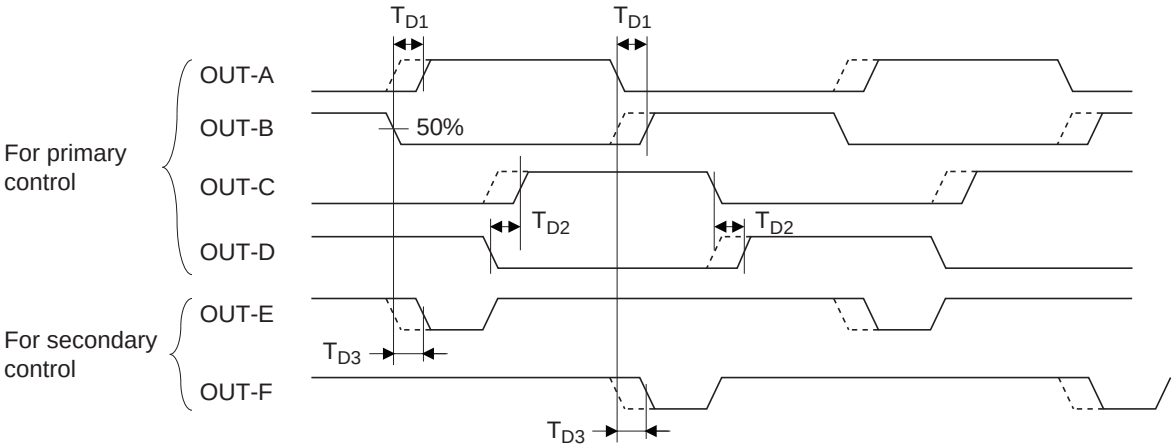
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
PHASE MODULATOR: R2A20124AFP/ASP						
RAMP offset voltage	V_{RAMP}	1.035	1.135	1.235	V	
RAMP source current	$Isource\text{-}_{RAMP}$	–220	–185	–150	µA	RAMP = 0.15 V, COMP; open
RAMP sink current	$I_{SINK\text{-}RAMP}$	3	10	—	mA	RAMP = 0.15 V, COMP = 0 V
Minimum phase shift	Dmin	—	0*1*4	—	%	RAMP = 0 V, COMP = 0 V
Maximum phase shift	Dmax	—	97.0*1*4	—	%	RAMP = 0 V, COMP = 2.1 V
Delay to OUT-C, -D *2	Tpd	—	100	200	ns	COMP = 1.6 V
RAMP discharge time *1	Tdis	—	80	120	ns	FB(–) = 0.75 V, COMP; open
RAMP-SLP voltage	$V_{RAMP\text{-}SLP}$	2.1	2.3	2.5	V	
DELAY: R2A20124AFP/ASP						
DELAY-1, -2 *3	$T_{D1, 2}$	70	100	130	ns	Delay set R = 51 kΩ
DELAY-3 *3	T_{D3}	45	65	85	ns	Delay set R = 51 kΩ
DELAY2-1, -2 *1*3	$T_{D2\_1, \_2}$	140	220	300	ns	Delay set R = 180 kΩ
DELAY2-3 *1*3	T_{D2_3}	110	170	230	ns	Delay set R = 180 kΩ
Terminal voltage	$V_{D1, 2, 3}$	1.9	2.0	2.1	V	Delay set R = 51 kΩ
SOFT START: R2A20124AFP/ASP						
Source current	I_{SS}	–14	–10	–6	µA	SS = 1 V
SS high voltage	$V_{OH\text{-}SS}$	3.9	4.0	4.1	V	

Notes: 1. Design specification (reference data)

2. Tpd is defined as;

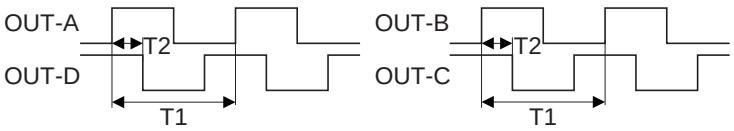


3. T_{D1}, T_{D2}, and T_{D3} are defined as;



4. Maximum/Minimum phase shift is defined as;

$$D = \frac{T2}{T1} \times 2 \times 100\ (\%)$$

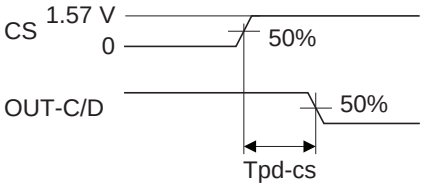


Electrical Characteristics (cont.)

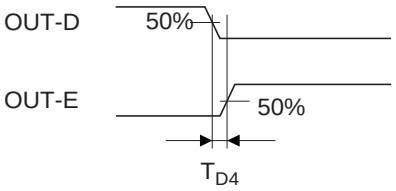
(Ta = 25°C, Vcc = 12 V, RT = 180 kΩ, Rdelay = 51 kΩ, Rramp-slp = 27 kΩ, unless otherwise specified.)

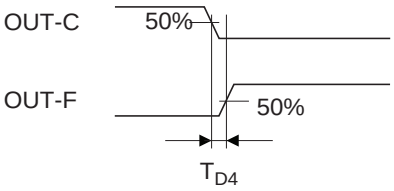
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
OVER CURRENT PROTECTION: R2A20124AFP/ASP						
Pulse-by-pulse current limit threshold	V_{CS-PP}	1.26	1.4	1.54	V	SEC-CONT = 0.3 V (AFP)
Delay to OUT pins *[1]	Tpd-cs	—	100	200	ns	CS = 0 V to 1.57 V, SEC-CONT = 0.3 V (AFP)
CS sink current	$I_{SINK-CS}$	2	5	—	mA	CS = 0.15 V, COMP = 0 V
OUTPUT: R2A20124AFP/ASP						
High voltage	V_{OH-OUT}	11.5	11.9	—	V	IOUT = –2 mA
Low voltage	V_{OL-OUT}	—	0.05	0.2	V	IOUT = 2 mA
Rise time	tr	—	30	100	ns	COUT = 100 pF
Fall time	tf	—	30	100	ns	COUT = 100 pF
Timing offset *[2]	T_{D4}	—	20	140	ns	
POWER INFORMATION AMPLIFIER: R2A20124AFP						
Tranceconductance	gm	15	20	25	µs	CS = 0.4 V
SECONDARY CONTROL: R2A20124AFP						
Forced synchronous rectification on voltage	Von-sec-cont	4.6	—	—	V	CS = 1 V
Forced synchronous rectification off voltage	Voff-sec-cont	—	—	0.4	V	CS = 0 V
Input bias current-1	$I_{SEC-CONT1}$	5	10	20	µA	CS = 0 V, SEC-CONT = 2.1 V
Input bias current-2	$I_{SEC-CONT2}$	10	20	40	µA	CS = 1 V, SEC-CONT = 2.1 V
Current hysteresis	$dI_{SEC-CONT}$	5	10	20	µA	

Notes: 1. Tpd-cs is defined as;



2. T_{D4} is defined as;

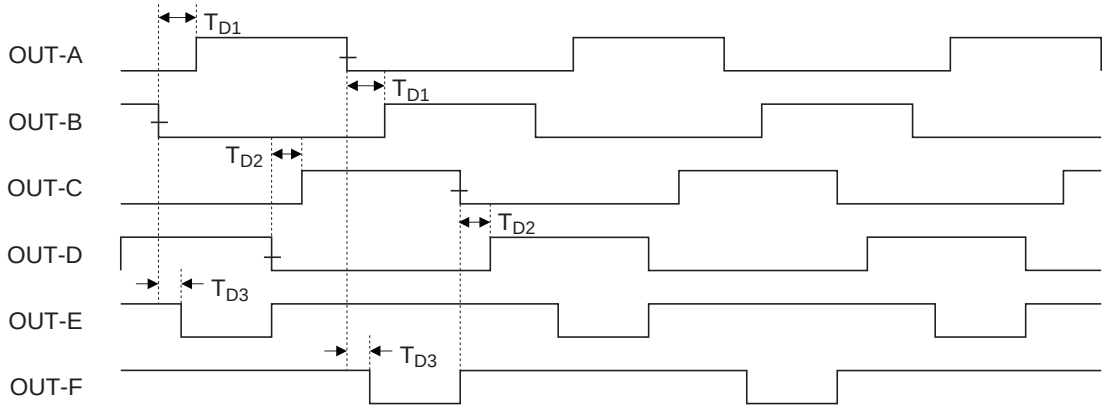




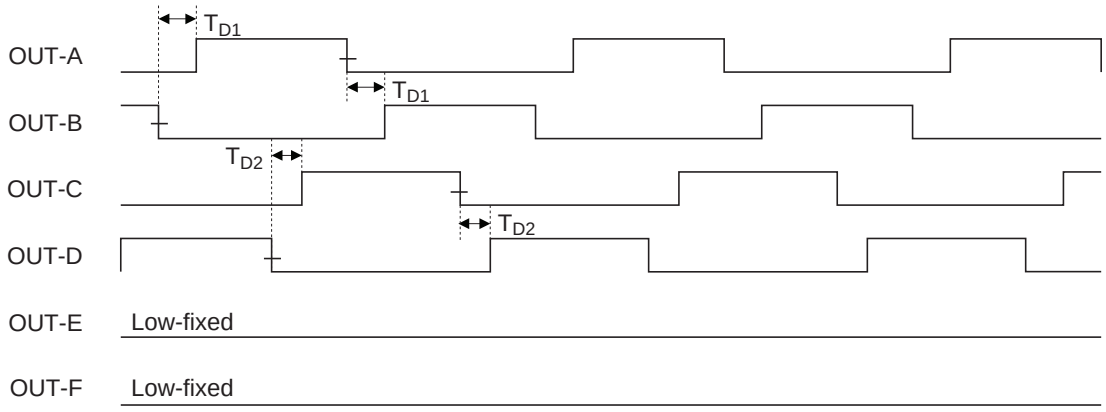
Timing Diagram

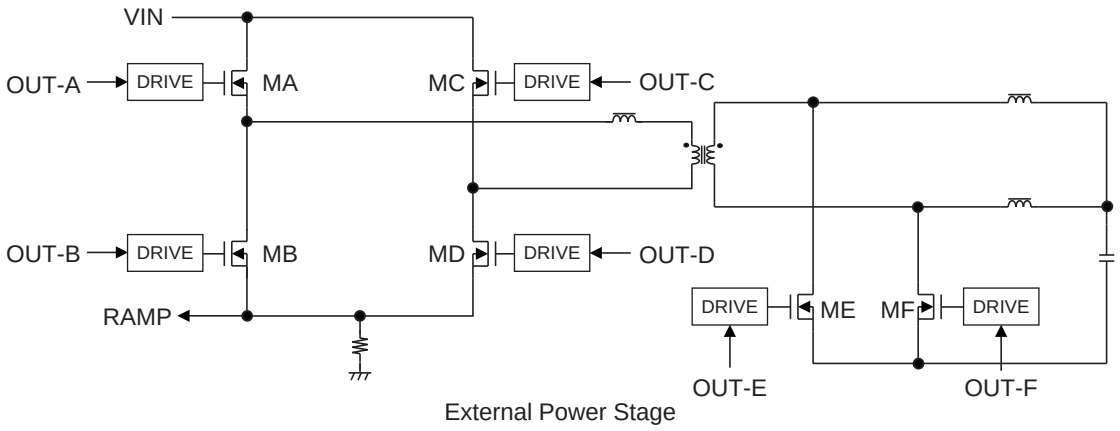
Note: All voltage, current, time shown in the diagram is typical value.

- Full Bridge and Secondary Control: R2A20124AFP/ASP



- Full Bridge and Secondary Control: R2A20124AFP (SEC-CONT > 4.6 V)

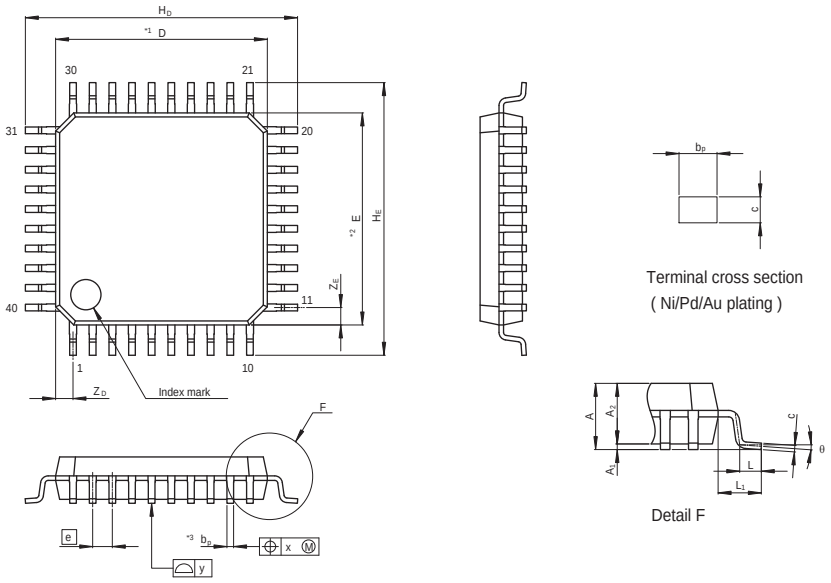




External Power Stage

Package Dimensions

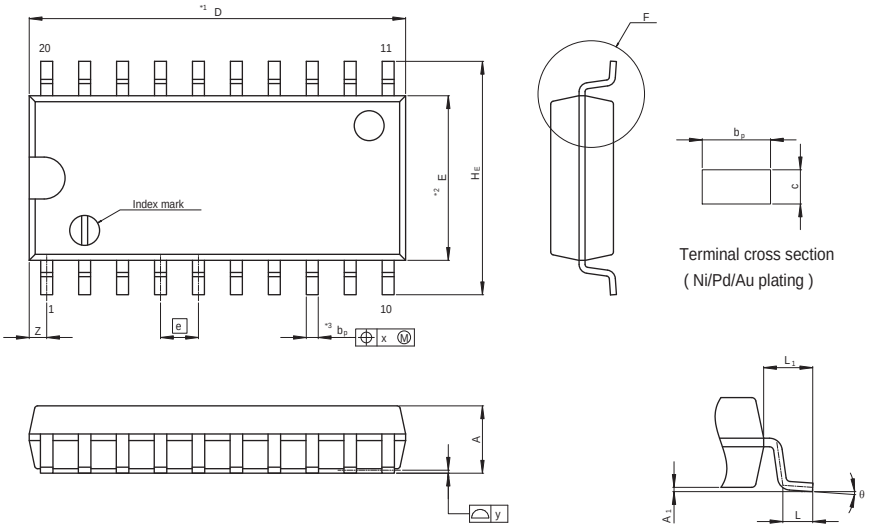
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP40-7x7-0.65	PLQP0040JB-C	FP-40EV	0.2g



NOTE)
1. DIMENSIONS"*1"AND"*2"
DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
A_2	—	1.40	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.70
A_1	0.08	0.13	0.22
b_p	0.17	0.22	0.27
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—
L	0.40	0.50	0.60
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.5x12.6-1.27	PRSP0020DD-B	FP-20DAV	0.31g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	12.60	13.0
E	—	5.50	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.20
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L_1	—	1.15	—

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