LM5170-Q1 Multiphase Bidirectional Current Controller

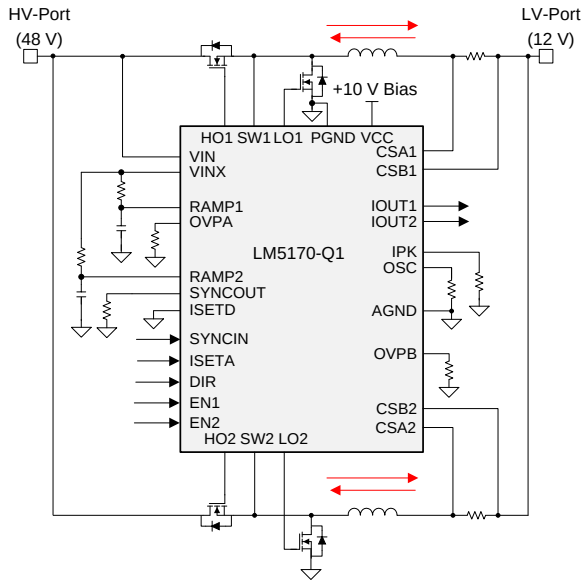
1 Features

- AEC-Q100 Qualified for Automotive Applications:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- 100-V HV-Port and 65-V LV-Port Max Ratings
- 1% Accurate Bidirectional Current Regulation
- 1% Accurate Channel Current Monitoring
- 5-A Peak Half-Bridge Gate Drivers
- Programmable or Adaptive Dead-Time Control
- Programmable Oscillator Frequency With Optional Synchronization to External Clock
- Independent Channel Enable Control Inputs
- Analog and Digital Channel Current Control Inputs
- Programmable Cycle-by-Cycle Peak Current Limit
- HV and LV Port Overvoltage Protection
- Diode Emulation Prevents Negative Current
- Programmable Soft-Start Timer
- MOSFET Failure Detect at Start-Up and Circuit Breaker Control
- Multiphase Operation Phase Adding or Dropping

2 Applications

- Automotive Dual Battery Systems
- Super-Cap or Battery Backup Power Converters
- Stackable Buck or Boost Converters

Simplified Application Circuit



3 Description

The LM5170-Q1 controller provides the essential high voltage and precision elements of a dual-channel bidirectional converter for automotive 48-V and 12-V dual battery systems. It regulates the average current flowing between the high voltage and low voltage ports in the direction designated by the DIR input signal. The current regulation level is programmed through analog or digital PWM inputs.

Dual-channel differential current sense amplifiers and dedicated channel current monitors achieve typical current accuracy of 1%. Robust 5-A half-bridge gate drivers are capable of driving parallel MOSFET switches delivering 500 W or more per channel. The diode emulation mode of the synchronous rectifiers prevents negative currents but also enables discontinuous mode operation for improved efficiency with light loads. Versatile protection features include cycle-by-cycle current limiting, overvoltage protection at both HV and LV ports, MOSFET failure detection and overtemperature protection.

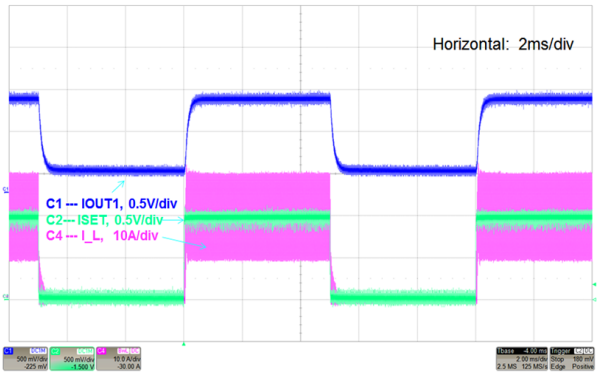
An innovative average current mode control scheme maintains constant loop gain allowing a single R-C network to compensate both buck and boost conversion. The oscillator is adjustable up to 500 kHz and can synchronize to an external clock. Multiphase parallel operation is achieved by connecting two LM5170-Q1 controllers for 3 or 4-phase operation, or by synchronizing multiple controllers to phase-shifted clocks for a higher number of phases. A low state on the UVLO pin disables the LM5170-Q1 in a low current shutdown mode.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5170-Q1	TQFP (48)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Channel Current Tracking ISETA Command



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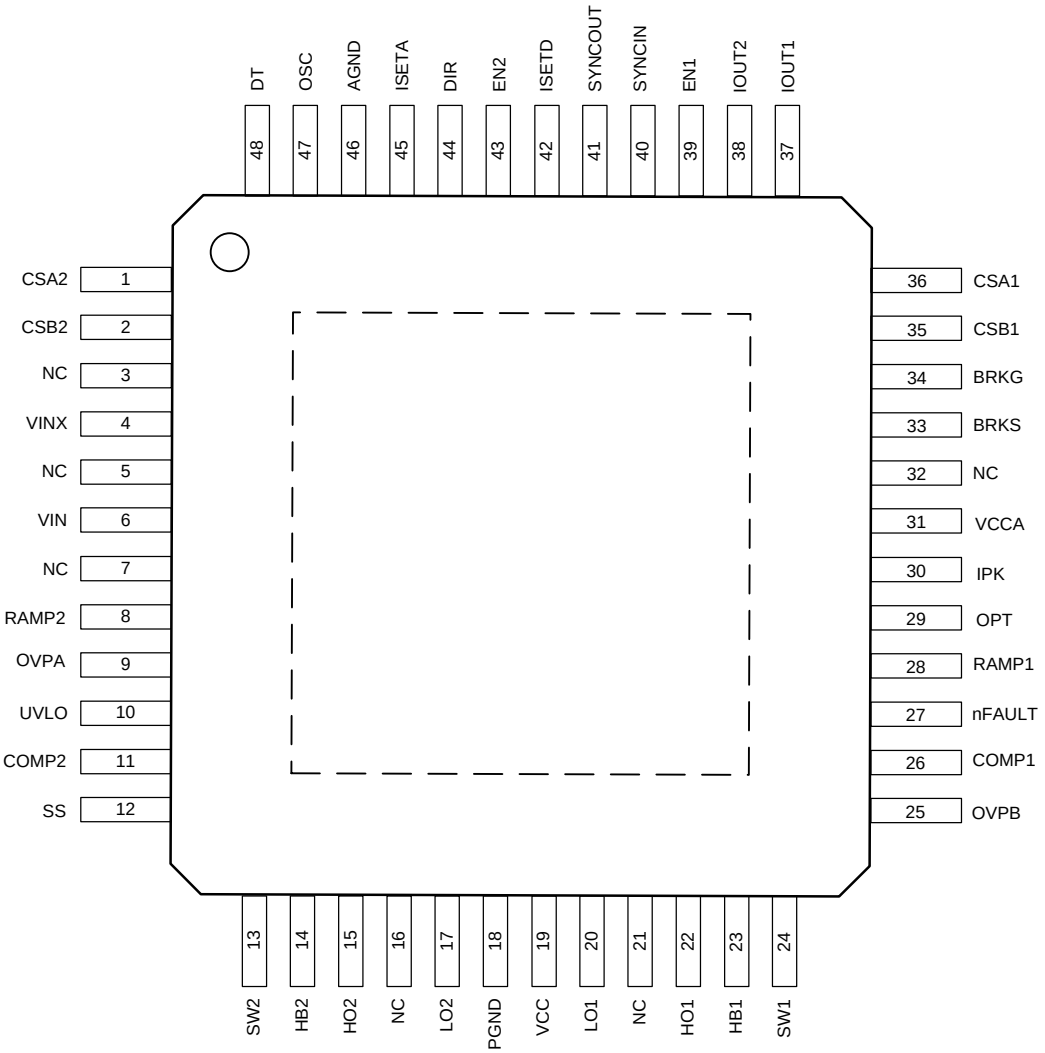
4 Revision History

DATE	REVISION	NOTES
November 2016	*	Initial release.

5 Pin Configuration and Functions

PHP Package
48-Pin TQFP
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	CSA2	I	CH-2 differential current sense inputs. The CSA2 pin connects to the CH-2 power inductor. The CSB2 pin connects to the circuit breaker or directly to the LV-Port if the circuit breaker is not used. The CH-2 current sense resistor is placed between these two pins.
2	CSB2	I	
3	NC	—	No Connect
4	VINX	O	Internally connected to VIN pin through a cutoff switch. When the controller is shutdown, VINX is disconnected from VIN, opening the current leakage path. When the controller is enabled, VINX is connected to VIN and serves as the pullup supply for the RC ramp generators at the RAMP1 and RAMP2 pins. VINX also pulls up the OVPA pin through an internal 3-MΩ resistor.
5	NC	—	No Connect
6	VIN	I	The input pin connecting to the HV-Port line voltage. It supplies the BRKG pin through an internal 330-µA current source.
7	NC	—	No Connect

(1) Note: G = Ground, I = Input, O = Output, P = Power

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
8	RAMP2	I	The inverting input of the CH-2 PWM Comparator. An external RC circuit tied between VINX, RAMP2, and AGND forms the ramp generator producing a ramp signal proportional to the HV-Port voltage, thus achieving a voltage feedforward function. The RAMP2 capacitor voltage is reset to AGND at the end of every switching cycle.
9	OVPA	I	Connected to the noninverting input of the HV-Port overvoltage comparator. An internal 3-MΩ pullup resistor and an external resistor across the OVPA and AGND pins form a divider that senses the HV-Port voltage. When the OVPA pin voltage is above the 1.185-V threshold, the SS capacitor is discharged and held low until the overvoltage condition is removed.
10	ULVO	I	The UVLO pin serves as the master enable pin. When UVLO is pulled below 1.25 V, the entire LM5170-Q1 is in a low quiescent current shutdown mode. When UVLO is pulled above 1.25 V but below 2.5 V, the LM5170-Q1 enters the initialization stage in which the nFAULT pin is first pulled up to 5 V, while the rest of the LM5170-Q1 is kept in the OFF state. When UVLO is pulled above the 2.5 V, the LM5170-Q1 enters a MOSFET failure detection stage. If no failure is detected, the circuit breaker gate driver (BRKS and BRKG) turns on, and the LM5170-Q1 enables the oscillator and RAMP generator, and stands by until the EN1 and EN2 commands enable the channel.
11	COMP2	O	Output of the CH-2 trans-conductance (gm) error amplifier and the noninverting input of the CH-2 PWM comparator. A loop compensation network must be connected to this pin.
12	SS	I	The soft-start programming pin. An external capacitor and an internal 25-μA current source set the ramp rate of the COMP pins voltage during soft start. If CH-2 is enabled after CH-1 completes soft start, the CH-2 turnon will not be controlled by the SS pin.
13	SW2	I	CH-2 switch node. Connect to the CH-2 high-side MOSFET source, the low-side MOSFET drain, and the bootstrap capacitor return terminal.
14	HB2	P	CH-2 high-side gate driver bootstrap supply input.
15	HO2	I/O	CH-2 high-side gate driver output.
16	NC	—	No Connect
17	LO2	I/O	CH-2 low-side gate driver output.
18	PGND	G	Power ground connection pin for the low-side gate drivers and external VCC bias supply.
19	VCC	I/P	VCC bias supply pin, powering the drivers. An external bias supply between 9 V to 12 V must be applied across the VCC and PGND pins.
20	LO1	I/O	CH-1 low-side gate driver output.
21	NC	—	No Connect
22	HO1	I/O	CH-1 high-side gate driver output.
23	HB1	P	CH-1 high-side gate driver bootstrap supply input.
24	SW1	I	CH-1 switch node. Connect to the CH-1 high-side MOSFET source, the low-side MOSFET drain, and the bootstrap capacitor return terminal.
25	OVPB	I	Connected to the noninverting input of the LV-Port overvoltage comparator. An internal 1-MΩ pullup resistor and an external resistor across the OVPB and AGND pins form the divider that senses the LV-Port voltage. When the converter operates in Boost mode the OVPB pin status is ignored. In Buck mode, when the OVPB pin voltage is above the 1.185-V threshold, the SS capacitor is discharged and held low until the overvoltage condition is removed.
26	COMP1	O	Output of the CH-1 trans-conductance (gm) error amplifier and the noninverting input of the CH-1 PWM comparator. A loop compensation network must be connected to this pin.
27	nFAULT	I/O	Fault flag pin or external shutdown pin. When a MOSFET drain-to-source short circuit failure is detected before start-up, the nFAULT pin will be internally pulled low to report the short-circuit failure, and the LM5170-Q1 will remain in a disabled state. The nFAULT pin can also be externally pulled low to shut down the LM5170-Q1, serving as a forced shutdown pin. In forced shutdown, all gate drivers turn off, and nFAULT is latched low until the UVLO pin is pulled below 1.25 V to release the latch and initiate a new start-up.
28	RAMP1	I	The inverting input of the CH-1 PWM comparator. An external RC circuit tied between VINX, RAMP1, and AGND forms the ramp generator producing a ramp signal proportional to the HV-Port voltage, thus achieving a voltage feedforward function. The RAMP1 capacitor voltage is reset to AGND at the end of every switching cycle.
29	OPT	I	Multiphase configuration pin. Tied to either VCCA or AGND, the OPT pin sets the phase lag of the SYNCOUT signal corresponding to 4 phase or 3 phase operation, respectively.
30	IPK	I	A resistor connected between IPK and AGND sets the threshold for the cycle-by-cycle current limit comparator
31	VCCA	I/P	Analog bias supply pin. Connect VCCA to VCC through an external 25-Ω resistor. A low-pass filter capacitor is required from the VCCA pin to AGND.
32	NC	—	No Connect.

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
33	BRKS	O	Connect to the common source of the circuit breaker MOSFET pair. When the circuit breaker function is disabled, simply connect to AGND through a 20-kΩ resistor.
34	BRKG	O	Connect to the gate pins of the circuit breaker MOSFET pair. Once the LM5170-Q1 is enabled, an internal 330-µA current source starts to charge the circuit breaker MOSFET gates. The BRKG to BRKS voltage is internally clamped at 12 V.
35	CSB1	I	CH-1 differential current sense inputs. The CSA1 pin connects to the CH-1 power inductor. The CSB1 pin connects to the circuit breaker, or directly to the LV-Port if the circuit breaker is not used. The CH-1 current sense resistor is placed between these two current sense pins. An internal 1-MΩ resistor is connected between the CSB1 and OVPB pins through an internal cutoff switch. During operation, the cutoff switch is closed and this internal resistor pulls up the OVPB pins. In shutdown mode, the internal resistor is disconnected by the cutoff switch.
36	CSA1	I	
37	IOUT1	O	CH-1 inductor current monitor pin. A current source proportional to the CH-1 inductor current flows out of this pin. Placing a terminating resistor and filter capacitor from IOUT1 to AGND produces a DC voltage representing the CH-1 DC current level. An internal 25-µA offset DC current source at the IOUT1 pin raises the active signal to be above the ground noise, thus improving the monitor noise immunity.
38	IOUT2	O	CH-2 inductor current monitor pin. A current proportional to the CH-2 inductor current flows out of this pin. Placing a terminating resistor and filter capacitor from IOUT2 to AGND produces a DC voltage representing the CH-2 DC current level. An internal 25-µA offset DC current source at the IOUT2 pin raises the active signal above the ground noise, thus improving the monitor noise immunity.
39	EN1	I	CH-1 enable pin. Pulling EN1 above 2.4 V turns off the SS pulldown and allows CH-1 to begin a soft-start sequence. Pulling EN1 below 1 V discharges the SS capacitor and holds it low. The high- and low-side gate drivers of both channels are held in the low state when SS is discharged.
40	SYNCIN	I	Input for an external clock that overrides the free-running internal oscillator. The SYNCIN pin can be left open or grounded when it is not used.
41	SYNCOUT	O	Clock output pin and fault check mode selector. SYNCOUT is connected to the downstream LM5170-Q1 in a 3- or 4-phase configuration. It also functions as a circuit breaker selection pin during start-up. Placing a 10-kΩ resistor from the SYNCOUT to AGND pins disables the fault check. feature. If no resistor is connected from SYNCOUT to AGND, the fault check is enabled.
42	ISETD	I	The PWM current programming pin. The inductor DC current level is proportional to the PWM duty cycle. Use either ISETA or ISETD but not both for channel current programming. When ISETD is not used, short ISETD to AGND.
43	EN2	I	CH-2 enable pin. Pulling EN2 above 2.4 V enables CH-2. Pulling EN2 below 1 V shuts down the HO2 and LO2 drivers.
44	DIR	I	Direction command input. Pulling DIR above 2 V sets the converter to the buck mode, which commands the current to flow from the HV-Port to LV-Port. Pulling DIR below 1 V sets the converter to the boost mode, which commands the current to flow from the LV-Port to HV-Port. If the DIR pin is left open, the LM5170-Q1 detects an invalid command and disables both channels with the MOSFET gate drivers in the low state.
45	ISETA	I, O	The analog current programming pin. The inductor DC current is proportional to the ISETA voltage. Use either ISETA or ISETD but not both for channel current programming. When ISETA is not used, connect a 100-pF to 0.1-µF capacitor from ISETA to AGND.
46	AGND	G	Analog ground reference. AGND must connect to PGND externally through a single point connection to improve the LM5170-Q1 noise immunity.
47	OSC	I	The internal oscillator frequency is programmed by a resistor between OSC and AGND.
48	DT	I	A resistor connected between DT and AGND sets the dead time between the high-side and low-side driver outputs. Tie the DT pin to VCCA to activate the internal adaptive dead time control.
—	EP	—	Exposed pad of the package. No internal electrical connections. Must be soldered to the large ground plane to reduce thermal resistance.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Voltage	VIN, VINX, to AGND	–0.3	95	V
	VIN, VINX, to AGND 50-ns Transient		100	
	VIN to VINX	–0.3	95	
	VIN to VINX 50-ns Transient		100	
	SW1, SW2 to PGND	–5	95	
	SW1, SW2 to PGND (20-ns Transient)		100	
	SW1, SW2 to PGND (50-ns Transient)	–16		
	HB1 to SW1, HB2 to SW2	–0.3	14	
	HO1 to SW1, HO2 to SW2	–0.3	HB + 0.3	
	HO1 to SW1, HO2 to SW2 (20-ns Transient)	–1.5		
	LO1, LO2 to PGND	–0.3	VCC + 0.3	
	LO1, LO2 to PGND (20-ns Transient)	–1.5		
	BRKG, BRKS, to PGND	–0.3	65	
	CSA1, CSB1, CSA2, CSB2 to PGND	–5	65	
	CSA1 to CSB1, CSA2 to CSB2	–0.3	0.3	
	BRKG to BRKS	–0.3	14	
	EN1, EN2, DIR, IOUT1, IOUT2, IPK, ISETA, ISETD, nFAULT, OSC, OVPA, OVPB, SYNCIN, SYNCOUT, UVLO, to AGND	–0.3	7	
	PGND to AGND	–0.3	0.3	
	VCC to PGND, VCCA, DT, OPT, COMP1, COMP2, RAMP1, RAMP2, SS, to AGND	–0.3	14	
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specs, see www.ti.com/packaging.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 12, 13, 24, 25, 36, 37, and 48)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
VIN, HV-Port		Buck mode	6		85	V
		Boost mode	6		85	
LV-Port		Buck mode	0		60	V
		Boost mode	3		60	
V_{VCC}	External voltage applied to VCC		9		12	V

(1) *Recommended Operating Conditions* are conditions under which the device is intended to be functional. For specifications and test conditions, see the *Electrical Characteristics*.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
T_J	Operating junction temperature(2)	–40		150	°C
F_{OSC}	Oscillator frequency	50		500	kHz
F_{EX_CLK}	Synchronization to external clock frequency (minimal 50 kHz)	0.8 × F_{OSC}		1.2 × F_{OSC}	kHz
t_{DT}	Programmable dead time	15		200	ns
	ISETD PWM frequency	1		100	kHz
	SYNCIN pulse width	100		500	ns

(2) High junction temperatures degrade operating lifetime. Operating lifetime is de-rated for junction temperature greater than 125°C.

6.4 Thermal Information

THERMAL METRIC(1)		LM5170-Q1 PHP (TQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

F_{OSC} = 100 kHz; V_{VCC} = 10 V; V_{VIN} = $V_{HV\text{-}Port}$ = 48 V and $V_{LV\text{-}Port}$ = 12 V, unless otherwise stated.(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
VIN SUPPLY (VIN, VINX)						
$I_{SHUTDOWN}$	VIN pin current in shutdown mode	V_{UVLO} = 0 V			10	µA
$I_{STANDBY}$	VIN pin current, no switching	V_{VCC} > 9 V, V_{UVLO} > 2.5 V, V_{EN1} = V_{EN2} = 0 V		1		mA
	VIN to VINX disconnect switch	V_{UVLO} < 1 V or V_{VCC} < 7.5 V	5			MΩ
	VIN to VINX disconnect switch	V_{UVLO} > 2.6 V, V_{VCC} > 9 V		100		Ω
VCC AND VCCA BIAS SUPPLIES						
V_{CCUVLO}	VCC undervoltage detection	V_{VCC} falling	7.6	8	8.3	V
V_{CCHYS}	VCC UVLO hysteresis	V_{VCC} rising	8.1	8.5	8.9	V
I_{VCC_SD}	VCC sink current in shutdown mode	V_{UVLO} = 0 V			20	µA
I_{VCC_SB}	VCC sink current in standby: no switching	V_{UVLO} > 2.6 V, V_{EN1} = V_{EN2} = 0 V			10	mA
MASTER ON/OFF CONTROL (UVLO)						
V_{UVLO_TH}	UVLO release threshold	UVLO voltage rising	2.4	2.5	2.6	V
I_{HYS}	UVLO hysteresis current	UVLO source current when V_{UVLO} > 2.6 V	21	25	29	µA
V_{SD}	UVLO shutdown threshold (IC shutdown)	UVLO voltage falling	1	1.25	1.5	V
	UVLO shutdown release	UVLO voltage rising above V_{SD}	0.15	0.25	0.35	V
t_{UVLO}	UVLO glitch filter time	UVLO voltage falling		2.5		µs
	UVLO internal pulldown current			1		µA
CHANNEL ENABLE INPUTS EN1 AND EN2						
V_{IL}	Enable input low state	Disabled the driver outputs			1	V
V_{IH}	Enable input high state	Enable the driver outputs	2			V

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Minimum and maximum limits apply over the –40°C to 125°C junction temperature range.
(3) Typical values correspond to T_J = 25°C.

Electrical Characteristics (continued)

F_{OSC} = 100 kHz; V_{VCC} = 10 V; V_{VIN} = $V_{HV-Port}$ = 48 V and $V_{LV-Port}$ = 12 V, unless otherwise stated.(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
	Internal pulldown impedance	EN1, EN2 internal pulldown resistor		100		kΩ
	EN glitch filter time (the rising and falling edges)			2		µs
DIRECTION COMMAND (DIR)						
V_{DIR}	Command for current flowing from LV-Port to HV-Port (boost mode 12 V to 48 V)	Actively pulled low by external circuit			1	V
	Command for current flowing from HV-Port to LV-Port (buck mode 48 V to 12 V)	Actively pulled high by external circuit	2			V
	Standby (invalid DIR command)	DIR neither active high nor active low		1.5		V
	DIR glitch filter	Both rising and falling edges		10		µs
ISET INPUT (ISETA, ISETD)						
G_{ISETA}	Regulated DC current sense voltage to ISETA voltage	$\|V_{CSA} - V_{CSB}\|$ = 50 mV	19.7	20	20.3	mV/V
	ISETA internal pulldown resistor			170		kΩ
G_{ISETD}	Conversion ratio of ISETA voltage to ISETD duty cycle	ISETD frequency = 10 kHz, Duty = 100%	30.63	31.25	31.88	mV / %
V_{ISETD_LO}	ISETD PWM signal low-state voltage				1	V
V_{ISETD_HI}	ISETD PWM signal high-state voltage		2			V
	ISETD internal pulldown resistor			100		kΩ
	ISETD internal decoder filter resistor (tied to ISETA pin)			100		kΩ
OUTPUT CURRENT MONITOR (IOUT1, IOUT2)						
G_{IOUT_BK1}	IOUT1 and IOUT2 versus channel current sense voltage, in buck mode	$\|V_{CSA} - V_{CSB}\|$ = 50 mV, V_{DIR} > 2 V	4.9	5	5.1	µA/mV
G_{IOUT_BST1}	IOUT1 and IOUT2 versus channel current sense voltage, in boost mode	$\|V_{CSA} - V_{CSB}\|$ = 50 mV, V_{DIR} < 1 V	4.9	5	5.1	µA/mV
G_{IOUT_BK2}	IOUT1 and IOUT2 versus channel current sense voltage, in buck mode	$\|V_{CSA} - V_{CSB}\|$ = 10 mV, V_{DIR} > 2 V, T_J = 25°C	4.91	5.18	5.43	µA/mV
G_{IOUT_BST2}	IOUT1 and IOUT2 versus channel current sense voltage, in boost mode	$\|V_{CSA} - V_{CSB}\|$ = 10 mV, V_{DIR} < 1 V, T_J = 25°C	4.47	4.77	5.1	µA/mV
	IOUT1 and IOUT2 DC offset currents	$\|V_{CSA} - V_{CSB}\|$ = 0 mV	22	25	28	µA
CURRENT SENSE AMPLIFIER (BOTH CHANNELS)						
G_{CS_BK1}	Amplifier output to current sense voltage in buck mode	$\|V_{CSA} - V_{CSB}\|$ = 50 mV, V_{DIR} > 2 V	49.25	50	50.75	V/V
G_{CS_BST1}	Amplifier output to current sense voltage in boost mode	$\|V_{CSA} - V_{CSB}\|$ = 50 mV, V_{DIR} < 1 V	49.25	50	50.75	V/V
G_{CS_BK2}	Amplifier output to current sense voltage in buck mode	$\|V_{CSA} - V_{CSB}\|$ = 10 mV, V_{DIR} > 2 V, T_J = 25°C	49	52	55	V/V
G_{CS_BST2}	Amplifier output to current sense voltage in boost mode	$\|V_{CSA} - V_{CSB}\|$ = 10 mV, V_{DIR} < 1 V, T_J = 25°C	45	48	51	V/V
BW_{CS}	Amplifier bandwidth			10		MHz
TRANSCONDUCTION AMPLIFIER (COMP1, COMP2)						
Gm	Transconductance			1		mA/V
I_{COMP}	Output source current limit	V_{ISETA} = 2.5 V, $\|V_{CSA} - V_{CSB}\|$ = 10 mV		2		mA
	Output sink current limit	V_{ISETA} = 0 V, $\|V_{CSA} - V_{CSB}\|$ = 50 mV		–2		mA
BW_{gm}	Amplifier bandwidth			4		MHz
PWM COMPARATOR						
	COMP to output delay			50		ns
	COMP to PWM offset			1		V
$T_{OFF(min)}$	Minimum OFF time		150	200	250	ns
RAMP GENERATOR (RAMP1 AND RAMP2)						
	RAMP discharge device $R_{DS(on)}$				15	Ω
	Threshold voltage for valid ramp signal		0.6			V
PEAK CURRENT LIMIT (IPK)						
	IPK internal current source		22.5	25	27.5	µA

Electrical Characteristics (continued)

F_{OSC} = 100 kHz; V_{VCC} = 10 V; V_{VIN} = $V_{HV-Port}$ = 48 V and $V_{LV-Port}$ = 12 V, unless otherwise stated.(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
IPK_{Buck}	Current sense voltage versus cycle-by-cycle limit threshold voltage given at IPK pin, in buck mode	R_{IPK} = 40 kΩ, V_{DIR} > 2 V		46		mV/V
IPK_{Boost}	Current sense voltage versus cycle-by-cycle limit threshold voltage given at IPK pin, in boost mode	R_{IPK} = 40 kΩ, V_{DIR} < 1 V		48		mV/V
OVERVOLTAGE PROTECTION (OVPA, OVPB)						
	OVP threshold	OVP voltage rising	1.15	1.185	1.22	V
OVP_{HYS}	OVP hysteresis (falling edge)			100		mV
	OVPA and OVPB glitch filter			5		µs
R_{OVPA}	Internal OVPA pullup resistor	VINX to OVPA impedance		3		MΩ
R_{OVPB}	Internal OVPB pullup resistor	CSB1 to OVPB impedance, V_{UVLO} > 2.6 V		1		MΩ
OSCILLATOR (OSC)						
	Oscillator frequency 1	R_{OSC} = 40 kΩ, SYNCIN open	90	100	110	kHz
	Oscillator frequency 2	R_{OSC} = 10 kΩ, SYNCIN open	335	375	410	kHz
V_{OSC}	OSC pin DC voltage			1.25		V
SYNCIN						
V_{SYNIH}	SYNCIN input threshold for high state		2			V
$V_{SYNIL\ SYNC}$	SYNCIN input threshold for low state				1	V
	Internal pulldown impedance	V_{SYNCIN} = 2.5 V		100		kΩ
	Delay to establish synchronization	0.8 × F_{OSC} < F_{SYNCIN} < 1.2 × F_{OSC}		200		µs
SYNCOUT						
V_{SYNOH}	SYNCOUT high state		2.5			V
V_{SYNOL}	SYNCOUT low state				0.4	V
	Sourcing current when SYNCOUT in high state	$V_{SYNCOUT}$ = 2.5 V		1		mA
	SYNCOUT pulse width		240	300	370	ns
	SYNCOUT phase delay configurations	V_{OPT} > 2 V		90		Degree
		V_{OPT} < 1 V		120		
$R_{SYNCOUT}$	Circuit breaker signature	Use circuit breaker function and fault detection at start-up		OPEN		kΩ
		Do not use circuit breaker function or disable fault detection at start-up		10		
BOOTSTRAP (HB1, HB2)						
V_{HB-UV}	Bootstrap undervoltage threshold	(V_{HB} – V_{SW}) voltage rising	5.7	6.5	7.3	V
$V_{HB-UV-HYS}$	Hysteresis			0.5		V
I_{HB-LK}	Bootstrap quiescent current	V_{HB} – V_{SW} = 10 V, V_{HO} – V_{SW} = 0 V			50	µA
HIGH-SIDE GATE DRIVERS (HO1, HO2)						
V_{OLH}	HO low-state output voltage	I_{HO} = 100 mA		0.1		V
V_{OHH}	HO high-state output voltage	I_{HO} = –100 mA, V_{OHH} = V_{HB} – V_{HO}		0.15		V
	HO rise time (10% to 90% pulse magnitude)	C_{LD} = 1000 pF		5		ns
	HO fall time (90% to 10% pulse magnitude)	C_{LD} = 1000 pF		4		ns
I_{OHH}	HO peak source current	V_{HB} – V_{SW} = 10 V		4		A
I_{OLH}	HO peak sink current	V_{HB} – V_{SW} = 10 V		5		A
LOW-SIDE GATE DRIVERS (LO1, LO2)						
V_{OLL}	LO low-state output voltage	I_{LO} = 100 mA		0.1		V
V_{OHL}	LO high-state output voltage	I_{LO} = –100 mA, V_{OHL} = V_{VCC} – V_{LO}		0.15		V
	LO rise time (10% to 90% pulse magnitude)	C_{LD} = 1000 pF		5		ns
	LO fall time (90% to 10% pulse magnitude)	C_{LD} = 1000 pF		4		ns
I_{OHL}	LO peak source current			4		A
I_{OLL}	LO peak sink current			5		A

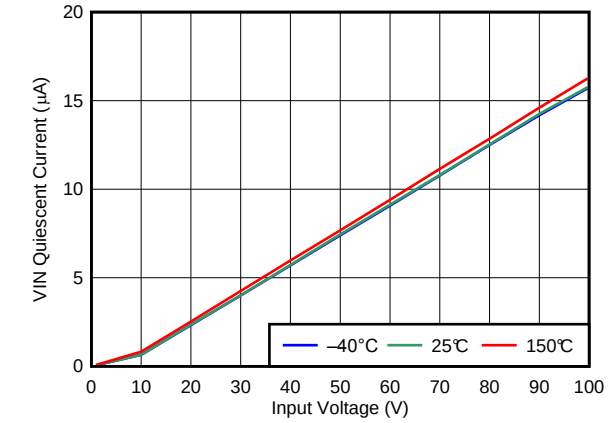
Electrical Characteristics (continued)

F_{OSC} = 100 kHz; V_{VCC} = 10 V; V_{VIN} = $V_{HV-Port}$ = 48 V and $V_{LV-Port}$ = 12 V, unless otherwise stated.(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
INTERLEAVE PHASE DELAY FROM CH-2 To CH-1 (OPT)						
V_{OPTL}	OPT input low state				1	V
V_{OPTH}	OPT input high state		2			V
	HO2 on-time rising edge versus HO1 on-time rising edge, or LO2 on-time rising edge versus LO1 on-time rising edge	V_{OPT} > 2 V for 2, 4, 6, and 8 phases	175	180	185	Degrees
		V_{OPT} < 1 V for 3 phases	235	240	245	
	Internal pulldown impedance			1		MΩ
DEAD TIME (DT)						
t_{DT}	LO falling edge to HO rising edge delay	R_{DT} = 7.5 kΩ		40		ns
t_{DT}	HO falling edge to LO rising edge delay	R_{DT} = 7.5 kΩ		40		ns
V_{DT}	DC voltage level for programming			1.25		V
V_{DT}	DC voltage for adaptive dead time scheme only (short DT to VCCA)			VCCA		V
V_{ADPT}	HO-SW or LO-GND voltage threshold to enable cross output for adaptive dead time scheme	V_{VCC} > 9 V, (V_{HB} – V_{SW}) > 8 V, HO or LO voltage falling		1.5		V
t_{ADPT}	LO falling edge to HO rising edge delay	V_{DT} = V_{VCC}		36		ns
t_{ADPT}	HO falling edge to LO rising edge delay	V_{DT} = V_{VCC}		41		ns
SOFT START (SS)						
I_{SS}	SS charging current source	V_{SS} = 0 V		25		µA
$V_{SS-OFFS}$	SS to PWM comparator offset	SS – PWM comparator noninverting input		1		V
R_{SS}	SS discharge device $R_{DS(on)}$	V_{SS} = 2 V		30		Ω
V_{SS_LOW}	SS discharge completion threshold	Once it is discharged by internal logic		0.23		V
DIODE EMULATION						
	Current zero cross threshold	Current sense voltage		0		mV
CKT BREAKER CONTROL (BRKG, BRKS)						
I_{BRKG}	Sourcing current	nFAULT = 5 v, V_{VIN} = 24 V, V_{BRKS} = 12 V	275	330	375	µA
$V_{BRK-CLP}$	Voltage clamp	nFAULT= 5 V, V_{VIN} = 48 V, V_{BRKS} = 12 V	9		14	V
$R_{BRK-SINK}$	Sinking capability	nFAULT = 0 V		20		Ω
V_{READY}	BRKG to BRKS voltage threshold to indicate readiness for operation	Rising edge	6.5	8.5		V
$I_{BRKG-LEAK}$	BRKG leakage current	nFAULT= 5 V, V_{VIN} – V_{BRKS} = 0 V, V_{BRKG} – V_{BRKS} = 10 V			10	µA
FAULT ALARM (nFAULT)						
	In normal operation, no fault		4	5		V
	Internal pull-up impedance for normal operation			30		kΩ
	Internal pull-down FET $R_{DS(on)}$ after fault detected				125	Ω
	External pull-down voltage threshold for IC shutdown				1	V
t_{FAULT}	External pul-ldown glitch filter			2		µs
t_{d1_FAULT}	Delay time of nFAULT pull-down below 1 V to (V_{BRKG} – V_{BRKS}) < 1.5 V				5	µs
t_{d2_FAULT}	Start-up fault detection duration	V_{UVLO} > 2.6 V, V_{VCC} > 9 V			3	ms
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown			175		ºC
T_{SD-HYS}	Thermal shutdown hysteresis			25		ºC

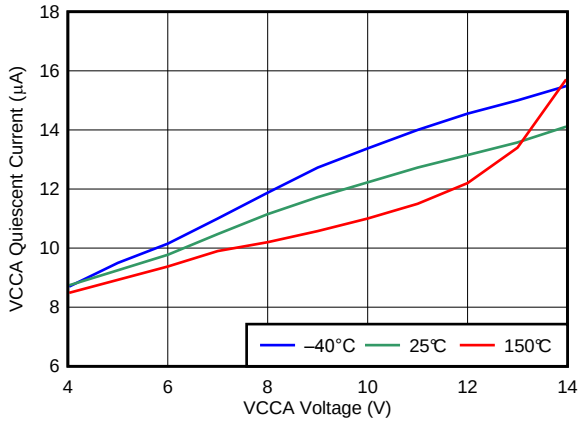
6.6 Typical Characteristics

V_{VIN} = 48 V, V_{VCC} = 10 V, V_{UVLO} = 3.3 V, T_J = 25°C, unless otherwise stated.



V_{UVLO} = 0 V

Figure 1. VIN Shutdown I_Q



V_{UVLO} = 0 V

Figure 2. VCCA Shutdown I_Q

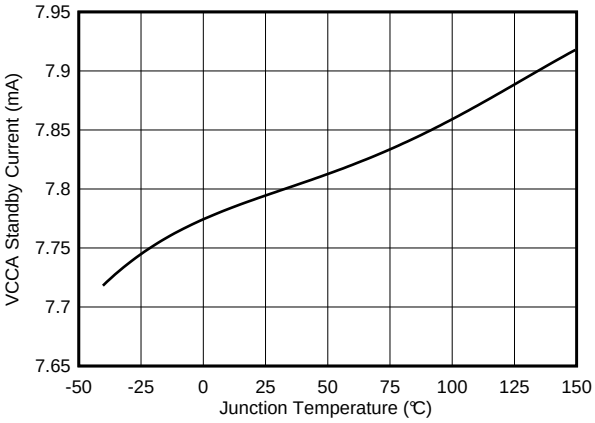


Figure 3. VCCA Standby Current vs Temperature

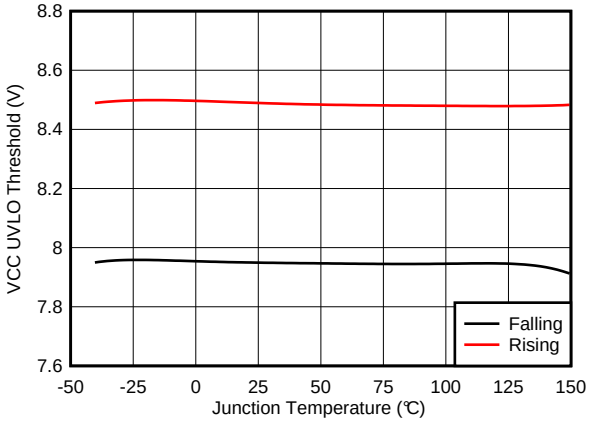
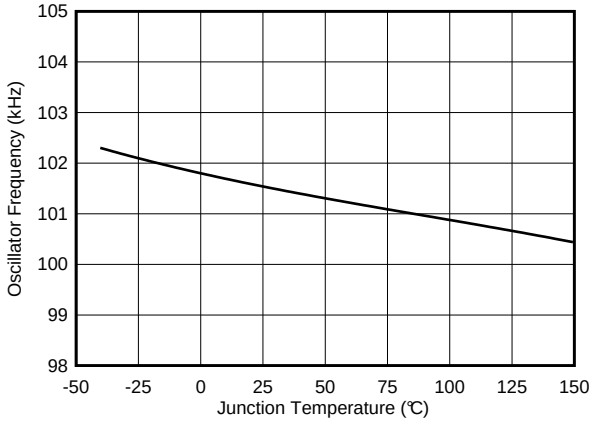


Figure 4. VCC UVLO Threshold vs Temperature



R_{OSC} = 40.2 kΩ

Figure 5. Oscillator Frequency vs Temperature

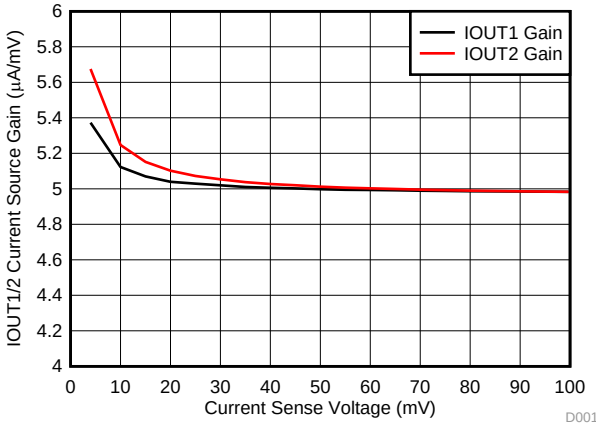


Figure 6. IOUT1/2 Current Monitor Accuracy vs V_{CS}

Typical Characteristics (continued)

V_{VIN} = 48 V, V_{VCC} = 10 V, V_{UVLO} = 3.3 V, T_J = 25°C, unless otherwise stated.

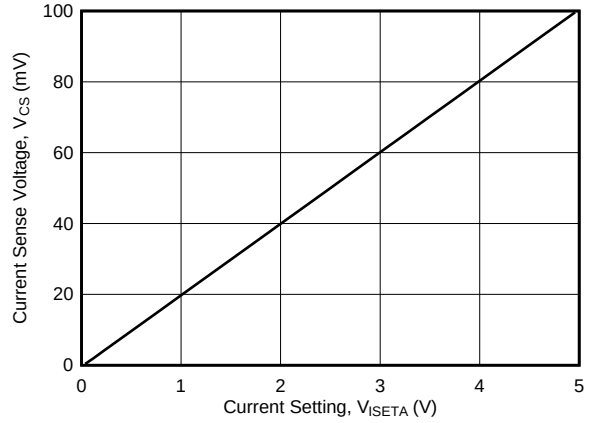
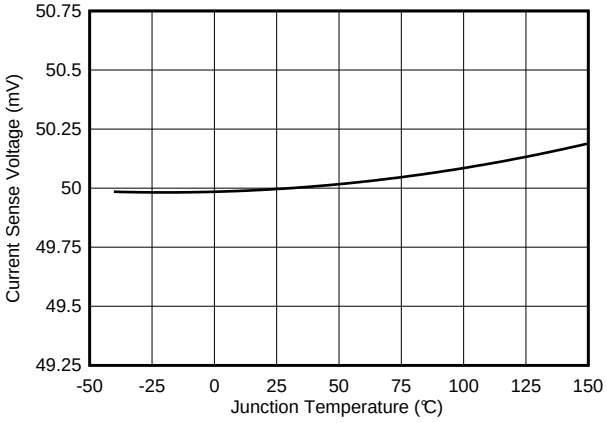


Figure 7. Regulated V_{CS} Voltage vs ISETA Voltage



V_{ISETA} = 2.5 V

Figure 8. Regulated V_{CS} Voltage vs Temperature

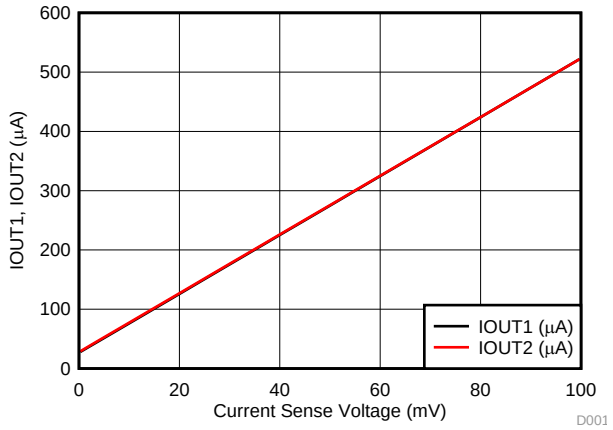
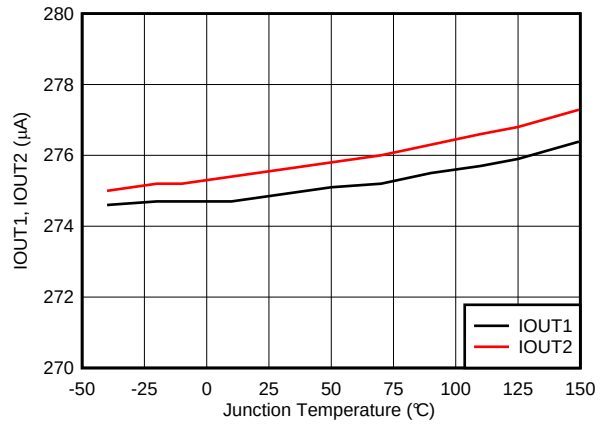


Figure 9. IOUT1/2 Current Monitor vs V_{CS} Voltage



V_{CS} = 50 mV

Figure 10. IOUT1/2 Current Monitor vs Temperature

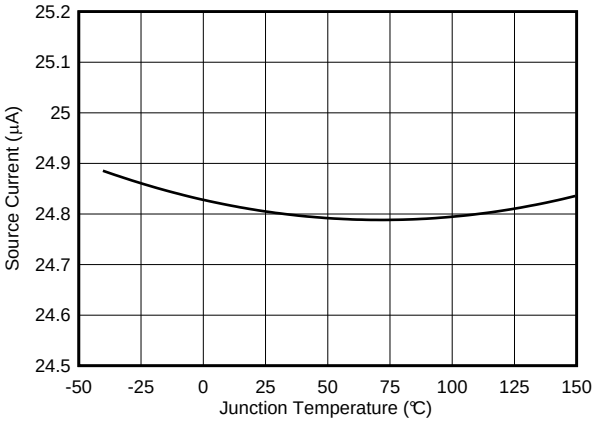


Figure 11. IPK Current Source vs Temperature

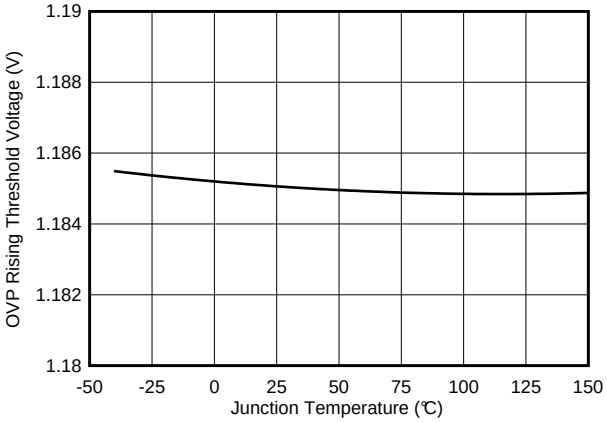


Figure 12. OVP Reference Voltage vs Temperature

Typical Characteristics (continued)

V_{VIN} = 48 V, V_{VCC} = 10 V, V_{UVLO} = 3.3 V, T_J = 25°C, unless otherwise stated.

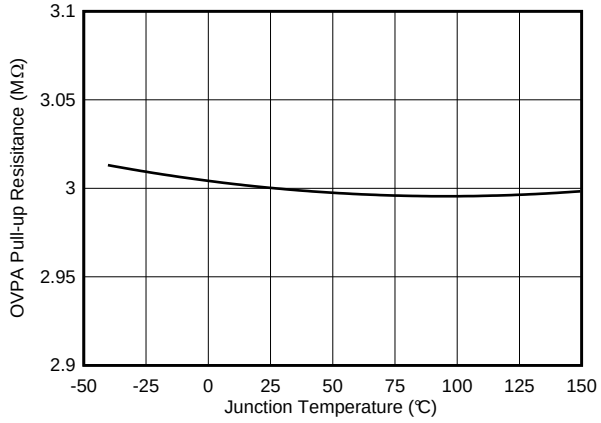


Figure 13. OVPA Pull-up Resistance vs Temperature

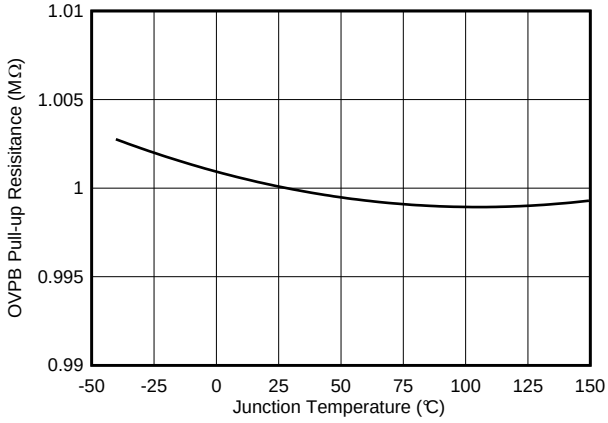
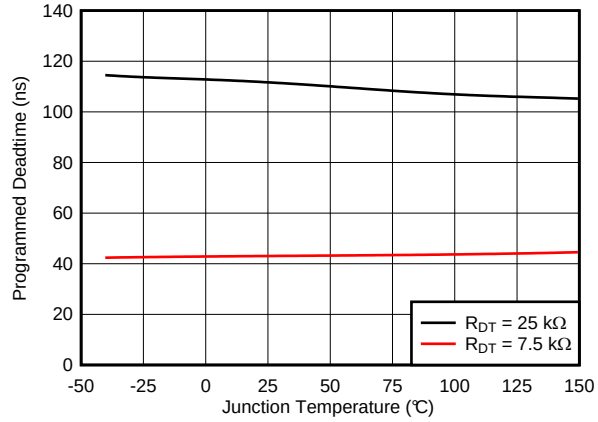
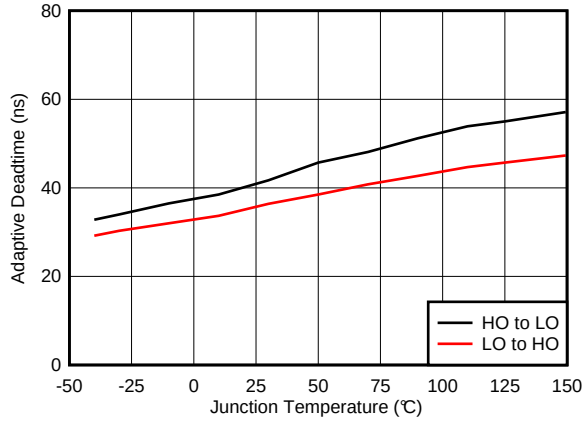


Figure 14. OVPB Pull-up Resistance vs Temperature



F_{SW} = 100 kΩ

Figure 15. Programmed Dead-Time vs Temperature



V_{DT} = V_{VCC}

Figure 16. Adaptive Dead Time vs Temperature

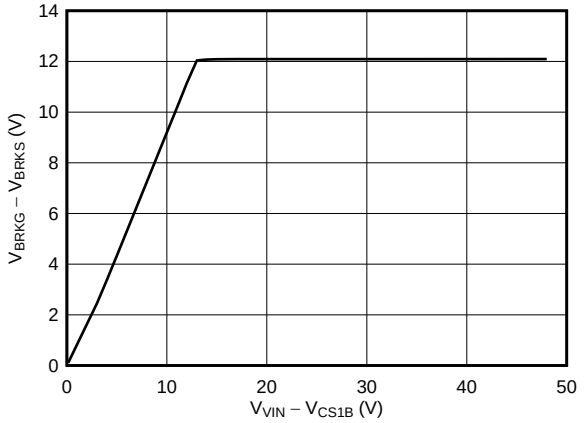


Figure 17. [V_{BRKG} – V_{BRKS}] vs [V_{VIN} – V_{BRKG}] Voltage

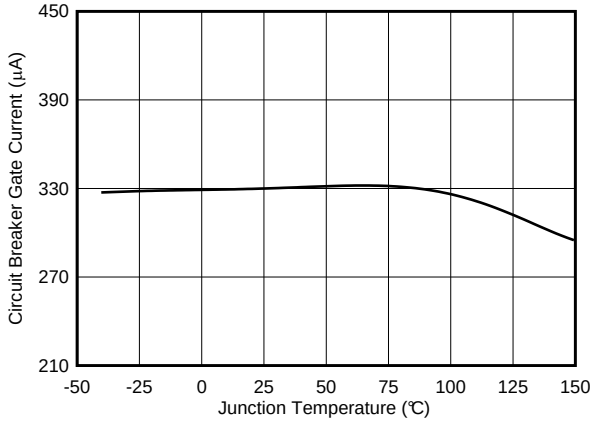


Figure 18. Circuit Breaker Gate Current vs Temperature

7 Detailed Description

7.1 Overview

The LM5170-Q1 device is a high performance, dual-channel bidirectional current controller intended to manage current transfer between a Higher Voltage Port (HV-Port) and a Lower Voltage Port (LV-Port) like the 48-V and 12-V ports of automotive dual battery systems. It integrates essential analog functions that enable the design of high power converters with a minimal number of external components. It regulates DC current in the direction designated by the DIR pin input signal. The current regulation level is programmed by the analog signal applied at the ISETA pin or the digital PWM signal at the ISETD pin. Independent enable signals activate each channel of the dual controller.

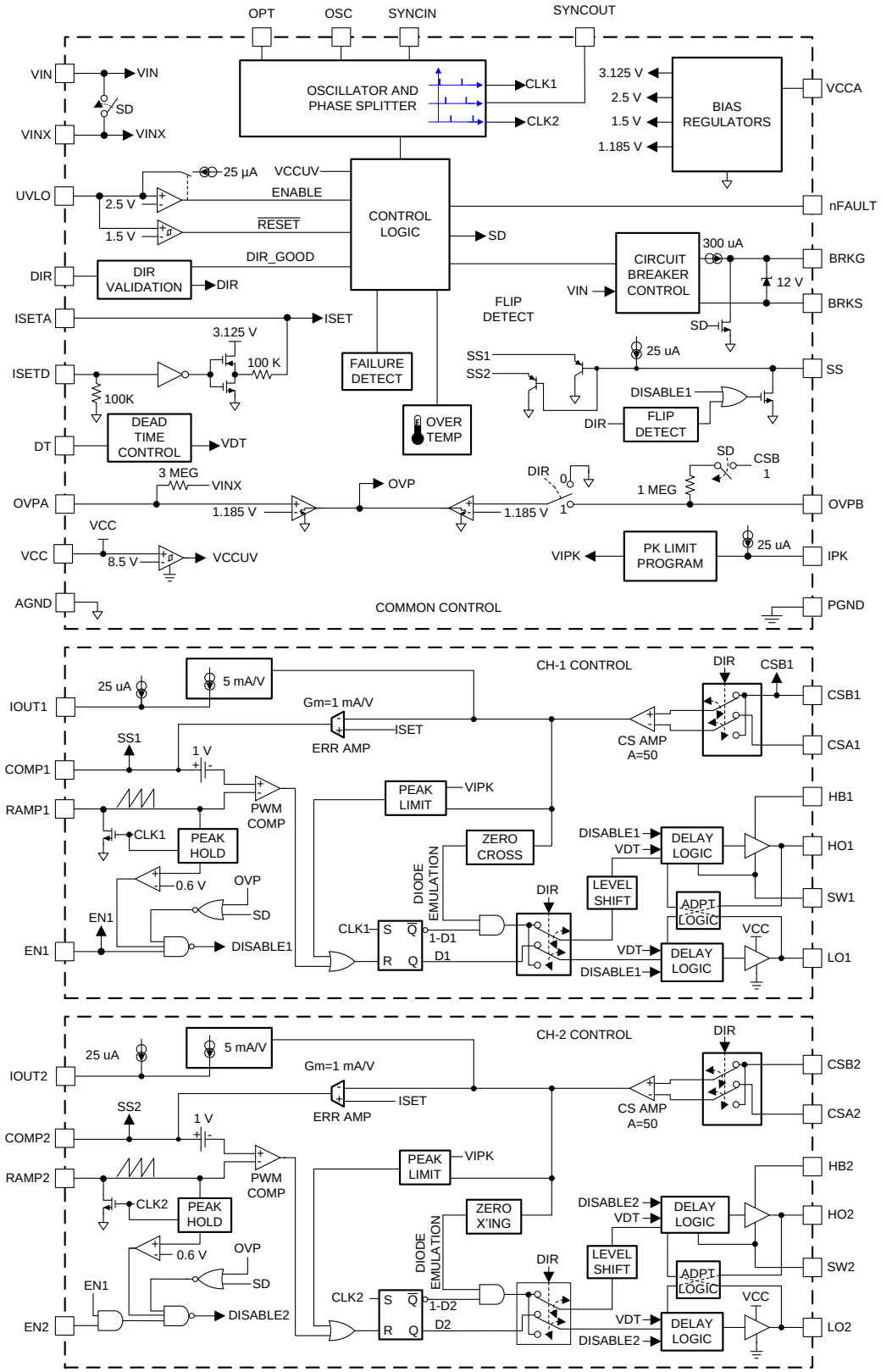
The dual-channel differential current sense amplifiers and dedicated channel current monitors achieve typical accuracy of 1%. The robust 5-A half-bridge gate drivers are capable of controlling parallel MOSFET switches delivering 500 W or more per channel. The diode emulation mode of the buck or boost synchronous rectifiers enables discontinuous mode operation for improved efficiency under light load conditions, and it also prevents negative current. Versatile protection features include the cycle-by-cycle peak current limit, overvoltage protection of both 48-V and 12-V battery rails, detection and protection of MOSFET switch failures, and overtemperature protection.

The LM5170-Q1 uses average current mode control which simplifies compensation by eliminating the right-half plane zero in the boost operating mode and by maintaining a constant loop gain regardless of the operating voltages and load level. The free-running oscillator is adjustable up to 500 kHz and can be synchronized to an external clock within ±20% of the free running oscillator frequency. Stackable multiphase parallel operation is achieved by connecting two LM5170-Q1 controllers in parallel for 3 or 4 phase operation, or by synchronizing multiple LM5170-Q1 controllers to external multiphase clocks for a higher number of phases. The UVLO pin provides master ON/OFF control that disables the LM5170-Q1 in a low quiescent current shutdown state when the pin is held low.

Definition of IC Operation Modes:

- **Shutdown Mode:** When the UVLO pin is < 1.25 V, or VCC < 8 V, or nFAULT < 1.25 V, the LM5170-Q1 is in the shutdown mode with all gate drivers in the low state, all internal logic reset, and the VINX pin disconnected from the VIN pin. When UVLO < 1.25 V, the IC draws < 20 µA through the VIN and VCC pins.
- **Initialization Mode:** When the UVLO pin is > 1.5 V but < 2.5 V, and VCC > 8.5 V, and nFAULT > 2 V, the LM5170-Q1 establishes proper internal logic states and prepares for circuit operation.
- **Standby Mode:** When the UVLO pin is > 2.5 V, and VCC > 8.5 V, and nFAULT > 2 V, the LM5170-Q1 first performs fault detection for 2 to 3 ms, during which the external power MOSFETs are each checked for drain-to-source short-circuit conditions. If a fault is detected, the LM5170-Q1 returns to the shutdown mode and is latched in shutdown until reset through UVLO or VCC pins. If no failure is detected, the LM5170-Q1 is ready to operate. The circuit breaker MOSFETs are turned on and the oscillator and ramp generators are activated, but the four gate drive outputs remain off until the EN1 or EN2 initiate the power delivery mode.
- **Power Delivery Mode:** When the UVLO pin > 2.5 V, VCC > 8.5 V, nFAULT > 2 V, EN1 and/or EN2 > 2 V, DIR is valid (either > 2 V or < 1 V), and ISETA > 0 V, the SS capacitor is released and the LM5170-Q1 regulates the DC current at the level set at the ISETA pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Bias Supply (VCC, VCCA)

The LM5170-Q1 requires an external bias supply of 9 V to 12 V at the VCC and VCCA pins to function. If an external supply voltage is greater than 12 V, a 10-V LDO or switching regulator should be used to produce 10 V for VCC and VCCA. Figure 19 shows typical connections of the bias supply. The VCC voltage is directly fed to the low-side MOSFET drivers. A 1-µF to 2.2-µF ceramic capacitor must be placed between the VCC and PGND pins to bypass the driver switching currents. The VCCA pin serves as the bias supply input for the internal logic and analog circuits for which the ground reference is the AGND pin. VCCA should be connected to VCC through a 25- to 50-Ω external resistor. A 0.1-µF to 1-µF bypass capacitor must be placed between the VCCA and AGND pins to filter out possible switching noise.

The internal VCC undervoltage (UV) detection circuit monitors the VCC voltage. When the VCC voltage falls below 8 V on the falling edge, the LM5170-Q1 is held in the shutdown state. For normal operation, the VCC and VCCA voltages must be greater than 8.5 V on a rising edge.

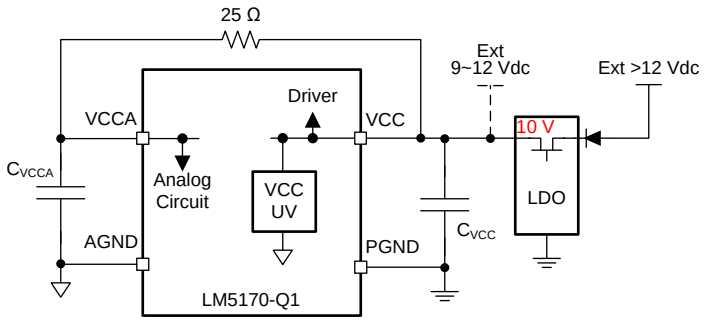


Figure 19. VCC Bias Supply Connections

7.3.2 Undervoltage Lockout (UVLO) and Master Enable or Disable

The UVLO pin serves as the master enable or disable pin. To use the UVLO pin to program undervoltage lockout control for the HV-port, LV-port, or VCC rail, see *Optional UVLO Programming* for details.

There are two UVLO voltage thresholds. When the pin voltage is externally pulled below 1.25 V, the LM5170-Q1 is in shutdown mode, in which all gate drivers are in the OFF state, all internal logic resets, the VINX pin is disconnected from VIN pin, and the IC draws less than 20 µA through the VIN, VCC and VCCA pins.

When the VCC voltage is above the 8.5 V and the UVLO pin voltage is pulled higher than 1.5 V but lower than 2.5 V, the LM5170-Q1 is in the initialization mode in which the nFAULT pin is pulled up to about 5 V, but the rest of the LM5170-Q1 remain off.

When the UVLO pin is pulled higher than 2.5 V, which is the UVLO release threshold and the master enable threshold, the LM5170-Q1 starts the MOSFET failure detection in a period of 2 to 3 ms (see *Power MOSFET Failure Detection and Failure Protection (nFAULT, BRKG, BRKS)*). If no failure is detected, BRKG pin starts to source a 330-µA current to charge the gates of the breaker MOSFETs.

When the BRKG to BRKS voltage is above 8.5 V, the LM5170-Q1 enters standby mode. In standby mode, the VINX pin is internally connected to the VIN pin through an internal cutoff switch (see Figure 20), and the internal 1-MΩ OVPB pullup resistor is connected to the CSB1 pin through another internal cutoff switch (see Figure 36). The oscillator and the RAMP1 and RAMP2 generators start to operate, and the SYNCOUT pin starts to send clock pulses at the oscillator frequency, and the LM5170-Q1 is ready to operate. The LO1, LO2, HO1, and HO2 drivers remain off until the EN1, EN2, and DIR inputs command them to operate.

When a MOSFET gate-to-source short-circuit failure is detected, the LM5170-Q1 is latched off. The latch can only be reset by pulling the VCC pin below 8 V, or by pulling the UVLO pin below 1.25 V. For details, see *Power MOSFET Failure Detection and Failure Protection (nFAULT, BRKG, BRKS)*.

Feature Description (continued)

7.3.3 High Voltage Input (VIN, VINX)

Figure 20 shows the external and internal configuration for the VIN and VINX pins. Both are rated at 100 Vdc. The VIN pin should be connected either directly to the voltage rail of the HV-Port, or through a small RC filter consisting of 10- to 20-Ω resistor and 0.1-µF to 1-µF bypass capacitor. The internal 330-µA current source supplying the BRKG pin is supplied by the VIN pin.

A cutoff switch connects and disconnects the VIN and VINX pins. When the UVLO pin voltage is greater than 2.5 V, and when the VCC voltage is greater than 8.5 V, the switch is closed and the VINX and VIN pins are connected.

The VINX pin serves as the supply pin for the RAMP generators (see Figure 20 and the *Ramp Generator* section for details). It is also the high-side terminal of the internal 3-MegΩ pullup resistor for the OVPA pin (see *Overvoltage Protection (OVPA, OVPB)* for details). Moreover, it serves as the HV-Port voltage sense for internal circuit use during operation.

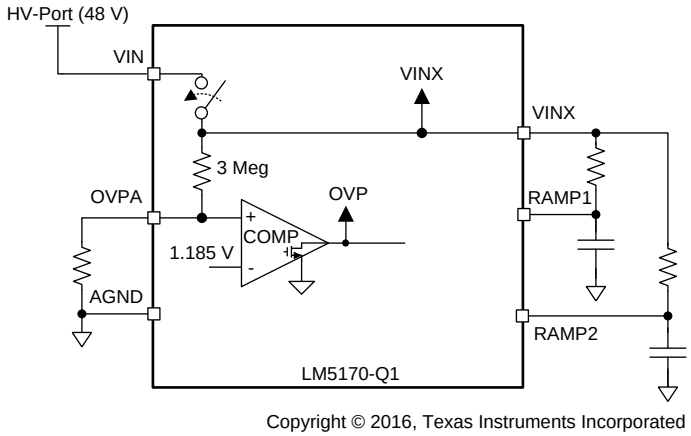


Figure 20. VIN and VINX Pins Configuration

7.3.4 Current Sense Amplifier

Each channel of the LM5170-Q1 has an independent bidirectional, high accuracy, and high-speed differential current sense amplifier. The differential current sense polarity is determined by the DIR command. The amplifier gain is 50, such that a smaller current sense resistor can be used to reduce power dissipation. The amplified current sense signal is used to perform the following functions:

- Applied to the inverting input of the error amplifier for current loop regulation.
- Used to reconstruct the channel current monitor signal at the IOUT1 and IOUT2 pins.
- Monitored by the cycle-by-cycle peak current limit comparator for instantaneous overcurrent protection.
- Sensed by the current zero cross detector to operate the synchronous rectifiers in diode emulation mode.

The current sense resistor Rcs should be selected for 50-mV current sense voltage when the channel DC current reaches the rated level. The CS1A, CS1B, CS2A, and CS2B pins should be Kelvin connected for accurate sensing.

It is very important that the current sense resistors are non-inductive. Otherwise the sensed current signals will be distorted even if the parasitic inductance is only a few nH. Such inductance may not affect the current regulation during continuous conduction mode, but it does affect current zero cross detection, and hence the performance of diode emulation mode under light load. As a consequence, the synchronous rectifier gate pulse will be truncated much earlier than the inductor current zero crossing, causing the body diode of the synchronous rectifier to conduct unnecessarily for a longer time. See the *Diode Emulation* section for details.

If the selected current sense resistor has parasitic inductance, see the *Application Information* section for methods to compensate for this condition and achieve optimal performance.

Feature Description (continued)

7.3.5 Control Commands

7.3.5.1 Channel Enable Commands (EN1, EN2)

These pins are two state function pins. Always use CH-1 if only single-channel operation is required. Note that CH-2 can only be enabled when CH-1 is also enabled.

a. When the EN1 pin voltage is pulled above 2 V (logic state of 1), the HO1 and LO1 outputs are enabled through soft start.
b. When the EN1 pin voltage is pulled below 1 V (logic state of 0), CH-1 controller is disabled and both HO1 and LO1 outputs are turned off.
c. Similar behaviors for EN2, HO2 and LO2 of CH-2, except that the EN2 pin does not affect the SS pin. Refer to *Soft Start* for details.
d. When the EN1 and EN2 pins are left open, an internal 100-kΩ pulldown resistor sets them to the low state.
e. The built-in 2-µs glitch filters prevent errant operation due to the noise on the EN1 and EN2 signals.

7.3.5.2 Direction Command (DIR)

This pin is a triple function pin.

a. When the DIR pin is actively pulled above 2 V (logic state of 1), the LM5170-Q1 operates in buck mode, and current flows from the HV-Port to the LV-Port.
b. When the DIR pin is actively pulled below 1 V (logic state of 0), the LM5170-Q1 operates in boost mode, and current flows from the LV-Port to the HV-Port.
c. When the DIR pin is in the third state that is different from the above two, it is considered an invalid command and the LM5170-Q1 remains in standby mode regardless of the EN1 and EN2 states. This tri-state function prevents faulty operation when losing the DIR signal connection to the MCU.
d. When DIR changes state between 1 and 0 dynamically during operation, the transition causes the SS pin to discharge first to below 0.23 V, then the SS pin pulldown is released and the LM5170-Q1 goes through a new soft-start process to produce the current in the new direction. This eliminates surge current during the direction change.
e. The built-in 10-µs glitch filter prevents errant operation by noise on the DIR signal.

7.3.5.3 Channel Current Setting Commands (ISETA or ISETD)

The LM5170-Q1 accepts the current setting command in the form of either an analog voltage or a PWM signal. The analog voltage uses the ISETA pin, and the PWM signal uses the ISETD pin. There is an internal ISETD decoder that converts the PWM duty ratio at the ISETD pin to an analog voltage at the ISETA pin. Owing to possible ground noise impact, TI recommends users to remove EN1 signal to achieve no load (0 A).

Figure 21 and Figure 22 show the pin configurations for current programming with an analog voltage or a PWM signal. The channel DC current is expressed in terms of resulted differential current sense voltage V_{CS_dc}. When ISETA is used, the ISETD pin can be left open or connected to AGND. When ISETD is used, place a ceramic capacitor C_{ISETA} between the ISETA pin and AGND. C_{ISETA} and the internal 100-kΩ at the output of the ISETD decoder forms a low-pass RC filter to attenuate the ripple voltage on ISETA. However, the RC filter delays the ISETD dynamic change to be reflected on ISETA. To limit the delay not to exceed T_{delay_ISETD}, the time constant of the RC filter should satisfy Equation 1.

$$100k\Omega \times C_{ISETA} \le \frac{T_{delay\_ISETD}}{4} \tag{1}$$

Therefore, the maximum C_{ISETA} should be determined by Equation 2:

$$C_{ISETA} \le \frac{T_{delay\_ISETD}}{4 \times 100k\Omega} \tag{2}$$

On the other hand, the time constant of the RC filter should be big enough for effective filtering. To attenuate the ripple by 40 dB, the RC filter corner frequency should be at least two decade below F_{ISETD}, that is, Equation 3

$$\frac{1}{2\pi \times 100k\Omega \times C_{ISETA}} \le 0.01 \times F_{ISETD} \tag{3}$$

Feature Description (continued)

Therefore the minimum ISETD signal frequency should be determined by Equation 4:

$$F_{ISETD} \geq \frac{1}{2\pi \times 1k\Omega \times C_{ISETA}} \geq \frac{400}{2\pi \times T_{delay\_ISETD}} \quad (4)$$

For instance, if ISETA is required to settle down to the steady-state in 1 ms following an ISETD duty ratio step change, namely T_{delay_ISETD} < 1 ms, the user should select C_{ISETA} < 2.5 nF, and F_{ISETD} > 64 kHz. If T_{delay_ISETD} < 0.1 ms, then C_{ISETA} < 250 pF, and F_{ISETD}> 640 kHz. Note that the feedback loop property causes additional delay for the actual current to settle to the new regulation level.

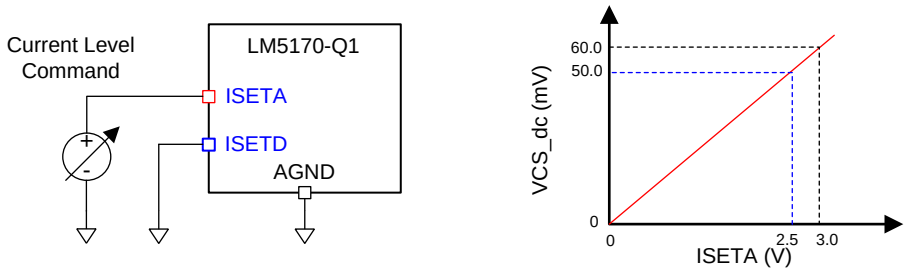


Figure 21. Pin Configurations for Current Setting Using an Analog Voltage Signal

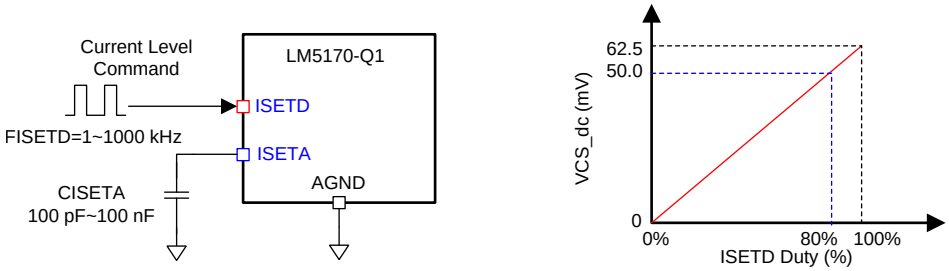


Figure 22. Pin Configurations for Current Setting Using a PWM Signal

The ISETA pin is directly connected to the noninverting input of the error amplifier. By ISETA programming, the channel DC current is determined by Equation 5:

$$V_{CS\ dc} = 0.02 \times V_{ISETA} \quad (5)$$

Or by Equation 6:

$$I\_channel\_dc = \frac{V_{CS\_dc\_}}{Rcs} \quad (6)$$

Or by Equation 7:

$$I\_channel\_dc = \frac{0.02 \times V_{ISETA}}{Rcs} \quad (7)$$

where

- Rcs is the channel current sensing resistor value.

When using ISETD, the produced V_{ISETA} by the internal decoder is equal to the product of the effective duty ratio of the ISETD PWM signal (D_{ISETD}) and the 3.125-V internal reference voltage. The channel current is determined by Equation 8:

$$IV_{ISETA} = 3.125V \times D_{ISETD} \quad (8)$$

Feature Description (continued)

Or by Equation 9:

$$V_{CS\ dc} = 0.0625V \times D_{ISETD} \quad (9)$$

Or by Equation 10:

$$I\_channel\_dc = \frac{0.0625V \times D_{ISETD}}{Rcs} \quad (10)$$

7.3.6 Channel Current Monitor (IOUT1, IOUT2)

The LM5170-Q1 monitors the real time inductor current in each channel at the IOUT1 and IOUT2 pins. The channel current is converted to a small current source scaled by the factors seen in Equation 11 and Equation 12:

$$IOUT1 = \frac{V_{CSI}}{200\Omega} + 25\mu A \quad (11)$$

$$IOUT2 = \frac{V_{CS2}}{200\Omega} + 25\mu A \quad (12)$$

where

- V_{CS1} and V_{CS2} are the real time current sense voltage of CH-1 and CH-2, respectively
- the 25 µA is a DC offset current superimposed on to the IOUT signals (refer to Figure 23).

The DC offset current is introduced to raise the no-load signal above the possible ground noise floor. Because the monitor signal is in the form of current, an accurate reading can be obtained across a termination resistor even if the resistor is located far from the LM5170-Q1 but close to the MCU, thus rejecting potential ground differences between the LM5170-Q1 and the MCU. Figure 24 shows a typical channel current monitor through a 9.09-KΩ termination resistor and a 10-nF to 100-nF ceramic capacitor in parallel. The RC network converts the current monitor signal into a DC voltage proportional to the channel DC current. For example, when the current sense voltage DC component is 50 mVdc, namely V_{CS_dc} = 50 mV, the termination RC network will produce a DC voltage of 2.5 V. Note that the maximum IOUT pin voltage will be internally clamped to about 4 V.

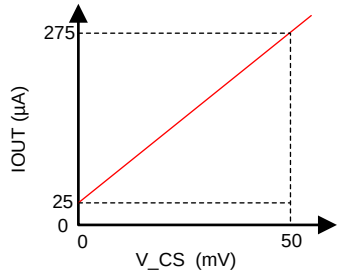


Figure 23. Channel Monitor Current Source vs Current Sense Voltage

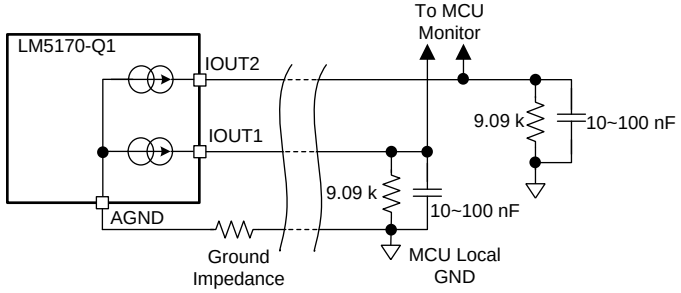


Figure 24. Channel Current Monitor

Feature Description (continued)

7.3.7 Cycle-by-Cycle Peak Current Limit (IPK)

The internal 25-µA current source and a single external resistor R_{IPK} establishes a voltage at the IPK pin to program the cycle-by-cycle current limit threshold. To set the inductor peak current limit value to I_{PK}, R_{IPK} should satisfy Equation 13:

$$R_{IPK} = \frac{Rcs \times I_{PK}}{1.1\mu A} \quad (13)$$

I_{PK} should be greater than the inductor peak current at full load, and lower than the inductor's rated saturation current I_{sat}.

Note that when the IPK pin voltage is greater than 4.5 V, either owing to a very large R_{IPK} value or the pin being open or some other reason, an internal monitor circuit will shut down the switching, preventing the LM5170-Q1 from operating with erroneous peak current limit threshold.

7.3.8 Error Amplifier

Each channel of the LM5170-Q1 has an independent gm error amplifier. The output of the error amplifier is connected to the COMP pin, allowing the loop compensation network to be applied between the COMP pins and AGND.

The LM5170-Q1 control loop is the inner current loop of the bidirectional converter system, of which the outer voltage loop can either be controlled by an MCU, a DSP, an FPGA, and so forth, or by an analog circuit. Because the LM5170-Q1 employs the averaged current mode control scheme, the inner loop is basically a first order system. As seen in Figure 25, a Type-II compensation network consisting of R_{COMP}, C_{COMP}, and C_{HF} is adequate to stabilize the LM5170-Q1 inner current loop. Refer to the *Application Information* section for details of the compensation network selection criteria.

7.3.9 Ramp Generator

Refer to Figure 25 for the circuit block diagram of the ramp generator, gm error amplifier, PWM comparator, and soft-start control circuit. The VINX pin serves as the supply pin for the ramp generator. Each ramp generator consists of an external RC circuit (R_{RAMP} and C_{RAMP}) and an internal pulldown switch controlled by the clock signal.

Feature Description (continued)

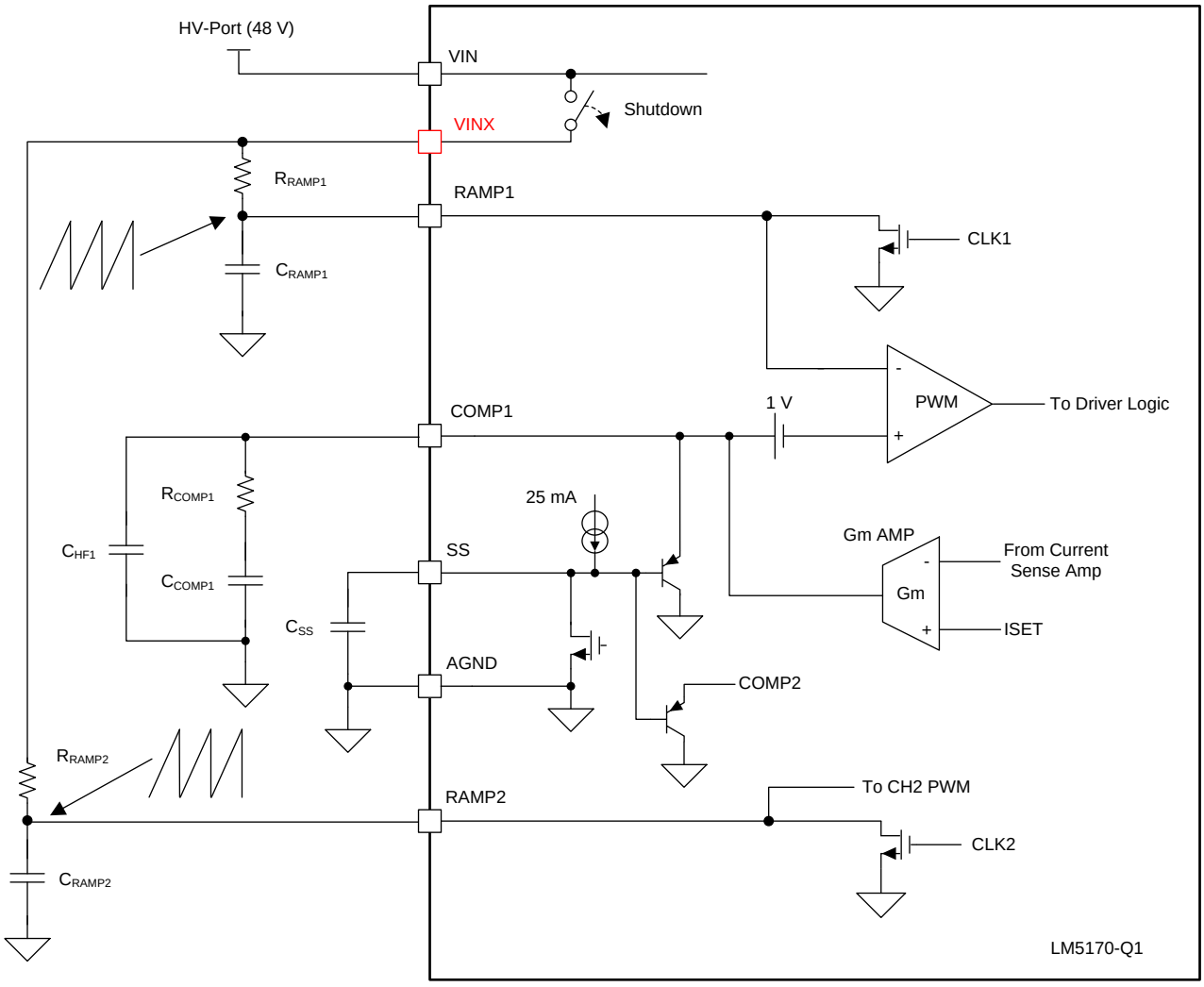


Figure 25. Error Amplifier, Ramp Generator, Soft Start, and PWM Comparator

When the LM5170-Q1 is enabled, $C_{RAMP1/2}$ is charged by the VINX pin through $R_{RAMP1/2}$ at the beginning of each switching cycle. The internal pulldown FET discharges $C_{RAMP1/2}$ at the end of the cycle within a 200-ns internal, then the pulldown is released, and $C_{RAMP1/2}$ repeats the charging and discharging cycles. In general the RAMP RC time constant is much greater than the period of a switching cycle. Therefore, the RAMP pin voltages are sawtooth signals with a slope proportional to the HV-Port voltage. In this way the RAMP signals convey the line voltage info. Being directly used by the PWM comparators to determine the instantaneous switching duty cycles, the RAMP signals fulfill the line voltage feedforward function and enable the LM5170-Q1 to have a fast response to line transients.

NOTE

TI recommends users to select appropriate R_{RAMP} and C_{RAMP} values by the following equation such that the RAMP pins reach the peak value of about 5 V each cycle when VIN is at 48 V.

$$R_{RAMP} = \frac{9.6}{F_{sw} \times C_{RAMP}} \quad (14)$$

Feature Description (continued)

For instance, if F_{sw} = 100 kHz, and C_{RAMP1} = C_{RAMP2} = 1 nF, a resistor of about 96 kΩ should be selected for R_{RAMP1} and R_{RAMP2}.

Because $C_{RAMP1/2}$ must be fully discharged every cycle through the 15-Ω channel resistor of the pulldown FET within the 150-ns minimum discharging interval, $C_{RAMP1/2}$ should be limited to be less than 2.5 nF nominal at room temperature.

There is also a valid RAMP signal detection circuit for each channel to prevent the channel from errantly running into the maximum duty cycle if RAMP goes away. It detects the peak voltage of the RAMP signal. If the peak voltage is less than 0.6 V in consecutive cycles, it is considered an invalid RAMP and the channel will stop switching by turning both HO and LO off until the RAMP signal recovers. This 0.6-V voltage threshold defines the minimum operating voltage of the HV-Port to be about 5.76 V.

7.3.10 Soft Start

The soft-start feature helps the converter to gradually reach the steady-state operating point, thus reducing start-up stresses and surge currents. With the LM5170-Q1, there are two ways to implement the soft start.

7.3.10.1 Soft-Start Control by the SS Pin

Place a ceramic capacitor C_{SS} between the SS pin and AGND to program the soft-start time. When the EN1 voltage is <1 V, an internal pulldown switch holds the SS pin at AGND. When the EN1 pin voltage is >2 V, the SS pulldown is released, and C_{SS} is charged up slowly by the internal 25-µA current source, as shown in Figure 25. The slow ramping SS voltage clamps the COMP1 and COMP2 pins through two separate clamp circuits. Once the SS voltage exceeds the 1-V offset voltage, the PWM duty cycle starts to increase gradually from zero.

When EN1 is pulled below 1 V, C_{SS} is discharged by the internal pulldown FET. Once this pulldown FET is turned on, it remains on until the SS voltage falls below 0.23 V, which is the threshold voltage indicating the completion of SS discharge.

Note that the EN2 pin does not affect the SS pin. When EN1 and EN2 are enabled together, the CH-2 output will follow CH-1 by going through the same soft-start process. If EN2 is enabled at a later time and CH-1 has already completed soft start, CH-2 will not be affected by the SS pin. This allows the CH-2 current to ramp up quickly to supply the increased load current. However, when SS is pulled low, both CH-1 and CH-2 are affected at the same time.

7.3.10.2 Soft Start by MCU Through the ISET Pin

The MCU can control the soft start by gradually ramping up the ISETA voltage, or the ISETD PWM duty ratio, whichever is applicable. When ISETA or ISETD is used to control the soft start, C_{SS} should be properly selected to a value such that it does not interfere with the ISETA/D soft start.

7.3.10.3 The SS Pin as the Restart Timer

The SS pin also fulfills the function of a restart timer in an OVP event or following a DIR command change:

(1) Restart Timer in OVP: When OVPA or OVPB catches an overvoltage event (refer to *Overvoltage Protection (OVPA, OVPB)*), C_{SS} is discharged immediately by the internal pulldown FET, and this FET remains ON as long as the overvoltage condition persists. When the overvoltage condition is removed and after the SS voltage is discharged to below 0.23 V, the SS pulldown is released, setting off a new soft-start cycle. The circuit may run in retry or hiccup mode if the overvoltage condition reappears. The retry frequency is determined by the SS capacitor as well as the nature of the overvoltage condition.

(2) Restart Timer: When DIR dynamically flips its state from 0 to 1, or 1 to 0 during operation, C_{SS} is first discharged to 0.23 V by the internal pulldown FET, then the pulldown is released to set off a new soft-start cycle to gradually build up the channel current in the new direction. In this way, the channel current overshoot is eliminated.

Feature Description (continued)

7.3.11 Gate Drive Outputs, Dead Time Programming and Adaptive Dead Time (HO1, HO2, LO1, LO2, DT)

Each channel of the LM5170-Q1 has a robust 5-A (peak) half bridge driver to drive external N-channel power MOSFETs. As shown in Figure 26, the low-side drive is directly powered by VCC, and the high-side driver by the bootstrap capacitor C_{BT}. During the on-time of the low-side driver, the SW pin is pulled down to PGND and C_{BT} is charged by VCC through the boot diode D_{BT}. TI recommends selecting a 0.1-µF or larger ceramic capacitor for C_{BT}, and an ultra-fast diode of 1 A and 100-V ratings for D_{BT}. TI also strongly recommends users to add a 2-Ω to 5-Ω resistor (R_{BT}) in series with D_{BT} to limit the surge charging current and improve the noise immunity of the high-side driver.

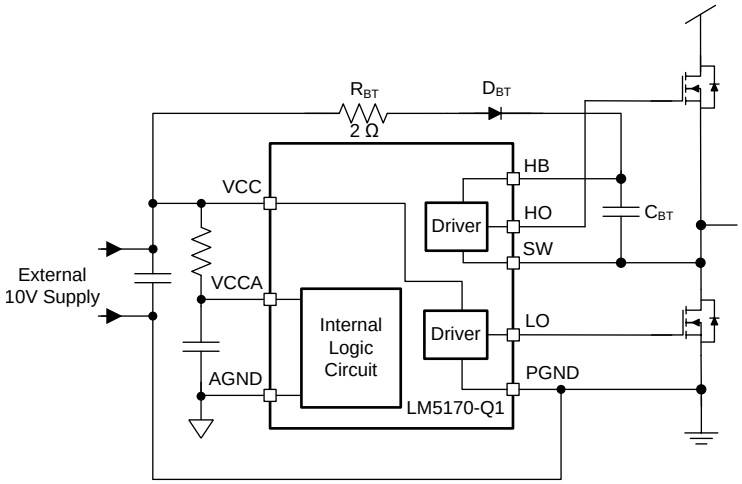


Figure 26. Bootstrap Circuit for High-Side Bias Supply

During start-up in buck mode, C_{BT} may not be charged initially; the LM5170-Q1 then holds off the high-side driver outputs (HO1 and HO2) and sends LO pulses of 200-ns width in consecutive cycles to pre-charge C_{BT}. When the boot voltage is greater than the 6.5-V boot UV threshold, the high-side drivers output PWM signals at the HO1 and HO2 pins for normal switching action.

During start-up in boost mode, C_{BT} is naturally charged by the normal turnon of the low side MOSFET, therefore there is no such 200-ns pre-charge pulse at the LO pins.

To prevent shoot-through between the high-side and low-side power MOSFETs on the same half bridge leg, two types of dead time schemes can be chosen with the DT pin: the programmable dead time or built-in adaptive dead time.

To program the dead time, place a resistor R_{DT} across the DT and AGND pins as shown in Figure 27.

The dead time t_{DT} as depicted in Figure 28 is determined by Equation 15:

$$t_{DT} = R_{DT} \times 4\frac{ns}{k\Omega} + 16ns \quad (15)$$

Note that this equation is valid for programming t_{DT} between 20 ns and 250 ns. When the power MOSFET is connected to the gate drive, its gate input capacitance C_{ISS} becomes a load of the gate drive output, and the HO and LO slew rate are reduced, leading to a reduced effective t_{DT} between the high- and low-side MOSFETs. The user should evaluate the effective t_{DT} to make sure it is adequate to prevent shoot-through between the high- and low-side MOSFETs.

When the DT programmability is not used, simply connect the DT pin to VCC as shown in Figure 29, to activate the built-in adaptive dead time. The adaptive dead time is implemented by real time monitoring of a driver's output (either HO or LO) by the other driver (LO or HO) of the same half bridge switch leg, as shown in Figure 29 and Figure 30. Only when a driver's output voltage falls below 1.25 V does the other driver starts turnon. The effectiveness of adaptive dead time will be greatly reduced if a series gate resistor is used, or if the PCB traces of the gate drive have excessive impedance due to poor layout design.

Feature Description (continued)

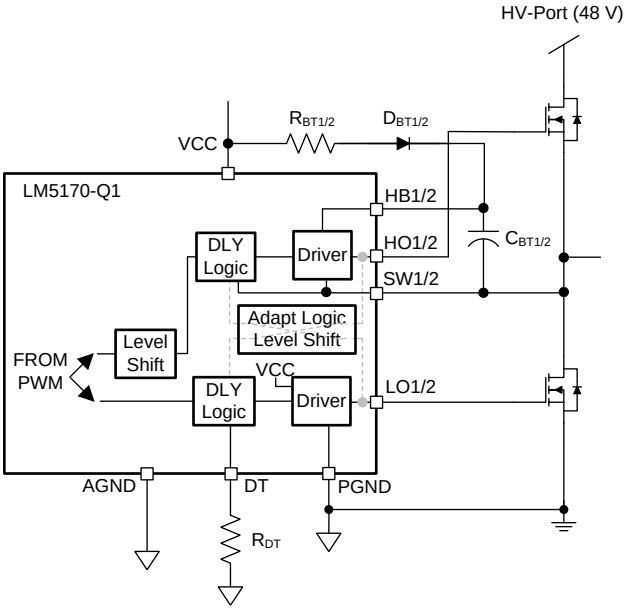


Figure 27. Dead Time Programming With DT Pin (Only One Channel is Shown)

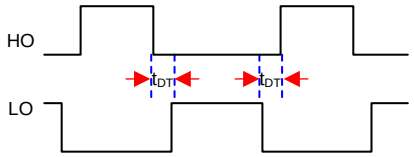


Figure 28. Gate Drive Dead Time (Only One Channel is Shown)

Feature Description (continued)

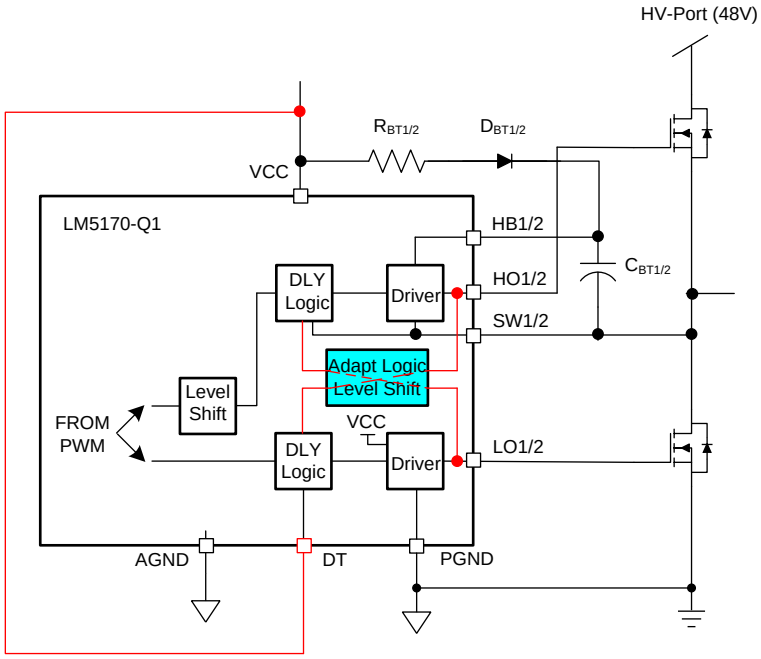


Figure 29. Dead Time Programming With DT Pin (Only One Channel is Shown)

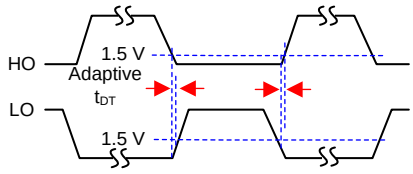


Figure 30. Adaptive Dead Time (Only One Channel is Shown)

7.3.12 PWM Comparator

Each channel of the LM5170-Q1 has a pulse width modulator (PWM) employing a high-speed comparator. It compares the RAMP pin signal and the COMP pin signal to produce the PWM duty cycle. Note that the COMP signal passes through a 1-V DC offset before it is applied to the PWM comparator, as shown in Figure 25. Owing to this DC offset, the duty cycle can reduce to zero when the COMP pin or SS pin is pulled lower than 1 V. The maximum duty cycle is limited by the 200-ns minimum off-time. Note that the programmed dead time may reduce the maximum duty cycle because it is additional to the minimum off-time. Therefore, the available maximum duty cycle, for both buck and boost mode operation, is determined by Equation 16.

$$D_{MAX} = 1 - (200ns + t_{DT}) \times F_{SW} \quad (16)$$

where

- t_{DT} is the dead time given by (15) or the adaptive dead time, whichever applicable.

This maximum duty cycle limits the minimum voltage step-down ratio in buck mode operation, and the maximum step-up ratio in boost mode operation.

Note that the maximum COMP voltage is clamped at about 1.5 V higher than the RAMP peak voltage. This prevents the COMP voltage from moving too far above the RAMP voltage which could cause longer recovery time during a large scale upward step load response.

Feature Description (continued)

7.3.13 Oscillator (OSC)

The LM5170-Q1 oscillator frequency is set by the external resistor R_{OSC} connected between the OSC pin and AGND, as shown in Figure 31. The OSC pin must never be left open whether or not an external clock is present. To set a desired oscillator frequency F_{OSC}, R_{OSC} is approximately determined by Equation 17:

$$R_{OSC} = \frac{40k\Omega \times 100\ kHz}{F_{OSC}} \quad (17)$$

R_{OSC} must be placed as close as possible to the OSC and AGND pins. Take the tolerance of the external resistor and the frequency tolerance indicated in the *Electrical Characteristics* table into account when determining the worst case operating frequency.

The LM5170-Q1 also includes a Phase-Locked Loop (PLL) circuit to manage multiphase interleaving phase angle as well as the synchronization to the external clock applied at the SYNCIN pin. When no external clock is present, the converter operates at the oscillator frequency given by Equation 17. If an external clock signal of a frequency within ± 20% of F_{SW} is applied (see the *Synchronization to an External Clock (SYNCIN, SYNCOUT)* section), the converter will switch at the frequency of the external clock F_{EX_CLK}, namely Equation 18:

$$F_{SW} = \begin{cases} F_{OSC} & \text{(in Standalone)} \\ F_{EX\_CLK} & \text{(in Synchronization)} \end{cases} \quad (18)$$

Two internal clock signals CLK1 and CLK2 are produced to control the interleaving operation of CH-1 and CH-2, respectively. The third clock signal is output at the SYNCOUT pin. All these three clock signals run at the same frequency of F_{SW}. The phase angles among these three clock signals are controlled by the state of the OPT pin. See the *Multiphase Configurations (SYNCOUT, OPT)* section for details.

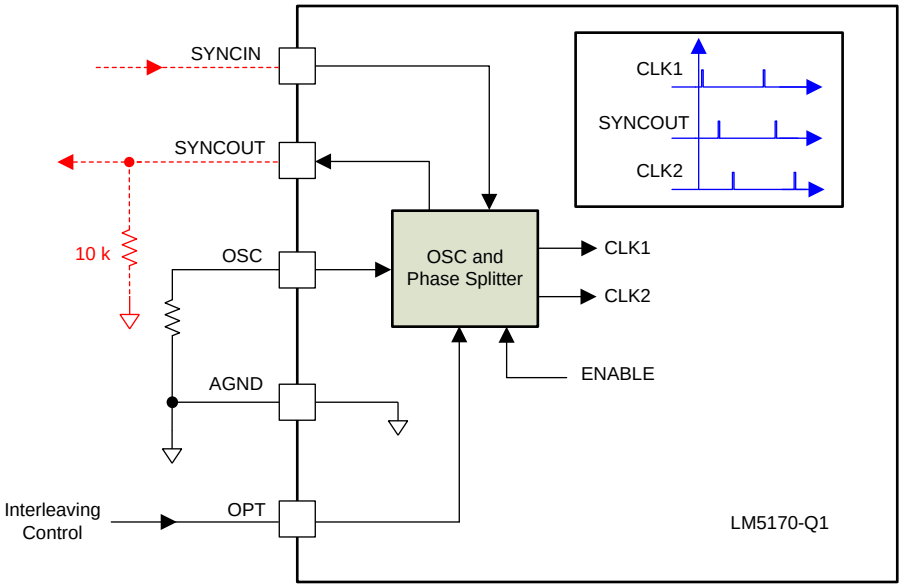


Figure 31. Oscillator and Interleaving Clock Programming

7.3.14 Synchronization to an External Clock (SYNCIN, SYNCOUT)

The LM5170-Q1 can synchronize to an external clock if F_{EX_CLK} is within ±20% of F_{OSC}. The SYNCIN clock pulse width should be in the range of 100 ns to 500 ns, with a high voltage level >2 V and low voltage level <1 V.

F_{EX_CLK} can be adjusted dynamically. However the LM5170-Q1 PLL takes about 500 µs to settle down to the newly asserted frequency. During the PLL transient, the instantaneous F_{SW} may temporarily drop by 25%. To avoid overstress during the transient, TI recommends the user to reduce the load current to less than 50% by lowering the ISETA voltage or ISETD duty, or to simply turn off the dual-channels by setting EN1=EN2=0 when making an the external clock change.

Feature Description (continued)

7.3.15 Diode Emulation

The LM5170-Q1 has a built-in diode emulation function. Each channel has a real time current zero crossing detector to monitor instantaneous V_{CS}. When V_{CS} is detected to cross zero, the LM5170-Q1 turns off the gate drive of the synchronous rectifier to prevent negative current. In this way, the negative current is prevented and the light load efficiency is improved. Figure 32 shows key waveforms of a typical operation transiting into the diode emulation mode.

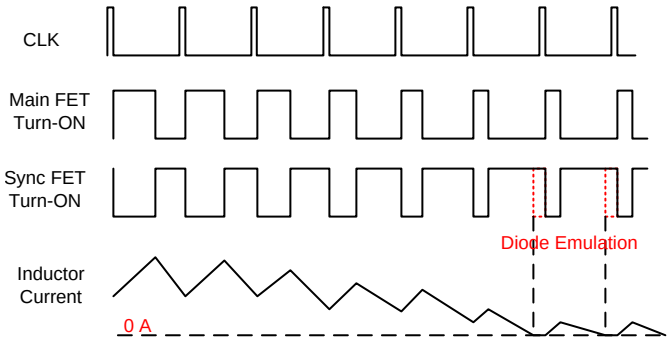


Figure 32. Diode Emulation Operation

To obtain optimal diode emulation performance, it requires the V_{CS} signal to be accurate in real time. Any signal distortion caused by parasitic inductances in the current sense resistor or sensing traces may lead to erroneous zero crossing detection and cause non-optimal diode emulation operation, and the sync FET may be turned off while the current is still high in the positive direction. See the *Application Information* section for coping with current sense parasitic inductances for optimal diode emulation operation.

7.3.16 Power MOSFET Failure Detection and Failure Protection (nFAULT, BRKG, BRKS)

The LM5170-Q1 includes a circuit to detect a MOSFET switch short-circuit failure during start-up. If a MOSFET drain and source are found shorted, the LM5170-Q1 pulls down the nFAULT pin to flag the fault, and the controller remains in an OFF state. This feature prevents the LM5170-Q1 from starting with a short-circuit-failed MOSFET, thereby preventing catastrophic failures.

The LM5170-Q1 also integrates a control circuit to control the circuit breaker. As shown in Figure 33, the circuit breaker consists of a pair of back-to-back MOSFETs. When the breaker is off, the current path between the HV-Port and LV-Port is cut-off so as to prevent possible catastrophic failures.

NOTE

The failure detection function must be deactivated if the circuit breaker is not present, or if the circuit breaker FETs are not controlled by the LM5170-Q1.

7.3.16.1 Failure Detection Selection at the SYNCOUT Pin

Depending on application preference, the failure detection function can be activated or deactivated by the SYNCOUT pin. During start-up, the LM5170-Q1 first detects the external resistor attached to the SYNCOUT pin. To enable the failure detection function, do not place resistor between the SYNCOUT and AGND pins (refer to Figure 33 or Figure 34).

To disable the failure detection function, place a 10-kΩ resistor between the SYNCOUT and AGND pins, as shown in Figure 35, and the LM5170-Q1 skips the 2- to 3-ms interval of MOSFET failure detection. Instead, it will activate the standby mode in about 300 µs after VCC is above 8.5 V and UVLO is greater than 2.5 V. If the circuit breaker is not present or not controlled by the LM5170-Q1, do not leave the BRKG and BRKS pins floating, but terminate the BRKG and BRKS pins with 20-kΩ resistors as shown in Figure 35.

Feature Description (continued)

7.3.16.2 Nominal Circuit Breaker Function

If the failure detection function is enabled, which also implies the circuit breaker being controlled by the LM5170-Q1, the LM5170-Q1 will perform a MOSFET failure detection during start-up. The detection starts after the UVLO is pulled higher than 2.5 V and VCC above 8.5 V. The detection operation lasts for 2 to 3 ms. During the detection, the LM5170-Q1 checks the high-side and low-side MOSFETs of both channels as well as the circuit breaker MOSFETs to see if any of them has drain-to-source shorted. If no failure is detected, a 330-µA current source at the BRKG pin is turned on to charge up the breaker MOSFET gates. When the BRKG to BRKS voltage rises above 8.5 V, the LM5170-Q1 enters standby mode, waiting for the EN1 and EN2 commands to operate in power delivery mode. The voltage across BRKG and BRKS is internally clamped to 12 V, preventing overvoltage stress on the breaker MOSFET gates.

If a failure of any MOSFET is detected, the LM5170-Q1 immediately pulls the nFAULT pin low, and keeps the LM5170-Q1 in a latched shutdown mode, thereby preventing catastrophic failure.

The nFAULT pin can also be externally pulled low during normal operation and the LM5170-Q1 immediately turns off the circuit breaker and stays in a latched shutdown. There is a 2-µs glitch filter at the nFAULT pin to prevent errant shutdown by possible noises at the nFAULT pin.

To release the nFAULT shutdown latch, it requires the UVLO pin to be externally forced below 1.25 V, or VCC is below 8 V.

Figure 33 and Figure 34 show two ways to use the circuit breaker function. A TVS is recommended to prevent surge voltage when the circuit breaker is turned off during operation.

The BRKG 330-µA current source is powered by the VIN pin, or the HV-Port. Therefore, the differential voltage between the HV-Port and LV-Port should be greater than 10 V to ensure that BRKG to BRKS voltage can establish >8.5 V and allow the LM5170-Q1 to enter power delivery mode. The BRKG to BRKS voltage is internally clamped to 12 V if the differential voltage of the two ports is greater.

The load dump transient at the LV-Port may raise the rail voltage and reduce the differential voltage of the two ports to below 10 V. To maintain the circuit breaker to be closed during the transient, TI recommends adding a 1-nF to 10-nF capacitor across BRKG and BRKS to hold the gate voltage during the transient.

Note that the BRKG 330-µA current source will always be turned on once the LM5170 starts up. If the failure detection mode is deactivated, the LM5170-Q1 will also skip checking the BRKG to BRKS votlage condition. Therefore, the circuit breaker can still be controlled by the LM5170-Q1 even if the failure detection is deactivated. If the steady-state differential voltage between the HV-Port and LV-Port is less than 10 V during power up, TI does not recommend the user to activate the failure detection function. Also, if the differential voltage is less than 8 V, TI recommends not to use the LM5170-Q1's circuit breaker function at all.

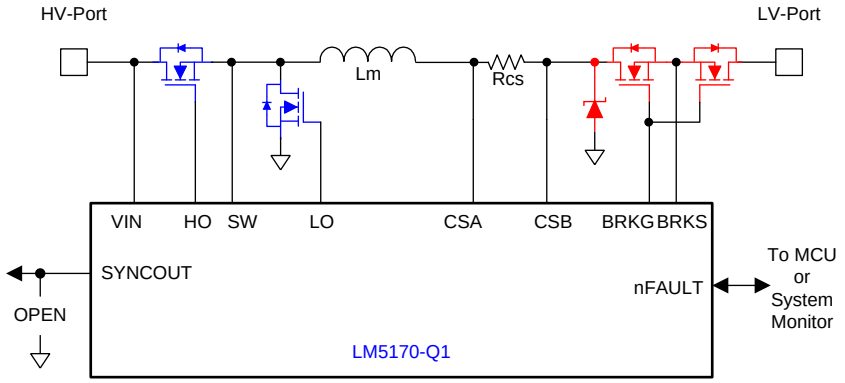


Figure 33. Controlling Dual-Channel Circuit Breaker for MOSFET Failure Protection

Feature Description (continued)

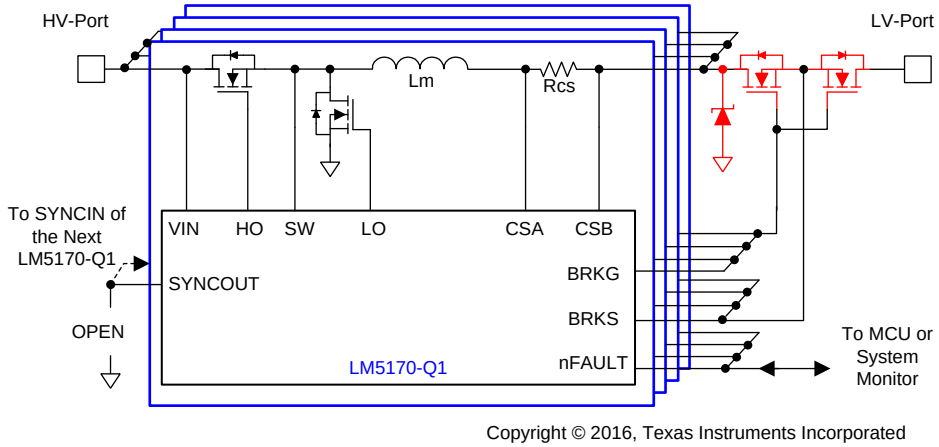


Figure 34. Controlling System Level Circuit Breaker for MOSFET Failure Protection

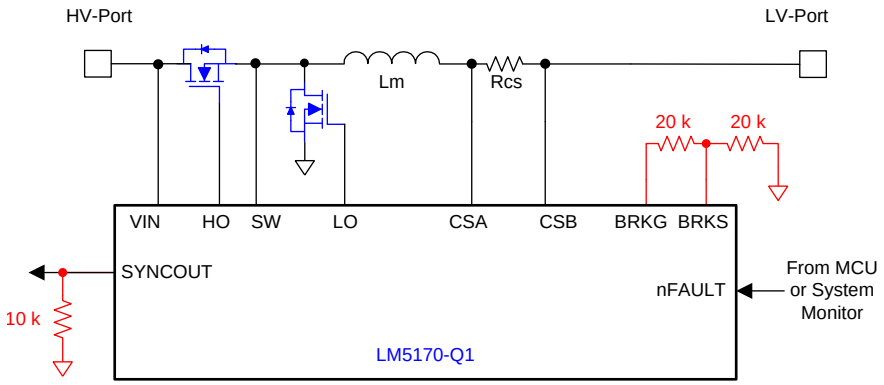


Figure 35. Circuit Breaker Function Disabled

7.3.17 Overvoltage Protection (OVPA, OVPB)

As shown in Figure 36 and Figure 37, the LM5170-Q1 includes the overvoltage protection function for both HV-Port and LV-Port. Use the OVPA pin for the HV-Port protection, and the OVPB pin for the LV-Port protection. It should be pointed out that the OVPB protection function is disabled during the boost operation mode, while the OVPA function is always enabled in both buck or boost operation modes.

7.3.17.1 HV-V- Port OVP (OVPA)

A dedicated comparator monitors the HV-Port voltage through a resistor divider. The divider consists of an internal 3-MegΩ pullup resistor between the VINX and OVPA pins, and an external pulldown resistor between the OVPA pin and AGND. When the OVPA pin voltage exceeds the 1.185-V threshold, both HOs and LOs are turned off. At the same time C_{SS} is discharged, preparing for the restart through soft start when the OV alarm is removed. See the *Soft Start* section for details.

7.3.17.2 LV-Port OVP (OVPB)

A dedicated comparator monitors the LV-Port voltage through a resistor divider. The divider consists of the internal 1-MegΩ pullup resistor between the CSB1 and OVPB pins, and an external pulldown resistor between the OVPB pin and AGND. When the OVPB pin voltage exceeds the 1.185-V threshold, both HOs and LOs are turned off. At the same time the SS capacitor is discharged, preparing to restart through soft start when the OV alarm is removed. See the *Soft Start* section for details.

Feature Description (continued)

Note the hysteresis voltage of both OVPA and OVPB comparators is about 100 mV. There are 5-µs built-in glitch filters for both OVPA and OVPB comparators. In addition, a small capacitor can be considered to place from the OVP pins to AGND. All these will help prevent errant operation by possible noises on the OVPA and OVPB signals.

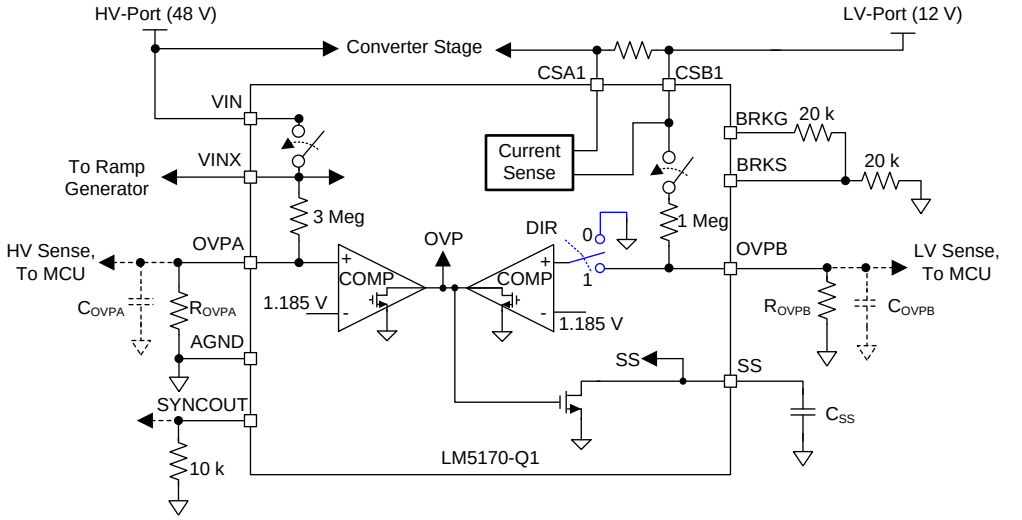


Figure 36. Overvoltage Protection: When Circuit Breaker Function is Not Used

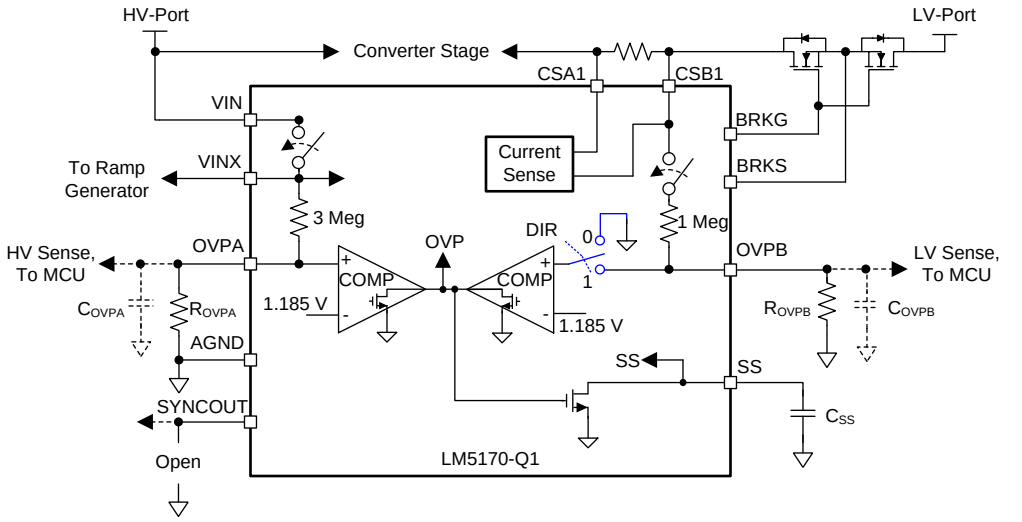


Figure 37. Overvoltage Protection: When Circuit Breaker Function is Used

7.4 Device Functional Modes

7.4.1 Multiphase Configurations (SYNCOUT, OPT)

There are various options to make multiphase configurations.

7.4.1.1 Multiphase in Star Configuration

Each LM5170 synchronizes to an external clock, and the clock signals should have appropriate phase delays among them for proper multiphase interleaving operation. The interleave angle between the two phases of each LM5170-Q1 can be programmed to 180° or 240° by the OPT pin.Table 1 summarizes the settings of the external clocks and the OPT pin state for multiphase configurations.

Table 1. Multiphase Configurations With Individual External Clock

NUMBER OF PHASES	PHASE SHIFT BETWEEN EXTERNAL CLOCKS FOR MULTIPHASE INTERLEAVING	OPT LOGIC STATE(1)	CH-2 PHASE LAGGING VS CH-1	NUMBER OF LM5170-Q1 CONTROLLERS NEEDED	NUMBER OF EXTERNAL CLOCKS NEEDED
2	180°	1	180°	1	1 or 0
3	120°	0	240°	2	2
4	90°	1	180°	2	2
6	60° or 120°	1	180°	3	3
8	45°	1	180°	4	4
2xN	(180°/N)	1	180°	N	N

(1) OPT State = 0 when the pin connects to AGND, and 1 when the pin voltage is >2.5 V.

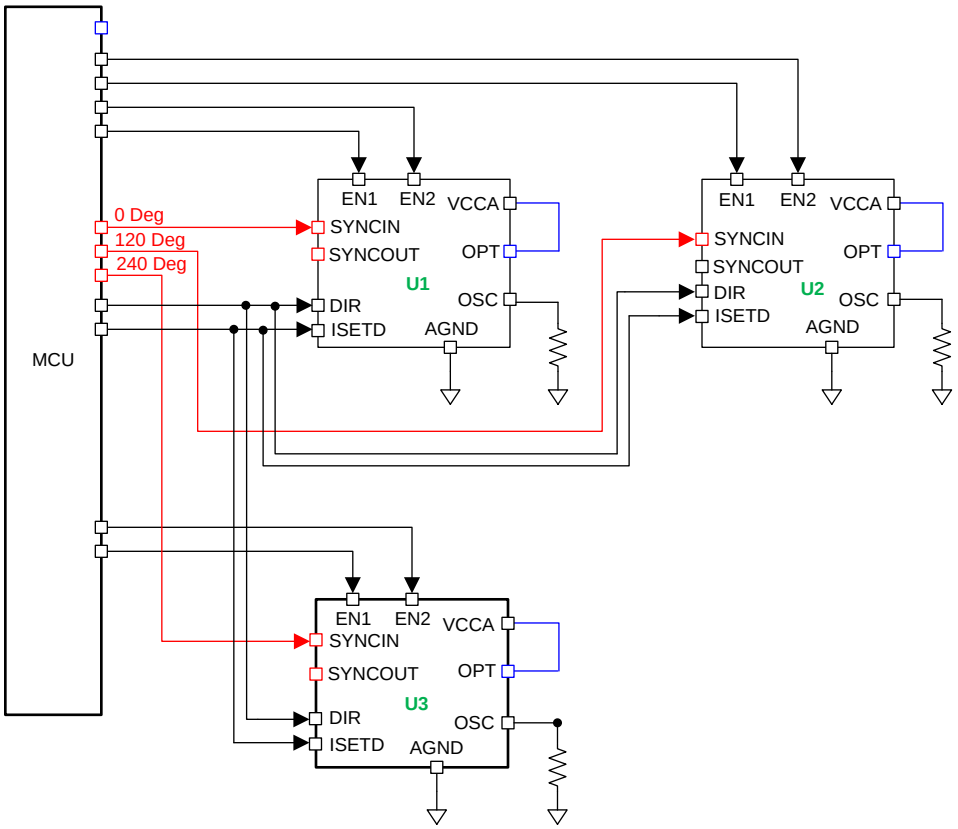


Figure 38. Example of Six Phase Star Configuration

7.4.1.2 Configuration of 2, 3, or 4 Phases in Master-slave Daisy Chain Configurations

This can be used to realize 1, 2, 3, or 4 phases without the need of external clock. Table 2 summarizes the OPT settings for the daisy chain multiphase configurations. Figure 39 shows the daisy chain connections for multiphase configurations.

Table 2. Multiphase Configurations With Built-In Daisy Chain Master-Slave Configuration

NUMBER OF PHASES	OPT LOGIC STATE(1)	CH-2 PHASE LAGGING VS CH-1	SYNCOUT PHASE LAGGING VS CH-1	NUMBER OF LM5170-Q1 CONTROLLERS NEEDED	NUMBER OF EXTERNAL CLOCKS NEEDED
2	1	180°	90°	1	0 or 1
3	0	240°	120°	2	0 or 1
4	1	180°	90°	2	0 or 1

(1) OPT State = 0 when the pin connects to AGND, and 1 when the pin voltage is >2.5 V.

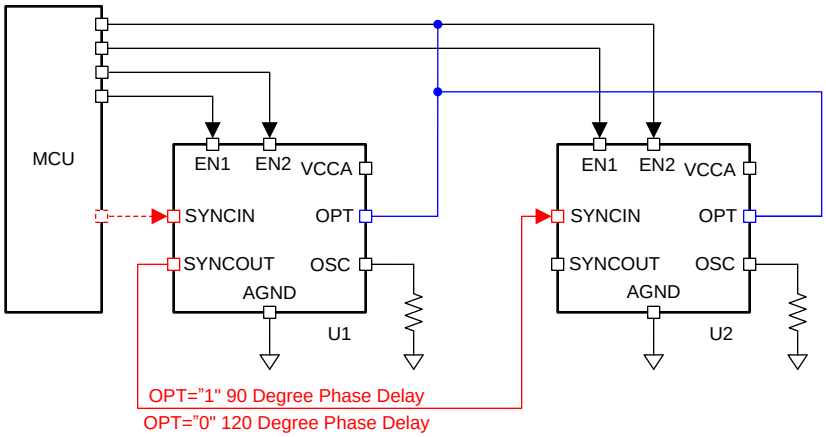


Figure 39. Three or Four Phases Interchangeable Configuration

7.4.1.3 Configuration of 6 or 8 Phases in Master-Slave Daisy Chain Configurations

To configure 6 or 8 phases, it requires two daisy chains shown in Figure 40 through Figure 43. Note that two phase-shifted external clock signals are required for proper interleaving operation. When external clock signals are not available, the 6-phase can be configured in 120° interleaving, and 8-phase in 90° interleaving by daisy chain (refer to Figure 41 and Figure 43), in which two phases of the system are synchronized in phase.

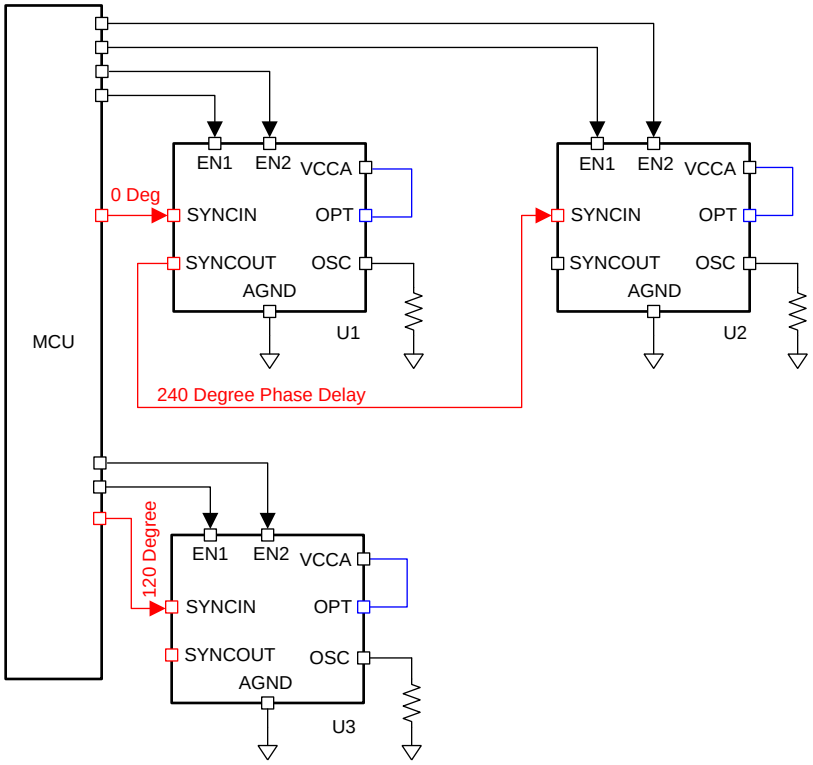


Figure 40. Six Phases 60° Interleaving Configuration

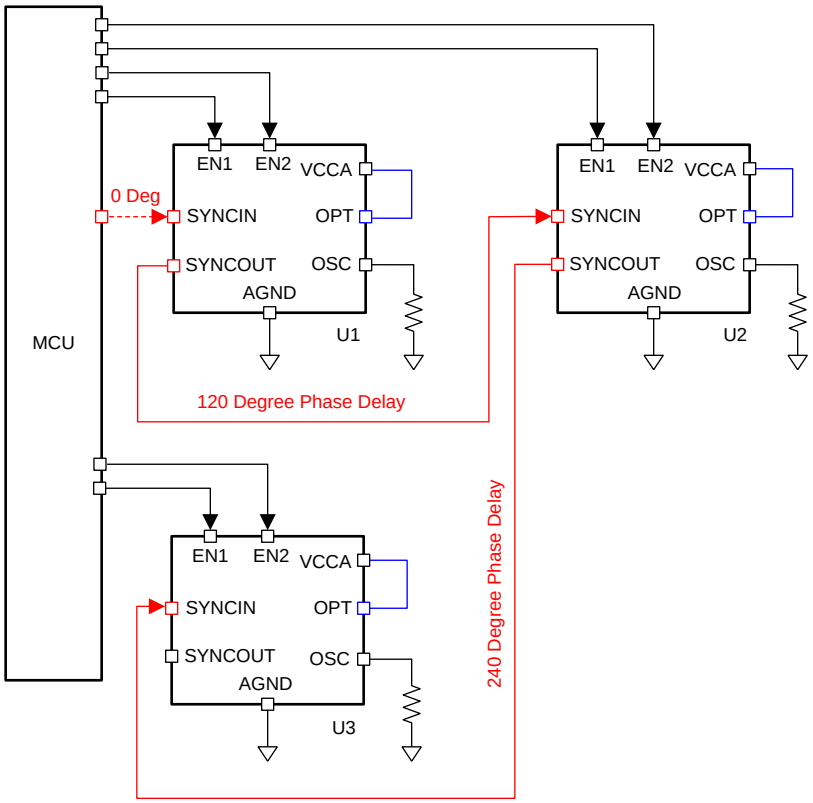


Figure 41. Six Phases 120° Interleaving Configuration

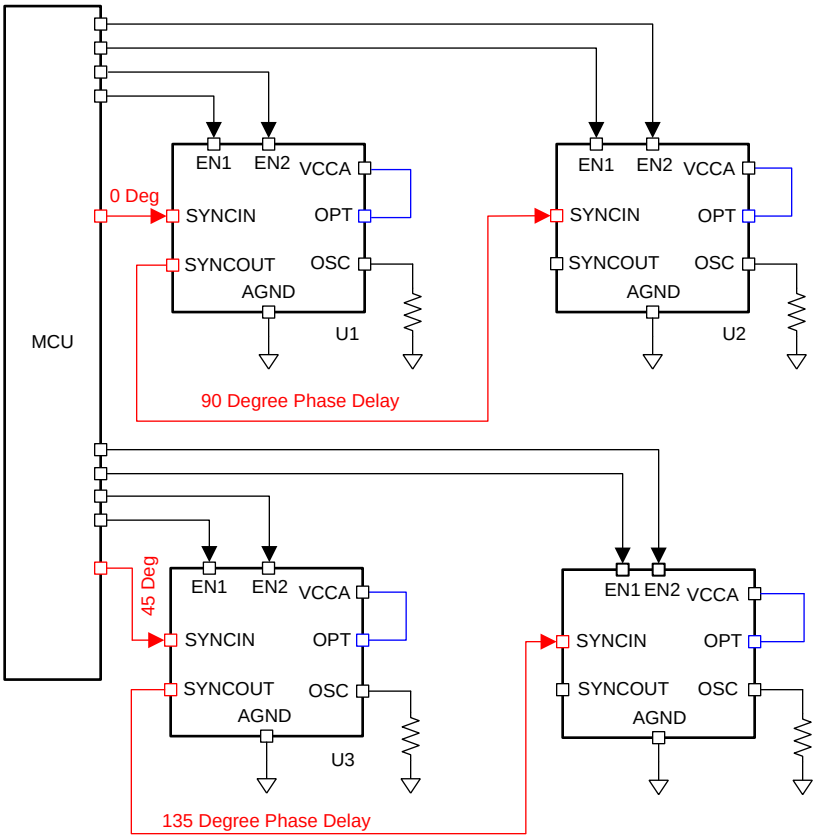


Figure 42. Eight Phases 45° Interleaving Configuration

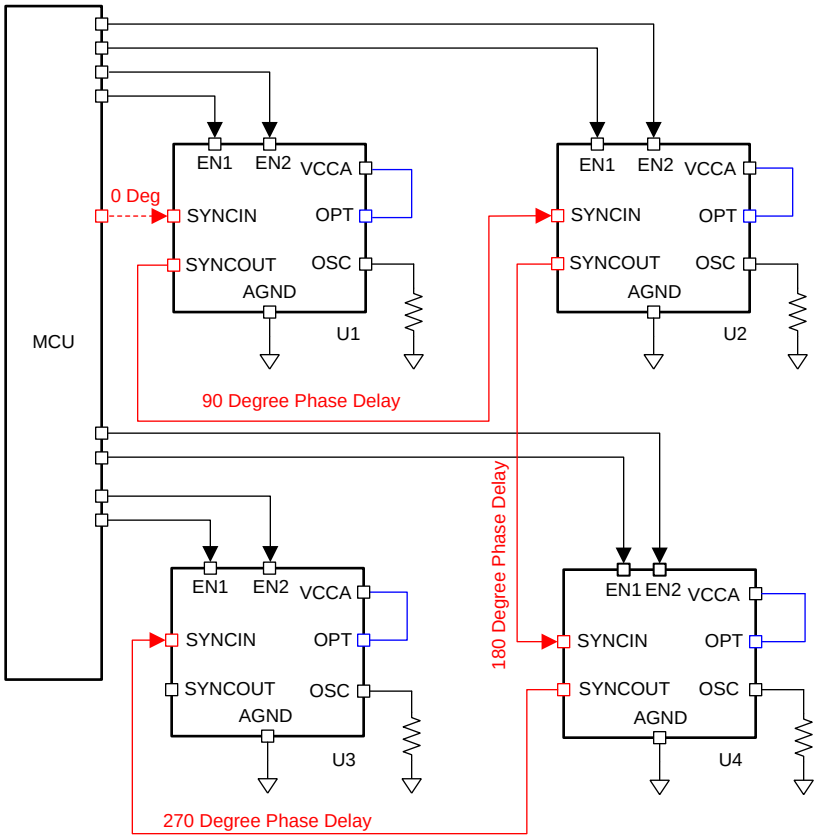


Figure 43. Eight Phases 90° Interleaving Configuration

7.4.2 Multiphase Total Current Monitoring

To minimize the number to signal lines, multichannel monitors can be combined into a total current monitor. Figure 44 shows an example of total current monitor of a three phase system in which the unused fourth phase monitor (U2-IOUT2) is grounded.

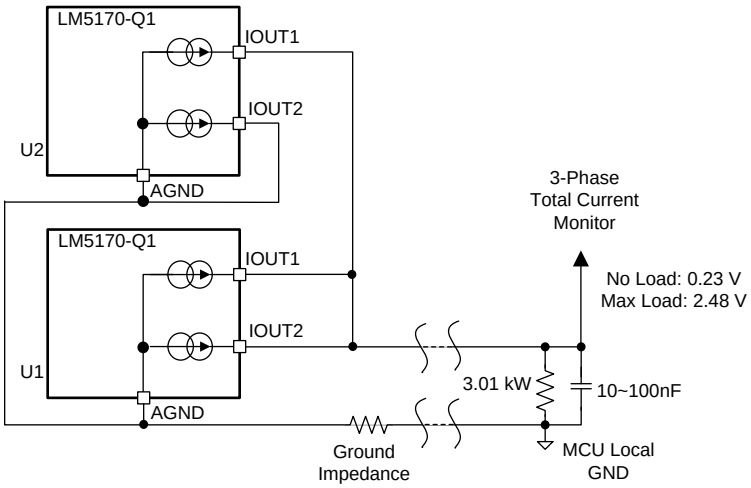
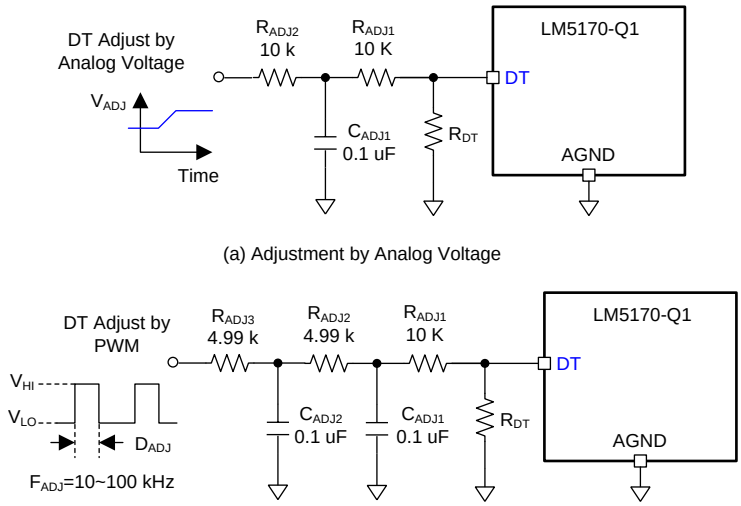


Figure 44. 3-Phase Total Current Monitor

7.5 Programming

7.5.1 Dynamic Dead Time Adjustment

In addition to a fixed dead time programming by R_{DT}, the dead time can be dynamically adjusted either by applying an analog voltage or a PWM signal as shown in Figure 45. Varying the analog voltage or the duty ratio of the PWM signal will adjust the DT programming. For analog adjustment, a single stage RC filter is recommended to filter out any possible noise. For PWM adjustment, a two-stage RC filter is recommended to minimize the ripple voltage resulted on the DT pin.



(a) Adjustment by Analog Voltage

(b) Dynamic Dead Time Adjustment

Figure 45. Dynamic Dead Time Adjustment

When an analog voltage is applied, the resulted dead time is determined by Equation 19:

$$t_{DT}(V_{ADJ}) = \left(\frac{1}{R_{DT}} + \frac{1}{R_{ADJ1} + R_{AJD2}} - \frac{0.8 \times V_{ADJ}}{R_{ADJ1} + R_{ADJ2}} \right)^{-1} \times 4 \frac{ns}{k\Omega} + 16 \text{ ns} \quad (19)$$

where

- V_{ADJ} is the analog voltage used to adjust the dead time

When a PWM signal is applied, the resulted dead time is determined by Equation 20:

$$t_{DT}(D_{ADJ}) = \left(\frac{1}{R_{DT}} + \frac{1}{R_{ADJ1} + R_{AJD2} + R_{AJD3}} - \frac{0.8 \times \left[(V_{HI} - V_{LO}) \times D_{ADJ} + V_{LO} \right]}{R_{ADJ1} + R_{ADJ2} + R_{ADJ3}} \right)^{-1} \times 4 \frac{ns}{k\Omega} + 16 \text{ ns} \quad (20)$$

where

- V_{HI} and V_{LO} are the high and low voltage levels of the PWM signal, respectively,
- D_{ADJ} is the duty factor of the PWM signal.

7.5.2 Optional UVLO Programming

The UVLO pin is the LM5170-Q1's master enable pin. It can be directly controlled by an external control unit like an MCU.

Programming (continued)

Nevertheless, the UVLO pin can also fulfill the undervoltage lockout function of a particular power rail. The rail can be either the HV-Port, or the LV-Port, or VCC. Use a resistor divider to set the UVLO threshold, as shown in Figure 46. The divider should satisfy Equation 21:

$$\frac{R_{UVLO2}}{R_{UVLO1}+R_{UVLO2}} \times V_{UVLO} = 2.5V \tag{21}$$

The UVLO hysteresis is accomplished with an internal 25-µA current source. When UVLO > 2.5 V, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 2.5-V threshold the current source is turned off, causing the voltage at the UVLO pin to fall. The UVLO hysteresis is determined by Equation 22:

$$V_{HYS} = R_{UVLO1} \times 25\mu A \tag{22}$$

An optional ceramic capacitor C_{UVLO} can be placed in parallel with R_{UVLO2} to improve the noise immunity. C_{UVLO} is usually between 1 nF to 10 nF. A large C_{UVLO} may cause excessive delay to respond to a real UVLO event.

If Equation 22 does not provide adequate hysteresis voltage, the user can add R_{UVLO3} as shown in Figure 47. The hysteresis voltage is thus given by Equation 23:

$$V_{HYS} = \left[R_{UVLO1} + R_{UVLO3} \times \left(1 + \frac{R_{UVLO1}}{R_{UVLO2}} \right) \right] \times 25\mu A \tag{23}$$

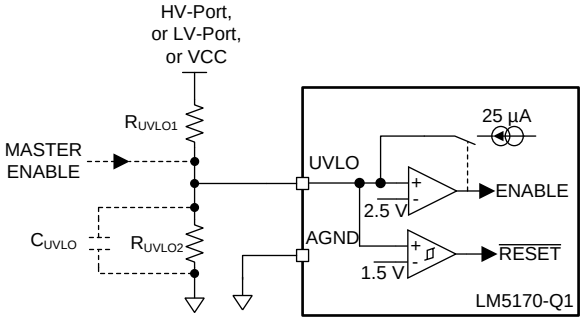


Figure 46. UVLO Programming

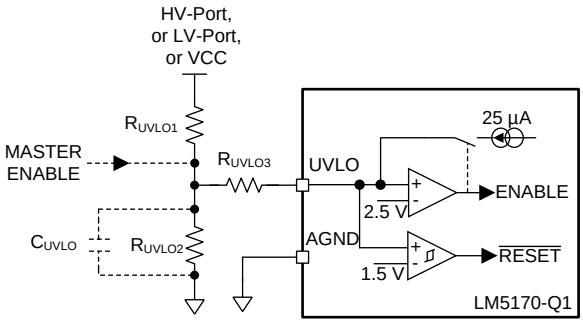


Figure 47. UVLO With Additional Hysteresis Programming

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5170-Q1 is suitable for the bidirectional DC-DC converters for the automotive 48-V and 12-V dual battery systems, and battery backup systems. It can also create stackable, high power, unidirectional buck or boost converters with balanced power sharing among multiphases.

8.1.1 Typical Key Waveforms

The following describes the typical power up sequence of the LM5170-Q1 bidirectional converter in a 48-V to 12-V dual battery system.

Application Information (continued)

8.1.1.1 Typical Power-Up Sequence

Figure 48 shows key waveforms of power-up sequence.

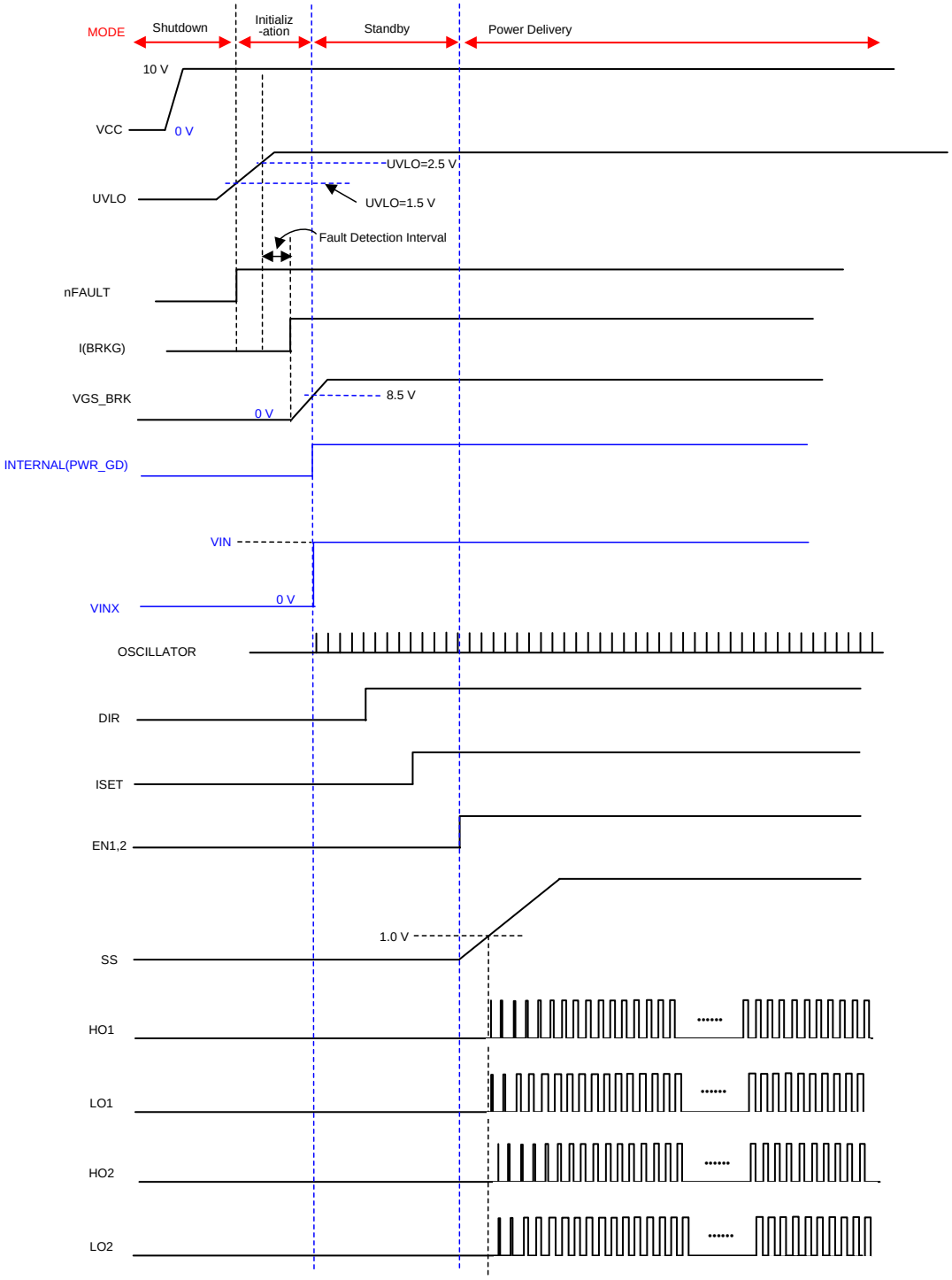


Figure 48. Typical Turnon Sequence Key Waveforms

Application Information (continued)

8.1.1.2 One to Eight Phase Programming

Figure 49 and Table 3 show a typical logic control signals and external clock requirements to run an eight phase system

Table 3. Multiphase Programming

	1Φ	2Φ	3Φ	4Φ	6Φ	8Φ
A7	0	0	0	0	0	1
A6	0	0	0	0	0	1
A5	0	0	0	0	1	1
A4	0	0	0	0	1	1
A3	0	0	0	1	1	1
A2	0	0	1	1	1	1
A1	0	1	1	1	1	1
A0	1	1	1	1	1	1
OPT (B0)	1	1	0	1	1	1
SYNC (C0)	—	—	—	—	0°	0°
(C1)	—	—	—	—	60°	45°

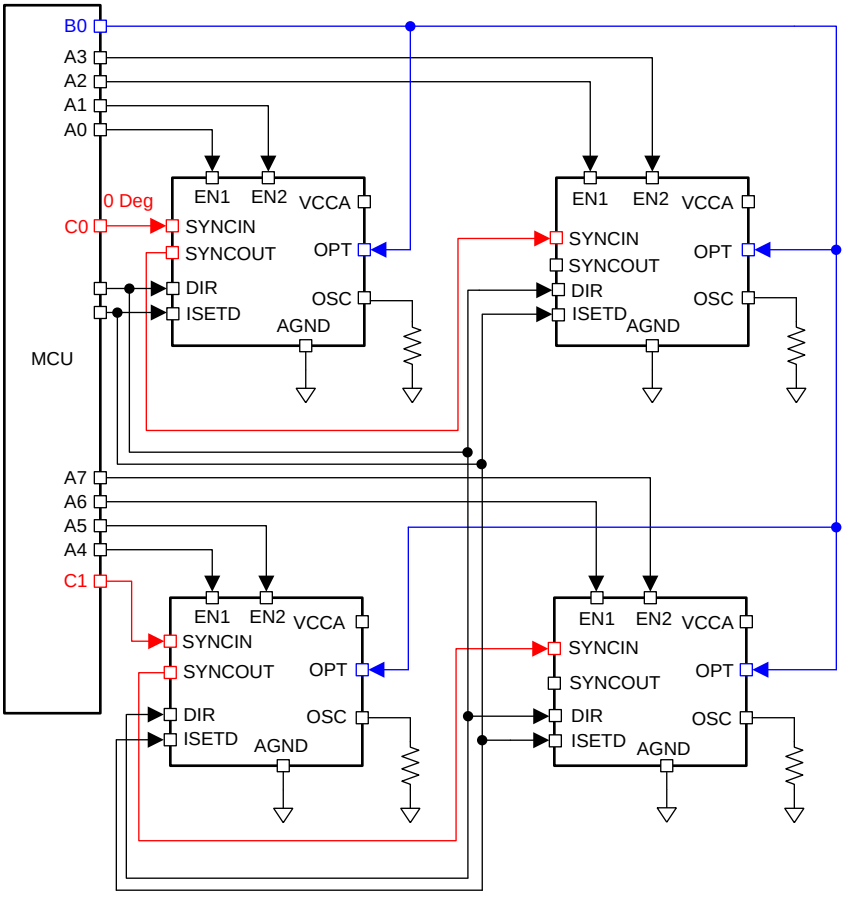


Figure 49. Eight Phase Configuration

8.1.2 Inner Current Loop Small Signal Models

The following describes the inner current loop that is controlled by the LM5170-Q1. The outer voltage loop should be managed by the MCU, or by an external analog circuit. The interface signals between the inner current loop and outer voltage loop are basically the DIR and ISET signals, of which the DIR signal controls the current direction, and the ISET signal carries the outer voltage loop's error information.

8.1.2.1 Small Signal Model

Figure 50 shows the current loop block diagram. The power plant transfer function from the error voltage (Vea) to the channel inductor current (i_{Lm}) is determined by the following, regardless the current flow direction.

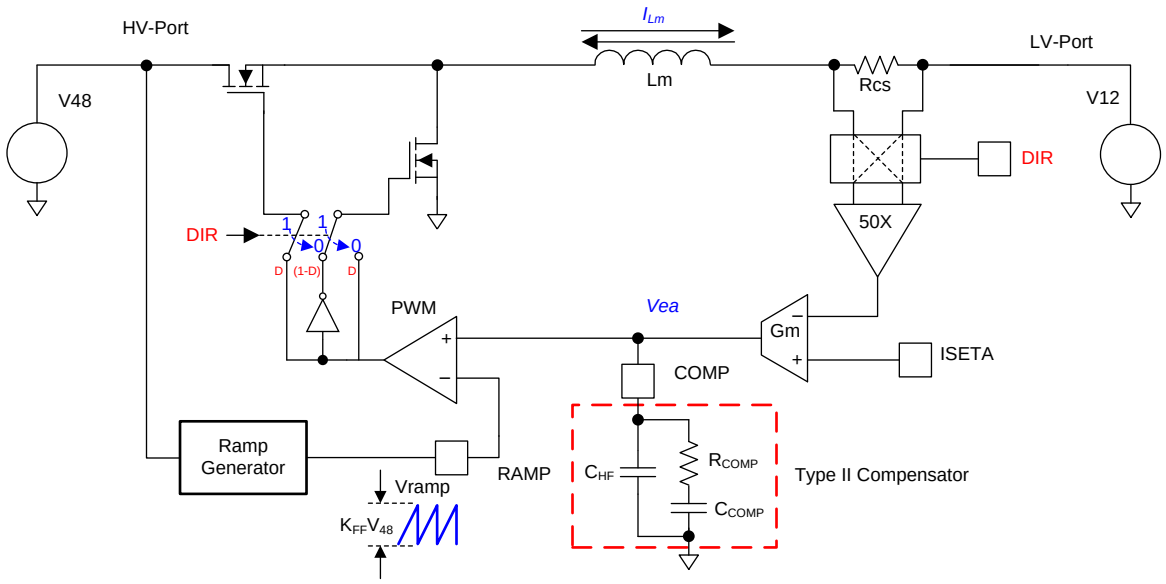


Figure 50. Control Loop Block Diagram

$$H(s) = \frac{\hat{i}_{Lm}}{\hat{V}_{ea}} = \frac{1}{K_{FF} \times (R_{CS} + R_S)} \times \frac{1}{s \times \frac{L_m}{R_{CS} + R_S} + 1}$$

where

- L_m is the power inductor,
- R_{CS} the current sense resistor,
- R_S the equivalent total resistance along the current path excluding R_{CS},
- K_{FF} the ramp generator coefficient. When the RAMP signal is generated per Equation 14 , K_{FF} = 0.104. (24)

8.1.2.2 Inner Current Loop Compensation

Equation 24 indicates that the power plant is basically a first-order system. A Type-II compensator as shown in Figure 50 is adequate to stabilize the loop for both buck and boost mode operations.

Assuming the output impedance of the gm amplifier is R_{GM}, the gain from the inductor to the output of gm amplifier is determined by Equation 25:

$$G(s) = \frac{\hat{V}_{ea}}{\hat{i}_{Lm}} = 50 \times R_{CS} \times Gm \times \left[R_{GM} \text{ II } Z_{COMP}(s)\right]$$

where

- the coefficient 50 is the current sense amplifier gain;
- Gm is the transconductance of the gm error amplifier, which is 1 mA/V;
- $Z_{COMP}(s)$ is the equivalent impedance of the compensation network seen at the COMP pin, namely Equation 26 (25)

$$Z_{COMP}(s) = \frac{1}{C_{HF} + C_{COMP}} \times \frac{1 + s \times R_{COMP} \times C_{COMP}}{s \times \left(1 + s \times R_{COMP} \times \frac{C_{HF} \times C_{COMP}}{C_{HF} + C_{COMP}}\right)} \quad (26)$$

Usually C_{HF} is << C_{COMP}. Thus Equation 26 can be simplified to Equation 27:

$$Z_{COMP}(s) = \frac{1}{C_{COMP}} \times \frac{1 + s \times R_{COMP} \times C_{COMP}}{s \times (1 + s \times R_{COMP} \times C_{HF})} \quad (27)$$

Because R_{GM} is > 5 MegΩ, and the frequency range for loop compensation is usually above a few kHz, the effects of RGM on the loop gain in the interested frequency range becomes negligible. Therefore, substituting Equation 28 into Equation 25, and neglecting R_{GM}, one can get the following:

$$G(s) = \frac{\hat{V}_{ea}}{\hat{i}_{Lm}} = \frac{50 \times R_{CS} \times Gm}{C_{COMP}} \times \frac{1 + s \times R_{COMP} \times C_{COMP}}{s \times (1 + s \times R_{COMP} \times C_{HF})} \quad (28)$$

The total open-loop gain of the inner current loop is the product of H(s) and G(s):

$$G_{total}(s) = H(s) \times G(s) \quad (29)$$

Or:

$$G_{total}(s) = \frac{1}{K_{FF} \times C_{COMP}} \times \frac{50 \times R_{CS} \times Gm}{s \times \frac{L_m}{R_{CS} + R_S} + 1} \times \frac{1 + s + R_{COMP} \times C_{COMP}}{s \times (1 + s \times R_{COMP} \times C_{HF})} \quad (30)$$

The poles and zeros of the total loop transfer function are determined by:

$$f_{p1} = 0 \quad (31)$$

$$f_{p2} = \frac{(R_{CS} + R_S)}{2\pi \times L_m} \quad (32)$$

$$f_{p3} = \frac{1}{2\pi \times R_{COMP} \times C_{HF}} \quad (33)$$

$$f_z = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \quad (34)$$

To tailor the total inner current loop gain to cross over at f_{CO}, select the components of the compensation network according to the following guidelines, then fine tune the network for optimal loop performance.

1. The zero f_z is placed at the power stage pole f_{p2},
2. The pole f_{p3} is placed at about two decade higher then f_{CO},
3. The total open-loop gain is set to unity at f_{CO}, namely,

$$\left|H(2i \times \pi \times f_{CO}) \times G(2i \times \pi \times f_{CO})\right| = 1 \quad (35)$$

Therefore, the compensation components can be derived from the above equations, as shown in Equation 36.

$$\begin{cases} R_{COMP} = \frac{1}{50 \times R_{CS} \times Gm \times \left|H(2i \times \pi \times f_{CO}\right|} = \frac{K_{FF}}{50 \times R_{CS} \times Gm} \times \left|2i \times \pi \times f_{CO} \times L_m + (R_{CS} + R_S)\right| \\ C_{COMP} = \frac{L_m}{(R_{CS} + R_S) \times R_{COMP}} \\ C_{HF} = \frac{C_{COMP}}{100} \end{cases} \quad (36)$$

8.1.3 Compensating for the Non-Ideal Current Sense Resistor

TI strongly recommends employing a non-inductive resistor for R_{CS}. Even a few nH of inductance will cause the current sense signal to be remarkably distorted, as shown in Figure 51. The adversary consequences include reduced peak current limit than actually programmed and false current zero-crossing detection well above 0 A. The former may reduce the available maximum current to be delivered; and the latter will terminate the sync FET gate early and the body diode will be used to conduct the remaining current, thereby reducing the efficiency as well as the accuracies of the channel DC current regulation and IOUT monitors under light load.

When the current sense resistor has some parasitic inductance, it is necessary to compensate the effects of inductance with an RC circuit, as shown in Figure 52. The user should place a 1-Ω resistor in each of the current sense signal path, and the selection of C_{CS} should satisfy Equation 37, assuming the inductance of the current sense resistor is L_{CS}:

$$C_{CS} = \frac{L_{CS}}{2\Omega \times R_{CS}} \tag{37}$$

For instance, if R_{CS} =1 mΩ, L_{CS} = 1 nH, the required compensation capacitor C_{CS} should be about 0.5 µF.

Note that selecting C_{CS} greater than the value given by Equation 37 would over compensate the inductance and consequently defer the current zero crossing detection point to a negative current. Excessively larger capacitor should not be used to prevent malfunction of the controller.

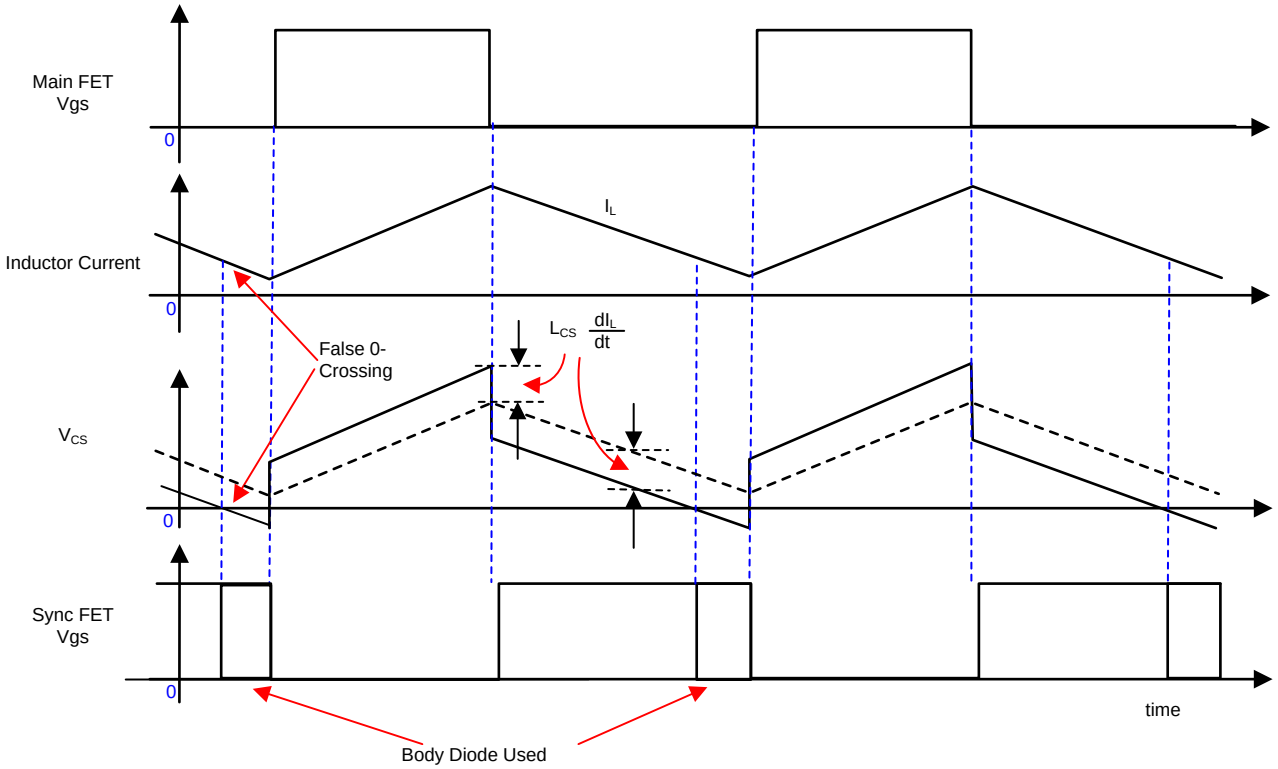


Figure 51. Effects of Parasitic Inductance on the Current Sense Signal and Zero Crossing Detection

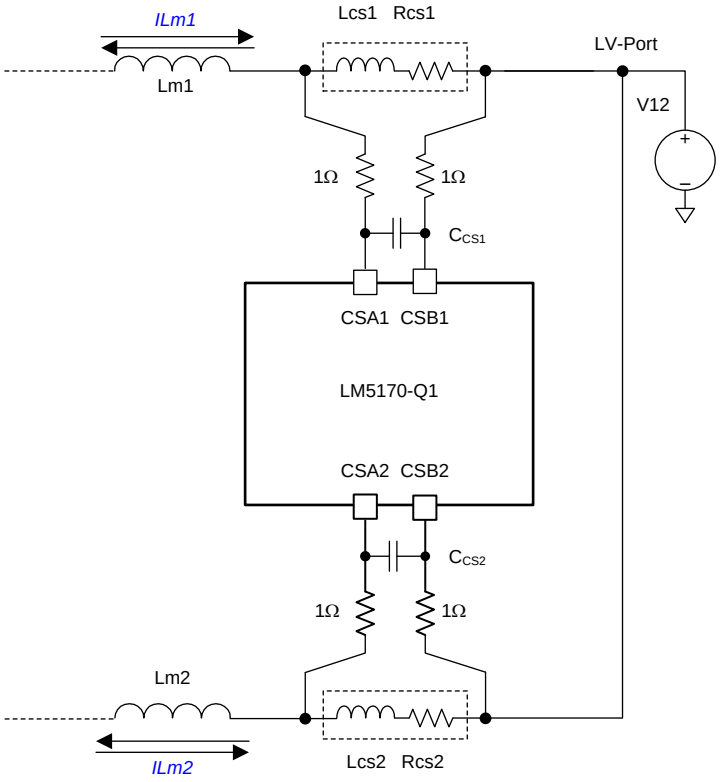


Figure 52. Compensation Network to Compensate the Current Sense Resistor's Parasitic Inductance

8.1.4 Outer Voltage Loop Control

The LM5170-Q1 serves as a current regulator that regulates the DC component of the power inductor current to the value programmed at the ISETA pin. To regulate the output voltage, an outer voltage loop should be employed. The outer voltage loop can be implemented with an analog circuit (see Figure 53) or a digital circuit like an MCU (see Figure 54). The error voltage signal of the output voltage loop is the ISET command for the inner current loop.TI advises that the outer voltage loop crossover frequency should be one decade below that of the inner current loop crossover frequency f_{CO}. Refer to the LM5170-Q1 Quick Start Calculator for the loop compensation guidance.

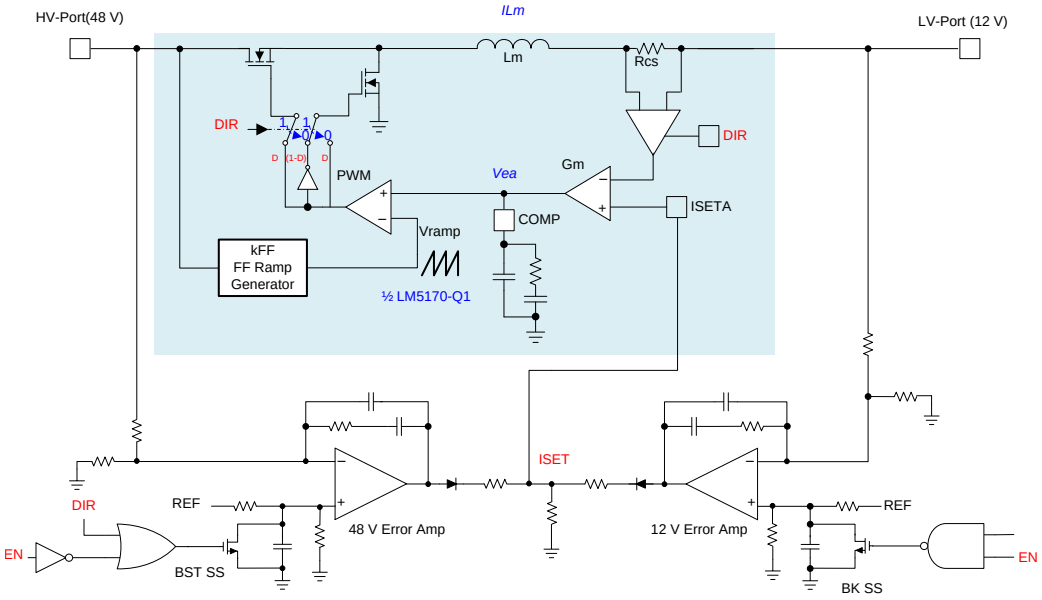


Figure 53. Analog Outer Voltage Loop Control

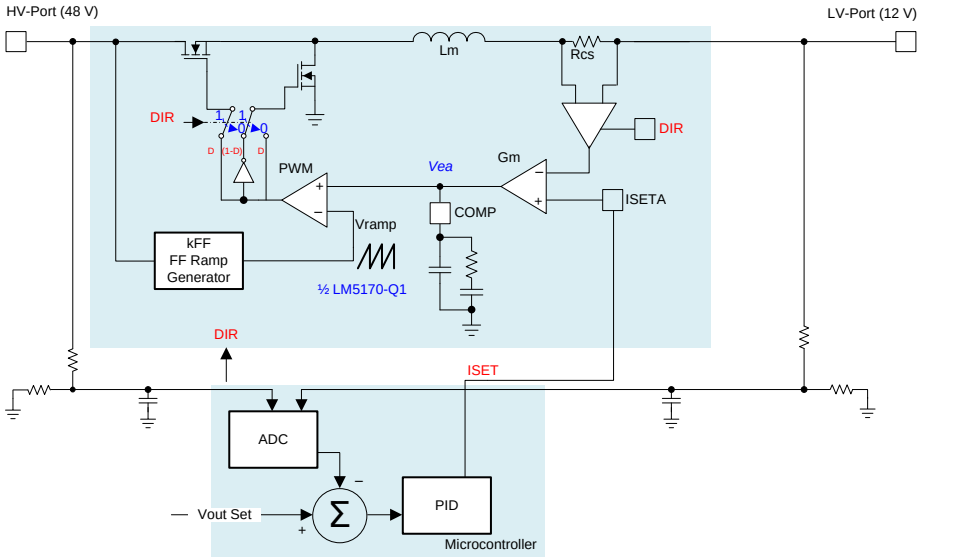


Figure 54. Digital Outer Voltage Loop Control

8.2 Typical Application

8.2.1 60-A, Dual-Phase, 48-V to 12-V Bidirectional Converter

A typical application example is a 60-A, dual-phase bidirectional converter as shown in Figure 55. The HV-Port voltage range is 32 V to 70 V and the LV-Port 0 V to 23 V. Each phase is able to deliver 30-Adc current through the inductor.

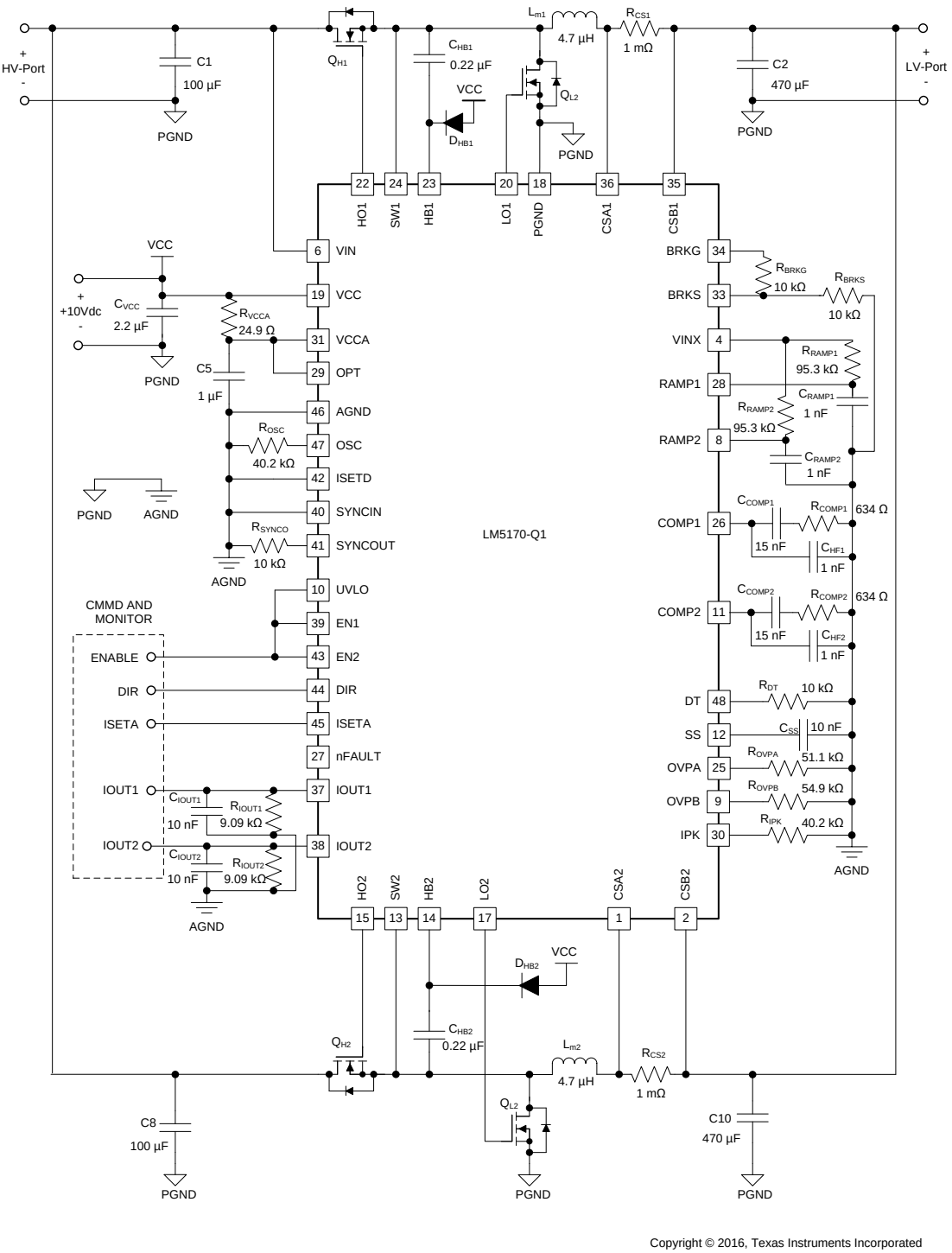


Figure 55. Schematic of the Example Dual-Phase Bidirectional Converter

Typical Application (continued)

8.2.1.1 Design Requirements

Table 4 lists the design parameters for this example.

Table 4. Design Parameters

PARAMETER	EXAMPLE VALUE	NOTE
V_{LV_min}	6 V	LV-Port minimum operating voltage
V_{LV_reg}	14 V	LV-Port nominal voltage
V_{LV_max}	18 V	LV-Port maximum operating voltage
V_{HV_min}	32 V	HV-Port minimum operating voltage
V_{HV_reg}	48 V	HV-Port nominal operating voltage
V_{HV_max}	60 V	HV-Port maximum operating voltage
F_{SW}	100 kHz	Switching frequency
I_{max}	30 A	Maximum channel DC current, bidirectional
I_{total}	60 A	Total bidirectional DC at the LV-Port

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Determining the Duty Cycle

Obviously, the duty cycles are determined by through :

$$D_{BK\_min} = \frac{V_{LV\_reg}}{V_{HV\ max}} = \frac{14V}{70V} = 0.2 \tag{38}$$

$$D_{BK\_max} = \frac{V_{LV\_reg}}{V_{HV\ min}} = \frac{14V}{32V} = 0.438 \tag{39}$$

$$D_{BST\_min} = \frac{V_{HV\_reg} - V_{LV\_max}}{V_{HV\_reg}} = \frac{50V - 23V}{50V} = 0.54 \tag{40}$$

$$D_{BST\_max} = \frac{V_{HV\_reg} - V_{LV\_min}}{V_{HV\_reg}} = \frac{50V - 6V}{50V} = 0.88 \tag{41}$$

8.2.1.2.2 Oscillator Programming

To operate the converter at the desired switching frequency F_{SW}, select the R_{OSC} by satisfying Equation 17, namely,

$$R_{OSC} = \frac{40k\Omega \times 100kHz}{100\ kHz} = 40\ k\Omega \tag{42}$$

Choose the closest standard resistor, that is, R_{OSC} =40.2 kΩ.

8.2.1.2.3 Power Inductor, RMS and Peak Currents

The inductor current has a triangle waveform, as shown in Figure 51. TI recommends selecting an inductor such that its peak-to-peak ripple current is less than 80% of the channel inductor full load DC current. Therefore, the inductor should satisfy Equation 43:

$$L_m \geq \frac{V_{LV\_reg} \times \left(1 - D_{BK\_min}\right)}{80\% \times I_{max} \times F_{sw}} = \frac{14V \times (1 - 0.2)}{0.8 \times 30A \times 100\ kHz} = 4.67\ \mu H \tag{43}$$

Select L_m = 4.7 µH.

Then, the actual inductor peak to peak inductor current is determined by Equation 44:

$$I_{pk-pk} = \frac{V_{LV\_reg} \times (1 - D_{BK\_min})}{L_m \times F_{sw}} = \frac{14V \times (1 - 0.2)}{4.7\mu H \times 100\ kHz} = 23.83\ A \tag{44}$$

The peak inductor current is determined by Equation 45:

$$I_{peak} = I_{max} + \frac{I_{pk-pk}}{2} = 30A + \frac{23.83}{2} = 41.9\ A \quad (45)$$

Select an inductor that has a saturation current I_{sat} at least 20% greater than I_{peak} to ensure full power with adequate margin. In this example, TI recommends selecting an inductor of I_{sat} > 49 A.

The power inductor's full load Root Mean Square (RMS) current I_{LM_RMS} determines its conduction losses. The RMS current is given by Equation 46:

$$I_{Lm\_RMS} = \sqrt{I_{max}^2 + \frac{1}{12} \times I_{pk-pk}^2} = 30.8\ A \quad (46)$$

8.2.1.2.4 Current Sense (R_{CS})

To achieve the highest regulation accuracy over wider load range, the user should target to create 50-mV of V_{CS} at full current. Therefore, R_{CS} should be selected as Equation 47:

$$R_{CS} \leq \frac{50mV}{I_{max}} = \frac{50mV}{30A} = 1.667\ m\Omega \quad (47)$$

Ideally, a 1.5-mΩ current sense resistor should be chosen for this example. However, owing to availability, a standard non-inductive 1-mΩ current sense resistor is selected, namely,

$$R_{CS} = 1.0\ m\Omega \quad (48)$$

Because R_{CS} conducts the same current as the power inductor, its power dissipation is also determined by I_{Lm_RMS}.

If the selected R_{CS} has parasitic inductance (assuming it is 1 nH), it should be compensated, and the compensation capacitor C_{CS} should satisfy Equation 37.

$$C_{CS} = \frac{L_{CS}}{2\Omega \times R_{sn}} = \frac{1nH}{2\Omega \times 1m\Omega} = 0.5\ \mu F \quad (49)$$

Select the closest standard capacitor, C_{CS} = 0.47 µF.

For optimal performance, it is good practice to add a 100-pF ceramic capacitor at each current sense pin to filter out common-mode noise, as shown in Figure 56.

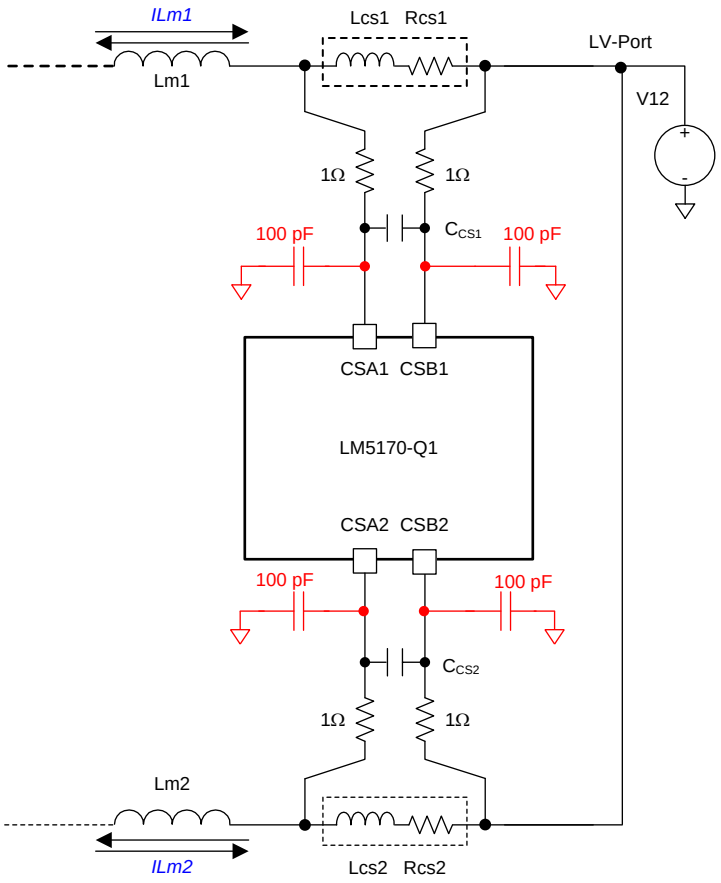


Figure 56. Current Sense With Compensation to Cancel the Effects of Parasitic Inductances

8.2.1.2.5 Current Setting Limits (ISETA or ISETD)

TI recommends setting a hard limit of the maximum current programming signal such that the converter cannot be over driven by an errant current programming signal. Assume the converter is allowed up to 10% overloading current. Refer to Equation 7, the analog current setting signal ISETA should be limited by the following voltage level:

$$V_{ISETA\_max} \le \frac{110\% \times I_{max} \times R_{CS}}{0.02} = \frac{110\% \times 30A \times 1m\Omega}{0.02} = 1.55\ V \tag{50}$$

Refer to Equation 10, the PWM current setting signal ISETD should be limited by the following duty cycle:

$$D_{ISETD\_max} \le \frac{110\% \times I_{max} \times R_{CS}}{0.0625V} = \frac{110\% \times 30A \times 1m\Omega}{0.0625V} = 52.8\% \tag{51}$$

8.2.1.2.6 Peak Current Limit

One purpose of the peak current limit is to protect the power inductor from saturation. Select R_{IPK} such that the peak current limit threshold is 5~10% greater than I_{peak}. According to Equation 13, one gets:

$$R_{IPK} = \frac{R_{CS} \times 105\% \times I_{peak}}{1.1\mu A} = \frac{1m\Omega \times 105\% \times 41.9A}{1.1\mu A} = 40\ k\Omega \tag{52}$$

Select R_{IPK} = 40.2 kΩ, which results in a nominal inductor peak current limit of 44.2 A per channel.

8.2.1.2.7 Power MOSFETS

The power MOSFETs must be chosen with a V_{DS} rating capable of withstanding the maximum HV-port voltage plus transient spikes (ringing). In this example, the maximum HV-rail voltage is 70 V. Selecting the 80 V rated MOSFETs will allow 10-V transient spikes.

When the voltage rating is determined, select the MOSFETs by making tradeoffs between the MOSFET $R_{ds(ON)}$ and total gate charge Qg to balance the conduction and switching losses. For high power applications, parallel MOSFETs to share total power and reduce the dissipation on any individual MOSFET, hence relieving the thermal stress. The conduction losses in each MOSFET is determined by Equation 53.

$$P_{Q\_cond} = \frac{1.8 \times R_{ds(ON)}}{N} \times I^2_{Q\_RMS} \quad (53)$$

where

- N is the number of MOSFETs in parallel
- 1.8 is the approximate temperature coefficient of the Rds(ON) at 125 °C
- and the total RMS switch current I_{Q_RMS} is approximately determined by Equation 54

$$I_{Q\_RMS} \approx \sqrt{D_{max}} \times I_{max} = \sqrt{D_{max}} \times I_{max} \quad (54)$$

where

- D_{max} is the maximum duty cycle, either in the buck mode or boost mode.

The switching transient rise and fall times are approximately determined by:

$$\Delta t_{rise} \approx \frac{N \times Q_g}{4A} \quad (55)$$

$$\Delta t_{fall} \approx \frac{N \times Q_g}{4A} \quad (56)$$

And the switching losses of each of the paralleled MOSFETs are approximately determined by:

$$P_{Q\_sw} = \frac{1}{2} \times C_{oss} \times V^2_{HV} \times F_{sw} + \frac{1}{2} \times \frac{I_{peak}}{N} \times V_{HV} \times (\Delta t_{rise} + \Delta t_{fall}) \times F_{sw} \quad (57)$$

where

- C_{oss} is the MOSFET's output capacitance.

The power MOSFET usually requires a gate-to-source resistor of 10 kΩ to 100 kΩ to mitigate the effects of a failed gate drive. When using parallel MOSFETs, a good practice is to use 1- to 2-Ω gate resistor for each MOSFET, as shown in Figure 57.

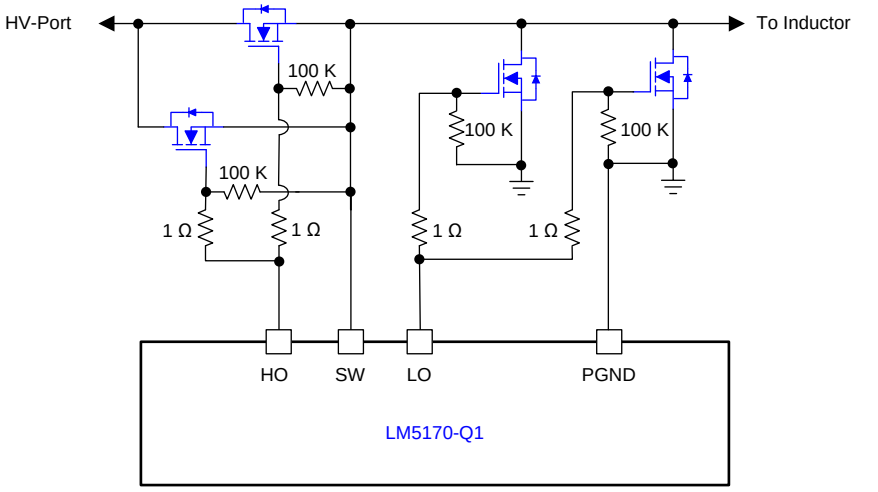


Figure 57. Paralleled MOSFET Configuration

If the dead time is not optimal, the body diode of the power synchronous rectifier MOSFET will cause losses in reverse recovery. Assuming the reverse recovery charge of the power MOSFET is Q_{rr}, the reverse recovery losses are thus determined by Equation 58:

$$P_{Q\_rr} = Q_{rr} \times V_{HV\_max} \times F_{sw} \quad (58)$$

To reduce the reverse recovery losses, an optional Schottky diode can be placed in parallel with the power MOSFETs. The diode should have the same voltage rating as the MOSFET, and it must be placed directly across the MOSFETs drain and source. The peak repetitive forward current rating should be greater than I_{peak}, and the continuous forward current rating should be greater than the following Equation 59:

$$I_{SD\_avg} = I_{pk} \times t_{DT} \times F_{sw} \quad (59)$$

8.2.1.2.8 Bias Supply

The LM5170-Q1 requires an external 10- to 12-V VCC bias supply to operate. If not available in the system, the user can generate it from the LV-port using a buck-boost or SEPIC converter, or from the HV-port using a buck converter. Refer to the Texas Instruments LM25118-Q1/LM5118-Q1 to implement a buck-boost converter, or LM5001-Q1 to implement a SEPIC converter, or the LM5160-Q1/LM5161-Q1 to implement a buck converter.

The total load current of the bias supply is mainly determined by the total MOSFET gate charge Qg. Assume the system employs multiple LM5170-Q1s to implement M number of phases, and each phase uses N number of MOSFETs in parallel as one switch. There will be 2x N MOSFETs per phase to drive. Then the total current to drive these MOSFETs through VCC bias supply is determined by Equation 60.

$$I_{VCC} = 2 \times M \times N \times Q_g \times F_{sw} + M \times 5mA$$

where

- 5 mA is the worst case maximum current used by the control logic circuit of each phase. (60)

In an example of a four-phase system employing two parallelled MOSFETs for one switch, where M=4, N=2, Q_g=100 nC, and F_{sw}=100 KHz, the bias supply should be able to support at least the following total load current:

$$I_{VCC} \geq 2 \times 4 \times 2 \times 100nC \times 100kHz + 4 \times 5mA = 180\ mA \quad (61)$$

In an example of an eight-phase system employing the same parallel MOSFETs for one switch, the bias supply should be able to support the following total load current:

$$I_{VCC\_8ph} = 2 \times 8 \times 2 \times 100nC \times 100kHz + 8 \times 5mA = 360\ mA \quad (62)$$

The VCC AC bypass ceramic capacitor C_{VCC} = 1 ~ 2.2 µF, rated at least 16 V, must be placed close to the VCC and PGND pins. Similarly, a ceramic capacitor C_{VCCA} = 1 µF, rated at least 16 V, must be placed close to the VCCA and AGND pins. Place a 24-Ω resistor between VCC and VCCA pins.

8.2.1.2.9 Boot Strap

Select a ceramic capacitor C_{HB1} = C_{HB2} =0.1 ~ 0.22 µF, placed close to the HB and SW pins. The fast switching diode of the forward current rated at 1-A and reverse voltage not lower than V_{HV_max} should be selected as the boot strap diode, through which the boot capacitor C_{HB1} or C_{HB2} is charged by VCC. To reduce the noise caused by the fast charging current, a 2-Ω to 5-Ω current limiting resistor must be placed in series with each boot diode.

8.2.1.2.10 RAMP Generators

According to Equation 14, the ramp generator should be selected such that a peak voltage of 5 V is produced each cycle when the HV-port voltage is 48 V.

Select C_{RAMP1} = C_{RAMP2} = 1 nF. Therefore,

$$R_{RAMP} = \frac{9.6}{F_{sw} \times C_{RAMP}} = \frac{9.6}{100kHz \times 1nF} = 96\ k\Omega \quad (63)$$

Choose the closest standard resistor value, namely,

R_{RAMP1} = R_{RAMP2} = 95.3 kΩ.

For optimal performance, C_{RAMP1} and C_{RAMP2} should be ceramic capacitors with tolerance not greater than 10%. Capacitors of the 5% or 1% C0G/NPO types are preferred.

8.2.1.2.11 OVP

As shown in Figure 36 and Figure 37, the HV-Port and LV-Port overvoltage protection thresholds can be programmed by R_{OVPA} and R_{OVPB}, respectively. These resistor values are determined by Equation 64 and Equation 65.

$$R_{OVPA} = \frac{1.185V}{V_{OVPA\ th} - 1.185V} \times 3000k\Omega = \frac{1.185V}{70V - 1.185V} \times 3000k\Omega = 51.66\ k\Omega \quad (64)$$

$$R_{OVPB} = \frac{1.185V}{V_{OVPB\ th} - 1.185V} \times 1000k\Omega = \frac{1.185V}{23V - 1.185V} \times 1000k\Omega = 54.3\ k\Omega \quad (65)$$

Select the closest standard resistor values. In this example, R_{OVPA} = 51.1 kΩ, and R_{OVPB} = 54.9 kΩ.

8.2.1.2.12 Dead Time

To use the built-in adaptive dead time, the DT pin must be connected to VCCA pin.

To program the dead time, follow Equation 15 to select the resistor R_{DT}. To dynamically adjust the dead time with an external analog voltage signal, follow Equation 19. To dynamically adjust the dead time with an external PWM signal, follow Equation 20.

In the example circuit, the nominal dead time is selected to be 55 ns. According to Equation 15, the programming resistor should be:

$$t_{DT} = R_{DT} \times 4\frac{ns}{k\Omega} + 16ns \quad (66)$$

$$R_{DT} = \frac{t_{DT} - 16ns}{4} \times 1\frac{k\Omega}{ns} = \frac{55\ ns - 16\ ns}{4} \times 1\frac{k\Omega}{ns} = 9.75\ k\Omega \quad (67)$$

Select the standard value, R_{DT} = 10 kΩ.

8.2.1.2.13 IOUT Monitors

TI recommends making the following selections:

$R_{IOUT1} = R_{IOUT2} = 9.09\ k\Omega$ (68)

$C_{IOUT1} = C_{IOUT2} = 0.01\ \mu F$ (69)

Then the monitors' delay is determined by the following time constant:

$$\tau_{IOUT} = R_{IOUT1} \times C_{CIOUT1} = 9.09k\Omega \times 0.01\mu F = 90.9\ \mu s \quad (70)$$

At full load, the DC component of the monitor voltage is determined by:

$$V_{IOUT1} = V_{IOUT2} = \left(\frac{I_{max} \times R_{CS}}{200\Omega} + 25\mu A\right) \times R_{IOUT1} = \left(\frac{30A \times 1m\Omega}{200\Omega} + 25\mu A\right) \times 9.09k\Omega = 1.591\ V \quad (71)$$

Because the inductor ripple current is 23.8 A, according to Equation 11, the IOUT peak to peak ripple current will be:

$$\Delta IOUT1 = \frac{I_{pk-pk} \times R_{CS}}{200\Omega} = \frac{23.8A \times 1m\Omega}{200\Omega} = 119\ \mu A \quad (72)$$

The RC filter corner frequency is thus given by:

$$F_{IOUT} = \frac{1}{6.28 \times R_{IOUT} \times C_{IOUT}} = \frac{1}{6.28 \times 9.09k\Omega \times 10nF} = 1.75\ kHz \quad (73)$$

The resulting peak-to-peak monitor ripple voltage is approximately determined by:

$$\Delta V_{IOUT} = \Delta IOUT1 \times R_{IOUT} \times 10^{-\log\left(\frac{F_{sw}}{F_{IOUT}}\right)} = 119\mu A \times 9.09k\Omega \times 10^{-\log\left(\frac{100kHz}{1.75kHz}\right)} = 19\ mV \quad (74)$$

Which is about 1.1% peak-to-peak ripple on top of the full load DC monitor voltage. Increasing C_{IOUT} value will further attenuate the ripple voltage, but also cause longer monitor delays.

8.2.1.2.14 UVLO Pin Usage

The example circuit uses the UVLO pin as the LM5170-Q1's master enable pin. However, the UVLO pin can also fulfill the function of undervoltage lockout, either the 48-V rail UVLO, or 12-V rail UVLO, or VCC UVLO.

Assume the user implements the 48-V rail UVLO, and the low-side resistor R_{UVLO2} = 10 kΩ, the 48 V UVLO release threshold V_{UVLO} = 24 V, and UVLO hysteresis is V_{HYS} =2.4 V. Referring to Figure 47 and Equation 21, one can find that R_{UVLO1} is given by:

$$R_{UVLO1} = \frac{U_{UVLO} - 2.5V}{2.5V} \times R_{UVLO2} = \frac{24V - 2.5V}{2.5V} \times 10k\Omega = 86\ k\Omega \tag{75}$$

The final selection should select the closest standard resistor of R_{UVLO1} = 86.6 kΩ.

And R_{UVLO3} should satisfy Equation 23, namely,

$$R_{UVLO3} = \frac{\frac{V_{HYS}}{25\mu A} - R_{UVLO1}}{1 + \frac{R_{UVLO1}}{R_{UVLO2}}} = \frac{\frac{24V}{25\mu A} - 86.6k\Omega}{1 + \frac{86.6k\Omega}{10k\Omega}} = 0.973\ k\Omega \tag{76}$$

Select the closest standard resistor, R_{UVLO1} = 976 Ω.

If the user chooses to add the capacitor C_{UVLO} = 1 nF, it leads to a delay time constant of 10 µs to filter possible noise at the at the UVLO pin.

8.2.1.2.15 VIN Pin Configuration

The VIN pin must always be connected to the HV voltage rail. It is good practice to add a small RC filter to improve the VIN noise immunity, as shown in Figure 58. Usually the filter resistor selection is 10 to 20 Ω, and the bypass capacitor is 0.1 µF to 1.0 µF.

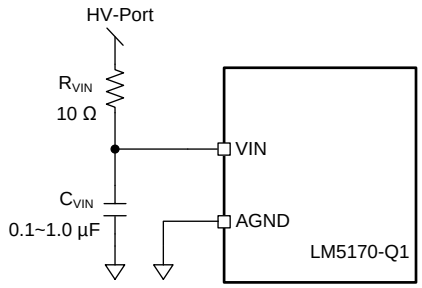


Figure 58. VIN Pin Configuration

8.2.1.2.16 Loop Compensation

Assuming the total resistance along the current path including the external power cables, PCB current tracks, and battery internal impedances is 50 mΩ, according to Equation 36, the compensation network for the inner current loop is determined by:

$$\begin{cases} R_{COMP} = \frac{K_{FF}}{50 \times R_{cs} \times Gm} \times \left| 2i \times \pi \times f_{CO} \times L_m + (R_{CS} + R_S) \right| = \frac{0.104}{50 \times 1m\Omega \times 1mA/V} \times \left| 2i \times \pi \times 10kHz \times 4.7\mu H + 51m\Omega \right| = 0.623\ k\Omega \\ C_{COMP} = \frac{L_m}{(R_{CS} + R_S) \times R_{COMP}} = \frac{4.7\mu H}{(50m\Omega + 1m\Omega) \times 0.632k\Omega} = 147\ nF \\ C_{HF} = \frac{C_{COMP}}{100} = 1.47nF \end{cases} \tag{77}$$

Selecting the closest standard values for the compensation network, namely,

$R_{COMP1} = R_{COMP2} = 634\ \Omega$

$C_{COMP1} = C_{COMP2} = 150$ nF

$C_{HF1} = C_{HF2} = 1$ nF

These initial component selections produce a total loop phase margin of 90°, which is larger than necessary. Fine tune the loop compensation by reselecting $C_{COMP1} = C_{COMP2} = 15$ nF, then the phase margin will be 45° for an optimal dynamic performance.

Figure 59 shows the Bode Plots of the power plant, the compensation gain, and the resulting total open loop.

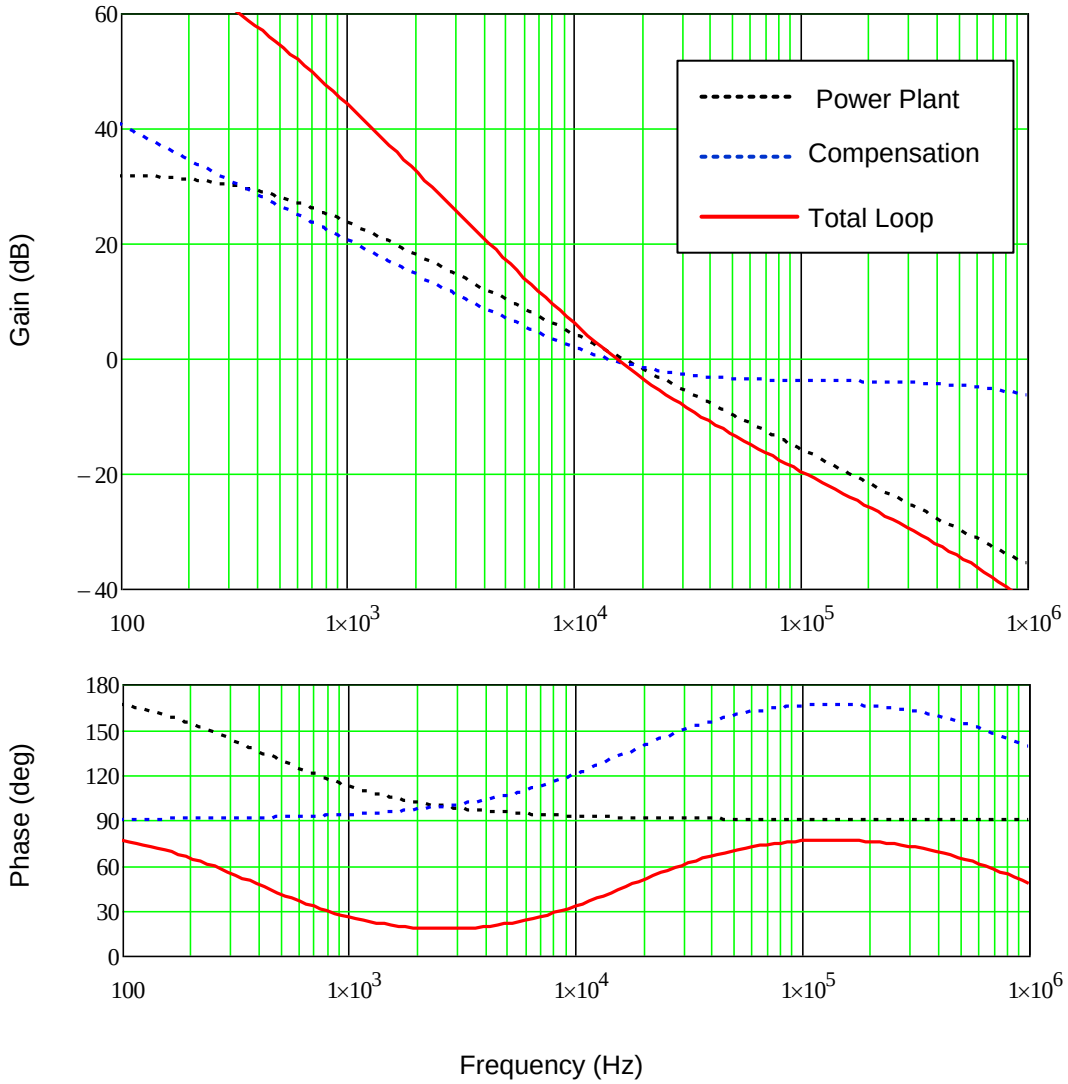


Figure 59. Bode Plots of the Example Converter

8.2.1.2.17 Soft Start

Soft start can be programmed with a ceramic capacitor C_{SS}. Note that C_{SS} also determines the retry frequency when the converter is an under overvoltage condition (OVPA or OVPB). Because the soft start completes when the SS pin voltage reaches about 5 V, the capacitor C_{SS} can be chosen by Equation 78 to limit the full load start-up time within $\Delta T_{SS} = 2$ ms:

$$C_{SS} = \frac{25\ \mu A \times \Delta T_{SS}}{5V} = \frac{25\ \mu A \times 2ms}{5V} = 10\ nF \quad (78)$$

Select the closest standard ceramic capacitor, that is, C_{SS} = 10 nF.

8.2.1.2.18 ISET Pins

To control the current setting by an analog voltage, ground the ISETD pin. To control the current setting by a PWM signal, there are two options to choose.

The first option is to use the built-in ISETD-to-ISETA decoder as shown in Figure 22. The PWM duty cycle to ISETA voltage conversion ratio satisfies Equation 8. The selection of C_{ISETA} and F_{ISETD} should be constrained by Equation 1 and Equation 4. The advantages of this option include convenience and current control accuracy. The drawback is the delay it may cause.

Another option is to use an external two-stage RC filter to convert the PWM ISETD signal to a DC voltage feeding the ISETA pin as shown in Figure 60. To achieve the same ISETA ripple voltage, this option only requires C_{ISETA} =1.5 nF, and the delay time of this two-stage filter is only 10% of the built-in decoder, or 15 µs versus the built-in decoder's 150 µs. The drawback of this option is the conversion errors if the PWM signal voltage levels are not well regulated. This option is more suitable for operation under a closed digital outer voltage loop because the ISETD to ISETA conversion error can be readily compensated by the closed outer voltage loop.

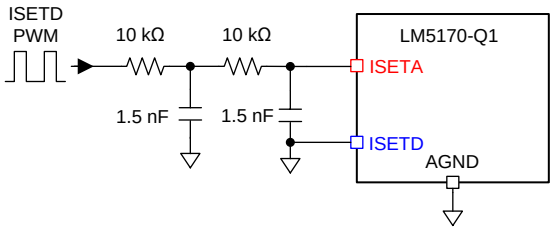


Figure 60. Two-Stage RC Filter to Convert the PWM into an Analog Voltage at the ISETA Pin

8.2.1.3 Application Curves

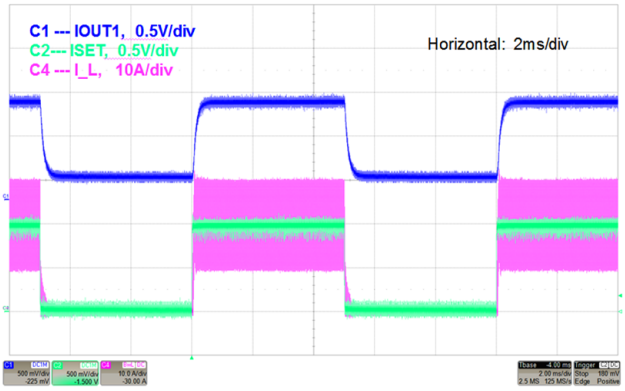


Figure 61. Channel Inductor Current and IOUT Tracking ISETA Command

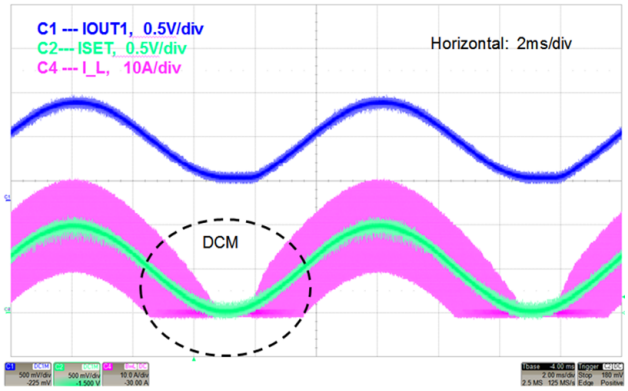


Figure 62. Diode Emulation Prevents Negative Current

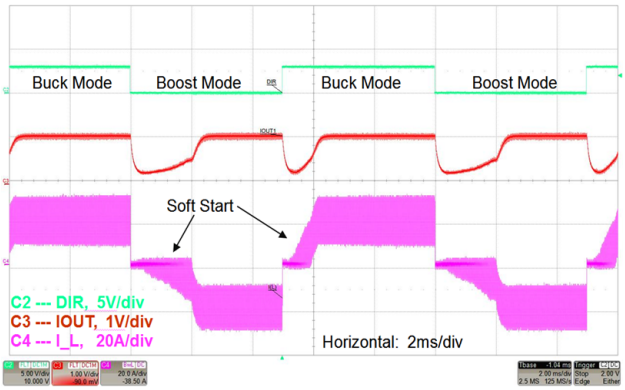


Figure 63. Channel Inductor Current and Monitor Responses to Dynamic DIR Change

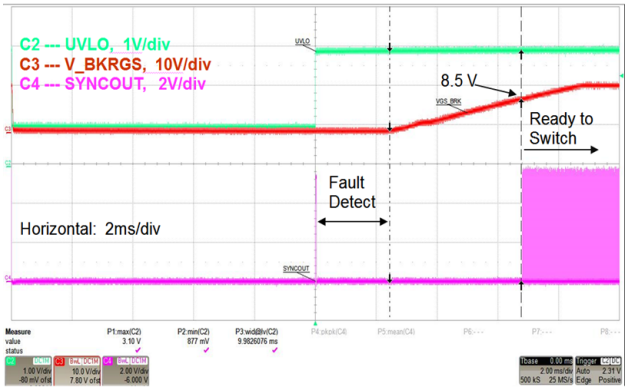


Figure 64. Start-Up Sequence Following UVLO Enable

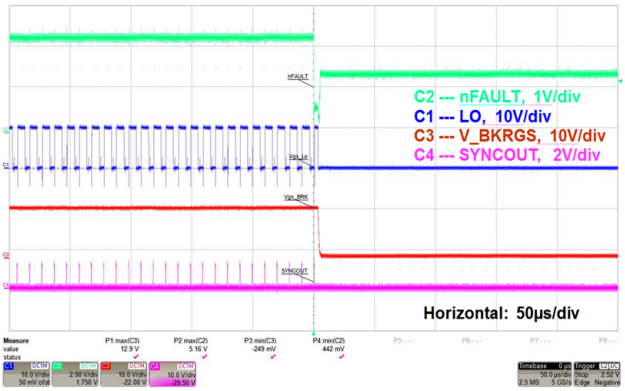


Figure 65. nFAULT Shutdown Latch

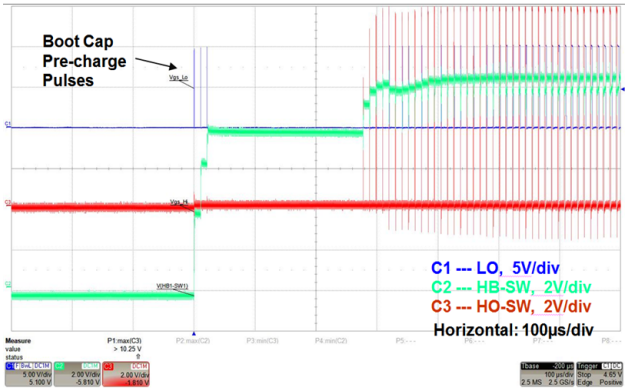


Figure 66. Boot Capacitor Pre-Charge During Start-Up in Buck Mode

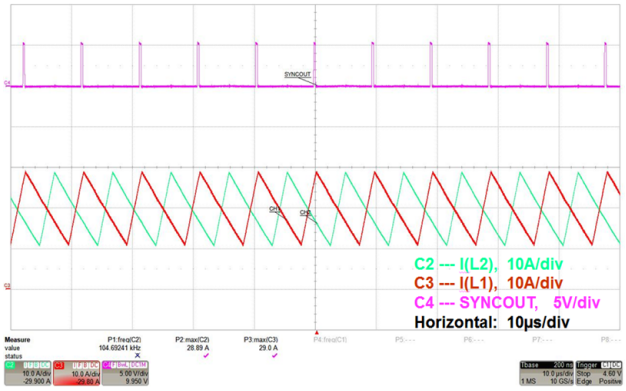


Figure 67. Dual=Channel Interleaving Operation: Buck Mode

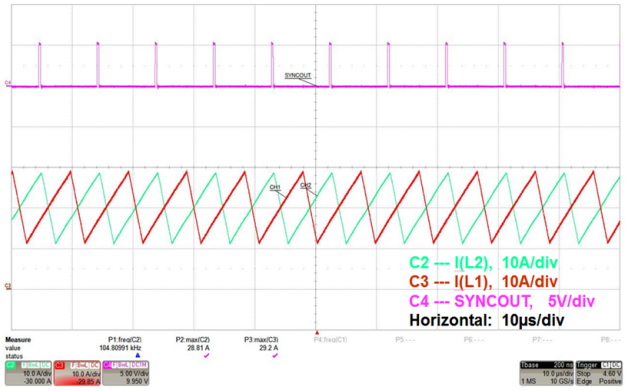


Figure 68. Dual-Channel Interleaving Operation: Boost Mode

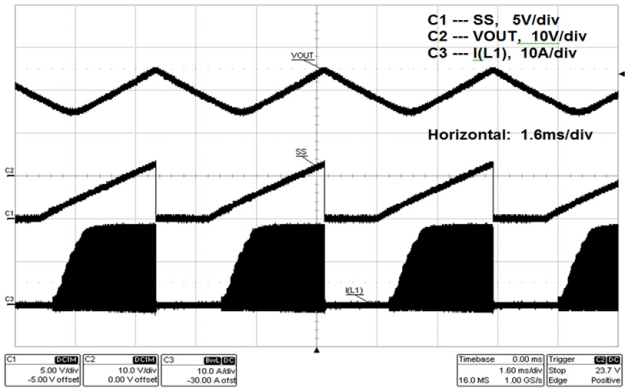


Figure 69. LV-Port OVP: Buck Mode

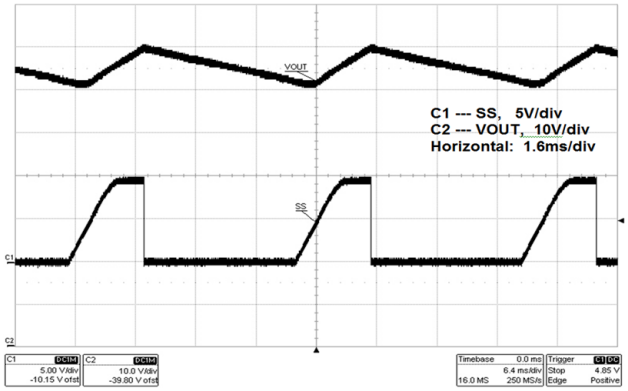


Figure 70. HV-Port OVP: Boost Mode

9 Power Supply Recommendations

The LM5170-Q1-based converter is designed to operate with two differential voltage rails like the 48-V and 12-V dual battery system, or a storage system having a battery on one end and the Super-Cap on the other end. When operating with bench power supplies, each supply should be capable of sourcing and sinking the maximum operating current. This may require to parallel an Electronic load (E-Load) with the bench power supply (PS) to emulate the batteries, as shown in Figure 71.

It can also be used with a voltage source on one end and a load on the other end if the outer voltage control loop is closed. The outer voltage loop can be implemented either with digital means like an MCU or with analog circuit, as shown in Figure 53 and Figure 54.

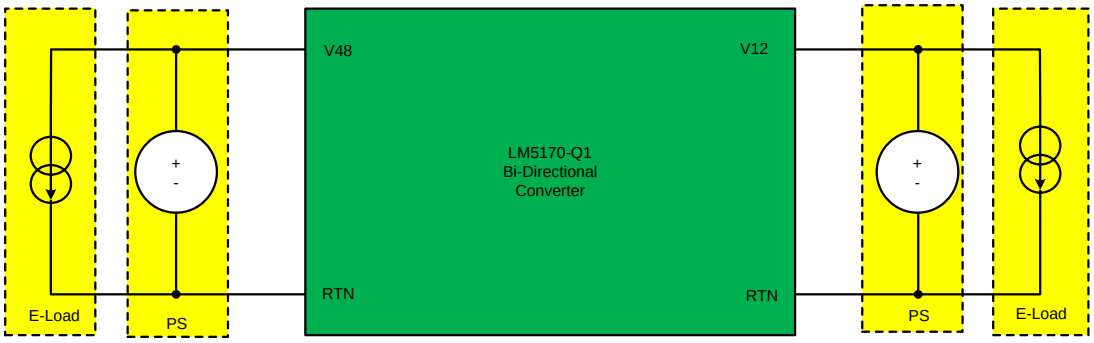


Figure 71. Emulated Dual Battery System With Bench Power Supplies and E-Loads

10 Layout

10.1 Layout Guidelines

Careful PCB layout is critical to achieve low EMI and stable power supply operation as well as optimal efficiency. Make the high frequency current loops as small as possible, and follow these guidelines of good layout practices:

1. For high power board design, use at least a 4-layer PCB of 2-oz or thicker copper planes. Make the first inner layer a ground plane that is adjacent to the top layer on which the power components are installed, and use the second inner layer for the critical control signals including the current sense, gate drive, commands, and so forth. The ground plane between the signal and top layers helps shield switching noises on the top layer away from affecting the control signals.
2. Optimize the component placements and orientations before routing any traces. Place the power components such that the power flow from port to port is direct, straight and short. Avoid making the power flow path zigzag on the board.
3. Identify the high frequency AC current loops. In the bidirectional converter, the AC current loop of each channel is along the path of the HV-port rail capacitors, high-side MOSFET, low-side MOSFET, and back to the HV-port rail capacitors' return. Place these components such that the current flow path is short, direct and the special area enclosed by the loop is minimized.
4. Place the power circuit symmetrically between CH-1 and CH-2. Split the HV-port rail capacitors and LV-port rail capacitors evenly between CH-1 and CH-2.
5. If more than one LM5170-Q1 is used on the same PCB for multi phases, place the circuits of each LM5170-Q1 in the similar pattern.
6. Use adequate copper for the power circuit, so as to minimize the conductions losses on high-current PCB tracks. Adequate copper can also help dissipate the heat generated by the power components, especially the power inductors, power MOSFETs, and current sense resistors. However, pay attention to the polygon of the switch node, which connects the high-side MOSFET source, low-side MOSFET drain, power inductor, and the controller SW pin. The switch node polygon sees high dv/dt during switching operation. To minimize the EMI emission by the switch node polygon, make its size sufficient but not excessive to conduct the switched current.
7. Use appropriate number of via holes to conduct current to, and heat through, the inner layers.
8. Always separate the power ground from the analog ground, and make a single point connection of the power ground, analog ground, and the EP pad, at the location of the PGND pin.
9. Minimize current-sensing errors by routing each pair of CSA and CSB traces using a kelvin-sensing directly across the current sense resistors. The pair of traces must be routed closely side by side for good noise immunity.
10. Route sensitive analog signals of the CS, IOUT, COMP, OVPA, and OVPB pins away from the high-speed switching nodes (HB, HO, LO, and SW).
11. Route the paired gate drive traces, namely the pairs of HO1 and SW1, HO2 and SW2, LO1 and return, and LO2 and return, closely side by side. Route CH-1 gate drive traces in symmetry with CH-2's.
12. Place the IC setting, programming and controlling components as close as possible to the corresponding pins, including the following component: R_{OSC}, R_{DT}, R_{IPK}, C_{RAMP1}, C_{RAMP2}, R_{OVPA}, R_{OVPB}, C_{ISETA}, C_{COMP1}, R_{COMP2}, C_{COMP1}, C_{COPM2}, C_{HF1}, and C_{HF2}.
13. Place the bypass capacitors as close as possible to the corresponding pins, including C_{VIN}, C_{VCC}, C_{VCCA}, C_{HB1}, C_{HB2}, C_{OPVA}, C_{OVPB}, as well as the 100-pF current sense common-mode bypassing capacitors.
14. Flood each layer with copper to take up the empty areas for optimal thermal performance.
15. Apply heat sink to components as necessary according to the system requirements.

10.2 Layout Examples

The following figures are some examples illustrating these layout guidelines. For the detailed PCB layout artwork of the LM5170-Q1 Evaluation Module (LM5170EVM-BIDIR), please refer to the *LM5170-Q1 EVM User's Guide* (SNVU543).

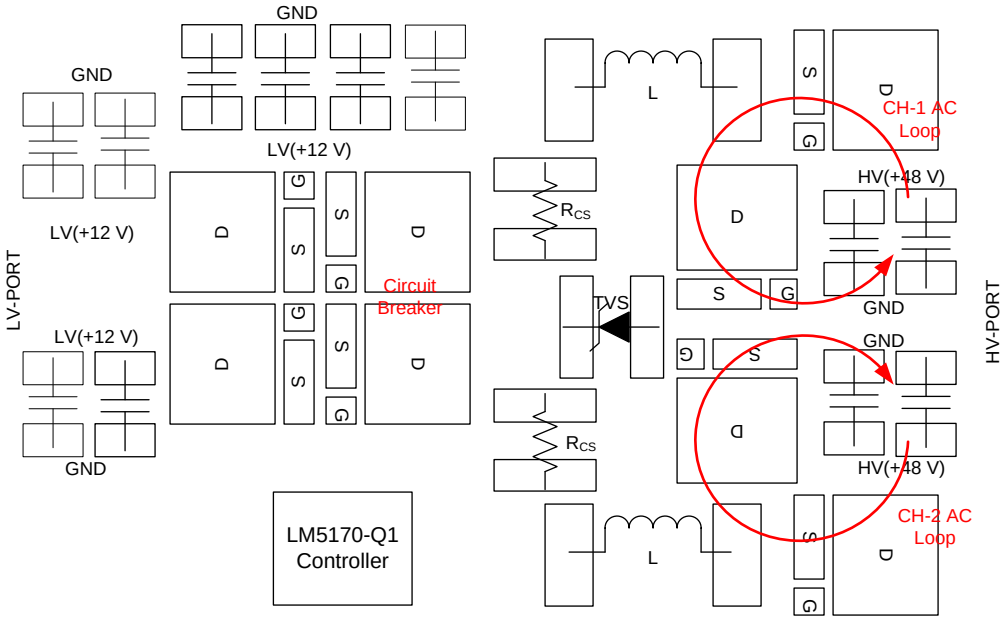


Figure 72. A Layout Example of Dual-Channel Power Circuit Placement

Layout Examples (continued)

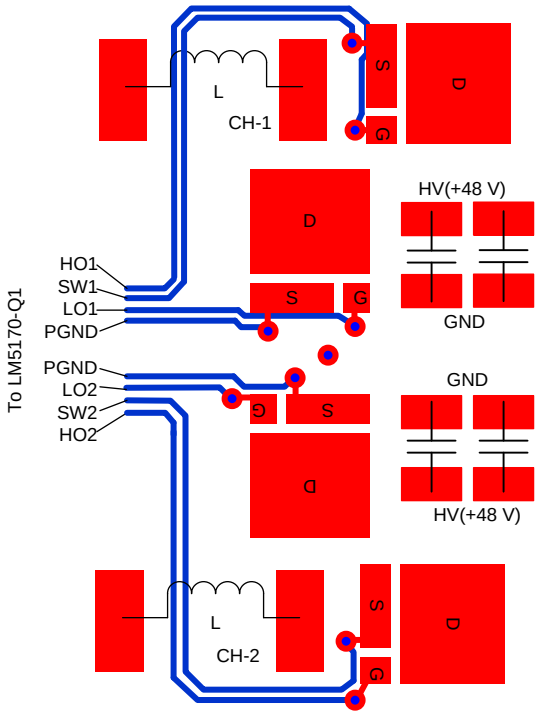
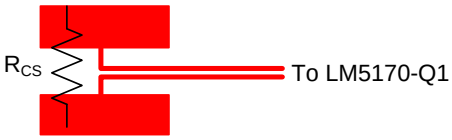
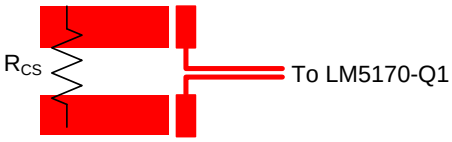


Figure 73. A Layout Example of MOSFET Gate Drive Routing



(a) Kelvin Contact of Resistor without Sense Pins



(b) Kelvin Contact of Resistor with Sense Pins

Figure 74. A Layout Example of Current Sense Routing

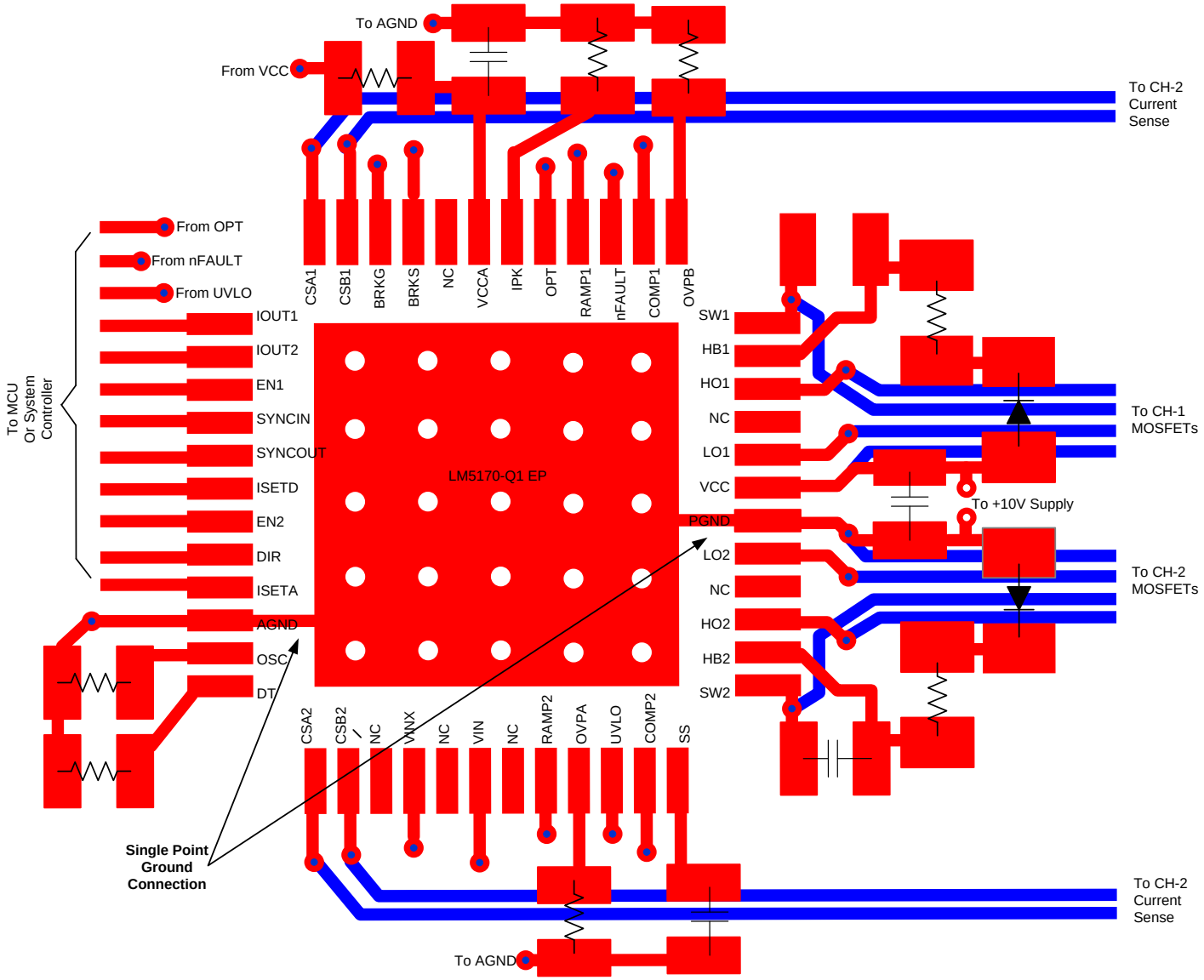


Figure 75. A Layout Example of LM5170-Q1 Critical Signal Routing

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For development support, see the following:

- LM25118-Q1
- LM5118-Q1
- LM5001-Q1
- LM5160-Q1
- LM5161-Q1

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5170QPHPRQ1	PREVIEW	HTQFP	PHP	48	1000	TBD	Call TI	Call TI	-40 to 150		
LM5170QPHPTQ1	PREVIEW	HTQFP	PHP	48	250	TBD	Call TI	Call TI	-40 to 150		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

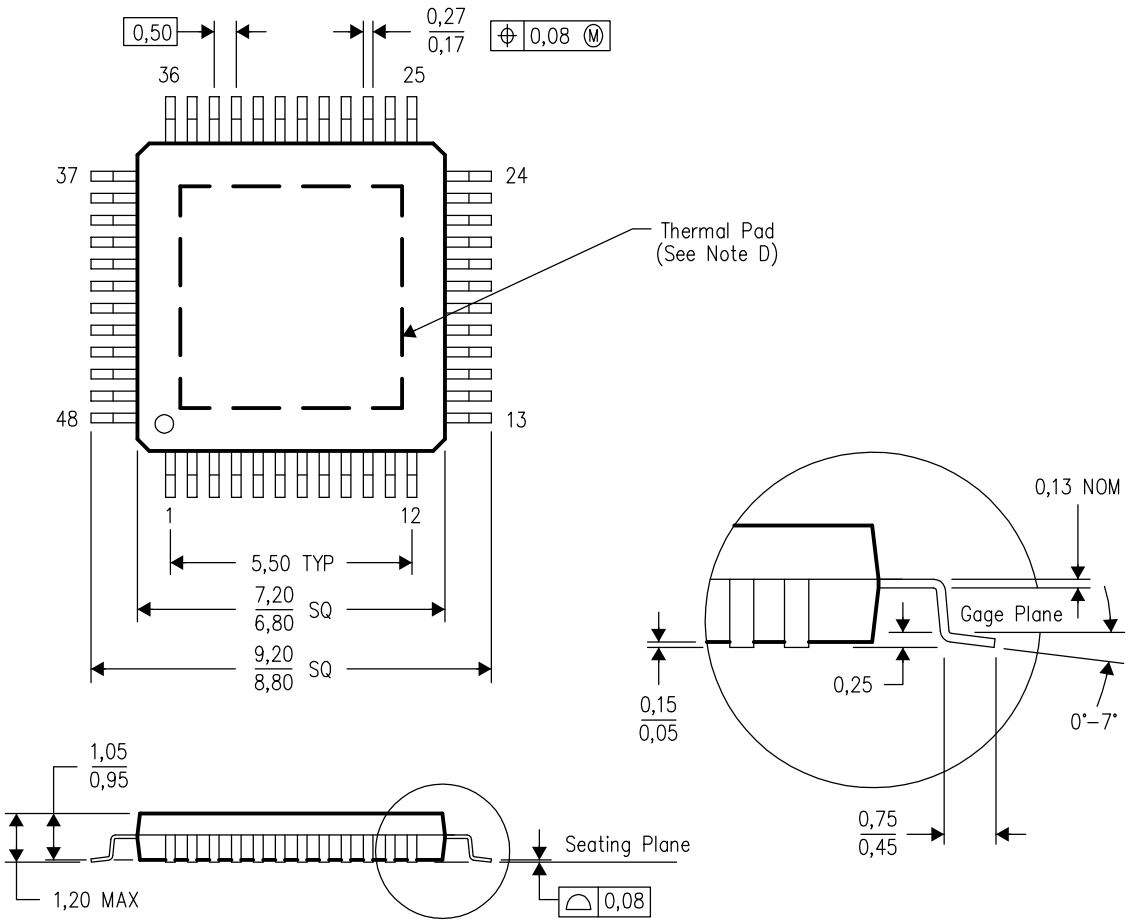
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

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