1. Overview

1.1 Features

The M16C Family offers a robust platform of 32-/16-bit CISC microcomputers (MCUs) featuring high ROM code efficiency, extensive EMI/EMS noise immunity, ultra-low power consumption, high-speed processing in actual applications, and numerous and varied integrated peripherals. Extensive device scalability from low- to high-end, featuring a single architecture as well as compatible pin assignments and peripheral functions, provides support for a vast range of application fields.

The R32C/100 Series is a high-end microcontroller series in the M16C Family. With a 4-Gbyte memory space, it achieves maximum code efficiency and high-speed processing with 32-bit CISC architecture, multiplier, multiply-accumulate unit, and floating point unit. The selection from the broadest choice of on-chip peripheral devices — UART, CRC, DMAC, A/D and D/A converters, timers, I^2C, and watchdog timer enables to minimize external components.

The R32C/100 Series, in particular, provides the R32C/153 Group, a product specific to vehicle network. This product, provided as 144-pin plastic molded LQFP package, configures four channels of CAN module, eight channels of LIN module, and standard peripherals.

1.1.1 Applications

Automotive, communication equipment, industrial equipment etc.

1.1.2 Performance Overview

Table 1.1 and Table 1.2 show the performance overview of the R32C/153 Group.

Table 1.1 R32C/153 Group Performance (1/2)

Unit	Function	Performance
CPU	Central processing unit	R32C/100 Series CPU Core • Basic instructions: 108 • Minimum instruction execution time: 15.625 ns (f(CPU) = 64 MHz) • Multiplier: 32-bit × 32-bit → 64-bit • Multiply-accumulate unit: 32-bit × 32-bit + 64-bit → 64-bit • IEEE-754 floating point standard: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode
Memory		Flash memory: 768 Kbytes, 1 Mbyte RAM: 48 Kbytes Data flash: 4 Kbytes × 2 blocks E2dataFlash: none (1)/8 Kbytes Refer to Table 1.3 for details
Voltage Detector	Low voltage detector	Optional (2) Low voltage detection interrupt
Clock	Clock generator	• 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/re-oscillation detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode
Interrupts		Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 9, key input × 4 Interrupt priority levels: 7 levels
Watchdog Timer		15 bits × 1 (selectable input frequency from prescaler output) Automatic timer start function is available
DMA	DMAC	4 channels • Cycle-steal transfer mode • Request sources: 52 • 2 transfer modes: Single transfer, repeat transfer
	DMAC II	• Can be activated by any peripheral interrupt source • 3 transfer functions: Immediate data transfer, calculation transfer, chained transfer
I/O Ports	Programmable I/O ports	• 2 input-only ports • 120 CMOS inputs/outputs • A pull-up resistor is selectable for every 4 input ports
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Three-phase motor control timer	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer

Notes:
1. Contact a Renesas Electronics sales office to use the non-E2dataFlash version.
2. Contact a Renesas Electronics sales office to use the optional feature.

Table 1.2 R32C/153 Group Performance (2/2)

Unit	Function	Performance
Serial Interface	UART0 to UART4	Asynchronous/synchronous serial interface × 5 channels • I^2C-bus (UART0 to UART2) • Special mode 2 (UART0 to UART2)
A/D Converter		10-bit resolution × 34 channels Sample and hold functionality integrated Self test/Open-circuit detection assist
D/A Converter		8-bit resolution × 2
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)
X-Y Converter		16 bits × 16 bits
Intelligent I/O		Time measurement (input capture): 16 bits × 32 Digital debounce circuit contained Waveform generation (output compare): 16 bits × 32 Phase shift waveform output mode contained
Serial Bus Interface		3 channels • Synchronous serial communication mode • 4-wire serial bus mode Programmable character length: 8 to 16 bits
LIN Module		8 channels
CAN Module		4 channels CAN functionality compliant with ISO11898-1 32 mailboxes
Flash Memory		Programming and erasure supply voltage: VCC = 3.0 to 5.5 V Minimum endurance: 1,000 program/erase cycles Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming
E^2dataFlash		Minimum endurance: 100,000 program/erase cycles
Operating Frequency/Supply Voltage		64 MHz/VCC = 3.0 to 5.5 V
Operating Temperature		-40°C to 85°C (J version) -40°C to 105°C (L version) (1) -40°C to 125°C (K version)
Current Consumption		43 mA (VCC = 5.0 V, f(CPU) = 64 MHz) 8 µA (VCC = 3.3 V, f(XCIN) = 32.768 kHz, wait mode)
Package		144-pin plastic molded LQFP (PLQP0144KA-A)

Note:
1. Contact a Renesas Electronics sales office to use the L version products.

1.2 Product Information

Table 1.3 lists the product information and Figure 1.1 shows the details of the part number.

Table 1.3 R32C/153 Group Product List As of September, 2010

Part Number	Package Code (1)	ROM Capacity (2)	RAM Capacity	E^{2}dataFlash	Remarks
R5F64534JFD	PLQP0144KA-A	768 Kbytes + 8 Kbytes	48 Kbytes	8 Kbytes	J version
R5F64534LFD					L version (3)
R5F64534KFD					K version
R5F6453MJFD				NA (3)	J version
R5F6453MLFD					L version (3)
R5F6453MKFD					K version
R5F64535JFD		1 Mbyte + 8 Kbytes		8 Kbytes	J version
R5F64535LFD					L version (3)
R5F64535KFD					K version
R5F6453NJFD				NA (3)	J version
R5F6453NLFD					L version (3)
R5F6453NKFD					K version

Notes:
1. The old package code is as follows:PLQP0144KA-A: 144P6Q-A
2. Data flash memory provides an additional 8 Kbytes of ROM capacity.
3. Contact a Renesas Electronics sales office to use the non-E^{2}dataFlash version or the L version products.

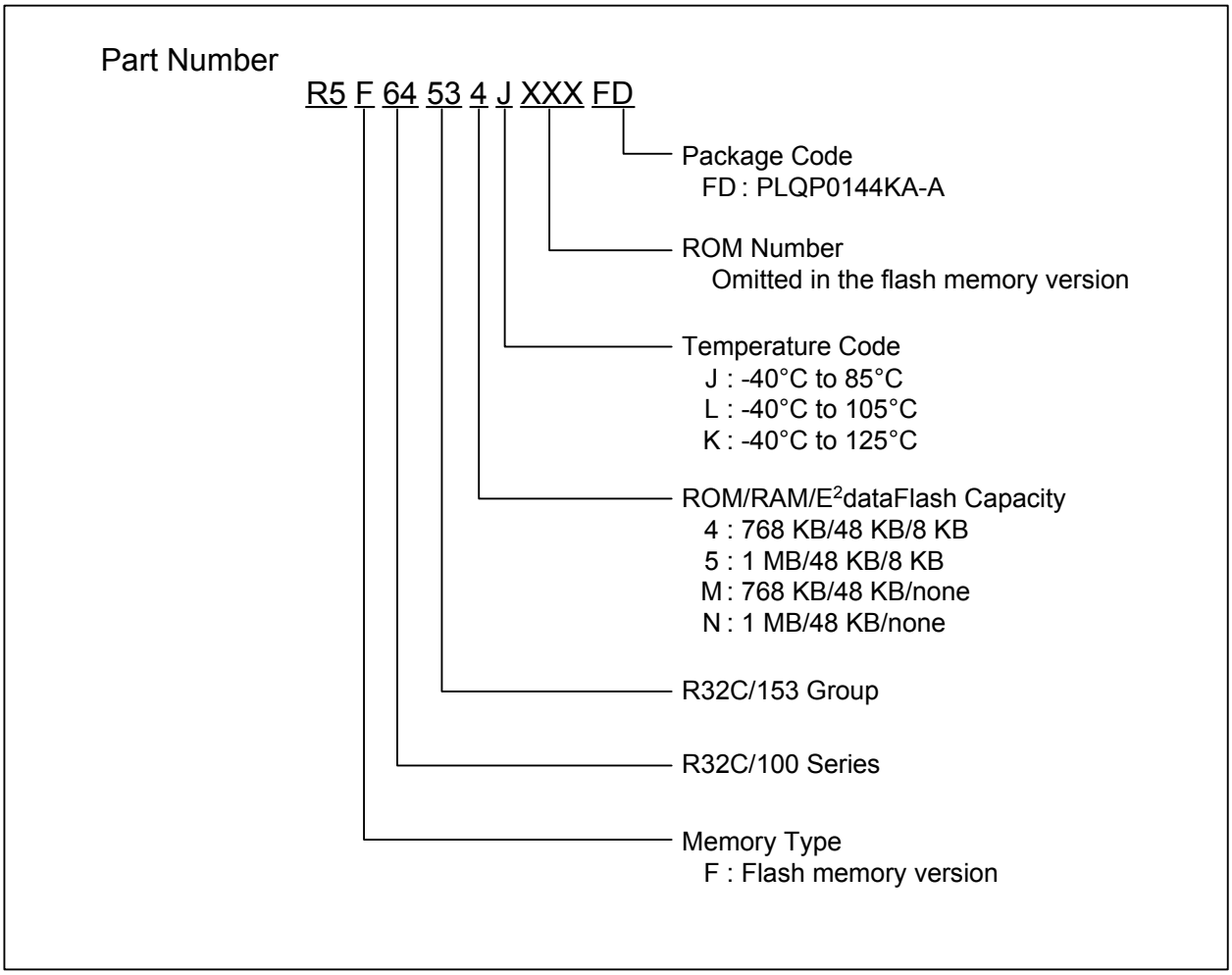


Figure 1.1 Part Numbering

1.3 Block Diagram

Figure 1.2 shows a block diagram of the R32C/153 Group.

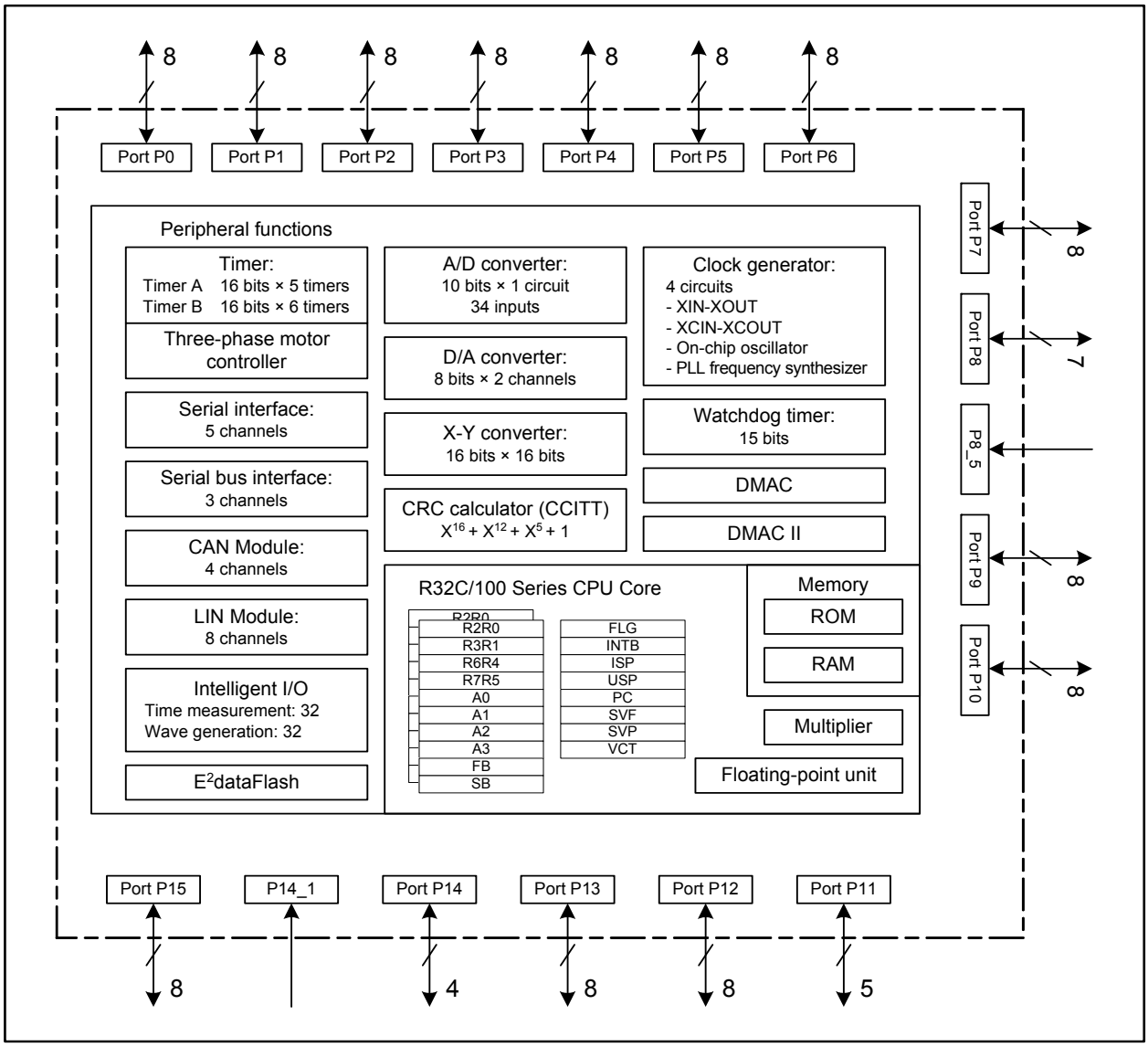
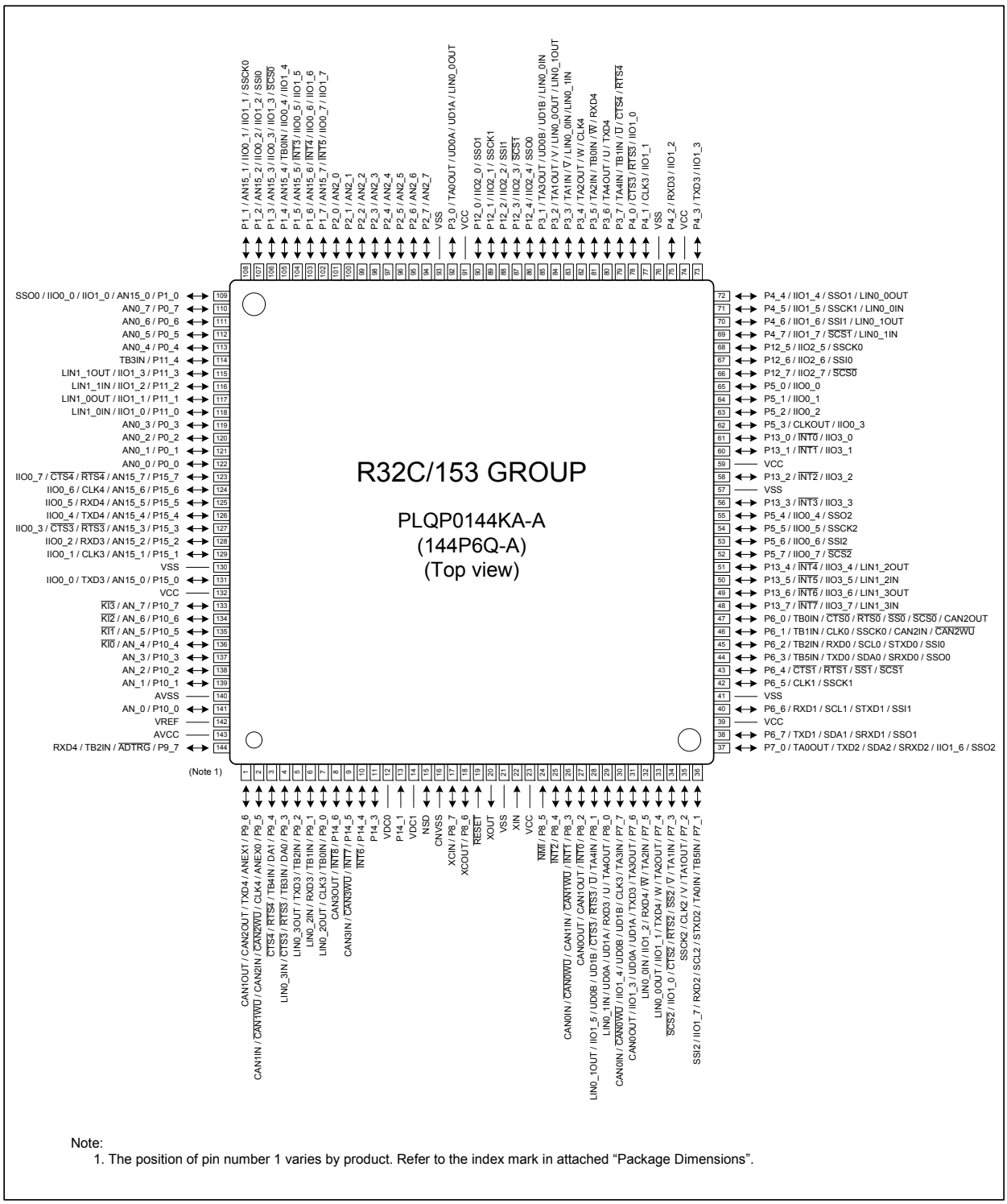


Figure 1.2 R32C/153 Group Block Diagram

1.4 Pin Assignment

Figure 1.3 shows the pin assignment (top view) and Table 1.4 to Table 1.7 show the pin characteristics.



Note:
1. The position of pin number 1 varies by product. Refer to the index mark in attached “Package Dimensions”.

Figure 1.3 Pin Assignment (top view)

Table 1.4 Pin Characteristics (1/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	LIN / CAN Module Pin	Analog Pin
1		P9_6			TXD4		CAN1OUT/ CAN2OUT	ANEX1
2		P9_5			CLK4		CAN1IN/$\overline{\text{CAN1WU}}$/ CAN2IN/$\overline{\text{CAN2WU}}$	ANEX0
3		P9_4		TB4IN	$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$			DA1
4		P9_3		TB3IN	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$		LIN0_3IN	DA0
5		P9_2		TB2IN	TXD3		LIN0_3OUT	
6		P9_1		TB1IN	RXD3		LIN0_2IN	
7		P9_0		TB0IN	CLK3		LIN0_2OUT	
8		P14_6	$\overline{\text{INT8}}$				CAN3OUT	
9		P14_5	$\overline{\text{INT7}}$				CAN3IN/$\overline{\text{CAN3WU}}$	
10		P14_4	$\overline{\text{INT6}}$					
11		P14_3						
12	VDC0							
13		P14_1						
14	VDC1							
15	NSD							
16	CNVSS							
17	XCIN	P8_7						
18	XCOUT	P8_6						
19	$\overline{\text{RESET}}$							
20	XOUT							
21	VSS							
22	XIN							
23	VCC							
24		P8_5	$\overline{\text{NMI}}$					
25		P8_4	$\overline{\text{INT2}}$					
26		P8_3	$\overline{\text{INT1}}$				CAN0IN/$\overline{\text{CAN0WU}}$/ CAN1IN/$\overline{\text{CAN1WU}}$	
27		P8_2	$\overline{\text{INT0}}$				CAN0OUT/ CAN1OUT	
28		P8_1		TA4IN/$\overline{\text{U}}$	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$	IIO1_5/UD0B/UD1B	LIN0_1OUT	
29		P8_0		TA4OUT/U	RXD3	UD0A/UD1A	LIN0_1IN	
30		P7_7		TA3IN	CLK3	IIO1_4/UD0B/UD1B	CAN0IN/$\overline{\text{CAN0WU}}$	
31		P7_6		TA3OUT	TXD3	IIO1_3/UD0A/UD1A	CAN0OUT	
32		P7_5		TA2IN/$\overline{\text{W}}$	RXD4	IIO1_2	LIN0_0IN	
33		P7_4		TA2OUT/W	TXD4	IIO1_1	LIN0_0OUT	
34		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$/ $\overline{\text{SCS2}}$	IIO1_0		
35		P7_2		TA1OUT/V	CLK2/SSCK2			
36		P7_1		TB5IN/ TA0IN	RXD2/SCL2/ STXD2/SSI2	IIO1_7		
37		P7_0		TA0OUT	TXD2/SDA2/ SRXD2/SSO2	IIO1_6		

Table 1.5 Pin Characteristics (2/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	LIN / CAN Module Pin	Analog Pin
38		P6_7			TXD1/SDA1/ SRXD1/SSO1			
39	VCC							
40		P6_6			RXD1/SCL1/ STXD1/SSI1			
41	VSS							
42		P6_5			CLK1/SSCK1			
43		P6_4			$\overline{\text{CTS1}}$/RTS1/$\overline{\text{SS1}}$/ $\overline{\text{SCS1}}$			
44		P6_3		TB5IN	TXD0/SDA0/ SRXD0/SSO0			
45		P6_2		TB2IN	RXD0/SCL0/ STXD0/SSI0			
46		P6_1		TB1IN	CLK0/SSCK0		CAN2IN/$\overline{\text{CAN2WU}}$	
47		P6_0		TB0IN	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$/ $\overline{\text{SCS0}}$		CAN2OUT	
48		P13_7	$\overline{\text{INT7}}$			IIO3_7	LIN1_3IN	
49		P13_6	$\overline{\text{INT6}}$			IIO3_6	LIN1_3OUT	
50		P13_5	$\overline{\text{INT5}}$			IIO3_5	LIN1_2IN	
51		P13_4	$\overline{\text{INT4}}$			IIO3_4	LIN1_2OUT	
52		P5_7			$\overline{\text{SCS2}}$	IIO0_7		
53		P5_6			SSI2	IIO0_6		
54		P5_5			SSCK2	IIO0_5		
55		P5_4			SSO2	IIO0_4		
56		P13_3	$\overline{\text{INT3}}$			IIO3_3		
57	VSS							
58		P13_2	$\overline{\text{INT2}}$			IIO3_2		
59	VCC							
60		P13_1	$\overline{\text{INT1}}$			IIO3_1		
61		P13_0	$\overline{\text{INT0}}$			IIO3_0		
62	CLKOUT	P5_3				IIO0_3		
63		P5_2				IIO0_2		
64		P5_1				IIO0_1		
65		P5_0				IIO0_0		
66		P12_7			$\overline{\text{SCS0}}$	IIO2_7		
67		P12_6			SSI0	IIO2_6		
68		P12_5			SSCK0	IIO2_5		
69		P4_7			$\overline{\text{SCS1}}$	IIO1_7	LIN0_1IN	
70		P4_6			SSI1	IIO1_6	LIN0_1OUT	
71		P4_5			SSCK1	IIO1_5	LIN0_0IN	
72		P4_4			SSO1	IIO1_4	LIN0_0OUT	

Table 1.6 Pin Characteristics (3/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	LIN / CAN Module Pin	Analog Pin
73		P4_3			TXD3	IIO1_3		
74	VCC							
75		P4_2			RXD3	IIO1_2		
76	VSS							
77		P4_1			CLK3	IIO1_1		
78		P4_0			$\overline{CTS3}/\overline{RTS3}$	IIO1_0		
79		P3_7		TB1IN/ TA4IN/$\overline{U}$	$\overline{CTS4}/\overline{RTS4}$			
80		P3_6		TA4OUT/U	TXD4			
81		P3_5		TB0IN/ TA2IN/$\overline{W}$	RXD4			
82		P3_4		TA2OUT/W	CLK4			
83		P3_3		TA1IN/$\overline{V}$			LIN0_0IN/LIN0_1IN	
84		P3_2		TA1OUT/V			LIN0_0OUT/ LIN0_1OUT	
85		P3_1		TA3OUT		UD0B/UD1B	LIN0_0IN	
86		P12_4			SSO0	IIO2_4		
87		P12_3			$\overline{SCS1}$	IIO2_3		
88		P12_2			SSI1	IIO2_2		
89		P12_1			SSCK1	IIO2_1		
90		P12_0			SSO1	IIO2_0		
91	VCC							
92		P3_0		TA0OUT		UD0A/UD1A	LIN0_0OUT	
93	VSS							
94		P2_7						AN2_7
95		P2_6						AN2_6
96		P2_5						AN2_5
97		P2_4						AN2_4
98		P2_3						AN2_3
99		P2_2						AN2_2
100		P2_1						AN2_1
101		P2_0						AN2_0
102		P1_7	$\overline{INT5}$			IIO0_7/IIO1_7		AN15_7
103		P1_6	$\overline{INT4}$			IIO0_6/IIO1_6		AN15_6
104		P1_5	$\overline{INT3}$			IIO0_5/IIO1_5		AN15_5
105		P1_4		TB0IN		IIO0_4/IIO1_4		AN15_4
106		P1_3			$\overline{SCS0}$	IIO0_3/IIO1_3		AN15_3
107		P1_2			SSI0	IIO0_2/IIO1_2		AN15_2
108		P1_1			SSCK0	IIO0_1/IIO1_1		AN15_1

Table 1.7 Pin Characteristics (4/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	LIN / CAN Module Pin	Analog Pin
109		P1_0			SSO0	IIO0_0/IIO1_0		AN15_0
110		P0_7						AN0_7
111		P0_6						AN0_6
112		P0_5						AN0_5
113		P0_4						AN0_4
114		P11_4		TB3IN				
115		P11_3				IIO1_3	LIN1_1OUT	
116		P11_2				IIO1_2	LIN1_1IN	
117		P11_1				IIO1_1	LIN1_0OUT	
118		P11_0				IIO1_0	LIN1_0IN	
119		P0_3						AN0_3
120		P0_2						AN0_2
121		P0_1						AN0_1
122		P0_0						AN0_0
123		P15_7			$\overline{CTS4}$/$\overline{RTS4}$	IIO0_7		AN15_7
124		P15_6			CLK4	IIO0_6		AN15_6
125		P15_5			RXD4	IIO0_5		AN15_5
126		P15_4			TXD4	IIO0_4		AN15_4
127		P15_3			$\overline{CTS3}$/$\overline{RTS3}$	IIO0_3		AN15_3
128		P15_2			RXD3	IIO0_2		AN15_2
129		P15_1			CLK3	IIO0_1		AN15_1
130	VSS							
131		P15_0			TXD3	IIO0_0		AN15_0
132	VCC							
133		P10_7	$\overline{KI3}$					AN_7
134		P10_6	$\overline{KI2}$					AN_6
135		P10_5	$\overline{KI1}$					AN_5
136		P10_4	$\overline{KI0}$					AN_4
137		P10_3						AN_3
138		P10_2						AN_2
139		P10_1						AN_1
140	AVSS							
141		P10_0						AN_0
142	VREF							
143	AVCC							
144		P9_7		TB2IN	RXD4			$\overline{ADTRG}$

1.5 Pin Definitions and Functions

Table 1.8 to Table 1.10 show the pin definitions and functions.

Table 1.8 Pin Definitions and Functions (1/3)

Function	Symbol	I/O	Description
Power supply	VCC, VSS	I	Applicable as follows: VCC = 3.0 to 5.5 V, VSS = 0 V
Analog power supply	AVCC, AVSS	I	Power supply for the A/D converter. AVCC and AVSS should be connected to VCC and VSS, respectively
Connecting pins for decoupling capacitor	VDC0, VDC1	—	A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1
Reset input	$\overline{\text{RESET}}$	I	The MCU is reset when this pin is driven low
CNVSS	CNVSS	I	This pin should be connected to VSS via a resistor
Debug port	NSD	I/O	This pin is to communicate with a debugger. It should be connected to VCC via a resistor of 1 to 4.7 kΩ
Main clock input	XIN	I	Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open
Main clock output	XOUT	O	
Sub clock input	XCIN	I	Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOUT. An external clock should be input at the XCIN while leaving the XCOUT open
Sub clock output	XCOUT	O	
Clock output	CLKOUT	O	Output of the clock with the same frequency as low speed clocks, f8, or f32
External interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT8}}$	I	Input for external interrupts
NMI input	P8_5/$\overline{\text{NMI}}$	I	Input for NMI
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input for the key input interrupt

Table 1.9 Pin Definitions and Functions (2/3)

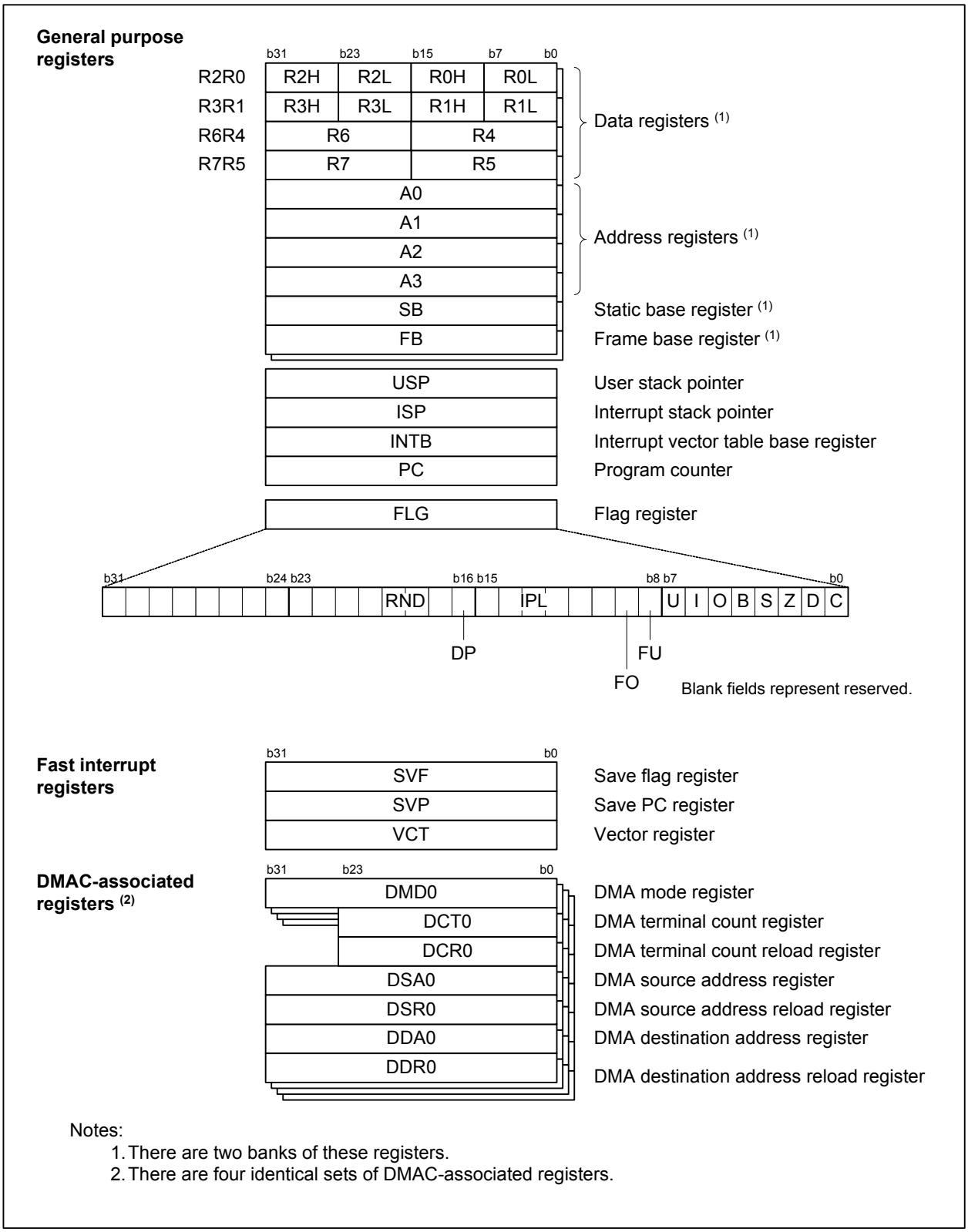
Function	Symbol	I/O	Description
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7	I/O	I/O ports in CMOS. Each port can be programmed to input or output under the control of the direction register. Pull-up resistors are selected for following 4-pin units, but are enabled only for the input pins: Pi_0 to Pi_3 and Pi_4 to Pi_7 (i = 0 to 15)
Input port	P14_1	I	Input port in CMOS. Pull-up resistors are selectable for P14_1 and P14_3
Timer A	TA0OUT to TA4OUT	I/O	Timers A0 to A4 input/output
	TA0IN to TA4IN	I	Timers A0 to A4 input
Timer B	TB0IN to TB5IN	I	Timers B0 to B5 input
Three-phase motor control timer output	U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$	O	Three-phase motor control timer output
Serial interface	$\overline{CTS0}$ to $\overline{CTS4}$	I	Handshake input
	$\overline{RTS0}$ to $\overline{RTS4}$	O	Handshake output
	CLK0 to CLK4	I/O	Transmit/receive clock input/output
	RXD0 to RXD4	I	Serial data input
	TXD0 to TXD4	O	Serial data output
I^2C bus (simplified)	SDA0 to SDA2	I/O	Serial data input/output
	SCL0 to SCL2	I/O	Transmit/receive clock input/output
Serial interface special functions	STXD0 to STXD2	O	Serial data output in slave mode
	SRXD0 to SRXD2	I	Serial data input in slave mode
	$\overline{SS0}$ to $\overline{SS2}$	I	Input to control serial interface special functions

Table 1.10 Pin Definitions and Functions (3/3)

Function	Symbol	I/O	Description
A/D converter	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7	I	Analog input for the A/D converter
	$\overline{\text{ADTRG}}$	I	External trigger input for the A/D converter
	ANEX0	I/O	Expanded analog input for the A/D converter and output in external op-amp connection mode
	ANEX1	I	Expanded analog input for the A/D converter
D/A converter	DA0, DA1	O	Output for the D/A converter
Reference voltage input	VREF	I	Reference voltage input for the A/D converter and D/A converter
Intelligent I/O	IIO0_0 to IIO0_7	I/O	Input/output for the Intelligent I/O group 0. Either input capture or output compare is selectable
	IIO1_0 to IIO1_7	I/O	Input/output for the Intelligent I/O group 1. Either input capture or output compare is selectable
	IIO2_0 to IIO2_7	I/O	Input/output for the Intelligent I/O group 2. Either input capture or output compare is selectable
	IIO3_0 to IIO3_7	I/O	Input/output for the Intelligent I/O group 3. Either input capture or output compare is selectable
	UD0A, UD1A, UD0B, UD1B	I	Input for the two-phase encoder
Serial bus interface	SSO0 to SSO2	I/O	Serial data output. Functions as serial data input/output in 4-wire serial bus mode
	SSI0 to SSI2	I/O	Serial data input. Functions as serial data input/output in 4-wire serial bus mode
	SSCK0 to SSCK2	I/O	Transmit/receive clock input/output
	$\overline{\text{SCS0}}$ to $\overline{\text{SCS2}}$	I/O	Input/output to control the synchronous serial interface
LIN module	LIN0_0OUT to LIN0_3OUT	O	Transmit data output for the LIN communications
	LIN0_0IN to LIN0_3IN	I	Receive data input for the LIN communications
	LIN1_0OUT to LIN1_3OUT	O	Transmit data output for the LIN communications
	LIN1_0IN to LIN1_3IN	I	Receive data input for the LIN communications
CAN module	CAN0IN to CAN3IN	I	Receive data input for the CAN communications
	CAN0OUT to CAN3OUT	O	Transmit data output for the CAN communications
	$\overline{\text{CAN0WU}}$ to $\overline{\text{CAN3WU}}$	I	Input for the CAN wake-up interrupt

2. Central Processing Unit (CPU)

The CPU contains registers as shown below. There are two register banks each consisting of registers R2R0, R3R1, R6R4, R7R5, A0 to A3, SB, and FB.



Notes:
1. There are two banks of these registers.
2. There are four identical sets of DMAC-associated registers.

Figure 2.1 CPU Registers

2.1 General Purpose Registers

2.1.1 Data Registers (R2R0, R3R1, R6R4, and R7R5)

These 32-bit registers are primarily used for transfers and arithmetic/logic operations.
Each of the registers can be divided into upper and lower 16-bit registers, e.g. R2R0 can be divided into R2 and R0, R3R0 can be divided into R3 and R1, etc.
Moreover, data registers R2R0 and R3R1 can be divided into four 8-bit data registers: upper (R2H and R3H), mid-upper (R2L and R3L), mid-lower (R0H and R1H), and lower (R0L and R1L).

2.1.2 Address Registers (A0, A1, A2, and A3)

These 32-bit registers have functions similar to data registers. They are also used for address register indirect addressing and address register relative addressing.

2.1.3 Static Base Register (SB)

This 32-bit register is used for SB relative addressing.

2.1.4 Frame Base Register (FB)

This 32-bit register is used for FB relative addressing.

2.1.5 Program Counter (PC)

This 32-bit counter indicates the address of the instruction to be executed next.

2.1.6 Interrupt Vector Table Base Register (INTB)

This 32-bit register indicates the start address of a relocatable vector table.

2.1.7 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Two types of 32-bit stack pointers (SPs) are provided: user stack pointer (USP) and interrupt stack pointer (ISP).
Use the stack pointer select flag (U flag) to select either the user stack pointer (USP) or the interrupt stack pointer (ISP). The U flag is bit 7 in the flag register (FLG). Refer to 2.1.8 “Flag Register (FLG)” for details.
To minimize the overhead of interrupt sequence due to less memory access, set the user stack pointer (USP) or the interrupt stack pointer (ISP) to a multiple of 4.

2.1.8 Flag Register (FLG)

This 32-bit register indicates the CPU status.

2.1.8.1 Carry Flag (C flag)

This flag becomes 1 when any of the carry, borrow, shifted-out bit, etc. is generated in the arithmetic logic unit (ALU).

2.1.8.2 Debug Flag (D flag)

This flag is only for debugging. Only set this bit to 0.

2.1.8.3 Zero Flag (Z flag)

This flag becomes 1 when the result of an operation is 0; otherwise it is 0.

2.1.8.4 Sign Flag (S flag)

This flag becomes 1 when the result of an operation is a negative value; otherwise it is 0.

2.1.8.5 Register Bank Select Flag (B flag)

This flag selects a register bank. It indicates 0 when the register bank 0 is selected, and 1 when the register bank 1 is selected.

2.1.8.6 Overflow Flag (O flag)

This flag becomes 1 if an overflow occurs in an operation; otherwise it is 0.

2.1.8.7 Interrupt Enable Flag (I flag)

This flag enables maskable interrupts. To disable maskable interrupts, set this flag to 0. To enable them, set this flag to 1. When an interrupt is accepted, the flag becomes 0.

2.1.8.8 Stack Pointer Select Flag (U flag)

To select the interrupt stack pointer (ISP), set this flag to 0. To select the user stack pointer (USP), set this flag to 1.
It becomes 0 when a hardware interrupts is accepted or when an INT instruction designated by a software interrupt number from 0 to 127 is executed.

2.1.8.9 Floating-point Underflow Flag (FU flag)

This flag becomes 1 when an underflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand has invalid numbers (subnormal numbers).

2.1.8.10 Floating-point Overflow Flag (FO flag)

This flag becomes 1 when an overflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand has invalid numbers (subnormal numbers).

2.1.8.11 Processor Interrupt Priority Level (IPL)

The processor interrupt priority level (IPL), consisting of three bits, selects a processor interrupt priority level from level 0 to 7. An interrupt is acceptable when the interrupt request level is higher than the selected IPL.
When the processor interrupt priority level (IPL) is set to 111b (level 7), all interrupts are disabled.

2.1.8.12 Fixed-point Radix Point Designation Bit (DP bit)

This bit designates the radix point. It also specifies which portion of the fixed-point multiplication result to take. It is used in the MULX instruction.

2.1.8.13 Floating-point Rounding Mode (RND)

The 2-bit floating-point rounding mode selects a rounding mode for floating-point calculation results.

2.1.8.14 Reserved

Only set this bit to 0. The read value is undefined.

2.2 Fast Interrupt Registers

The following three registers are provided to minimize the overhead of interrupt sequence.

2.2.1 Save Flag Register (SVF)

This 32-bit register is used to save the flag register when a fast interrupt is generated.

2.2.2 Save PC Register (SVP)

This 32-bit register is used to save the program counter when a fast interrupt is generated.

2.2.3 Vector Register (VCT)

This 32-bit register is used to indicate a jump address when a fast interrupt is generated.

2.3 DMAC-associated Registers

There are seven types of DMAC-associated registers.

2.3.1 DMA Mode Registers (DMD0, DMD1, DMD2, and DMD3)

These 32-bit registers are used to set DMA transfer mode, bit rate, etc.

2.3.2 DMA Terminal Count Registers (DCT0, DCT1, DCT2, and DCT3)

These 24-bit registers are used to set DMA transfer counting.

2.3.3 DMA Terminal Count Reload Registers (DCR0, DCR1, DCR2, and DCR3)

These 24-bit registers are used to set the reloaded values for DMA terminal count registers.

2.3.4 DMA Source Address Registers (DSA0, DSA1, DSA2, and DSA3)

These 32-bit registers are used to set DMA source addresses.

2.3.5 DMA Source Address Reload Registers (DSR0, DSR1, DSR2, and DSR3)

These 32-bit registers are used to set the reloaded value for DMA source address register.

2.3.6 DMA Destination Address Registers (DDA0, DDA1, DDA2, and DDA3)

These 32-bit registers are used to set DMA destination address.

2.3.7 DMA Destination Address Reload Registers (DDR0, DDR1, DDR2, and DDR3)

These 32-bit registers are used to set reloaded values for DMA destination address registers.

3. Memory

Figure 3.1 shows the memory map of the R32C/153 Group.
The R32C/153 Group provides a 4-Gbyte address space from 00000000h to FFFFFFFFh.

The internal ROM is mapped to the end of the memory map with the ending address fixed at FFFFFFFFh. Therefore, the 1-Mbyte internal ROM is mapped from FFF00000h to FFFFFFFFh.
The fixed interrupt vector table which contains each start address of interrupt handlers is mapped from FFFFFFDCh to FFFFFFFFh.
The internal RAM is mapped to the beginning of the memory map with the starting address fixed at 00000400h. Therefore, the 48-Kbyte internal RAM is mapped from 00000400h to 0000C3FFh. Besides being used for data storage, the internal RAM functions as a stack(s) for subroutines and/or interrupt handlers.

Special Function Registers (SFRs), which are control registers for peripheral functions, are mapped from 00000000h to 000003FFh, and from 00040000h to 0004FFFFh. Unoccupied SFR locations are reserved. No access is allowed.

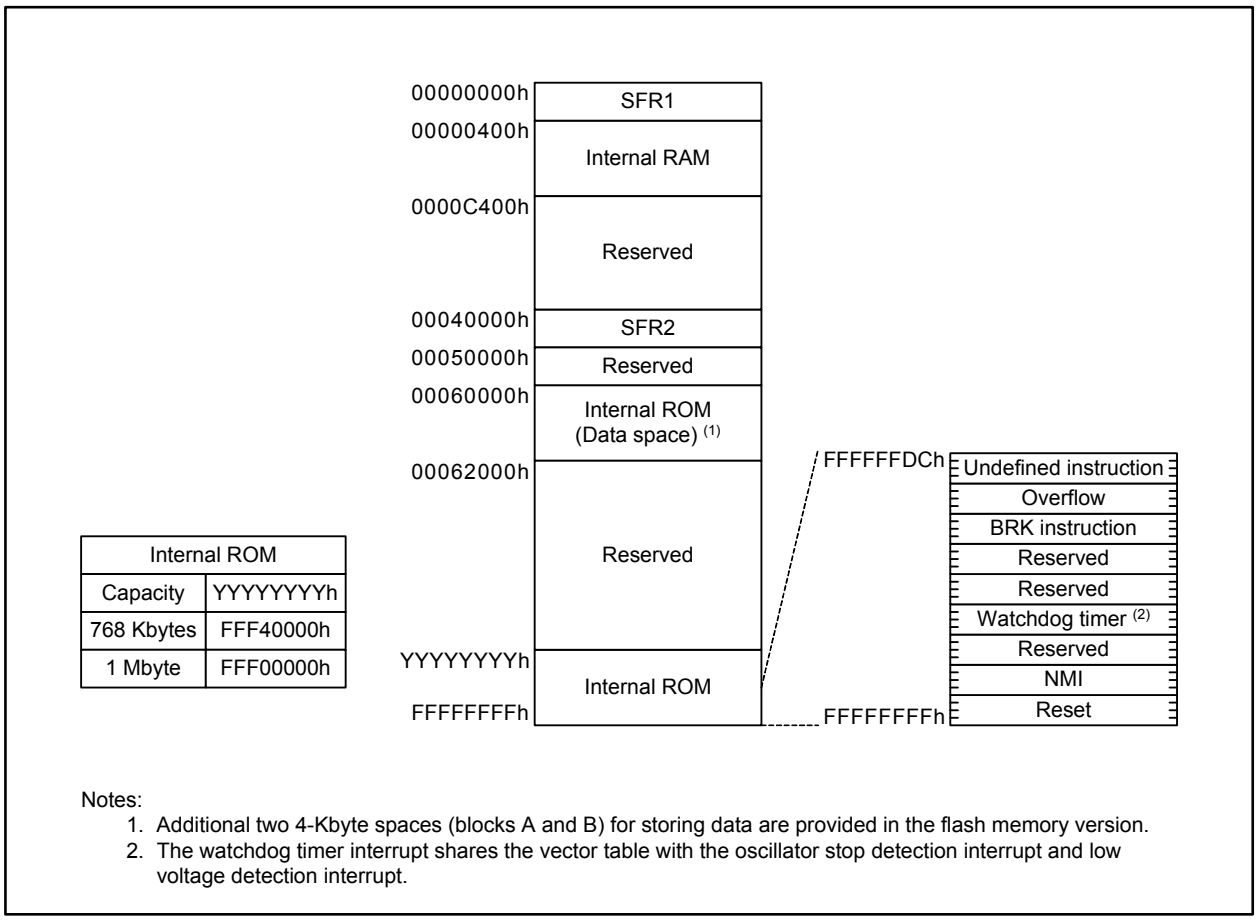


Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

SFRs are memory-mapped peripheral registers that control the operation of peripherals. Table 4.1 SFR List (1) to Table 4.87 SFR List (87) list the SFR details.

Table 4.1 SFR List (1)

Address	Register	Symbol	Reset Value
000000h			
000001h			
000002h			
000003h			
000004h	Clock Control Register	CCR	0001 1000b
000005h			
000006h	Flash Memory Control Register	FMCR	0000 0001b
000007h	Protect Release Register	PRR	00h
000008h			
000009h			
00000Ah			
00000Bh			
00000Ch			
00000Dh			
00000Eh			
00000Fh			
000010h			
000011h			
000012h			
000013h			
000014h			
000015h			
000016h			
000017h			
000018h			
000019h			
00001Ah			
00001Bh			
00001Ch	Flash Memory Rewrite Bus Control Register	FEBC	0000h
00001Dh			
00001Eh	Peripheral Bus Control Register	PBC	0504h
00001Fh			
000020h to 00005Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.2 SFR List (2)

Address	Register	Symbol	Reset Value
000060h			
000061h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
000062h			
000063h	UART2 Receive/ACK Interrupt Control Register	S2RIC	XXXX X000b
000064h			
000065h			
000066h			
000067h			
000068h	DMA0 Transfer Complete Interrupt Control Register	DM0IC	XXXX X000b
000069h	UART0 Start Condition/Stop Condition Detection Interrupt Control Register	BCN0IC	XXXX X000b
00006Ah	DMA2 Transfer Complete Interrupt Control Register	DM2IC	XXXX X000b
00006Bh	A/D Converter 0 Convert Completion Interrupt Control Register	AD0IC	XXXX X000b
00006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
00006Dh	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X000b
00006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
00006Fh	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X000b
000070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
000071h	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000b
000072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
000073h	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X000b
000074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
000075h	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X000b
000076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
000077h	Intelligent I/O Interrupt Control Register 10	IIO10IC	XXXX X000b
000078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
000079h			
00007Ah	INT5 Interrupt Control Register	INT5IC	XX00 X000b
00007Bh	CAN0 Wake-up Interrupt Control Register	C0WIC	XXXX X000b
00007Ch	INT3 Interrupt Control Register	INT3IC	XX00 X000b
00007Dh	CAN2 Wake-up Interrupt Control Register	C2WIC	XXXX X000b
00007Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
00007Fh	LIN0 Low Detection Interrupt Control Register	L0LDIC	XXXX X000b
000080h			
000081h	UART2 Transmit/NACK Interrupt Control Register	S2TIC	XXXX X000b
000082h			
000083h			
000084h			
000085h			
000086h			
000087h	UART2 Start Condition/Stop Condition Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.3 SFR List (3)

Address	Register	Symbol	Reset Value
000088h	DMA1 Transfer Complete Interrupt Control Register	DM1IC	XXXX X000b
000089h	UART1 Start Condition/Stop Condition Detection Interrupt Control Register	BCN1IC	XXXX X000b
00008Ah	DMA3 Transfer Complete Interrupt Control Register	DM3IC	XXXX X000b
00008Bh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
00008Ch	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
00008Dh	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X000b
00008Eh	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
00008Fh	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X000b
000090h	UART0 Transmit/NACK Interrupt Control Register	S0TIC	XXXX X000b
000091h	Intelligent I/O Interrupt Control Register 5	IIO5IC	XXXX X000b
000092h	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000b
000093h	Intelligent I/O Interrupt Control Register 7	IIO7IC	XXXX X000b
000094h	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
000095h	Intelligent I/O Interrupt Control Register 9	IIO9IC	XXXX X000b
000096h	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
000097h	Intelligent I/O Interrupt Control Register 11	IIO11IC	XXXX X000b
000098h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
000099h			
00009Ah	INT4 Interrupt Control Register	INT4IC	XX00 X000b
00009Bh	CAN1 Wake-up Interrupt Control Register	C1WIC	XXXX X000b
00009Ch	INT2 Interrupt Control Register	INT2IC	XX00 X000b
00009Dh	CAN3 Wake-up Interrupt Control Register	C3WIC	XXXX X000b
00009Eh	INT0 Interrupt Control Register	INT0IC	XX00 X000b
00009Fh	LIN1 Low Detection Interrupt Control Register	L1LDIC	XXXX X000b
0000A0h	Intelligent I/O Interrupt Request Register 0	IIO0IR	0000 0XX1b
0000A1h	Intelligent I/O Interrupt Request Register 1	IIO1IR	0000 0XX1b
0000A2h	Intelligent I/O Interrupt Request Register 2	IIO2IR	0000 0X01b
0000A3h	Intelligent I/O Interrupt Request Register 3	IIO3IR	0000 XXX1b
0000A4h	Intelligent I/O Interrupt Request Register 4	IIO4IR	000X XXX1b
0000A5h	Intelligent I/O Interrupt Request Register 5	IIO5IR	0000 XXX1b
0000A6h	Intelligent I/O Interrupt Request Register 6	IIO6IR	0000 XXX1b
0000A7h	Intelligent I/O Interrupt Request Register 7	IIO7IR	000X XXX1b
0000A8h	Intelligent I/O Interrupt Request Register 8	IIO8IR	000X XXX1b
0000A9h	Intelligent I/O Interrupt Request Register 9	IIO9IR	0X00 XXX1b
0000AAh	Intelligent I/O Interrupt Request Register 10	IIO10IR	0X00 XXX1b
0000ABh	Intelligent I/O Interrupt Request Register 11	IIO11IR	0X0X XXX1b
0000ACh			
0000ADh			
0000AEh			
0000AFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.4 SFR List (4)

Address	Register	Symbol	Reset Value
0000B0h	Intelligent I/O Interrupt Enable Register 0	IIO0IE	00h
0000B1h	Intelligent I/O Interrupt Enable Register 1	IIO1IE	00h
0000B2h	Intelligent I/O Interrupt Enable Register 2	IIO2IE	00h
0000B3h	Intelligent I/O Interrupt Enable Register 3	IIO3IE	00h
0000B4h	Intelligent I/O Interrupt Enable Register 4	IIO4IE	00h
0000B5h	Intelligent I/O Interrupt Enable Register 5	IIO5IE	00h
0000B6h	Intelligent I/O Interrupt Enable Register 6	IIO6IE	00h
0000B7h	Intelligent I/O Interrupt Enable Register 7	IIO7IE	00h
0000B8h	Intelligent I/O Interrupt Enable Register 8	IIO8IE	00h
0000B9h	Intelligent I/O Interrupt Enable Register 9	IIO9IE	00h
0000BAh	Intelligent I/O Interrupt Enable Register 10	IIO10IE	00h
0000BBh	Intelligent I/O Interrupt Enable Register 11	IIO11IE	00h
0000BCh			
0000BDh			
0000BEh			
0000BFh			
0000C0h	Serial Bus Interface 0 Interrupt Control Register	SS0IC	XXXX X000b
0000C1h	CAN0 Transmit Interrupt Control Register	C0TIC	XXXX X000b
0000C2h	Serial Bus Interface 2 Interrupt Control Register	SS2IC	XXXX X000b
0000C3h	CAN0 Error Interrupt Control Register	C0EIC	XXXX X000b
0000C4h			
0000C5h	CAN1 Receive Interrupt Control Register	C1RIC	XXXX X000b
0000C6h			
0000C7h	CAN2 Transmit Interrupt Control Register	C2TIC	XXXX X000b
0000C8h			
0000C9h	CAN2 Error Interrupt Control Register	C2EIC	XXXX X000b
0000CAh			
0000CBh	CAN3 Receive Interrupt Control Register	C3RIC	XXXX X000b
0000CCh			
0000CDh			
0000CEh			
0000CFh			
0000D0h	CAN0 Transmit FIFO Interrupt Control Register	C0FTIC	XXXX X000b
0000D1h			
0000D2h	CAN1 Transmit FIFO Interrupt Control Register	C1FTIC	XXXX X000b
0000D3h			
0000D4h	CAN2 Transmit FIFO Interrupt Control Register	C2FTIC	XXXX X000b
0000D5h	LIN0_0 Interrupt Control Register	L0_0IC	XXXX X000b
0000D6h	CAN3 Transmit FIFO Interrupt Control Register	C3FTIC	XXXX X000b
0000D7h	LIN0_2 Interrupt Control Register	L0_2IC	XXXX X000b
0000D8h	E^2dataFlash Interrupt Control Register	E2FIC	XXXX X000b
0000D9h	LIN1_0 Interrupt Control Register	L1_0IC	XXXX X000b
0000DAh			
0000DBh	LIN1_2 Interrupt Control Register	L1_2IC	XXXX X000b
0000DCh			
0000DDh	UART3 Transmit Interrupt Control Register	S3TIC	XXXX X000b
0000DEh	INT7 Interrupt Control Register	INT7IC	XX00 X000b
0000DFh	UART4 Transmit Interrupt Control Register	S4TIC	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.5 SFR List (5)

Address	Register	Symbol	Reset Value
0000E0h	Serial Bus Interface 1 Interrupt Control Register	SS1IC	XXXX X000b
0000E1h	CAN0 Receive Interrupt Control Register	C0RIC	XXXX X000b
0000E2h			
0000E3h	CAN1 Transmit Interrupt Control Register	C1TIC	XXXX X000b
0000E4h			
0000E5h	CAN1 Error Interrupt Control Register	C1EIC	XXXX X000b
0000E6h			
0000E7h	CAN2 Receive Interrupt Control Register	C2RIC	XXXX X000b
0000E8h			
0000E9h	CAN3 Transmit Interrupt Control Register	C3TIC	XXXX X000b
0000EAh			
0000EBh	CAN3 Error Interrupt Control Register	C3EIC	XXXX X000b
0000ECh			
0000EDh			
0000EEh			
0000EFh			
0000F0h	CAN0 Receive FIFO Interrupt Control Register	C0FRIC	XXXX X000b
0000F1h			
0000F2h	CAN1 Receive FIFO Interrupt Control Register	C1FRIC	XXXX X000b
0000F3h			
0000F4h	CAN2 Receive FIFO Interrupt Control Register	C2FRIC	XXXX X000b
0000F5h	LIN0_1 Interrupt Control Register	L0_1IC	XXXX X000b
0000F6h	CAN3 Receive FIFO Interrupt Control Register	C3FRIC	XXXX X000b
0000F7h	LIN0_3 Interrupt Control Register	L0_3IC	XXXX X000b
0000F8h			
0000F9h	LIN1_1 Interrupt Control Register	L1_1IC	XXXX X000b
0000FAh			
0000FBh	LIN1_3 Interrupt Control Register	L1_3IC	XXXX X000b
0000FCh	INT8 Interrupt Control Register	INT8IC	XX00 X000b
0000FDh	UART3 Receive Interrupt Control Register	S3RIC	XXXX X000b
0000FEh	INT6 Interrupt Control Register	INT6IC	XX00 X000b
0000FFh	UART4 Receive Interrupt Control Register	S4RIC	XXXX X000b
000100h	Group 1 Time Measurement/Waveform Generation Register 0	G1TM0/G1PO0	XXXXh
000101h			
000102h	Group 1 Time Measurement/Waveform Generation Register 1	G1TM1/G1PO1	XXXXh
000103h			
000104h	Group 1 Time Measurement/Waveform Generation Register 2	G1TM2/G1PO2	XXXXh
000105h			
000106h	Group 1 Time Measurement/Waveform Generation Register 3	G1TM3/G1PO3	XXXXh
000107h			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.6 SFR List (6)

Address	Register	Symbol	Reset Value
000108h	Group 1 Time Measurement/Waveform Generation Register 4	G1TM4/G1PO4	XXXXh
000109h			
00010Ah	Group 1 Time Measurement/Waveform Generation Register 5	G1TM5/G1PO5	XXXXh
00010Bh			
00010Ch	Group 1 Time Measurement/Waveform Generation Register 6	G1TM6/G1PO6	XXXXh
00010Dh			
00010Eh	Group 1 Time Measurement/Waveform Generation Register 7	G1TM7/G1PO7	XXXXh
00010Fh			
000110h	Group 1 Waveform Generation Control Register 0	G1POCR0	0000 X000b
000111h	Group 1 Waveform Generation Control Register 1	G1POCR1	0X00 X000b
000112h	Group 1 Waveform Generation Control Register 2	G1POCR2	0X00 X000b
000113h	Group 1 Waveform Generation Control Register 3	G1POCR3	0X00 X000b
000114h	Group 1 Waveform Generation Control Register 4	G1POCR4	0X00 X000b
000115h	Group 1 Waveform Generation Control Register 5	G1POCR5	0X00 X000b
000116h	Group 1 Waveform Generation Control Register 6	G1POCR6	0X00 X000b
000117h	Group 1 Waveform Generation Control Register 7	G1POCR7	0X00 X000b
000118h	Group 1 Time Measurement Control Register 0	G1TMCR0	00h
000119h	Group 1 Time Measurement Control Register 1	G1TMCR1	00h
00011Ah	Group 1 Time Measurement Control Register 2	G1TMCR2	00h
00011Bh	Group 1 Time Measurement Control Register 3	G1TMCR3	00h
00011Ch	Group 1 Time Measurement Control Register 4	G1TMCR4	00h
00011Dh	Group 1 Time Measurement Control Register 5	G1TMCR5	00h
00011Eh	Group 1 Time Measurement Control Register 6	G1TMCR6	00h
00011Fh	Group 1 Time Measurement Control Register 7	G1TMCR7	00h
000120h	Group 1 Base Timer Register	G1BT	XXXXh
000121h			
000122h	Group 1 Base Timer Control Register 0	G1BCR0	00h
000123h	Group 1 Base Timer Control Register 1	G1BCR1	0000 0000b
000124h	Group 1 Time Measurement Prescaler Register 6	G1TPR6	00h
000125h	Group 1 Time Measurement Prescaler Register 7	G1TPR7	00h
000126h	Group 1 Function Enable Register	G1FE	00h
000127h	Group 1 Function Select Register	G1FS	00h
000128h			
000129h			
00012Ah			
00012Bh			
00012Ch			
00012Dh			
00012Eh			
00012Fh			
000130h to 00013Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.7 SFR List (7)

Address	Register	Symbol	Reset Value
000140h	Group 2 Time Measurement/Waveform Generation Register 0	G2TM0/G2PO0	XXXXh
000141h			
000142h	Group 2 Time Measurement/Waveform Generation Register 1	G2TM1/G2PO1	XXXXh
000143h			
000144h	Group 2 Time Measurement/Waveform Generation Register 2	G2TM2/G2PO2	XXXXh
000145h			
000146h	Group 2 Time Measurement/Waveform Generation Register 3	G2TM3/G2PO3	XXXXh
000147h			
000148h	Group 2 Time Measurement/Waveform Generation Register 4	G2TM4/G2PO4	XXXXh
000149h			
00014Ah	Group 2 Time Measurement/Waveform Generation Register 5	G2TM5/G2PO5	XXXXh
00014Bh			
00014Ch	Group 2 Time Measurement/Waveform Generation Register 6	G2TM6/G2PO6	XXXXh
00014Dh			
00014Eh	Group 2 Time Measurement/Waveform Generation Register 7	G2TM7/G2PO7	XXXXh
00014Fh			
000150h	Group 2 Waveform Generation Control Register 0	G2POCR0	0000 X000b
000151h	Group 2 Waveform Generation Control Register 1	G2POCR1	0X00 X000b
000152h	Group 2 Waveform Generation Control Register 2	G2POCR2	0X00 X000b
000153h	Group 2 Waveform Generation Control Register 3	G2POCR3	0X00 X000b
000154h	Group 2 Waveform Generation Control Register 4	G2POCR4	0X00 X000b
000155h	Group 2 Waveform Generation Control Register 5	G2POCR5	0X00 X000b
000156h	Group 2 Waveform Generation Control Register 6	G2POCR6	0X00 X000b
000157h	Group 2 Waveform Generation Control Register 7	G2POCR7	0X00 X000b
000158h	Group 2 Time Measurement Control Register 0	G2TMCR0	00h
000159h	Group 2 Time Measurement Control Register 1	G2TMCR1	00h
00015Ah	Group 2 Time Measurement Control Register 2	G2TMCR2	00h
00015Bh	Group 2 Time Measurement Control Register 3	G2TMCR3	00h
00015Ch	Group 2 Time Measurement Control Register 4	G2TMCR4	00h
00015Dh	Group 2 Time Measurement Control Register 5	G2TMCR5	00h
00015Eh	Group 2 Time Measurement Control Register 6	G2TMCR6	00h
00015Fh	Group 2 Time Measurement Control Register 7	G2TMCR7	00h
000160h	Group 2 Base Timer Register	G2BT	XXXXh
000161h			
000162h	Group 2 Base Timer Control Register 0	G2BCR0	00h
000163h	Group 2 Base Timer Control Register 1	G2BCR1	0000 0000b
000164h	Group 2 Time Measurement Prescaler Register 6	G2TPR6	00h
000165h	Group 2 Time Measurement Prescaler Register 7	G2TPR7	00h
000166h	Group 2 Function Enable Register	G2FE	00h
000167h	Group 2 Function Select Register	G2FS	00h
000168h			
000169h			
00016Ah			
00016Bh			
00016Ch			
00016Dh			
00016Eh			
00016Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.8 SFR List (8)

Address	Register	Symbol	Reset Value
000170h			
000171h			
000172h			
000173h			
000174h			
000175h			
000176h			
000177h			
000178h			
000179h			
00017Ah			
00017Bh			
00017Ch			
00017Dh			
00017Eh			
00017Fh			
000180h	Group 0 Time Measurement/Waveform Generation Register 0	G0TM0/G0PO0	XXXXh
000181h			
000182h	Group 0 Time Measurement/Waveform Generation Register 1	G0TM1/G0PO1	XXXXh
000183h			
000184h	Group 0 Time Measurement/Waveform Generation Register 2	G0TM2/G0PO2	XXXXh
000185h			
000186h	Group 0 Time Measurement/Waveform Generation Register 3	G0TM3/G0PO3	XXXXh
000187h			
000188h	Group 0 Time Measurement/Waveform Generation Register 4	G0TM4/G0PO4	XXXXh
000189h			
00018Ah	Group 0 Time Measurement/Waveform Generation Register 5	G0TM5/G0PO5	XXXXh
00018Bh			
00018Ch	Group 0 Time Measurement/Waveform Generation Register 6	G0TM6/G0PO6	XXXXh
00018Dh			
00018Eh	Group 0 Time Measurement/Waveform Generation Register 7	G0TM7/G0PO7	XXXXh
00018Fh			
000190h	Group 0 Waveform Generation Control Register 0	G0POCR0	0000 X000b
000191h	Group 0 Waveform Generation Control Register 1	G0POCR1	0X00 X000b
000192h	Group 0 Waveform Generation Control Register 2	G0POCR2	0X00 X000b
000193h	Group 0 Waveform Generation Control Register 3	G0POCR3	0X00 X000b
000194h	Group 0 Waveform Generation Control Register 4	G0POCR4	0X00 X000b
000195h	Group 0 Waveform Generation Control Register 5	G0POCR5	0X00 X000b
000196h	Group 0 Waveform Generation Control Register 6	G0POCR6	0X00 X000b
000197h	Group 0 Waveform Generation Control Register 7	G0POCR7	0X00 X000b
000198h	Group 0 Time Measurement Control Register 0	G0TMCR0	00h
000199h	Group 0 Time Measurement Control Register 1	G0TMCR1	00h
00019Ah	Group 0 Time Measurement Control Register 2	G0TMCR2	00h
00019Bh	Group 0 Time Measurement Control Register 3	G0TMCR3	00h
00019Ch	Group 0 Time Measurement Control Register 4	G0TMCR4	00h
00019Dh	Group 0 Time Measurement Control Register 5	G0TMCR5	00h
00019Eh	Group 0 Time Measurement Control Register 6	G0TMCR6	00h
00019Fh	Group 0 Time Measurement Control Register 7	G0TMCR7	00h

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.9 SFR List (9)

Address	Register	Symbol	Reset Value
0001A0h	Group 0 Base Timer Register	G0BT	XXXXh
0001A1h			
0001A2h	Group 0 Base Timer Control Register 0	G0BCR0	00h
0001A3h	Group 0 Base Timer Control Register 1	G0BCR1	0000 0000b
0001A4h	Group 0 Time Measurement Prescaler Register 6	G0TPR6	00h
0001A5h	Group 0 Time Measurement Prescaler Register 7	G0TPR7	00h
0001A6h	Group 0 Function Enable Register	G0FE	00h
0001A7h	Group 0 Function Select Register	G0FS	00h
0001A8h			
0001A9h			
0001AAh			
0001ABh			
0001ACh			
0001ADh			
0001AEh			
0001AFh			
0001B0h			
0001B1h			
0001B2h			
0001B3h			
0001B4h			
0001B5h			
0001B6h			
0001B7h			
0001B8h			
0001B9h			
0001BAh			
0001BBh			
0001BCh			
0001BDh			
0001BEh			
0001BFh			
0001C0h			
0001C1h			
0001C2h			
0001C3h			
0001C4h			
0001C5h			
0001C6h			
0001C7h			
0001C8h			
0001C9h			
0001CAh			
0001CBh			
0001CCh			
0001CDh			
0001CEh			
0001CFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.10 SFR List (10)

Address	Register	Symbol	Reset Value
0001D0h			
0001D1h			
0001D2h			
0001D3h			
0001D4h			
0001D5h			
0001D6h			
0001D7h			
0001D8h			
0001D9h			
0001DAh			
0001DBh			
0001DCh			
0001DDh			
0001DEh			
0001DFh			
0001E0h	UART3 Transmit/Receive Mode Register	U3MR	00h
0001E1h	UART3 Bit Rate Register	U3BRG	XXh
0001E2h	UART3 Transmit Buffer Register	U3TB	XXXXh
0001E3h			
0001E4h	UART3 Transmit/Receive Control Register 0	U3C0	00X0 1000b
0001E5h	UART3 Transmit/Receive Control Register 1	U3C1	XXXX 0010b
0001E6h	UART3 Receive Buffer Register	U3RB	XXXXh
0001E7h			
0001E8h	UART4 Transmit/Receive Mode Register	U4MR	00h
0001E9h	UART4 Bit Rate Register	U4BRG	XXh
0001EAh	UART4 Transmit Buffer Register	U4TB	XXXXh
0001EBh			
0001ECh	UART4 Transmit/Receive Control Register 0	U4C0	00X0 1000b
0001EDh	UART4 Transmit/Receive Control Register 1	U4C1	XXXX 0010b
0001EEh	UART4 Receive Buffer Register	U4RB	XXXXh
0001EFh			
0001F0h	UART3, UART4 Transmit/Receive Control Register 2	U34CON	X000 0000b
0001F1h			
0001F2h			
0001F3h			
0001F4h			
0001F5h			
0001F6h			
0001F7h			
0001F8h			
0001F9h			
0001FAh			
0001FBh			
0001FCh			
0001FDh			
0001FEh			
0001FFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.11 SFR List (11)

Address	Register	Symbol	Reset Value
000200h	Group0 Phase Shift Waveform Output Mode Clock Division Setting Register	G0SDR	00h
000201h	Group0 Phase Shift Waveform Output Mode Control Register	G0PSCR	00h
000202h	Group1 Phase Shift Waveform Output Mode Clock Division Setting Register	G1SDR	00h
000203h	Group1 Phase Shift Waveform Output Mode Control Register	G1PSCR	00h
000204h	Group2 Phase Shift Waveform Output Mode Clock Division Setting Register	G2SDR	00h
000205h	Group2 Phase Shift Waveform Output Mode Control Register	G2PSCR	00h
000206h	Group3 Phase Shift Waveform Output Mode Clock Division Setting Register	G3SDR	00h
000207h	Group3 Phase Shift Waveform Output Mode Control Register	G3PSCR	00h
000208h	Timer B Event Clock Select Register	TBECKS	0000 0000b
000209h			
00020Ah			
00020Bh			
00020Ch			
00020Dh			
00020Eh			
00020Fh			
000210h	IIO0_7 Digital Debounce Register	IC07DDR	FFh
000211h	IIO1_7 Digital Debounce Register	IC17DDR	FFh
000212h	IIO2_7 Digital Debounce Register	IC27DDR	FFh
000213h	IIO3_7 Digital Debounce Register	IC37DDR	FFh
000214h			
000215h			
000216h			
000217h			
000218h			
000219h			
00021Ah			
00021Bh			
00021Ch			
00021Dh			
00021Eh			
00021Fh			
000220h	Timer A1 Mirror Register	TA1M	XXXXh
000221h			
000222h	Timer A1-1 Mirror Register	TA11M	XXXXh
000223h			
000224h	Timer A2 Mirror Register	TA2M	XXXXh
000225h			
000226h	Timer A2-1 Mirror Register	TA21M	XXXXh
000227h			
000228h	Timer A4 Mirror Register	TA4M	XXXXh
000229h			
00022Ah	Timer A4-1 Mirror Register	TA41M	XXXXh
00022Bh			
00022Ch			
00022Dh			
00022Eh			
00022Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.12 SFR List (12)

Address	Register	Symbol	Reset Value
000230h to 00023F			
000240h	Group 3 Time Measurement/Waveform Generation Register 0	G3TM0/G3PO0	XXXXh
000241h			
000242h	Group 3 Time Measurement/Waveform Generation Register 1	G3TM1/G3PO1	XXXXh
000243h			
000244h	Group 3 Time Measurement/Waveform Generation Register 2	G3TM2/G3PO2	XXXXh
000245h			
000246h	Group 3 Time Measurement/Waveform Generation Register 3	G3TM3/G3PO3	XXXXh
000247h			
000248h	Group 3 Time Measurement/Waveform Generation Register 4	G3TM4/G3PO4	XXXXh
000249h			
00024Ah	Group 3 Time Measurement/Waveform Generation Register 5	G3TM5/G3PO5	XXXXh
00024Bh			
00024Ch	Group 3 Time Measurement/Waveform Generation Register 6	G3TM6/G3PO6	XXXXh
00024Dh			
00024Eh	Group 3 Time Measurement/Waveform Generation Register 7	G3TM7/G3PO7	XXXXh
00024Fh			
000250h	Group 3 Waveform Generation Control Register 0	G3POCR0	0000 X000b
000251h	Group 3 Waveform Generation Control Register 1	G3POCR1	0X00 X000b
000252h	Group 3 Waveform Generation Control Register 2	G3POCR2	0X00 X000b
000253h	Group 3 Waveform Generation Control Register 3	G3POCR3	0X00 X000b
000254h	Group 3 Waveform Generation Control Register 4	G3POCR4	0X00 X000b
000255h	Group 3 Waveform Generation Control Register 5	G3POCR5	0X00 X000b
000256h	Group 3 Waveform Generation Control Register 6	G3POCR6	0X00 X000b
000257h	Group 3 Waveform Generation Control Register 7	G3POCR7	0X00 X000b
000258h	Group 3 Time Measurement Control Register 0	G3TMCR0	00h
000259h	Group 3 Time Measurement Control Register 1	G3TMCR1	00h
00025Ah	Group 3 Time Measurement Control Register 2	G3TMCR2	00h
00025Bh	Group 3 Time Measurement Control Register 3	G3TMCR3	00h
00025Ch	Group 3 Time Measurement Control Register 4	G3TMCR4	00h
00025Dh	Group 3 Time Measurement Control Register 5	G3TMCR5	00h
00025Eh	Group 3 Time Measurement Control Register 6	G3TMCR6	00h
00025Fh	Group 3 Time Measurement Control Register 7	G3TMCR7	00h
000260h	Group 3 Base Timer Register	G3BT	XXXXh
000261h			
000262h	Group 3 Base Timer Control Register 0	G3BCR0	00h
000263h	Group 3 Base Timer Control Register 1	G3BCR1	0000 0000b
000264h	Group 3 Time Measurement Prescaler Register 6	G3TPR6	00h
000265h	Group 3 Time Measurement Prescaler Register 7	G3TPR7	00h
000266h	Group 3 Function Enable Register	G3FE	00h
000267h	Group 3 Function Select Register	G3FS	00h
000268h			
000269h			
00026Ah			
00026Bh			
00026Ch			
00026Dh			
00026Eh			
00026Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.13 SFR List (13)

Address	Register	Symbol	Reset Value
000270h to 0002BFh			
0002C0h	X0 Register/Y0 Register	X0R/Y0R	XXXXh
0002C1h			
0002C2h	X1 Register/Y1 Register	X1R/Y1R	XXXXh
0002C3h			
0002C4h	X2 Register/Y2 Register	X2R/Y2R	XXXXh
0002C5h			
0002C6h	X3 Register/Y3 Register	X3R/Y3R	XXXXh
0002C7h			
0002C8h	X4 Register/Y4 Register	X4R/Y4R	XXXXh
0002C9h			
0002CAh	X5 Register/Y5 Register	X5R/Y5R	XXXXh
0002CBh			
0002CCh	X6 Register/Y6 Register	X6R/Y6R	XXXXh
0002CDh			
0002CEh	X7 Register/Y7 Register	X7R/Y7R	XXXXh
0002CFh			
0002D0h	X8 Register/Y8 Register	X8R/Y8R	XXXXh
0002D1h			
0002D2h	X9 Register/Y9 Register	X9R/Y9R	XXXXh
0002D3h			
0002D4h	X10 Register/Y10 Register	X10R/Y10R	XXXXh
0002D5h			
0002D6h	X11 Register/Y11 Register	X11R/Y11R	XXXXh
0002D7h			
0002D8h	X12 Register/Y12 Register	X12R/Y12R	XXXXh
0002D9h			
0002DAh	X13 Register/Y13 Register	X13R/Y13R	XXXXh
0002DBh			
0002DCh	X14 Register/Y14 Register	X14R/Y14R	XXXXh
0002DDh			
0002DEh	X15 Register/Y15 Register	X15R/Y15R	XXXXh
0002DFh			
0002E0h	X-Y Control Register	XYC	XXXX XX00b
0002E1h			
0002E2h			
0002E3h			
0002E4h	UART1 Special Mode Register 4	U1SMR4	00h
0002E5h	UART1 Special Mode Register 3	U1SMR3	00h
0002E6h	UART1 Special Mode Register 2	U1SMR2	00h
0002E7h	UART1 Special Mode Register	U1SMR	00h
0002E8h	UART1 Transmit/Receive Mode Register	U1MR	00h
0002E9h	UART1 Bit Rate Register	U1BRG	XXh
0002EAh	UART1 Transmit Buffer Register	U1TB	XXXXh
0002EBh			
0002ECh	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
0002EDh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
0002EEh	UART1 Receive Buffer Register	U1RB	XXXXh
0002EFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.14 SFR List (14)

Address	Register	Symbol	Reset Value
0002F0h			
0002F1h			
0002F2h			
0002F3h			
0002F4h			
0002F5h			
0002F6h			
0002F7h			
0002F8h			
0002F9h			
0002FAh			
0002FBh			
0002FCh			
0002FDh			
0002FEh			
0002FFh			
000300h	Count Start Register for Timers B3, B4, and B5	TBSR	000X XXXXb
000301h			
000302h	Timer A1-1 Register	TA11	XXXXh
000303h			
000304h	Timer A2-1 Register	TA21	XXXXh
000305h			
000306h	Timer A4-1 Register	TA41	XXXXh
000307h			
000308h	Three-phase PWM Control Register 0	INVC0	00h
000309h	Three-phase PWM Control Register 1	INVC1	00h
00030Ah	Three-phase Output Buffer Register 0	IDB0	XX11 1111b
00030Bh	Three-phase Output Buffer Register 1	IDB1	XX11 1111b
00030Ch	Dead Time Timer	DTT	XXh
00030Dh	Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	XXh
00030Eh			
00030Fh			
000310h	Timer B3 Register	TB3	XXXXh
000311h			
000312h	Timer B4 Register	TB4	XXXXh
000313h			
000314h	Timer B5 Register	TB5	XXXXh
000315h			
000316h			
000317h			
000318h			
000319h			
00031Ah			
00031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
00031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
00031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
00031Eh			
00031Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.15 SFR List (15)

Address	Register	Symbol	Reset Value
000320h			
000321h			
000322h			
000323h			
000324h			
000325h			
000326h			
000327h			
000328h			
000329h			
00032Ah			
00032Bh			
00032Ch			
00032Dh			
00032Eh			
00032Fh			
000330h			
000331h			
000332h			
000333h			
000334h	UART2 Special Mode Register 4	U2SMR4	00h
000335h	UART2 Special Mode Register 3	U2SMR3	00h
000336h	UART2 Special Mode Register 2	U2SMR2	00h
000337h	UART2 Special Mode Register	U2SMR	00h
000338h	UART2 Transmit/Receive Mode Register	U2MR	00h
000339h	UART2 Bit Rate Register	U2BRG	XXh
00033Ah	UART2 Transmit Buffer Register	U2TB	XXXXh
00033Bh			
00033Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
00033Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
00033Eh	UART2 Receive Buffer Register	U2RB	XXXXh
00033Fh			
000340h	Count Start Register	TABSR	0000 0000b
000341h	Clock Prescaler Reset Register	CPSRF	0XXX XXXXb
000342h	One-shot Start Register	ONSF	0000 0000b
000343h	Trigger Select Register	TRGSR	0000 0000b
000344h	Increment/Decrement Counting Select Register	UDF	0000 0000b
000345h			
000346h	Timer A0 Register	TA0	XXXXh
000347h			
000348h	Timer A1 Register	TA1	XXXXh
000349h			
00034Ah	Timer A2 Register	TA2	XXXXh
00034Bh			
00034Ch	Timer A3 Register	TA3	XXXXh
00034Dh			
00034Eh	Timer A4 Register	TA4	XXXXh
00034Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.16 SFR List (16)

Address	Register	Symbol	Reset Value
000350h	Timer B0 Register	TB0	XXXXh
000351h			
000352h	Timer B1 Register	TB1	XXXXh
000353h			
000354h	Timer B2 Register	TB2	XXXXh
000355h			
000356h	Timer A0 Mode Register	TA0MR	0000 0000b
000357h	Timer A1 Mode Register	TA1MR	0000 0000b
000358h	Timer A2 Mode Register	TA2MR	0000 0000b
000359h	Timer A3 Mode Register	TA3MR	0000 0000b
00035Ah	Timer A4 Mode Register	TA4MR	0000 0000b
00035Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
00035Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
00035Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
00035Eh	Timer B2 Special Mode Register	TB2SC	XXXX XXX0b
00035Fh	Count Source Prescaler Register	TCSPR	0000 0000b
000360h			
000361h			
000362h			
000363h			
000364h	UART0 Special Mode Register 4	U0SMR4	00h
000365h	UART0 Special Mode Register 3	U0SMR3	00h
000366h	UART0 Special Mode Register 2	U0SMR2	00h
000367h	UART0 Special Mode Register	U0SMR	00h
000368h	UART0 Transmit/Receive Mode Register	U0MR	00h
000369h	UART0 Bit Rate Register	U0BRG	XXh
00036Ah	UART0 Transmit Buffer Register	U0TB	XXXXh
00036Bh			
00036Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
00036Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
00036Eh	UART0 Receive Buffer Register	U0RB	XXXXh
00036Fh			
000370h			
000371h			
000372h			
000373h			
000374h			
000375h			
000376h			
000377h			
000378h			
000379h			
00037Ah			
00037Bh			
00037Ch	CRC Data Register	CRCD	XXXXh
00037Dh			
00037Eh	CRC Input Register	CRCIN	XXh
00037Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.17 SFR List (17)

Address	Register	Symbol	Reset Value
000380h	A/D0 Register 0	AD00	00XXh
000381h			
000382h	A/D0 Register 1	AD01	00XXh
000383h			
000384h	A/D0 Register 2	AD02	00XXh
000385h			
000386h	A/D0 Register 3	AD03	00XXh
000387h			
000388h	A/D0 Register 4	AD04	00XXh
000389h			
00038Ah	A/D0 Register 5	AD05	00XXh
00038Bh			
00038Ch	A/D0 Register 6	AD06	00XXh
00038Dh			
00038Eh	A/D0 Register 7	AD07	00XXh
00038Fh			
000390h			
000391h			
000392h	A/D0 Control Register 4	AD0CON4	XXXX 00XXb
000393h	A/D0 Control Register 5	AD0CON5	00h
000394h	A/D0 Control Register 2	AD0CON2	X00X X000b
000395h	A/D0 Control Register 3	AD0CON3	XXXX X000b
000396h	A/D0 Control Register 0	AD0CON0	00h
000397h	A/D0 Control Register 1	AD0CON1	00h
000398h	D/A Register 0	DA0	XXh
000399h			
00039Ah	D/A Register 1	DA1	XXh
00039Bh			
00039Ch	D/A Control Register	DACON	XXXX XX00b
00039Dh			
00039Eh			
00039Fh			
0003A0h			
0003A1h			
0003A2h			
0003A3h			
0003A4h			
0003A5h			
0003A6h			
0003A7h			
0003A8h			
0003A9h			
0003AAh			
0003ABh			
0003ACh			
0003ADh			
0003AEh			
0003AFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.18 SFR List (18)

Address	Register	Symbol	Reset Value
0003B0h			
0003B1h			
0003B2h			
0003B3h			
0003B4h			
0003B5h			
0003B6h			
0003B7h			
0003B8h			
0003B9h			
0003BAh			
0003BBh			
0003BCh			
0003BDh			
0003BEh			
0003BFh			
0003C0h	Port P0 Register	P0	XXh
0003C1h	Port P1 Register	P1	XXh
0003C2h	Port P0 Direction Register	PD0	0000 0000b
0003C3h	Port P1 Direction Register	PD1	0000 0000b
0003C4h	Port P2 Register	P2	XXh
0003C5h	Port P3 Register	P3	XXh
0003C6h	Port P2 Direction Register	PD2	0000 0000b
0003C7h	Port P3 Direction Register	PD3	0000 0000b
0003C8h	Port P4 Register	P4	XXh
0003C9h	Port P5 Register	P5	XXh
0003CAh	Port P4 Direction Register	PD4	0000 0000b
0003CBh	Port P5 Direction Register	PD5	0000 0000b
0003CCh	Port P6 Register	P6	XXh
0003CDh	Port P7 Register	P7	XXh
0003CEh	Port P6 Direction Register	PD6	0000 0000b
0003CFh	Port P7 Direction Register	PD7	0000 0000b
0003D0h	Port P8 Register	P8	XXh
0003D1h	Port P9 Register	P9	XXh
0003D2h	Port P8 Direction Register	PD8	00X0 0000b
0003D3h	Port P9 Direction Register	PD9	0000 0000b
0003D4h	Port P10 Register	P10	XXh
0003D5h	Port P11 Register	P11	XXh
0003D6h	Port P10 Direction Register	PD10	0000 0000b
0003D7h	Port P11 Direction Register	PD11	XXX0 0000b
0003D8h	Port P12 Register	P12	XXh
0003D9h	Port P13 Register	P13	XXh
0003DAh	Port P12 Direction Register	PD12	0000 0000b
0003DBh	Port P13 Direction Register	PD13	0000 0000b
0003DCh	Port P14 Register	P14	XXh
0003DDh	Port P15 Register	P15	XXh
0003DEh	Port P14 Direction Register	PD14	X000 0X0Xb
0003DFh	Port P15 Direction Register	PD15	0000 0000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.19 SFR List (19)

Address	Register	Symbol	Reset Value
0003E0h			
0003E1h			
0003E2h			
0003E3h			
0003E4h			
0003E5h			
0003E6h			
0003E7h			
0003E8h			
0003E9h			
0003EAh			
0003EBh			
0003ECh			
0003EDh			
0003EEh			
0003EFh			
0003F0h	Pull-up Control Register 0	PUR0	0000 0000b
0003F1h	Pull-up Control Register 1	PUR1	XXXX 0000b
0003F2h	Pull-up Control Register 2	PUR2	0000 0000b
0003F3h	Pull-up Control Register 3	PUR3	0000 0000b
0003F4h	Pull-up Control Register 4	PUR4	XXXX 0000b
0003F5h			
0003F6h			
0003F7h			
0003F8h			
0003F9h			
0003FAh			
0003FBh			
0003FCh			
0003FDh			
0003FEh			
0003FFh	Port Control Register	PCR	XXXX XXX0b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.20 SFR List (20)

Address	Register	Symbol	Reset Value
040000h	Flash Memory Control Register 0	FMR0	0X01 XX00b
040001h	Flash Memory Status Register 0	FMSR0	1000 0000b
040002h			
040003h			
040004h			
040005h			
040006h			
040007h			
040008h	Flash Register Protection Unlock Register 0	FPR0	00h
040009h	Flash Memory Control Register 1	FMR1	0000 0010b
04000Ah	Block Protect Bit Monitor Register 0	FBPM0	??X? ????b (1)
04000Bh	Block Protect Bit Monitor Register 1	FBPM1	XXX? ????b (1)
04000Ch			
04000Dh			
04000Eh			
04000Fh			
040010h			
040011h	Block Protect Bit Monitor Register 2	FBPM2	???? ????b (1)
040012h			
040013h			
040014h			
040015h			
040016h			
040017h			
040018h			
040019h			
04001Ah			
04001Bh			
04001Ch			
04001Dh			
04001Eh			
04001Fh			
040020h	PLL Control Register 0	PLC0	0000 0001b
040021h	PLL Control Register 1	PLC1	0001 1111b
040022h			
040023h			
040024h	PLL Status Register	PLS	1XXX XX00b
040025h			
040026h			
040027h			
040028h			
040029h			
04002Ah			
04002Bh			
04002Ch			
04002Dh			
04002Eh			
04002Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. The status of protect bit of each block in flash memory is reflected.

Table 4.21 SFR List (21)

Address	Register	Symbol	Reset Value
040030h to 04003Fh			
040040h			
040041h			
040042h			
040043h			
040044h	Processor Mode Register 0	PM0	1000 0000b
040045h			
040046h	System Clock Control Register 0	CM0	0000 1000b
040047h	System Clock Control Register 1	CM1	0010 0000b
040048h	Processor Mode Register 3	PM3	00h
040049h			
04004Ah	Protect Register	PRCR	XXXX X000b
04004Bh			
04004Ch	Protect Register 3	PRCR3	0000 0000b
04004Dh	Oscillator Stop Detection Register	CM2	00h
04004Eh			
04004Fh			
040050h			
040051h			
040052h			
040053h	Processor Mode Register 2	PM2	00h
040054h			
040055h			
040056h			
040057h			
040058h			
040059h			
04005Ah	Low Speed Mode Clock Control Register	CM3	XXXX XX00b
04005Bh			
04005Ch			
04005Dh			
04005Eh			
04005Fh			
040060h	Voltage Regulator Control Register	VRCR	0000 0000b
040061h			
040062h	Low Voltage Detector Control Register	LVDC	0000 XX00b
040063h			
040064h	Detection Voltage Configuration Register	DVCR	0000 XXXXb
040065h			
040066h			
040067h			
040068h to 040093h			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.22 SFR List (22)

Address	Register	Symbol	Reset Value
040094h			
040095h			
040096h			
040097h	Three-phase Output Buffer Control Register	IOBC	0XXX XX0Xb
040098h	Input Function Select Register 0	IFS0	0000 0000b
040099h	Input Function Select Register 1	IFS1	XXX0 X0X0b
04009Ah	Input Function Select Register 2	IFS2	0000 0000b
04009Bh			
04009Ch			
04009Dh	Input Function Select Register 5	IFS5	XXX0 0000b
04009Eh	Input Function Select Register 6	IFS6	XXXX 0000b
04009Fh	Input Function Select Register 7	IFS7	XXXX XXX0b
0400A0h	Port P0_0 Function Select Register	P0_0S	0XXX X000b
0400A1h	Port P1_0 Function Select Register	P1_0S	0XXX X000b
0400A2h	Port P0_1 Function Select Register	P0_1S	0XXX X000b
0400A3h	Port P1_1 Function Select Register	P1_1S	0XXX X000b
0400A4h	Port P0_2 Function Select Register	P0_2S	0XXX X000b
0400A5h	Port P1_2 Function Select Register	P1_2S	0XXX X000b
0400A6h	Port P0_3 Function Select Register	P0_3S	0XXX X000b
0400A7h	Port P1_3 Function Select Register	P1_3S	0XXX X000b
0400A8h	Port P0_4 Function Select Register	P0_4S	0XXX X000b
0400A9h	Port P1_4 Function Select Register	P1_4S	0XXX X000b
0400AAh	Port P0_5 Function Select Register	P0_5S	0XXX X000b
0400ABh	Port P1_5 Function Select Register	P1_5S	0XXX X000b
0400ACh	Port P0_6 Function Select Register	P0_6S	0XXX X000b
0400ADh	Port P1_6 Function Select Register	P1_6S	0XXX X000b
0400AEh	Port P0_7 Function Select Register	P0_7S	0XXX X000b
0400AFh	Port P1_7 Function Select Register	P1_7S	0XXX X000b
0400B0h	Port P2_0 Function Select Register	P2_0S	0XXX X000b
0400B1h	Port P3_0 Function Select Register	P3_0S	XXXX X000b
0400B2h	Port P2_1 Function Select Register	P2_1S	0XXX X000b
0400B3h	Port P3_1 Function Select Register	P3_1S	XXXX X000b
0400B4h	Port P2_2 Function Select Register	P2_2S	0XXX X000b
0400B5h	Port P3_2 Function Select Register	P3_2S	XXXX X000b
0400B6h	Port P2_3 Function Select Register	P2_3S	0XXX X000b
0400B7h	Port P3_3 Function Select Register	P3_3S	XXXX X000b
0400B8h	Port P2_4 Function Select Register	P2_4S	0XXX X000b
0400B9h	Port P3_4 Function Select Register	P3_4S	XXXX X000b
0400BAh	Port P2_5 Function Select Register	P2_5S	0XXX X000b
0400BBh	Port P3_5 Function Select Register	P3_5S	XXXX X000b
0400BCh	Port P2_6 Function Select Register	P2_6S	0XXX X000b
0400BDh	Port P3_6 Function Select Register	P3_6S	XXXX X000b
0400BEh	Port P2_7 Function Select Register	P2_7S	0XXX X000b
0400BFh	Port P3_7 Function Select Register	P3_7S	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.23 SFR List (23)

Address	Register	Symbol	Reset Value
0400C0h	Port P4_0 Function Select Register	P4_0S	XXXX X000b
0400C1h	Port P5_0 Function Select Register	P5_0S	XXXX X000b
0400C2h	Port P4_1 Function Select Register	P4_1S	XXXX X000b
0400C3h	Port P5_1 Function Select Register	P5_1S	XXXX X000b
0400C4h	Port P4_2 Function Select Register	P4_2S	XXXX X000b
0400C5h	Port P5_2 Function Select Register	P5_2S	XXXX X000b
0400C6h	Port P4_3 Function Select Register	P4_3S	XXXX X000b
0400C7h	Port P5_3 Function Select Register	P5_3S	XXXX X000b
0400C8h	Port P4_4 Function Select Register	P4_4S	XXXX X000b
0400C9h	Port P5_4 Function Select Register	P5_4S	XXXX X000b
0400CAh	Port P4_5 Function Select Register	P4_5S	XXXX X000b
0400CBh	Port P5_5 Function Select Register	P5_5S	XXXX X000b
0400CCh	Port P4_6 Function Select Register	P4_6S	XXXX X000b
0400CDh	Port P5_6 Function Select Register	P5_6S	XXXX X000b
0400CEh	Port P4_7 Function Select Register	P4_7S	XXXX X000b
0400CFh	Port P5_7 Function Select Register	P5_7S	XXXX X000b
0400D0h	Port P6_0 Function Select Register	P6_0S	XXXX X000b
0400D1h	Port P7_0 Function Select Register	P7_0S	XXXX X000b
0400D2h	Port P6_1 Function Select Register	P6_1S	XXXX X000b
0400D3h	Port P7_1 Function Select Register	P7_1S	XXXX X000b
0400D4h	Port P6_2 Function Select Register	P6_2S	XXXX X000b
0400D5h	Port P7_2 Function Select Register	P7_2S	XXXX X000b
0400D6h	Port P6_3 Function Select Register	P6_3S	XXXX X000b
0400D7h	Port P7_3 Function Select Register	P7_3S	XXXX X000b
0400D8h	Port P6_4 Function Select Register	P6_4S	XXXX X000b
0400D9h	Port P7_4 Function Select Register	P7_4S	XXXX X000b
0400DAh	Port P6_5 Function Select Register	P6_5S	XXXX X000b
0400DBh	Port P7_5 Function Select Register	P7_5S	XXXX X000b
0400DCh	Port P6_6 Function Select Register	P6_6S	XXXX X000b
0400DDh	Port P7_6 Function Select Register	P7_6S	XXXX X000b
0400DEh	Port P6_7 Function Select Register	P6_7S	XXXX X000b
0400DFh	Port P7_7 Function Select Register	P7_7S	XXXX X000b
0400E0h	Port P8_0 Function Select Register	P8_0S	XXXX X000b
0400E1h	Port P9_0 Function Select Register	P9_0S	XXXX X000b
0400E2h	Port P8_1 Function Select Register	P8_1S	XXXX X000b
0400E3h	Port P9_1 Function Select Register	P9_1S	XXXX X000b
0400E4h	Port P8_2 Function Select Register	P8_2S	XXXX X000b
0400E5h	Port P9_2 Function Select Register	P9_2S	XXXX X000b
0400E6h	Port P8_3 Function Select Register	P8_3S	XXXX X000b
0400E7h	Port P9_3 Function Select Register	P9_3S	0XXX X000b
0400E8h	Port P8_4 Function Select Register	P8_4S	XXXX X000b
0400E9h	Port P9_4 Function Select Register	P9_4S	0XXX X000b
0400EAh			
0400EBh	Port P9_5 Function Select Register	P9_5S	0XXX X000b
0400ECh	Port P8_6 Function Select Register	P8_6S	XXXX X000b
0400EDh	Port P9_6 Function Select Register	P9_6S	0XXX X000b
0400EEh	Port P8_7 Function Select Register	P8_7S	XXXX X000b
0400EFh	Port P9_7 Function Select Register	P9_7S	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.24 SFR List (24)

Address	Register	Symbol	Reset Value
0400F0h	Port P10_0 Function Select Register	P10_0S	0XXX X000b
0400F1h	Port P11_0 Function Select Register	P11_0S	XXXX X000b
0400F2h	Port P10_1 Function Select Register	P10_1S	0XXX X000b
0400F3h	Port P11_1 Function Select Register	P11_1S	XXXX X000b
0400F4h	Port P10_2 Function Select Register	P10_2S	0XXX X000b
0400F5h	Port P11_2 Function Select Register	P11_2S	XXXX X000b
0400F6h	Port P10_3 Function Select Register	P10_3S	0XXX X000b
0400F7h	Port P11_3 Function Select Register	P11_3S	XXXX X000b
0400F8h	Port P10_4 Function Select Register	P10_4S	0XXX X000b
0400F9h	Port P11_4 Function Select Register	P11_4S	XXXX X000b
0400FAh	Port P10_5 Function Select Register	P10_5S	0XXX X000b
0400FBh			
0400FCh	Port P10_6 Function Select Register	P10_6S	0XXX X000b
0400FDh			
0400FEh	Port P10_7 Function Select Register	P10_7S	0XXX X000b
0400FFh			
040100h	Port P12_0 Function Select Register	P12_0S	XXXX X000b
040101h	Port P13_0 Function Select Register	P13_0S	XXXX X000b
040102h	Port P12_1 Function Select Register	P12_1S	XXXX X000b
040103h	Port P13_1 Function Select Register	P13_1S	XXXX X000b
040104h	Port P12_2 Function Select Register	P12_2S	XXXX X000b
040105h	Port P13_2 Function Select Register	P13_2S	XXXX X000b
040106h	Port P12_3 Function Select Register	P12_3S	XXXX X000b
040107h	Port P13_3 Function Select Register	P13_3S	XXXX X000b
040108h	Port P12_4 Function Select Register	P12_4S	XXXX X000b
040109h	Port P13_4 Function Select Register	P13_4S	XXXX X000b
04010Ah	Port P12_5 Function Select Register	P12_5S	XXXX X000b
04010Bh	Port P13_5 Function Select Register	P13_5S	XXXX X000b
04010Ch	Port P12_6 Function Select Register	P12_6S	XXXX X000b
04010Dh	Port P13_6 Function Select Register	P13_6S	XXXX X000b
04010Eh	Port P12_7 Function Select Register	P12_7S	XXXX X000b
04010Fh	Port P13_7 Function Select Register	P13_7S	XXXX X000b
040110h			
040111h	Port P15_0 Function Select Register	P15_0S	0XXX X000b
040112h			
040113h	Port P15_1 Function Select Register	P15_1S	0XXX X000b
040114h			
040115h	Port P15_2 Function Select Register	P15_2S	0XXX X000b
040116h	Port P14_3 Function Select Register	P14_3S	XXXX X000b
040117h	Port P15_3 Function Select Register	P15_3S	0XXX X000b
040118h	Port P14_4 Function Select Register	P14_4S	XXXX X000b
040119h	Port P15_4 Function Select Register	P15_4S	0XXX X000b
04011Ah	Port P14_5 Function Select Register	P14_5S	XXXX X000b
04011Bh	Port P15_5 Function Select Register	P15_5S	0XXX X000b
04011Ch	Port P14_6 Function Select Register	P14_6S	XXXX X000b
04011Dh	Port P15_6 Function Select Register	P15_6S	0XXX X000b
04011Eh			
04011Fh	Port P15_7 Function Select Register	P15_7S	0XXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.25 SFR List (25)

Address	Register	Symbol	Reset Value
040120h to 04403Fh			
044040h			
044041h			
044042h			
044043h			
044044h			
044045h			
044046h			
044047h			
044048h			
044049h			
04404Ah			
04404Bh			
04404Ch	Protect Register 4	PRCR4	0000 0000b
04404Dh	Watchdog Timer Clock Control Register	WDK	0000 0000b
04404Eh	Watchdog Timer Start Register	WDTS	XXXX XXXXb
04404Fh	Watchdog Timer Control Register	WDC	000X XXXXb
044050h			
044051h			
044052h			
044053h			
044054h			
044055h			
044056h			
044057h			
044058h			
044059h			
04405Ah			
04405Bh			
04405Ch			
04405Dh			
04405Eh			
04405Fh	Protect Register 2	PRCR2	0XXX XXXXb

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.26 SFR List (26)

Address	Register	Symbol	Reset Value
044060h			
044061h			
044062h			
044063h			
044064h			
044065h			
044066h			
044067h			
044068h			
044069h			
04406Ah			
04406Bh			
04406Ch			
04406Dh	External Interrupt Request Source Select Register 1	IFSR1	XXXX X000b
04406Eh			
04406Fh	External Interrupt Request Source Select Register 0	IFSR0	0000 0000b
044070h	DMA0 Request Source Select Register 2	DM0SL2	XX00 0000b
044071h	DMA1 Request Source Select Register 2	DM1SL2	XX00 0000b
044072h	DMA2 Request Source Select Register 2	DM2SL2	XX00 0000b
044073h	DMA3 Request Source Select Register 2	DM3SL2	XX00 0000b
044074h			
044075h			
044076h			
044077h			
044078h	DMA0 Request Source Select Register	DM0SL	XXX0 0000b
044079h	DMA1 Request Source Select Register	DM1SL	XXX0 0000b
04407Ah	DMA2 Request Source Select Register	DM2SL	XXX0 0000b
04407Bh	DMA3 Request Source Select Register	DM3SL	XXX0 0000b
04407Ch			
04407Dh	Wake-up IPL Setting Register 2	RIPL2	XX0X 0000b
04407Eh			
04407Fh	Wake-up IPL Setting Register 1	RIPL1	XX0X 0000b
044080h	External Interrupt Input Filter Select Register 0	INTF0	0000 0000b
044081h			
044082h	External Interrupt Input Filter Select Register 1	INTF1	0000 0000b
044083h			
044084h	External Interrupt Input Filter Select Register 2	INTF2	0000 0000b
044085h			
044086h			
044087h			
044088h	External Interrupt Input Pin Select Register	INTSR	0000 0000b
044089h			
04408Ah			
04408Bh			
04408Ch			
04408Dh			
04408Eh			
04408Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.27 SFR List (27)

Address	Register	Symbol	Reset Value
044090h to 044DFFh			
044E00h	LIN0 Channel Window Select/Input Signal Low Detection Status Register	L0CW	0000 0000b
044E01h	LIN0 Baud Rate Generator Control Register	L0BRG	0000 0000b
044E02h	LIN0 Baud Rate Prescaler 0	L0BRP0	00h
044E03h	LIN0 Baud Rate Prescaler 1	L0BRP1	00h
044E04h	LIN0 Mode Register 0	L0MD0	0000 0000b
044E05h	LIN0 Mode Register 1	L0MD1	00h
044E06h	LIN0 Wake-up Setting Register	L0WUP	00h
044E07h			
044E08h	LIN0 Break Field Setting Register	L0BRK	0000 0000b
044E09h	LIN0 Space Setting Register	L0SPC	0000 0000b
044E0Ah	LIN0 Response Field Setting Register	L0RFC	0000 0000b
044E0Bh	LIN0 ID Buffer Register	L0IDB	00h
044E0Ch	LIN0 Status Control Register	L0SC	0000 0000b
044E0Dh	LIN0 Transmission Control Register	L0TC	0000 0000b
044E0Eh	LIN0 Status Register	L0ST	0000 0000b
044E0Fh	LIN0 Error Status Register	L0EST	0000 0000b
044E10h	LIN0 Data 1 Buffer Register	L0DB1	00h
044E11h	LIN0 Data 2 Buffer Register	L0DB2	00h
044E12h	LIN0 Data 3 Buffer Register	L0DB3	00h
044E13h	LIN0 Data 4 Buffer Register	L0DB4	00h
044E14h	LIN0 Data 5 Buffer Register	L0DB5	00h
044E15h	LIN0 Data 6 Buffer Register	L0DB6	00h
044E16h	LIN0 Data 7 Buffer Register	L0DB7	00h
044E17h	LIN0 Data 8 Buffer Register	L0DB8	00h
044E18h			
044E19h			
044E1Ah			
044E1Bh			
044E1Ch			
044E1Dh			
044E1Eh			
044E1Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.28 SFR List (28)

Address	Register	Symbol	Reset Value
044E20h	LIN1 Channel Window Select/Input Signal Low Detection Status Register	L1CW	0000 0000b
044E21h	LIN1 Baud Rate Generator Control Register	L1BRG	0000 0000b
044E22h	LIN1 Baud Rate Prescaler 0	L10BRP0	00h
044E23h	LIN1 Baud Rate Prescaler 1	L1BRP1	00h
044E24h	LIN1 Mode Register 0	L1MD0	0000 0000b
044E25h	LIN1 Mode Register 1	L1MD1	00h
044E26h	LIN1 Wake-up Setting Register	L1WUP	00h
044E27h			
044E28h	LIN1 Break Field Setting Register	L1BRK	0000 0000b
044E29h	LIN1 Space Setting Register	L1SPC	0000 0000b
044E2Ah	LIN1 Response Field Setting Register	L1RFC	0000 0000b
044E2Bh	LIN1 ID Buffer Register	L1IDB	00h
044E2Ch	LIN1 Status Control Register	L1SC	0000 0000b
044E2Dh	LIN1 Transmission Control Register	L1TC	0000 0000b
044E2Eh	LIN1 Status Register	L1ST	0000 0000b
044E2Fh	LIN1 Error Status Register	L1EST	0000 0000b
044E30h	LIN1 Data 1 Buffer Register	L1DB1	00h
044E31h	LIN1 Data 2 Buffer Register	L1DB2	00h
044E32h	LIN1 Data 3 Buffer Register	L1DB3	00h
044E33h	LIN1 Data 4 Buffer Register	L1DB4	00h
044E34h	LIN1 Data 5 Buffer Register	L1DB5	00h
044E35h	LIN1 Data 6 Buffer Register	L1DB6	00h
044E36h	LIN1 Data 7 Buffer Register	L1DB7	00h
044E37h	LIN1 Data 8 Buffer Register	L1DB8	00h
044E38h			
044E39h			
044E3Ah			
044E3Bh			
044E3Ch			
044E3Dh			
044E3Eh			
044E3Fh			
044E41h			
044E42h			
044E43h			
044E44h			
044E45h			
044E46h			
044E47h			
044E48h			
044E49h			
044E4Ah			
044E4Bh			
044E4Ch			
044E4Dh			
044E4Eh			
044E4Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.29 SFR List (29)

Address	Register	Symbol	Reset Value
044E50h to 044EFFh			
044F00h			
044F01h			
044F02h			
044F03h			
044F04h			
044F05h			
044F06h	SS0 Receive Data Register	SS0RDR	FFh
044F07h	SS0 Receive Data Register (H)	SS0RDR (H)	FFh
044F08h	SS0 Control Register H	SS0CRH	00h
044F09h	SS0 Control Register L	SS0CRL	0111 1101b
044F0Ah	SS0 Mode Register	SS0MR	0001 0000b
044F0Bh	SS0 Enable Register	SS0ER	00h
044F0Ch	SS0 Status Register	SS0SR	00h
044F0Dh	SS0 Mode Register 2	SS0MR2	00h
044F0Eh	SS0 Transmit Data Register	SS0TDR	FFh
044F0Fh	SS0 Transmit Data Register (H)	SS0TDR (H)	FFh
044F10h			
044F11h			
044F12h			
044F13h			
044F14h			
044F15h			
044F16h	SS1 Receive Data Register	SS1RDR	FFh
044F17h	SS1 Receive Data Register (H)	SS1RDR (H)	FFh
044F18h	SS1 Control Register H	SS1CRH	00h
044F19h	SS1 Control Register L	SS1CRL	0111 1101b
044F1Ah	SS1 Mode Register	SS1MR	0001 0000b
044F1Bh	SS1 Enable Register	SS1ER	00h
044F1Ch	SS1 Status Register	SS1SR	00h
044F1Dh	SS1 Mode Register 2	SS1MR2	00h
044F1Eh	SS1 Transmit Data Register	SS1TDR	FFh
044F1Fh	SS1 Transmit Data Register (H)	SS1TDR (H)	FFh
044F20h			
044F21h			
044F22h			
044F23h			
044F24h			
044F25h			
044F26h	SS2 Receive Data Register	SS2RDR	FFh
044F27h	SS2 Receive Data Register (H)	SS2RDR (H)	FFh

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.30 SFR List (30)

Address	Register	Symbol	Reset Value
044F28h	SS2 Control Register H	SS2CRH	00h
044F29h	SS2 Control Register L	SS2CRL	0111 1101b
044F2Ah	SS2 Mode Register	SS2MR	0001 0000b
044F2Bh	SS2 Enable Register	SS2ER	00h
044F2Ch	SS2 Status Register	SS2SR	00h
044F2Dh	SS2 Mode Register 2	SS2MR2	00h
044F2Eh	SS2 Transmit Data Register	SS2TDR	FFh
044F2Fh	SS2 Transmit Data Register (H)	SS2TDR (H)	FFh
044F30h			
044F31h			
044F32h			
044F33h			
044F34h			
044F35h			
044F36h			
044F37h			
044F38h			
044F39h			
044F3Ah			
044F3Bh			
044F3Ch			
044F3Dh			
044F3Eh			
044F3Fh			
044F40h			
044F41h			
044F42h			
044F43h			
044F44h			
044F45h			
044F46h			
044F47h			
044F48h			
044F49h			
044F4Ah			
044F4Bh			
044F4Ch			
044F4Dh			
044F4Eh			
044F4Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.31 SFR List (31)

Address	Register	Symbol	Reset Value
044F50h to 044FDFh			
044FE0h	E²dataFlash Address Register	E2FA	XXXX 0000h
044FE1h			
044FE2h			
044FE3h			
044FE4h			
044FE5h			
044FE6h			
044FE7h			
044FE8h	E²dataFlash Instruction Register	E2FI	XX00h
044FE9h			
044FEAh			
044FEBh			
044FECh	E²dataFlash Data Register	E2FD	XXXXh
044FEDh			
044FEEh			
044FEFh			
044FF0h	E²dataFlash Mode Register	E2FM	0000 0000b
044FF1h			
044FF2h	E²dataFlash Control Register	E2FC	XXXX XXX0b
044FF3h			
044FF4h	E²dataFlash Status Register 1	E2FS1	XXXX XXX0b
044FF5h			
044FF6h			
044FF7h			
044FF8h			
044FF9h			
044FFAh			
044FFBh			
044FFCh			
044FFDh			
044FFEh			
044FFFh			
045000h			
045001h	E²dataFlash Status Register 0	E2FS0	XXXX XXXXb
045002h			
045003h			
045004h			
045005h			
045006h			
045007h			
045008h to 045FFFh			
046000h to 0467FFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.32 SFR List (32)

Address	Register	Symbol	Reset Value
046800h to 046BFFh			
046C00h	CAN3 Mailbox 0: Message Identifier	C3MB0	XXXX XXXXh
046C01h			
046C02h			
046C03h			
046C04h			
046C05h	CAN3 Mailbox 0: Data Length		XXh
046C06h	CAN3 Mailbox 0: Data Field		XXXX XXXX
046C07h			XXXX XXXXh
046C08h			
046C09h			
046C0Ah			
046C0Bh			
046C0Ch			
046C0Dh			
046C0Eh	CAN3 Mailbox 0: Time Stamp		XXXXh
046C0Fh			
046C10h	CAN3 Mailbox 1: Message Identifier	C3MB1	XXXX XXXXh
046C11h			
046C12h			
046C13h			
046C14h			
046C15h	CAN3 Mailbox 1: Data Length		XXh
046C16h	CAN3 Mailbox 1: Data Field		XXXX XXXX
046C17h			XXXX XXXXh
046C18h			
046C19h			
046C1Ah			
046C1Bh			
046C1Ch			
046C1Dh			
046C1Eh	CAN3 Mailbox 1: Time Stamp		XXXXh
046C1Fh			
046C20h	CAN3 Mailbox 2: Message Identifier	C3MB2	XXXX XXXXh
046C21h			
046C22h			
046C23h			
046C24h			
046C25h	CAN3 Mailbox 2: Data Length		XXh
046C26h	CAN3 Mailbox 2: Data Field		XXXX XXXX
046C27h			XXXX XXXXh
046C28h			
046C29h			
046C2Ah			
046C2Bh			
046C2Ch			
046C2Dh			
046C2Eh	CAN3 Mailbox 2: Time Stamp		XXXXh
046C2Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.33 SFR List (33)

Address	Register	Symbol	Reset Value
046C30h	CAN3 Mailbox 3: Message Identifier	C3MB3	XXXX XXXXh
046C31h			
046C32h			
046C33h			
046C34h			
046C35h	CAN3 Mailbox 3: Data Length		XXh
046C36h	CAN3 Mailbox 3: Data Field		XXXX XXXX
046C37h			XXXX XXXXh
046C38h			
046C39h			
046C3Ah			
046C3Bh			
046C3Ch			
046C3Dh			
046C3Eh	CAN3 Mailbox 3: Time Stamp		XXXXh
046C3Fh			
046C40h	CAN3 Mailbox 4: Message Identifier	C3MB4	XXXX XXXXh
046C41h			
046C42h			
046C43h			
046C44h			
046C45h	CAN3 Mailbox 4: Data Length		XXh
046C46h	CAN3 Mailbox 4: Data Field		XXXX XXXX
046C47h			XXXX XXXXh
046C48h			
046C49h			
046C4Ah			
046C4Bh			
046C4Ch			
046C4Dh			
046C4Eh	CAN3 Mailbox 4: Time Stamp		XXXXh
046C4Fh			
046C50h	CAN3 Mailbox 5: Message Identifier	C3MB5	XXXX XXXXh
046C51h			
046C52h			
046C53h			
046C54h			
046C55h	CAN3 Mailbox 5: Data Length		XXh
046C56h	CAN3 Mailbox 5: Data Field		XXXX XXXX
046C57h			XXXX XXXXh
046C58h			
046C59h			
046C5Ah			
046C5Bh			
046C5Ch			
046C5Dh			
046C5Eh	CAN3 Mailbox 5: Time Stamp		XXXXh
046C5Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.34 SFR List (34)

Address	Register	Symbol	Reset Value
046C60h	CAN3 Mailbox 6: Message Identifier	C3MB6	XXXX XXXXh
046C61h			
046C62h			
046C63h			
046C64h			
047065h	CAN3 Mailbox 6: Data Length		XXh
046C66h	CAN3 Mailbox 6: Data Field		XXXX XXXX
046C67h			XXXX XXXXh
046C68h			
046C69h			
046C6Ah			
046C6Bh			
046C6Ch			
046C6Dh			
046C6Eh	CAN3 Mailbox 6: Time Stamp		XXXXh
046C6Fh			
046C70h	CAN3 Mailbox 7: Message Identifier	C3MB7	XXXX XXXXh
046C71h			
046C72h			
046C73h			
046C74h			
046C75h	CAN3 Mailbox 7: Data Length		XXh
046C76h	CAN3 Mailbox 7: Data Field		XXXX XXXX
046C77h			XXXX XXXXh
046C78h			
046C79h			
046C7Ah			
046C7Bh			
046C7Ch			
046C7Dh			
046C7Eh	CAN3 Mailbox 7: Time Stamp		XXXXh
046C7Fh			
046C80h	CAN3 Mailbox 8: Message Identifier	C3MB8	XXXX XXXXh
046C81h			
046C82h			
046C83h			
046C84h			
046C85h	CAN3 Mailbox 8: Data Length		XXh
046C86h	CAN3 Mailbox 8: Data Field		XXXX XXXX
046C87h			XXXX XXXXh
046C88h			
046C89h			
046C8Ah			
046C8Bh			
046C8Ch			
046C8Dh			
046C8Eh	CAN3 Mailbox 8: Time Stamp		XXXXh
046C8Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.35 SFR List (35)

Address	Register	Symbol	Reset Value
046C90h	CAN3 Mailbox 9: Message Identifier	C3MB9	XXXX XXXXh
046C91h			
046C92h			
046C93h			
046C94h			
046C95h	CAN3 Mailbox 9: Data Length		XXh
046C96h	CAN3 Mailbox 9: Data Field		XXXX XXXX
046C97h			XXXX XXXXh
046C98h			
046C99h			
046C9Ah			
046C9Bh			
046C9Ch			
046C9Dh			
046C9Eh	CAN3 Mailbox 9: Time Stamp		XXXXh
046C9Fh			
046CA0h	CAN3 Mailbox 10: Message Identifier	C3MB10	XXXX XXXXh
046CA1h			
046CA2h			
046CA3h			
046CA4h			
046CA5h	CAN3 Mailbox 10: Data Length		XXh
046CA6h	CAN3 Mailbox 10: Data Field		XXXX XXXX
046CA7h			XXXX XXXXh
046CA8h			
046CA9h			
046CAAh			
046CABh			
046CACh			
046CADh			
046CAEh	CAN3 Mailbox 10: Time Stamp		XXXXh
046CAFh			
046CB0h	CAN3 Mailbox 11: Message Identifier	C3MB11	XXXX XXXXh
046CB1h			
046CB2h			
046CB3h			
046CB4h			
046CB5h	CAN3 Mailbox 11: Data Length		XXh
046CB6h	CAN3 Mailbox 11: Data Field		XXXX XXXX
046CB7h			XXXX XXXXh
046CB8h			
046CB9h			
046CBAh			
046CBBh			
046CBCh			
046CBDh			
046CBEh	CAN3 Mailbox 11: Time Stamp		XXXXh
046CBFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.36 SFR List (36)

Address	Register	Symbol	Reset Value
046CC0h	CAN3 Mailbox 12: Message Identifier	C3MB12	XXXX XXXXh
046CC1h			
046CC2h			
046CC3h			
046CC4h			
046CC5h	CAN3 Mailbox 12: Data Length		XXh
046CC6h	CAN3 Mailbox 12: Data Field		XXXX XXXX
046CC7h			XXXX XXXXh
046CC8h			
046CC9h			
046CCAh			
046CCBh			
046CCCh			
046CCDh			
046CCEh	CAN3 Mailbox 12: Time Stamp		XXXXh
046CCFh			
046CD0h	CAN3 Mailbox 13: Message Identifier	C3MB13	XXXX XXXXh
046CD1h			
046CD2h			
046CD3h			
046CD4h			
046CD5h	CAN3 Mailbox 13: Data Length		XXh
046CD6h	CAN3 Mailbox 13: Data Field		XXXX XXXX
046CD7h			XXXX XXXXh
046CD8h			
046CD9h			
046CDAh			
046CDBh			
046CDCh			
046CDDh			
046CDEh	CAN3 Mailbox 13: Time Stamp		XXXXh
046CDFh			
046CE0h	CAN3 Mailbox 14: Message Identifier	C3MB14	XXXX XXXXh
046CE1h			
046CE2h			
046CE3h			
046CE4h			
046CE5h	CAN3 Mailbox 14: Data Length		XXh
046CE6h	CAN3 Mailbox 14: Data Field		XXXX XXXX
046CE7h			XXXX XXXXh
046CE8h			
046CE9h			
046CEAh			
046CEBh			
046CECh			
046CEDh			
046CEEh	CAN3 Mailbox 14: Time Stamp		XXXXh
046CEFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.37 SFR List (37)

Address	Register	Symbol	Reset Value
046CF0h	CAN3 Mailbox 15: Message Identifier	C3MB15	XXXX XXXXh
046CF1h			
046CF2h			
046CF3h			
046CF4h			
046CF5h	CAN3 Mailbox 15: Data Length		XXh
046CF6h	CAN3 Mailbox 15: Data Field		XXXX XXXX
046CF7h			XXXX XXXXh
046CF8h			
046CF9h			
046CFAh			
046CFBh			
046CFCh			
046CFDh			
046CFEh	CAN3 Mailbox 15: Time Stamp		XXXXh
046CFFh			
046D00h	CAN3 Mailbox 16: Message Identifier	C3MB16	XXXX XXXXh
046D01h			
046D02h			
046D03h			
046D04h			
046D05h	CAN3 Mailbox 16: Data Length		XXh
046D06h	CAN3 Mailbox 16: Data Field		XXXX XXXX
046D07h			XXXX XXXXh
046D08h			
046D09h			
046D0Ah			
046D0Bh			
046D0Ch			
046D0Dh			
046D0Eh	CAN3 Mailbox 16: Time Stamp		XXXXh
046D0Fh			
046D10h	CAN3 Mailbox 17: Message Identifier	C3MB17	XXXX XXXXh
046D11h			
046D12h			
046D13h			
046D14h			
046D15h	CAN3 Mailbox 17: Data Length		XXh
046D16h	CAN3 Mailbox 17: Data Field		XXXX XXXX
046D17h			XXXX XXXXh
046D18h			
046D19h			
046D1Ah			
046D1Bh			
046D1Ch			
046D1Dh			
046D1Eh	CAN3 Mailbox 17: Time Stamp		XXXXh
046D1Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.38 SFR List (38)

Address	Register	Symbol	Reset Value
046D20h	CAN3 Mailbox 18: Message Identifier	C3MB18	XXXX XXXXh
046D21h			
046D22h			
046D23h			
046D24h			
046D25h	CAN3 Mailbox 18: Data Length		XXh
046D26h	CAN3 Mailbox 18: Data Field		XXXX XXXX
046D27h			XXXX XXXXh
046D28h			
046D29h			
046D2Ah			
046D2Bh			
046D2Ch			
046D2Dh			
046D2Eh	CAN3 Mailbox 18: Time Stamp		XXXXh
046D2Fh			
046D30h	CAN3 Mailbox 19: Message Identifier	C3MB19	XXXX XXXXh
046D31h			
046D32h			
046D33h			
046D34h			
046D35h	CAN3 Mailbox 19: Data Length		XXh
046D36h	CAN3 Mailbox 19: Data Field		XXXX XXXX
046D37h			XXXX XXXXh
046D38h			
046D39h			
046D3Ah			
046D3Bh			
046D3Ch			
046D3Dh			
046D3Eh	CAN3 Mailbox 19: Time Stamp		XXXXh
046D3Fh			
046D40h	CAN3 Mailbox 20: Message Identifier	C3MB20	XXXX XXXXh
046D41h			
046D42h			
046D43h			
046D44h			
046D45h	CAN3 Mailbox 20: Data Length		XXh
046D46h	CAN3 Mailbox 20: Data Field		XXXX XXXX
046D47h			XXXX XXXXh
046D48h			
046D49h			
046D4Ah			
046D4Bh			
046D4Ch			
046D4Dh			
046D4Eh	CAN3 Mailbox 20: Time Stamp		XXXXh
046D4Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.39 SFR List (39)

Address	Register	Symbol	Reset Value
046D50h	CAN3 Mailbox 21: Message Identifier	C3MB21	XXXX XXXXh
046D51h			
046D52h			
046D53h			
046D54h			
046D55h	CAN3 Mailbox 21: Data Length		XXh
046D56h	CAN3 Mailbox 21: Data Field		XXXX XXXX
046D57h			XXXX XXXXh
046D58h			
046D59h			
046D5Ah			
046D5Bh			
046D5Ch			
046D5Dh			
046D5Eh	CAN3 Mailbox 21: Time Stamp		XXXXh
046D5Fh			
046D60h	CAN3 Mailbox 22: Message Identifier	C3MB22	XXXX XXXXh
046D61h			
046D62h			
046D63h			
046D64h			
046D65h	CAN3 Mailbox 22: Data Length		XXh
046D66h	CAN3 Mailbox 22: Data Field		XXXX XXXX
046D67h			XXXX XXXXh
046D68h			
046D69h			
046D6Ah			
046D6Bh			
046D6Ch			
046D6Dh			
046D6Eh	CAN3 Mailbox 22: Time Stamp		XXXXh
046D6Fh			
046D70h	CAN3 Mailbox 23: Message Identifier	C3MB23	XXXX XXXXh
046D71h			
046D72h			
046D73h			
046D74h			
046D75h	CAN3 Mailbox 23: Data Length		XXh
046D76h	CAN3 Mailbox 23: Data Field		XXXX XXXX
046D77h			XXXX XXXXh
046D78h			
046D79h			
046D7Ah			
046D7Bh			
046D7Ch			
046D7Dh			
046D7Eh	CAN3 Mailbox 23: Time Stamp		XXXXh
046D7Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.40 SFR List (40)

Address	Register	Symbol	Reset Value
046D80h	CAN3 Mailbox 24: Message Identifier	C3MB24	XXXX XXXXh
046D81h			
046D82h			
046D83h			
046D84h			
046D85h	CAN3 Mailbox 24: Data Length		XXh
046D86h	CAN3 Mailbox 24: Data Field		XXXX XXXX
046D87h			XXXX XXXXh
046D88h			
046D89h			
046D8Ah			
046D8Bh			
046D8Ch			
046D8Dh			
046D8Eh	CAN3 Mailbox 24: Time Stamp		XXXXh
046D8Fh			
046D90h	CAN3 Mailbox 25: Message Identifier	C3MB25	XXXX XXXXh
046D91h			
046D92h			
046D93h			
046D94h			
046D95h	CAN3 Mailbox 25: Data Length		XXh
046D96h	CAN3 Mailbox 25: Data Field		XXXX XXXX
046D97h			XXXX XXXXh
046D98h			
046D99h			
046D9Ah			
046D9Bh			
046D9Ch			
046D9Dh			
046D9Eh	CAN3 Mailbox 25: Time Stamp		XXXXh
046D9Fh			
046DA0h	CAN3 Mailbox 26: Message Identifier	C3MB26	XXXX XXXXh
046DA1h			
046DA2h			
046DA3h			
046DA4h			
046DA5h	CAN3 Mailbox 26: Data Length		XXh
046DA6h	CAN3 Mailbox 26: Data Field		XXXX XXXX
046DA7h			XXXX XXXXh
046DA8h			
046DA9h			
046DAAh			
046DABh			
046DACh			
046DADh			
046DAEh	CAN3 Mailbox 26: Time Stamp		XXXXh
046DAFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.41 SFR List (41)

Address	Register	Symbol	Reset Value
046DB0h	CAN3 Mailbox 27: Message Identifier	C3MB27	XXXX XXXXh
046DB1h			
046DB2h			
046DB3h			
046DB4h			
046DB5h	CAN3 Mailbox 27: Data Length		XXh
046DB6h	CAN3 Mailbox 27: Data Field		XXXX XXXX
046DB7h			XXXX XXXXh
046DB8h			
046DB9h			
046DBAh			
046DBBh			
046DBCh			
046DBDh			
046DBEh	CAN3 Mailbox 27: Time Stamp		XXXXh
046DBFh			
046DC0h	CAN3 Mailbox 28: Message Identifier	C3MB28	XXXX XXXXh
06DC1h			
046DC2h			
046DC3h			
046DC4h			
046DC5h	CAN3 Mailbox 28: Data Length		XXh
046DC6h	CAN3 Mailbox 28: Data Field		XXXX XXXX
046DC7h			XXXX XXXXh
046DC8h			
046DC9h			
046DCAh			
046DCBh			
046DCCh			
046DCDh			
046DCEh	CAN3 Mailbox 28: Time Stamp		XXXXh
046DCFh			
046DD0h	CAN3 Mailbox 29: Message Identifier	C3MB29	XXXX XXXXh
046DD1h			
046DD2h			
046DD3h			
046DD4h			
046DD5h	CAN3 Mailbox 29: Data Length		XXh
046DD6h	CAN3 Mailbox 29: Data Field		XXXX XXXX
046DD7h			XXXX XXXXh
046DD8h			
046DD9h			
046DDAh			
046DDBh			
046DDCh			
046DDDh			
046DDEh	CAN3 Mailbox 29: Time Stamp		XXXXh
046DDFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.42 SFR List (42)

Address	Register	Symbol	Reset Value
046DE0h	CAN3 Mailbox 30: Message Identifier	C3MB30	XXXX XXXXh
046DE1h			
046DE2h			
046DE3h			
046DE4h			
046DE5h	CAN3 Mailbox 30: Data Length		XXh
046DE6h	CAN3 Mailbox 30: Data Field		XXXX XXXX
046DE7h			XXXX XXXXh
046DE8h			
046DE9h			
046DEAh			
046DEBh			
046DECh			
046DEDh			
046DEEh	CAN3 Mailbox 30: Time Stamp		XXXXh
046DEFh			
046DF0h	CAN3 Mailbox 31: Message Identifier	C3MB31	XXXX XXXXh
046DF1h			
046DF2h			
046DF3h			
046DF4h			
046DF5h	CAN3 Mailbox 31: Data Length		XXh
046DF6h	CAN3 Mailbox 31: Data Field		XXXX XXXX
046DF7h			XXXX XXXXh
046DF8h			
046DF9h			
046DFAh			
046DFBh			
046DFCh			
046DFDh			
046DFEh	CAN3 Mailbox 31: Time Stamp		XXXXh
046DFFh			
046E00h	CAN3 Acceptance Mask Register 0	C3MKR0	XXXX XXXXh
046E01h			
046E02h			
046E03h			
046E04h	CAN3 Acceptance Mask Register 1	C3MKR1	XXXX XXXXh
046E05h			
046E06h			
046E07h			
046E08h	CAN3 Acceptance Mask Register 2	C3MKR2	XXXX XXXXh
046E09h			
046E0Ah			
046E0Bh			
046E0Ch	CAN3 Acceptance Mask Register 3	C3MKR 3	XXXX XXXXh
046E0Dh			
046E0Eh			
046E0Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.43 SFR List (43)

Address	Register	Symbol	Reset Value
046E10h	CAN3 Acceptance Mask Register 4	C3MKR4	XXXX XXXXh
046E11h			
046E12h			
046E13h			
046E14h	CAN3 Acceptance Mask Register 5	C3MKR5	XXXX XXXXh
046E15h			
046E16h			
046E17h			
046E18h	CAN3 Acceptance Mask Register 6	C3MKR6	XXXX XXXXh
046E19h			
046E2Ah			
046E2Bh			
046E2Ch	CAN3 Acceptance Mask Register 7	C3MKR7	XXXX XXXXh
046E2Dh			
046E2Eh			
0462EFh			
046E20h	CAN3 FIFO Received ID Compare Register 0	C3FIDCR0	XXXX XXXXh
046E21h			
046E22h			
046E23h			
046E24h	CAN3 FIFO Received ID Compare Register 1	C3FIDCR1	XXXX XXXXh
046E25h			
046E26h			
046E27h			
046E28h	CAN3 Mask Invalid Register	C3MKIVLR	XXXX XXXXh
046E29h			
046E2Ah			
046E2Bh			
046E2Ch	CAN3 Mailbox Interrupt Enable Register	C3MIER	XXXX XXXXh
046E2Dh			
046E2Eh			
046E2Fh			
046E30h			
046E31h			
046E32h			
046E33h			
046E34h			
046E35h			
046E36h			
046E37h			
046E38h			
046E39h			
046E3Ah			
046E3Bh			
046E3Ch			
046E3Dh			
046E3Eh			
046E3Fh			
046E40h to 046F1Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.44 SFR List (44)

Address	Register	Symbol	Reset Value
046F20h	CAN3 Message Control Register 0	C3MCTL0	00h
046F21h	CAN3 Message Control Register 1	C3MCTL1	00h
046F22h	CAN3 Message Control Register 2	C3MCTL2	00h
046F23h	CAN3 Message Control Register 3	C3MCTL3	00h
046F24h	CAN3 Message Control Register 4	C3MCTL4	00h
046F25h	CAN3 Message Control Register 5	C3MCTL5	00h
046F26h	CAN3 Message Control Register 6	C3MCTL6	00h
046F27h	CAN3 Message Control Register 7	C3MCTL7	00h
046F28h	CAN3 Message Control Register 8	C3MCTL8	00h
046F29h	CAN3 Message Control Register 9	C3MCTL9	00h
046F2Ah	CAN3 Message Control Register 10	C3MCTL10	00h
046F2Bh	CAN3 Message Control Register 11	C3MCTL11	00h
046F2Ch	CAN3 Message Control Register 12	C3MCTL12	00h
046F2Dh	CAN3 Message Control Register 13	C3MCTL13	00h
046F2Eh	CAN3 Message Control Register 14	C3MCTL14	00h
046F2Fh	CAN3 Message Control Register 15	C3MCTL15	00h
046F30h	CAN3 Message Control Register 16	C3MCTL16	00h
046F31h	CAN3 Message Control Register 17	C3MCTL17	00h
046F32h	CAN3 Message Control Register 18	C3MCTL18	00h
046F33h	CAN3 Message Control Register 19	C3MCTL19	00h
046F34h	CAN3 Message Control Register 20	C3MCTL20	00h
046F35h	CAN3 Message Control Register 21	C3MCTL21	00h
046F36h	CAN3 Message Control Register 22	C3MCTL22	00h
046F37h	CAN3 Message Control Register 23	C3MCTL23	00h
046F38h	CAN3 Message Control Register 24	C3MCTL24	00h
046F39h	CAN3 Message Control Register 25	C3MCTL25	00h
046F3Ah	CAN3 Message Control Register 26	C3MCTL26	00h
046F3Bh	CAN3 Message Control Register 27	C3MCTL27	00h
046F3Ch	CAN3 Message Control Register 28	C3MCTL28	00h
046F3Dh	CAN3 Message Control Register 29	C3MCTL29	00h
046F3Eh	CAN3 Message Control Register 30	C3MCTL30	00h
046F3Fh	CAN3 Message Control Register 31	C3MCTL31	00h

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.45 SFR List (45)

Address	Register	Symbol	Reset Value
046F40h	CAN3 Control Register	C3CTLR	0000 0101b
046F41h			0000 0000b
046F42h	CAN3 Status Register	C3STR	0000 0101b
046F43h			0000 0000b
046F44h	CAN3 Bit Configuration Register	C3BCR	00 0000h
046F45h			
046F46h			
046F47h	CAN3 Clock Select Register	C3CLKR	000X 0000b
046F48h	CAN3 Receive FIFO Control Register	C3RFCR	1000 0000b
046F49h	CAN3 Receive FIFO Pointer Control Register	C3RFPCR	XXh
046F4Ah	CAN3 Transmit FIFO Control Register	C3TFCR	1000 0000b
046F4Bh	CAN3 Transmit FIFO Pointer Control Register	C3TFPCR	XXh
046F4Ch	CAN3 Error Interrupt Enable Register	C3EIER	00h
046F4Dh	CAN3 Error Interrupt Factor Judge Register	C3EIFR	00h
046F4Eh	CAN3 Receive Error Count Register	C3RECR	00h
046F4Fh	CAN3 Transmit Error Count Register	C3TECR	00h
046F50h	CAN3 Error Code Store Register	C3ECSR	00h
046F51h	CAN3 Channel Search Support Register	C3CSSR	XXh
046F52h	CAN3 Mailbox Search Status Register	C3MSSR	1000 0000b
046F53h	CAN3 Mailbox Search Mode Register	C3MSMR	XXXX XX00b
046F54h	CAN3 Time Stamp Register	C3TSR	0000h
046F55h			
046F56h	CAN3 Acceptance Filter Support Register	C3AFSR	XXXXh
046F57h			
046F58h	CAN3 Test Control Register	C3TCR	00h
046F59h			
046F5Ah			
046F5Bh			
046F5Ch			
046F5Dh			
046F5Eh			
046F5Fh			
046F60h to 0473FFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.46 SFR List (46)

Address	Register	Symbol	Reset Value
047400h	CAN2 Mailbox 0: Message Identifier	C2MB0	XXXX XXXXh
047401h			
047402h			
047403h			
047404h			
047405h	CAN2 Mailbox 0: Data Length		XXh
047406h	CAN2 Mailbox 0: Data Field		XXXX XXXX
047407h			XXXX XXXXh
047408h			
047409h			
04740Ah			
04740Bh			
04740Ch			
04740Dh			
04740Eh	CAN2 Mailbox 0: Time Stamp		XXXXh
04740Fh			
047410h	CAN2 Mailbox 1: Message Identifier	C2MB1	XXXX XXXXh
047411h			
047412h			
047413h			
047414h			
047415h	CAN2 Mailbox 1: Data Length		XXh
047416h	CAN2 Mailbox 1: Data Field		XXXX XXXX
047417h			XXXX XXXXh
047418h			
047419h			
04741Ah			
04741Bh			
04741Ch			
04741Dh			
04741Eh	CAN2 Mailbox 1: Time Stamp		XXXXh
04741Fh			
047420h	CAN2 Mailbox 2: Message Identifier	C2MB2	XXXX XXXXh
047421h			
047422h			
047423h			
047424h			
047425h	CAN2 Mailbox 2: Data Length		XXh
047426h	CAN2 Mailbox 2: Data Field		XXXX XXXX
047427h			XXXX XXXXh
047428h			
047429h			
04742Ah			
04742Bh			
04742Ch			
04742Dh			
04742Eh	CAN2 Mailbox 2: Time Stamp		XXXXh
04742Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.47 SFR List (47)

Address	Register	Symbol	Reset Value
047430h	CAN2 Mailbox 3: Message Identifier	C2MB3	XXXX XXXXh
047431h			
047432h			
047433h			
047434h			
047435h	CAN2 Mailbox 3: Data Length		XXh
047436h	CAN2 Mailbox 3: Data Field		XXXX XXXX
047437h			XXXX XXXXh
047438h			
047439h			
04743Ah			
04743Bh			
04743Ch			
04743Dh			
04743Eh	CAN2 Mailbox 3: Time Stamp		XXXXh
04743Fh			
047440h	CAN2 Mailbox 4: Message Identifier	C2MB4	XXXX XXXXh
047441h			
047442h			
047443h			
047444h			
047445h	CAN2 Mailbox 4: Data Length		XXh
047446h	CAN2 Mailbox 4: Data Field		XXXX XXXX
047447h			XXXX XXXXh
047448h			
047449h			
04744Ah			
04744Bh			
04744Ch			
04744Dh			
04744Eh	CAN2 Mailbox 4: Time Stamp		XXXXh
04744Fh			
047450h	CAN2 Mailbox 5: Message Identifier	C2MB5	XXXX XXXXh
047451h			
047452h			
047453h			
047454h			
047455h	CAN2 Mailbox 5: Data Length		XXh
047456h	CAN2 Mailbox 5: Data Field		XXXX XXXX
047457h			XXXX XXXXh
047458h			
047459h			
04745Ah			
04745Bh			
04745Ch			
04745Dh			
04745Eh	CAN2 Mailbox 5: Time Stamp		XXXXh
04745Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.48 SFR List (48)

Address	Register	Symbol	Reset Value
047460h	CAN2 Mailbox 6: Message Identifier	C2MB6	XXXX XXXXh
047461h			
047462h			
047463h			
047464h			
047465h	CAN2 Mailbox 6: Data Length		XXh
047466h	CAN2 Mailbox 6: Data Field		XXXX XXXX
047467h			XXXX XXXXh
047468h			
047469h			
04746Ah			
04746Bh			
04746Ch			
04746Dh			
04746Eh	CAN2 Mailbox 6: Time Stamp		XXXXh
04746Fh			
047470h	CAN2 Mailbox 7: Message Identifier	C2MB7	XXXX XXXXh
047471h			
047472h			
047473h			
047474h			
047475h	CAN2 Mailbox 7: Data Length		XXh
047476h	CAN2 Mailbox 7: Data Field		XXXX XXXX
047477h			XXXX XXXXh
047478h			
047479h			
04747Ah			
04747Bh			
04747Ch			
04747Dh			
04747Eh	CAN2 Mailbox 7: Time Stamp		XXXXh
04747Fh			
047480h	CAN2 Mailbox 8: Message Identifier	C2MB8	XXXX XXXXh
047481h			
047482h			
047483h			
047484h			
047485h	CAN2 Mailbox 8: Data Length		XXh
047486h	CAN2 Mailbox 8: Data Field		XXXX XXXX
047487h			XXXX XXXXh
047488h			
047489h			
04748Ah			
04748Bh			
04748Ch			
04748Dh			
04748Eh	CAN2 Mailbox 8: Time Stamp		XXXXh
04748Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.49 SFR List (49)

Address	Register	Symbol	Reset Value
047490h	CAN2 Mailbox 9: Message Identifier	C2MB9	XXXX XXXXh
047491h			
047492h			
047493h			
047494h			
047495h	CAN2 Mailbox 9: Data Length		XXh
047496h	CAN2 Mailbox 9: Data Field		XXXX XXXX
047497h			XXXX XXXXh
047498h			
047499h			
04749Ah			
04749Bh			
04749Ch			
04749Dh			
04749Eh	CAN2 Mailbox 9: Time Stamp		XXXXh
04749Fh			
0474A0h	CAN2 Mailbox 10: Message Identifier	C2MB10	XXXX XXXXh
0474A1h			
0474A2h			
0474A3h			
0474A4h			
0474A5h	CAN2 Mailbox 10: Data Length		XXh
0474A6h	CAN2 Mailbox 10: Data Field		XXXX XXXX
0474A7h			XXXX XXXXh
0474A8h			
0474A9h			
0474AAh			
0474ABh			
0474ACh			
0474ADh			
0474AEh	CAN2 Mailbox 10: Time Stamp		XXXXh
0474AFh			
0474B0h	CAN2 Mailbox 11: Message Identifier	C2MB11	XXXX XXXXh
0474B1h			
0474B2h			
0474B3h			
0474B4h			
0474B5h	CAN2 Mailbox 11: Data Length		XXh
0474B6h	CAN2 Mailbox 11: Data Field		XXXX XXXX
0474B7h			XXXX XXXXh
0474B8h			
0474B9h			
0474BAh			
0474BBh			
0474BCh			
0474BDh			
0474BEh	CAN2 Mailbox 11: Time Stamp		XXXXh
0474BFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.50 SFR List (50)

Address	Register	Symbol	Reset Value
0474C0h	CAN2 Mailbox 12: Message Identifier	C2MB12	XXXX XXXXh
0474C1h			
0474C2h			
0474C3h			
0474C4h			
0474C5h	CAN2 Mailbox 12: Data Length		XXh
0474C6h	CAN2 Mailbox 12: Data Field		XXXX XXXX
0474C7h			XXXX XXXXh
0474C8h			
0474C9h			
0474CAh			
0474CBh			
0474CCh			
0474CDh			
0474CEh	CAN2 Mailbox 12: Time Stamp		XXXXh
0474CFh			
0474D0h	CAN2 Mailbox 13: Message Identifier	C2MB13	XXXX XXXXh
0474D1h			
0474D2h			
0474D3h			
0474D4h			
0474D5h	CAN2 Mailbox 13: Data Length		XXh
0474D6h	CAN2 Mailbox 13: Data Field		XXXX XXXX
0474D7h			XXXX XXXXh
0474D8h			
0474D9h			
0474DAh			
0474DBh			
0474DCh			
0474DDh			
0474DEh	CAN2 Mailbox 13: Time Stamp		XXXXh
0474DFh			
0474E0h	CAN2 Mailbox 14: Message Identifier	C2MB14	XXXX XXXXh
0474E1h			
0474E2h			
0474E3h			
0474E4h			
0474E5h	CAN2 Mailbox 14: Data Length		XXh
0474E6h	CAN2 Mailbox 14: Data Field		XXXX XXXX
0474E7h			XXXX XXXXh
0474E8h			
0474E9h			
0474EAh			
0474EBh			
0474ECh			
0474EDh			
0474EEh	CAN2 Mailbox 14: Time Stamp		XXXXh
0474EFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.51 SFR List (51)

Address	Register	Symbol	Reset Value
0474F0h	CAN2 Mailbox 15: Message Identifier	C2MB15	XXXX XXXXh
0474F1h			
0474F2h			
0474F3h			
0474F4h			
0474F5h	CAN2 Mailbox 15: Data Length		XXh
0474F6h	CAN2 Mailbox 15: Data Field		XXXX XXXX
0474F7h			XXXX XXXXh
0474F8h			
0474F9h			
0474FAh			
0474FBh			
0474FCh			
0474FDh			
0474FEh	CAN2 Mailbox 15: Time Stamp		XXXXh
0474FFh			
047500h	CAN2 Mailbox 16: Message Identifier	C2MB16	XXXX XXXXh
047501h			
047502h			
047503h			
047504h			
047505h	CAN2 Mailbox 16: Data Length		XXh
047506h	CAN2 Mailbox 16: Data Field		XXXX XXXX
047507h			XXXX XXXXh
047508h			
047509h			
04750Ah			
04750Bh			
04750Ch			
04750Dh			
04750Eh	CAN2 Mailbox 16: Time Stamp		XXXXh
04750Fh			
047510h	CAN2 Mailbox 17: Message Identifier	C2MB17	XXXX XXXXh
047511h			
047512h			
047513h			
047514h			
047515h	CAN2 Mailbox 17: Data Length		XXh
047516h	CAN2 Mailbox 17: Data Field		XXXX XXXX
047517h			XXXX XXXXh
047518h			
047519h			
04751Ah			
04751Bh			
04751Ch			
04751Dh			
04751Eh	CAN2 Mailbox 17: Time Stamp		XXXXh
04751Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.52 SFR List (52)

Address	Register	Symbol	Reset Value
047520h	CAN2 Mailbox 18: Message Identifier	C2MB18	XXXX XXXXh
047521h			
047522h			
047523h			
047524h			
047525h	CAN2 Mailbox 18: Data Length		XXh
047526h	CAN2 Mailbox 18: Data Field		XXXX XXXX
047527h			XXXX XXXXh
047528h			
047529h			
04752Ah			
04752Bh			
04752Ch			
04752Dh			
04752Eh	CAN2 Mailbox 18: Time Stamp		XXXXh
04752Fh			
047530h	CAN2 Mailbox 19: Message Identifier	C2MB19	XXXX XXXXh
047531h			
047532h			
047533h			
047534h			
047535h	CAN2 Mailbox 19: Data Length		XXh
047536h	CAN2 Mailbox 19: Data Field		XXXX XXXX
047537h			XXXX XXXXh
047538h			
047539h			
04753Ah			
04753Bh			
04753Ch			
04753Dh			
04753Eh	CAN2 Mailbox 19: Time Stamp		XXXXh
04753Fh			
047540h	CAN2 Mailbox 20: Message Identifier	C2MB20	XXXX XXXXh
047541h			
047542h			
047543h			
047544h			
047545h	CAN2 Mailbox 20: Data Length		XXh
047546h	CAN2 Mailbox 20: Data Field		XXXX XXXX
047547h			XXXX XXXXh
047548h			
047549h			
04754Ah			
04754Bh			
04754Ch			
04754Dh			
04754Eh	CAN2 Mailbox 20: Time Stamp		XXXXh
04754Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.53 SFR List (53)

Address	Register	Symbol	Reset Value
047550h	CAN2 Mailbox 21: Message Identifier	C2MB21	XXXX XXXXh
047551h			
047552h			
047553h			
047554h			
047555h	CAN2 Mailbox 21: Data Length		XXh
047556h	CAN2 Mailbox 21: Data Field		XXXX XXXX
047557h			XXXX XXXXh
047558h			
047559h			
04755Ah			
04755Bh			
04755Ch			
04755Dh			
04755Eh	CAN2 Mailbox 21: Time Stamp		XXXXh
04755Fh			
047560h	CAN2 Mailbox 22: Identifier	C2MB22	XXXX XXXXh
047561h			
047562h			
047563h			
047564h			
047565h	CAN2 Mailbox 22: Data Length		XXh
047566h	CAN2 Mailbox 22: Data Field		XXXX XXXX
047567h			XXXX XXXXh
047568h			
047569h			
04756Ah			
04756Bh			
04756Ch			
04756Dh			
04756Eh	CAN2 Mailbox 22: Time Stamp		XXXXh
04756Fh			
047570h	CAN2 Mailbox 23: Message Identifier	C2MB23	XXXX XXXXh
047571h			
047572h			
047573h			
047574h			
047575h	CAN2 Mailbox 23: Data Length		XXh
047576h	CAN2 Mailbox 23: Data Field		XXXX XXXX
047577h			XXXX XXXXh
047578h			
047579h			
04757Ah			
04757Bh			
04757Ch			
04757Dh			
04757Eh	CAN2 Mailbox 23: Time Stamp		XXXXh
04757Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.54 SFR List (54)

Address	Register	Symbol	Reset Value
047580h	CAN2 Mailbox 24: Message Identifier	C2MB24	XXXX XXXXh
047581h			
047582h			
047583h			
047584h			
047585h	CAN2 Mailbox 24: Data Length		XXh
047586h	CAN2 Mailbox 24: Data Field		XXXX XXXX
047587h			XXXX XXXXh
047588h			
047589h			
04758Ah			
04758Bh			
04758Ch			
04758Dh			
04758Eh	CAN2 Mailbox 24: Time Stamp		XXXXh
04758Fh			
047590h	CAN2 Mailbox 25: Message Identifier	C2MB25	XXXX XXXXh
047591h			
047592h			
047593h			
047594h			
047595h	CAN2 Mailbox 25: Data Length		XXh
047596h	CAN2 Mailbox 25: Data Field		XXXX XXXX
047597h			XXXX XXXXh
047598h			
047599h			
04759Ah			
04759Bh			
04759Ch			
04759Dh			
04759Eh	CAN2 Mailbox 25: Time Stamp		XXXXh
04759Fh			
0475A0h	CAN2 Mailbox 26: Message Identifier	C2MB26	XXXX XXXXh
0475A1h			
0475A2h			
0475A3h			
0475A4h			
0475A5h	CAN2 Mailbox 26: Data Length		XXh
0475A6h	CAN2 Mailbox 26: Data Field		XXXX XXXX
0475A7h			XXXX XXXXh
0475A8h			
0475A9h			
0475AAh			
0475ABh			
0475ACh			
0475ADh			
0475AEh	CAN2 Mailbox 26: Time Stamp		XXXXh
0475AFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.55 SFR List (55)

Address	Register	Symbol	Reset Value
0475B0h	CAN2 Mailbox 27: Message Identifier	C2MB27	XXXX XXXXh
0475B1h			
0475B2h			
0475B3h			
0475B4h			
0475B5h	CAN2 Mailbox 27: Data Length		XXh
0475B6h	CAN2 Mailbox 27: Data Field		XXXX XXXX
0475B7h			XXXX XXXXh
0475B8h			
0475B9h			
0475BAh			
0475BBh			
0475BCh			
0475BDh			
0475BEh	CAN2 Mailbox 27: Time Stamp		XXXXh
0475BFh			
0475C0h	CAN2 Mailbox 28: Message Identifier	C2MB28	XXXX XXXXh
0475C1h			
0475C2h			
0475C3h			
0475C4h			
0475C5h	CAN2 Mailbox 28: Data Length		XXh
0475C6h	CAN2 Mailbox 28: Data Field		XXXX XXXX
0475C7h			XXXX XXXXh
0475C8h			
0475C9h			
0475CAh			
0475CBh			
0475CCh			
0475CDh			
0475CEh	CAN2 Mailbox 28: Time Stamp		XXXXh
0475CFh			
0475D0h	CAN2 Mailbox 29: Message Identifier	C2MB29	XXXX XXXXh
0475D1h			
0475D2h			
0475D3h			
0475D4h			
0475D5h	CAN2 Mailbox 29: Data Length		XXh
0475D6h	CAN2 Mailbox 29: Data Field		XXXX XXXX
0475D7h			XXXX XXXXh
0475D8h			
0475D9h			
0475DAh			
0475DBh			
0475DCh			
0475DDh			
0475DEh	CAN2 Mailbox 29: Time Stamp		XXXXh
0475DFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.56 SFR List (56)

Address	Register	Symbol	Reset Value
0475E0h	CAN2 Mailbox 30: Message Identifier	C2MB30	XXXX XXXXh
0475E1h			
0475E2h			
0475E3h			
0475E4h			
0475E5h	CAN2 Mailbox 30: Data Length		XXh
0475E6h	CAN2 Mailbox 30: Data Field		XXXX XXXX
0475E7h			XXXX XXXXh
0475E8h			
0475E9h			
0475EAh			
0475EBh			
0475ECh			
0475EDh			
0475EEh	CAN2 Mailbox 30: Time Stamp		XXXXh
0475EFh			
0475F0h	CAN2 Mailbox 31: Message Identifier	C2MB31	XXXX XXXXh
0475F1h			
0475F2h			
0475F3h			
0475F4h			
0475F5h	CAN2 Mailbox 31: Data Length		XXh
0475F6h	CAN2 Mailbox 31: Data Field		XXXX XXXX
0475F7h			XXXX XXXXh
0475F8h			
0475F9h			
0475FAh			
0475FBh			
0475FCh			
0475FDh			
0475FEh	CAN2 Mailbox 31: Time Stamp		XXXXh
0475FFh			
047600h	CAN2 Acceptance Mask Register 0	C2MKR0	XXXX XXXXh
047601h			
047602h			
047603h			
047604h	CAN2 Acceptance Mask Register 1	C2MKR1	XXXX XXXXh
047605h			
047606h			
047607h			
047608h	CAN2 Acceptance Mask Register 2	C2MKR2	XXXX XXXXh
047609h			
04760Ah			
04760Bh			
04760Ch	CAN2 Acceptance Mask Register 3	C2MKR3	XXXX XXXXh
04760Dh			
04760Eh			
04760Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.57 SFR List (57)

Address	Register	Symbol	Reset Value
047610h	CAN2 Acceptance Mask Register 4	C2MKR4	XXXX XXXXh
047611h			
047612h			
047613h			
047614h	CAN2 Acceptance Mask Register 5	C2MKR5	XXXX XXXXh
047615h			
047616h			
047617h			
047618h	CAN2 Acceptance Mask Register 6	C2MKR6	XXXX XXXXh
047619h			
04761Ah			
04761Bh			
04761Ch	CAN2 Acceptance Mask Register 7	C2MKR7	XXXX XXXXh
04761Dh			
04761Eh			
04761Fh			
047620h	CAN2 FIFO Received ID Compare Register 0	C2FIDCR0	XXXX XXXXh
047621h			
047622h			
047623h			
047624h	CAN2 FIFO Received ID Compare Register 1	C2FIDCR1	XXXX XXXXh
047625h			
047626h			
047627h			
047628h	CAN2 Mask Invalid Register	C2MKIVLR	XXXX XXXXh
047629h			
04762Ah			
04762Bh			
04762Ch	CAN2 Mailbox Interrupt Enable Register	C2MIER	XXXX XXXXh
04762Dh			
04762Eh			
04762Fh			
047630h			
047631h			
047632h			
047633h			
047634h			
047635h			
047636h			
047637h			
047638h			
047639h			
04763Ah			
04763Bh			
04763Ch			
04763Dh			
04763Eh			
04763Fh			
047640h to 04771Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.58 SFR List (58)

Address	Register	Symbol	Reset Value
047720h	CAN2 Message Control Register 0	C2MCTL0	00h
047721h	CAN2 Message Control Register 1	C2MCTL1	00h
047722h	CAN2 Message Control Register 2	C2MCTL2	00h
047723h	CAN2 Message Control Register 3	C2MCTL3	00h
047724h	CAN2 Message Control Register 4	C2MCTL4	00h
047725h	CAN2 Message Control Register 5	C2MCTL5	00h
047726h	CAN2 Message Control Register 6	C2MCTL6	00h
047727h	CAN2 Message Control Register 7	C2MCTL7	00h
047728h	CAN2 Message Control Register 8	C2MCTL8	00h
047729h	CAN2 Message Control Register 9	C2MCTL9	00h
04772Ah	CAN2 Message Control Register 10	C2MCTL10	00h
04772Bh	CAN2 Message Control Register 11	C2MCTL11	00h
04772Ch	CAN2 Message Control Register 12	C2MCTL12	00h
04772Dh	CAN2 Message Control Register 13	C2MCTL13	00h
04772Eh	CAN2 Message Control Register 14	C2MCTL14	00h
04772Fh	CAN2 Message Control Register 15	C2MCTL15	00h
047730h	CAN2 Message Control Register 16	C2MCTL16	00h
047731h	CAN2 Message Control Register 17	C2MCTL17	00h
047732h	CAN2 Message Control Register 18	C2MCTL18	00h
047733h	CAN2 Message Control Register 19	C2MCTL19	00h
047734h	CAN2 Message Control Register 20	C2MCTL20	00h
047735h	CAN2 Message Control Register 21	C2MCTL21	00h
047736h	CAN2 Message Control Register 22	C2MCTL22	00h
047737h	CAN2 Message Control Register 23	C2MCTL23	00h
047738h	CAN2 Message Control Register 24	C2MCTL24	00h
047739h	CAN2 Message Control Register 25	C2MCTL25	00h
04773Ah	CAN2 Message Control Register 26	C2MCTL26	00h
04773Bh	CAN2 Message Control Register 27	C2MCTL27	00h
04773Ch	CAN2 Message Control Register 28	C2MCTL28	00h
04773Dh	CAN2 Message Control Register 29	C2MCTL29	00h
04773Eh	CAN2 Message Control Register 30	C2MCTL30	00h
04773Fh	CAN2 Message Control Register 31	C2MCTL31	00h

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.59 SFR List (59)

Address	Register	Symbol	Reset Value
047740h	CAN2 Control Register	C2CTLR	0000 0101b
047741h			0000 0000b
047742h	CAN2 Status Register	C2STR	0000 0101b
047743h			0000 0000b
047744h	CAN2 Bit Configuration Register	C2BCR	00 0000h
047745h			
047746h			
047747h	CAN2 Clock Select Register	C2CLKR	000X 0000b
047748h	CAN2 Receive FIFO Control Register	C2RFCR	1000 0000b
047749h	CAN2 Receive FIFO Pointer Control Register	C2RFPCR	XXh
04774Ah	CAN2 Transmit FIFO Control Register	C2TFCR	1000 0000b
04774Bh	CAN2 Transmit FIFO Pointer Control Register	C2TFPCR	XXh
04774Ch	CAN2 Error Interrupt Enable Register	C2EIER	00h
04774Dh	CAN2 Error Interrupt Factor Judge Register	C2EIFR	00h
04774Eh	CAN2 Receive Error Count Register	C2RECR	00h
04774Fh	CAN2 Transmit Error Count Register	C2TECR	00h
047750h	CAN2 Error Code Store Register	C2ECSR	00h
047751h	CAN2 Channel Search Support Register	C2CSSR	XXh
047752h	CAN2 Mailbox Search Status Register	C2MSSR	1000 0000b
047753h	CAN2 Mailbox Search Mode Register	C2MSMR	XXXX XX00b
047754h	CAN2 Time Stamp Register	C2TSR	0000h
047755h			
047756h	CAN2 Acceptance Filter Support Register	C2AFSR	XXXXh
047757h			
047758h	CAN2 Test Control Register	C2TCR	00h
047759h			
04775Ah			
04775Bh			
04775Ch			
04775Dh			
04775Eh			
04775Fh			
047760h to 0477FFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.60 SFR List (60)

Address	Register	Symbol	Reset Value
047800h	CAN1 Mailbox 0: Message Identifier	C1MB0	XXXX XXXXh
047801h			
047802h			
047803h			
047804h			
047805h	CAN1 Mailbox 0: Data Length		XXh
047806h	CAN1 Mailbox 0: Data Field		XXXX XXXX
047807h			XXXX XXXXh
047808h			
047809h			
04780Ah			
04780Bh			
04780Ch			
04780Dh			
04780Eh	CAN1 Mailbox 0: Time Stamp		XXXXh
04780Fh			
047810h	CAN1 Mailbox 1: Message Identifier	C1MB1	XXXX XXXXh
047811h			
047812h			
047813h			
047814h			
047815h	CAN1 Mailbox 1: Data Length		XXh
047816h	CAN1 Mailbox 1: Data Field		XXXX XXXX
047817h			XXXX XXXXh
047818h			
047819h			
04781Ah			
04781Bh			
04781Ch			
04781Dh			
04781Eh	CAN1 Mailbox 1: Time Stamp		XXXXh
04781Fh			
047820h	CAN1 Mailbox 2: Message Identifier	C1MB2	XXXX XXXXh
047821h			
047822h			
047823h			
047824h			
047825h	CAN1 Mailbox 2: Data Length		XXh
047826h	CAN1 Mailbox 2: Data Field		XXXX XXXX
047827h			XXXX XXXXh
047828h			
047829h			
04782Ah			
04782Bh			
04782Ch			
04782Dh			
04782Eh	CAN1 Mailbox 2: Time Stamp		XXXXh
04782Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.61 SFR List (61)

Address	Register	Symbol	Reset Value
047830h	CAN1 Mailbox 3: Message Identifier	C1MB3	XXXX XXXXh
047831h			
047832h			
047833h			
047834h			
047835h	CAN1 Mailbox 3: Data Length		XXh
047836h	CAN1 Mailbox 3: Data Field		XXXX XXXX
047837h			XXXX XXXXh
047838h			
047839h			
04783Ah			
04783Bh			
04783Ch			
04783Dh			
04783Eh	CAN1 Mailbox 3: Time Stamp		XXXXh
04783Fh			
047840h	CAN1 Mailbox 4: Message Identifier	C1MB4	XXXX XXXXh
047841h			
047842h			
047843h			
047844h			
047845h	CAN1 Mailbox 4: Data Length		XXh
047846h	CAN1 Mailbox 4: Data Field		XXXX XXXX
047847h			XXXX XXXXh
047848h			
047849h			
04784Ah			
04784Bh			
04784Ch			
04784Dh			
04784Eh	CAN1 Mailbox 4: Time Stamp		XXXXh
04784Fh			
047850h	CAN1 Mailbox 5: Message Identifier	C1MB5	XXXX XXXXh
047851h			
047852h			
047853h			
047854h			
047855h	CAN1 Mailbox 5: Data Length		XXh
047856h	CAN1 Mailbox 5: Data Field		XXXX XXXX
047857h			XXXX XXXXh
047858h			
047859h			
04785Ah			
04785Bh			
04785Ch			
04785Dh			
04785Eh	CAN1 Mailbox 5: Time Stamp		XXXXh
04785Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.62 SFR List (62)

Address	Register	Symbol	Reset Value
047860h	CAN1 Mailbox 6: Message Identifier	C1MB6	XXXX XXXXh
047861h			
047862h			
047863h			
047864h			
047865h	CAN1 Mailbox 6: Data Length		XXh
047866h	CAN1 Mailbox 6: Data Field		XXXX XXXX
047867h			XXXX XXXXh
047868h			
047869h			
04786Ah			
04786Bh			
04786Ch			
04786Dh			
04786Eh	CAN1 Mailbox 6: Time Stamp		XXXXh
04786Fh			
047870h	CAN1 Mailbox 7: Message Identifier	C1MB7	XXXX XXXXh
047871h			
047872h			
047873h			
047874h			
047875h	CAN1 Mailbox 7: Data Length		XXh
047876h	CAN1 Mailbox 7: Data Field		XXXX XXXX
047877h			XXXX XXXXh
047878h			
047879h			
04787Ah			
04787Bh			
04787Ch			
04787Dh			
04787Eh	CAN1 Mailbox 7: Time Stamp		XXXXh
04787Fh			
047880h	CAN1 Mailbox 8: Message Identifier	C1MB8	XXXX XXXXh
047881h			
047882h			
047883h			
047884h			
047885h	CAN1 Mailbox 8: Data Length		XXh
047886h	CAN1 Mailbox 8: Data Field		XXXX XXXX
047887h			XXXX XXXXh
047888h			
047889h			
04788Ah			
04788Bh			
04788Ch			
04788Dh			
04788Eh	CAN1 Mailbox 8: Time Stamp		XXXXh
04788Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.63 SFR List (63)

Address	Register	Symbol	Reset Value
047890h	CAN1 Mailbox 9: Message Identifier	C1MB9	XXXX XXXXh
047891h			
047892h			
047893h			
047894h			
047895h	CAN1 Mailbox 9: Data Length		XXh
047896h	CAN1 Mailbox 9: Data Field		XXXX XXXX
047897h			XXXX XXXXh
047898h			
047899h			
04789Ah			
04789Bh			
04789Ch			
04789Dh			
04789Eh	CAN1 Mailbox 9: Time Stamp		XXXXh
04789Fh			
0478A0h	CAN1 Mailbox 10: Message Identifier	C1MB10	XXXX XXXXh
0478A1h			
0478A2h			
0478A3h			
0478A4h			
0478A5h	CAN1 Mailbox 10: Data Length		XXh
0478A6h	CAN1 Mailbox 10: Data Field		XXXX XXXX
0478A7h			XXXX XXXXh
0478A8h			
0478A9h			
0478AAh			
0478ABh			
0478ACh			
0478ADh			
0478AEh	CAN1 Mailbox 10: Time Stamp		XXXXh
0478AFh			
0478B0h	CAN1 Mailbox 11: Message Identifier	C1MB11	XXXX XXXXh
0478B1h			
0478B2h			
0478B3h			
0478B4h			
0478B5h	CAN1 Mailbox 11: Data Length		XXh
0478B6h	CAN1 Mailbox 11: Data Field		XXXX XXXX
0478B7h			XXXX XXXXh
0478B8h			
0478B9h			
0478BAh			
0478BBh			
0478BCh			
0478BDh			
0478BEh	CAN1 Mailbox 11: Time Stamp		XXXXh
0478BFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.64 SFR List (64)

Address	Register	Symbol	Reset Value
0478C0h	CAN1 Mailbox 12: Message Identifier	C1MB12	XXXX XXXXh
0478C1h			
0478C2h			
0478C3h			
0478C4h			
0478C5h	CAN1 Mailbox 12: Data Length		XXh
0478C6h	CAN1 Mailbox 12: Data Field		XXXX XXXX
0478C7h			XXXX XXXXh
0478C8h			
0478C9h			
0478CAh			
0478CBh			
0478CCh			
0478CDh			
0478CEh	CAN1 Mailbox 12: Time Stamp		XXXXh
0478CFh			
0478D0h	CAN1 Mailbox 13: Message Identifier	C1MB13	XXXX XXXXh
0478D1h			
0478D2h			
0478D3h			
0478D4h			
0478D5h	CAN1 Mailbox 13: Data Length		XXh
0478D6h	CAN1 Mailbox 13: Data Field		XXXX XXXX
0478D7h			XXXX XXXXh
0478D8h			
0478D9h			
0478DAh			
0478DBh			
0478DCh			
0478DDh			
0478DEh	CAN1 Mailbox 13: Time Stamp		XXXXh
0478DFh			
0478E0h	CAN1 Mailbox 14: Message Identifier	C1MB14	XXXX XXXXh
0478E1h			
0478E2h			
0478E3h			
0478E4h			
0478E5h	CAN1 Mailbox 14: Data Length		XXh
0478E6h	CAN1 Mailbox 14: Data Field		XXXX XXXX
0478E7h			XXXX XXXXh
0478E8h			
0478E9h			
0478EAh			
0478EBh			
0478ECh			
0478EDh			
0478EEh	CAN1 Mailbox 14: Time Stamp		XXXXh
0478EFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.65 SFR List (65)

Address	Register	Symbol	Reset Value
0478F0h	CAN1 Mailbox 15: Message Identifier	C1MB15	XXXX XXXXh
0478F1h			
0478F2h			
0478F3h			
0478F4h			
0478F5h	CAN1 Mailbox 15: Data Length		XXh
0478F6h	CAN1 Mailbox 15: Data Field		XXXX XXXX
0478F7h			XXXX XXXXh
0478F8h			
0478F9h			
0478FAh			
0478FBh			
0478FCh			
0478FDh			
0478FEh	CAN1 Mailbox 15: Time Stamp		XXXXh
0478FFh			
047900h	CAN1 Mailbox 16: Message Identifier	C1MB16	XXXX XXXXh
047901h			
047902h			
047903h			
047904h			
047905h	CAN1 Mailbox 16: Data Length		XXh
047906h	CAN1 Mailbox 16: Data Field		XXXX XXXX
047907h			XXXX XXXXh
047908h			
047909h			
04790Ah			
04790Bh			
04790Ch			
04790Dh			
04790Eh	CAN1 Mailbox 16: Time Stamp		XXXXh
04790Fh			
047910h	CAN1 Mailbox 17: Message Identifier	C1MB17	XXXX XXXXh
047911h			
047912h			
047913h			
047914h			
047915h	CAN1 Mailbox 17: Data Length		XXh
047916h	CAN1 Mailbox 17: Data Field		XXXX XXXX
047917h			XXXX XXXXh
047918h			
047919h			
04791Ah			
04791Bh			
04791Ch			
04791Dh			
04791Eh	CAN1 Mailbox 17: Time Stamp		XXXXh
04791Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.66 SFR List (66)

Address	Register	Symbol	Reset Value
047920h	CAN1 Mailbox 18: Message Identifier	C1MB18	XXXX XXXXh
047921h			
047922h			
047923h			
047924h			
047925h	CAN1 Mailbox 18: Data Length		XXh
047926h	CAN1 Mailbox 18: Data Field		XXXX XXXX
047927h			XXXX XXXXh
047928h			
047929h			
04792Ah			
04792Bh			
04792Ch			
04792Dh			
04792Eh	CAN1 Mailbox18: Time Stamp		XXXXh
04792Fh			
047930h	CAN1 Mailbox 19: Message Identifier	C1MB19	XXXX XXXXh
047931h			
047932h			
047933h			
047934h			
047935h	CAN1 Mailbox 19: Data Length		XXh
047936h	CAN1 Mailbox 19: Data Field		XXXX XXXX
047937h			XXXX XXXXh
047938h			
047939h			
04793Ah			
04793Bh			
04793Ch			
04793Dh			
04793Eh	CAN1 Mailbox 19: Time Stamp		XXXXh
04793Fh			
047940h	CAN1 Mailbox 20: Message Identifier	C1MB20	XXXX XXXXh
047941h			
047942h			
047943h			
047944h			
047945h	CAN1 Mailbox 20: Data Length		XXh
047946h	CAN1 Mailbox 20: Data Field		XXXX XXXX
047947h			XXXX XXXXh
047948h			
047949h			
04794Ah			
04794Bh			
04794Ch			
04794Dh			
04794Eh	CAN1 Mailbox 20: Time Stamp		XXXXh
04794Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.67 SFR List (67)

Address	Register	Symbol	Reset Value
047950h	CAN1 Mailbox 21: Message Identifier	C1MB21	XXXX XXXXh
047951h			
047952h			
047953h			
047954h			
047955h	CAN1 Mailbox 21: Data Length		XXh
047956h	CAN1 Mailbox 21: Data Field		XXXX XXXX
047957h			XXXX XXXXh
047958h			
047959h			
04795Ah			
04795Bh			
04795Ch			
04795Dh			
04795Eh	CAN1 Mailbox 21: Time Stamp		XXXXh
04795Fh			
047960h	CAN1 Mailbox 22: Identifier	C1MB22	XXXX XXXXh
047961h			
047962h			
047963h			
047964h			
047965h	CAN1 Mailbox 22: Data Length		XXh
047966h	CAN1 Mailbox 22: Data Field		XXXX XXXX
047967h			XXXX XXXXh
047968h			
047969h			
04796Ah			
04796Bh			
04796Ch			
04796Dh			
04796Eh	CAN1 Mailbox 22: Time Stamp		XXXXh
04796Fh			
047970h	CAN1 Mailbox 23: Message Identifier	C1MB23	XXXX XXXXh
047971h			
047972h			
047973h			
047974h			
047975h	CAN1 Mailbox 23: Data Length		XXh
047976h	CAN1 Mailbox 23: Data Field		XXXX XXXX
047977h			XXXX XXXXh
047978h			
047979h			
04797Ah			
04797Bh			
04797Ch			
04797Dh			
04797Eh	CAN1 Mailbox 23: Time Stamp		XXXXh
04797Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.68 SFR List (68)

Address	Register	Symbol	Reset Value
047980h	CAN1 Mailbox 24: Message Identifier	C1MB24	XXXX XXXXh
047981h			
047982h			
047983h			
047984h			
047985h	CAN1 Mailbox 24: Data Length		XXh
047986h	CAN1 Mailbox 24: Data Field		XXXX XXXX
047987h			XXXX XXXXh
047988h			
047989h			
04798Ah			
04798Bh			
04798Ch			
04798Dh			
04798Eh	CAN1 Mailbox 24: Time Stamp		XXXXh
04798Fh			
047990h	CAN1 Mailbox 25: Message Identifier	C1MB25	XXXX XXXXh
047991h			
047992h			
047993h			
047994h			
047995h	CAN1 Mailbox 25: Data Length		XXh
047996h	CAN1 Mailbox 25: Data Field		XXXX XXXX
047997h			XXXX XXXXh
047998h			
047999h			
04799Ah			
04799Bh			
04799Ch			
04799Dh			
04799Eh	CAN1 Mailbox 25: Time Stamp		XXXXh
04799Fh			
0479A0h	CAN1 Mailbox 26: Message Identifier	C1MB26	XXXX XXXXh
0479A1h			
0479A2h			
0479A3h			
0479A4h			
0479A5h	CAN1 Mailbox 26: Data Length		XXh
0479A6h	CAN1 Mailbox 26: Data Field		XXXX XXXX
0479A7h			XXXX XXXXh
0479A8h			
0479A9h			
0479AAh			
0479ABh			
0479ACh			
0479ADh			
0479AEh	CAN1 Mailbox 26: Time Stamp		XXXXh
0479AFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.69 SFR List (69)

Address	Register	Symbol	Reset Value
0479B0h	CAN1 Mailbox 27: Message Identifier	C1MB27	XXXX XXXXh
0479B1h			
0479B2h			
0479B3h			
0479B4h			
0479B5h	CAN1 Mailbox 27: Data Length		XXh
0479B6h	CAN1 Mailbox 27: Data Field		XXXX XXXX
0479B7h			XXXX XXXXh
0479B8h			
0479B9h			
0479BAh			
0479BBh			
0479BCh			
0479BDh			
0479BEh	CAN1 Mailbox 27: Time Stamp		XXXXh
0479BFh			
0479C0h	CAN1 Mailbox 28: Message Identifier	C1MB28	XXXX XXXXh
0479C1h			
0479C2h			
0479C3h			
0479C4h			
0479C5h	CAN1 Mailbox 28: Data Length		XXh
0479C6h	CAN1 Mailbox 28: Data Field		XXXX XXXX
0479C7h			XXXX XXXXh
0479C8h			
0479C9h			
0479CAh			
0479CBh			
0479CCh			
0479CDh			
0479CEh	CAN1 Mailbox 28: Time Stamp		XXXXh
0479CFh			
0479D0h	CAN1 Mailbox 29: Message Identifier	C1MB29	XXXX XXXXh
0479D1h			
0479D2h			
0479D3h			
0479D4h			
0479D5h	CAN1 Mailbox 29: Data Length		XXh
0479D6h	CAN1 Mailbox 29: Data Field		XXXX XXXX
0479D7h			XXXX XXXXh
0479D8h			
0479D9h			
0479DAh			
0479DBh			
0479DCh			
0479DDh			
0479DEh	CAN1 Mailbox 29: Time Stamp		XXXXh
0479DFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.70 SFR List (70)

Address	Register	Symbol	Reset Value
0479E0h	CAN1 Mailbox 30: Message Identifier	C1MB30	XXXX XXXXh
0479E1h			
0479E2h			
0479E3h			
0479E4h			
0479E5h	CAN1 Mailbox 30: Data Length		XXh
0479E6h	CAN1 Mailbox 30: Data Field		XXXX XXXX
0479E7h			XXXX XXXXh
0479E8h			
0479E9h			
0479EAh			
0479EBh			
0479ECh			
0479EDh			
0479EEh	CAN1 Mailbox 30: Time Stamp		XXXXh
0479EFh			
0479F0h	CAN1 Mailbox 31: Message Identifier	C1MB31	XXXX XXXXh
0479F1h			
0479F2h			
0479F3h			
0479F4h			
0479F5h	CAN1 Mailbox 31: Data Length		XXh
0479F6h	CAN1 Mailbox 31: Data Field		XXXX XXXX
0479F7h			XXXX XXXXh
0479F8h			
0479F9h			
0479FAh			
0479FBh			
0479FCh			
0479FDh			
0479FEh	CAN1 Mailbox 31: Time Stamp		XXXXh
0479FFh			
047A00h	CAN1 Acceptance Mask Register 0	C1MKR0	XXXX XXXXh
047A01h			
047A02h			
047A03h			
047A04h	CAN1 Acceptance Mask Register 1	C1MKR1	XXXX XXXXh
047A05h			
047A06h			
047A07h			
047A08h	CAN1 Acceptance Mask Register 2	C1MKR2	XXXX XXXXh
047A09h			
047A0Ah			
047A0Bh			
047A0Ch	CAN1 Acceptance Mask Register 3	C1MKR3	XXXX XXXXh
047A0Dh			
047A0Eh			
047A0Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.71 SFR List (71)

Address	Register	Symbol	Reset Value
047A10h	CAN1 Acceptance Mask Register 4	C1MKR4	XXXX XXXXh
047A11h			
047A12h			
047A13h			
047A14h	CAN1 Acceptance Mask Register 5	C1MKR5	XXXX XXXXh
047A15h			
047A16h			
047A17h			
047A18h	CAN1 Acceptance Mask Register 6	C1MKR6	XXXX XXXXh
047A19h			
047A1Ah			
047A1Bh			
047A1Ch	CAN1 Acceptance Mask Register 7	C1MKR7	XXXX XXXXh
047A1Dh			
047A1Eh			
047A1Fh			
047A20h	CAN1 FIFO Received ID Compare Register 0	C1FIDCR0	XXXX XXXXh
047A21h			
047A22h			
047A23h			
047A24h	CAN1 FIFO Received ID Compare Register 1	C1FIDCR1	XXXX XXXXh
047A25h			
047A26h			
047A27h			
047A28h	CAN1 Mask Invalid Register	C1MKIVLR	XXXX XXXXh
047A29h			
047A2Ah			
047A2Bh			
047A2Ch	CAN1 Mailbox Interrupt Enable Register	C1MIER	XXXX XXXXh
047A2Dh			
047A2Eh			
047A2Fh			
047A30h			
047A31h			
047A32h			
047A33h			
047A34h			
047A35h			
047A36h			
047A37h			
047A38h			
047A39h			
047A3Ah			
047A3Bh			
047A3Ch			
047A3Dh			
047A3Eh			
047A3Fh			
047A40h to 047B1Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.72 SFR List (72)

Address	Register	Symbol	Reset Value
047B20h	CAN1 Message Control Register 0	C1MCTL0	00h
047B21h	CAN1 Message Control Register 1	C1MCTL1	00h
047B22h	CAN1 Message Control Register 2	C1MCTL2	00h
047B23h	CAN1 Message Control Register 3	C1MCTL3	00h
047B24h	CAN1 Message Control Register 4	C1MCTL4	00h
047B25h	CAN1 Message Control Register 5	C1MCTL5	00h
047B26h	CAN1 Message Control Register 6	C1MCTL6	00h
047B27h	CAN1 Message Control Register 7	C1MCTL7	00h
047B28h	CAN1 Message Control Register 8	C1MCTL8	00h
047B29h	CAN1 Message Control Register 9	C1MCTL9	00h
047B2Ah	CAN1 Message Control Register 10	C1MCTL10	00h
047B2Bh	CAN1 Message Control Register 11	C1MCTL11	00h
047B2Ch	CAN1 Message Control Register 12	C1MCTL12	00h
047B2Dh	CAN1 Message Control Register 13	C1MCTL13	00h
047B2Eh	CAN1 Message Control Register 14	C1MCTL14	00h
047B2Fh	CAN1 Message Control Register 15	C1MCTL15	00h
047B30h	CAN1 Message Control Register 16	C1MCTL16	00h
047B31h	CAN1 Message Control Register 17	C1MCTL17	00h
047B32h	CAN1 Message Control Register 18	C1MCTL18	00h
047B33h	CAN1 Message Control Register 19	C1MCTL19	00h
047B34h	CAN1 Message Control Register 20	C1MCTL20	00h
047B35h	CAN1 Message Control Register 21	C1MCTL21	00h
047B36h	CAN1 Message Control Register 22	C1MCTL22	00h
047B37h	CAN1 Message Control Register 23	C1MCTL23	00h
047B38h	CAN1 Message Control Register 24	C1MCTL24	00h
047B39h	CAN1 Message Control Register 25	C1MCTL25	00h
047B3Ah	CAN1 Message Control Register 26	C1MCTL26	00h
047B3Bh	CAN1 Message Control Register 27	C1MCTL27	00h
047B3Ch	CAN1 Message Control Register 28	C1MCTL28	00h
047B3Dh	CAN1 Message Control Register 29	C1MCTL29	00h
047B3Eh	CAN1 Message Control Register 30	C1MCTL30	00h
047B3Fh	CAN1 Message Control Register 31	C1MCTL31	00h

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.73 SFR List (73)

Address	Register	Symbol	Reset Value
047B40h	CAN1 Control Register	C1CTLR	0000 0101b
047B41h			0000 0000b
047B42h	CAN1 Status Register	C1STR	0000 0101b
047B43h			0000 0000b
047B44h	CAN1 Bit Configuration Register	C1BCR	00 0000h
047B45h			
047B46h			
047B47h	CAN1 Clock Select Register	C1CLKR	000X 0000b
047B48h	CAN1 Receive FIFO Control Register	C1RFCR	1000 0000b
047B49h	CAN1 Receive FIFO Pointer Control Register	C1RFPCR	XXh
047B4Ah	CAN1 Transmit FIFO Control Register	C1TFCR	1000 0000b
047B4Bh	CAN1 Transmit FIFO Pointer Control Register	C1TFPCR	XXh
047B4Ch	CAN1 Error Interrupt Enable Register	C1EIER	00h
047B4Dh	CAN1 Error Interrupt Factor Judge Register	C1EIFR	00h
047B4Eh	CAN1 Receive Error Count Register	C1RECR	00h
047B4Fh	CAN1 Transmit Error Count Register	C1TECR	00h
047B50h	CAN1 Error Code Store Register	C1ECSR	00h
047B51h	CAN1 Channel Search Support Register	C1CSSR	XXh
047B52h	CAN1 Mailbox Search Status Register	C1MSSR	1000 0000b
047B53h	CAN1 Mailbox Search Mode Register	C1MSMR	XXXX XX00b
047B54h	CAN1 Time Stamp Register	C1TSR	0000h
047B55h			
047B56h	CAN1 Acceptance Filter Support Register	C1AFSR	XXXXh
047B57h			
047B58h	CAN1 Test Control Register	C1TCR	00h
047B59h			
047B5Ah			
047B5Bh			
047B5Ch			
047B5Dh			
047B5Eh			
047B5Fh			
047B60h to 047BFFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.74 SFR List (74)

Address	Register	Symbol	Reset Value
047C00h	CAN0 Mailbox 0: Message Identifier	C0MB0	XXXX XXXXh
047C01h			
047C02h			
047C03h			
047C04h			
047C05h	CAN0 Mailbox 0: Data Length		XXh
047C06h	CAN0 Mailbox 0: Data Field		XXXX XXXX
047C07h			XXXX XXXXh
047C08h			
047C09h			
047C0Ah			
047C0Bh			
047C0Ch			
047C0Dh			
047C0Eh	CAN0 Mailbox 0: Time Stamp		XXXXh
047C0Fh			
047C10h	CAN0 Mailbox 1: Message Identifier	C0MB1	XXXX XXXXh
047C11h			
047C12h			
047C13h			
047C14h			
047C15h	CAN0 Mailbox 1: Data Length		XXh
047C16h	CAN0 Mailbox 1: Data Field		XXXX XXXX
047C17h			XXXX XXXXh
047C18h			
047C19h			
047C1Ah			
047C1Bh			
047C1Ch			
047C1Dh			
047C1Eh	CAN0 Mailbox 1: Time Stamp		XXXXh
047C1Fh			
047C20h	CAN0 Mailbox 2: Message Identifier	C0MB2	XXXX XXXXh
047C21h			
047C22h			
047C23h			
047C24h			
047C25h	CAN0 Mailbox 2: Data Length		XXh
047C26h	CAN0 Mailbox 2: Data Field		XXXX XXXX
047C27h			XXXX XXXXh
047C28h			
047C29h			
047C2Ah			
047C2Bh			
047C2Ch			
047C2Dh			
047C2Eh	CAN0 Mailbox 2: Time Stamp		XXXXh
047C2Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.75 SFR List (75)

Address	Register	Symbol	Reset Value
047C30h	CAN0 Mailbox 3: Message Identifier	C0MB3	XXXX XXXXh
047C31h			
047C32h			
047C33h			
047C34h			
047C35h	CAN0 Mailbox 3: Data Length		XXh
047C36h	CAN0 Mailbox 3: Data Field		XXXX XXXX
047C37h			XXXX XXXXh
047C38h			
047C39h			
047C3Ah			
047C3Bh			
047C3Ch			
047C3Dh			
047C3Eh	CAN0 Mailbox 3: Time Stamp		XXXXh
047C3Fh			
047C40h	CAN0 Mailbox 4: Message Identifier	C0MB4	XXXX XXXXh
047C41h			
047C42h			
047C43h			
047C44h			
047C45h	CAN0 Mailbox 4: Data Length		XXh
047C46h	CAN0 Mailbox 4: Data Field		XXXX XXXX
047C47h			XXXX XXXXh
047C48h			
047C49h			
047C4Ah			
047C4Bh			
047C4Ch			
047C4Dh			
047C4Eh	CAN0 Mailbox 4: Time Stamp		XXXXh
047C4Fh			
047C50h	CAN0 Mailbox 5: Message Identifier	C0MB5	XXXX XXXXh
047C51h			
047C52h			
047C53h			
047C54h			
047C55h	CAN0 Mailbox 5: Data Length		XXh
047C56h	CAN0 Mailbox 5: Data Field		XXXX XXXX
047C57h			XXXX XXXXh
047C58h			
047C59h			
047C5Ah			
047C5Bh			
047C5Ch			
047C5Dh			
047C5Eh	CAN0 Mailbox 5: Time Stamp		XXXXh
047C5Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.76 SFR List (76)

Address	Register	Symbol	Reset Value
047C60h	CAN0 Mailbox 6: Message Identifier	C0MB6	XXXX XXXXh
047C61h			
047C62h			
047C63h			
047C64h			
047C65h	CAN0 Mailbox 6: Data Length		XXh
047C66h	CAN0 Mailbox 6: Data Field		XXXX XXXX
047C67h			XXXX XXXXh
047C68h			
047C69h			
047C6Ah			
047C6Bh			
047C6Ch			
047C6Dh			
047C6Eh	CAN0 Mailbox 6: Time Stamp		XXXXh
047C6Fh			
047C70h	CAN0 Mailbox 7: Message Identifier	C0MB7	XXXX XXXXh
047C71h			
047C72h			
047C73h			
047C74h			
047C75h	CAN0 Mailbox 7: Data Length		XXh
047C76h	CAN0 Mailbox 7: Data Field		XXXX XXXX
047C77h			XXXX XXXXh
047C78h			
047C79h			
047C7Ah			
047C7Bh			
047C7Ch			
047C7Dh			
047C7Eh	CAN0 Mailbox 7: Time Stamp		XXXXh
047C7Fh			
047C80h	CAN0 Mailbox 8: Message Identifier	C0MB8	XXXX XXXXh
047C81h			
047C82h			
047C83h			
047C84h			
047C85h	CAN0 Mailbox 8: Data Length		XXh
047C86h	CAN0 Mailbox 8: Data Field		XXXX XXXX
047C87h			XXXX XXXXh
047C88h			
047C89h			
047C8Ah			
047C8Bh			
047C8Ch			
047C8Dh			
047C8Eh	CAN0 Mailbox 8: Time Stamp		XXXXh
047C8Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.77 SFR List (77)

Address	Register	Symbol	Reset Value
047C90h	CAN0 Mailbox 9: Message Identifier	C0MB9	XXXX XXXXh
047C91h			
047C92h			
047C93h			
047C94h			
047C95h	CAN0 Mailbox 9: Data Length		XXh
047C96h	CAN0 Mailbox 9: Data Field		XXXX XXXX
047C97h			XXXX XXXXh
047C98h			
047C99h			
047C9Ah			
047C9Bh			
047C9Ch			
047C9Dh			
047C9Eh	CAN0 Mailbox 9: Time Stamp		XXXXh
047C9Fh			
047CA0h	CAN0 Mailbox 10: Message Identifier	C0MB10	XXXX XXXXh
047CA1h			
047CA2h			
047CA3h			
047CA4h			
047CA5h	CAN0 Mailbox 10: Data Length		XXh
047CA6h	CAN0 Mailbox 10: Data Field		XXXX XXXX
047CA7h			XXXX XXXXh
047CA8h			
047CA9h			
047CAAh			
047CABh			
047CACh			
047CADh			
047CAEh	CAN0 Mailbox 10: Time Stamp		XXXXh
047CAFh			
047CB0h	CAN0 Mailbox 11: Message Identifier	C0MB11	XXXX XXXXh
047CB1h			
047CB2h			
047CB3h			
047CB4h			
047CB5h	CAN0 Mailbox 11: Data Length		XXh
047CB6h	CAN0 Mailbox 11: Data Field		XXXX XXXX
047CB7h			XXXX XXXXh
047CB8h			
047CB9h			
047CBAh			
047CBBh			
047CBCh			
047CBDh			
047CBEh	CAN0 Mailbox 11: Time Stamp		XXXXh
047CBFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.78 SFR List (78)

Address	Register	Symbol	Reset Value
047CC0h	CAN0 Mailbox 12: Message Identifier	C0MB12	XXXX XXXXh
047CC1h			
047CC2h			
047CC3h			
047CC4h			
047CC5h	CAN0 Mailbox 12: Data Length		XXh
047CC6h	CAN0 Mailbox 12: Data Field		XXXX XXXX
047CC7h			XXXX XXXXh
047CC8h			
047CC9h			
047CCAh			
047CCBh			
047CCCh			
047CCDh			
047CCEh	CAN0 Mailbox 12: Time Stamp		XXXXh
047CCFh			
047CD0h	CAN0 Mailbox 13: Message Identifier	C0MB13	XXXX XXXXh
047CD1h			
047CD2h			
047CD3h			
047CD4h			
047CD5h	CAN0 Mailbox 13: Data Length		XXh
047CD6h	CAN0 Mailbox 13: Data Field		XXXX XXXX
047CD7h			XXXX XXXXh
047CD8h			
047CD9h			
047CDAh			
047CDBh			
047CDCh			
047CDDh			
047CDEh	CAN0 Mailbox 13: Time Stamp		XXXXh
047CDFh			
047CE0h	CAN0 Mailbox 14: Message Identifier	C0MB14	XXXX XXXXh
047CE1h			
047CE2h			
047CE3h			
047CE4h			
047CE5h	CAN0 Mailbox 14: Data Length		XXh
047CE6h	CAN0 Mailbox 14: Data Field		XXXX XXXX
047CE7h			XXXX XXXXh
047CE8h			
047CE9h			
047CEAh			
047CEBh			
047CECh			
047CEDh			
047CEEh	CAN0 Mailbox 14: Time Stamp		XXXXh
047CEFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.79 SFR List (79)

Address	Register	Symbol	Reset Value
047CF0h	CAN0 Mailbox 15: Message Identifier	C0MB15	XXXX XXXXh
047CF1h			
047CF2h			
047CF3h			
047CF4h			
047CF5h	CAN0 Mailbox 15: Data Length		XXh
047CF6h	CAN0 Mailbox 15: Data Field		XXXX XXXX
047CF7h			XXXX XXXXh
047CF8h			
047CF9h			
047CFAh			
047CFBh			
047CFCh			
047CFDh			
047CFEh	CAN0 Mailbox 15: Time Stamp		XXXXh
047CFFh			
047D00h	CAN0 Mailbox 16: Message Identifier	C0MB16	XXXX XXXXh
047D01h			
047D02h			
047D03h			
047D04h			
047D05h	CAN0 Mailbox 16: Data Length		XXh
047D06h	CAN0 Mailbox 16: Data Field		XXXX XXXX
047D07h			XXXX XXXXh
047D08h			
047D09h			
047D0Ah			
047D0Bh			
047D0Ch			
047D0Dh			
047D0Eh	CAN0 Mailbox 16: Time Stamp		XXXXh
047D0Fh			
047D10h	CAN0 Mailbox 17: Message Identifier	C0MB17	XXXX XXXXh
047D11h			
047D12h			
047D13h			
047D14h			
047D15h	CAN0 Mailbox 17: Data Length		XXh
047D16h	CAN0 Mailbox 17: Data Field		XXXX XXXX
047D17h			XXXX XXXXh
047D18h			
047D19h			
047D1Ah			
047D1Bh			
047D1Ch			
047D1Dh			
047D1Eh	CAN0 Mailbox 17: Time Stamp		XXXXh
047D1Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.80 SFR List (80)

Address	Register	Symbol	Reset Value
047D20h	CAN0 Mailbox 18: Message Identifier	C0MB18	XXXX XXXXh
047D21h			
047D22h			
047D23h			
047D24h			
047D25h	CAN0 Mailbox 18: Data Length		XXh
047D26h	CAN0 Mailbox 18: Data Field		XXXX XXXX
047D27h			XXXX XXXXh
047D28h			
047D29h			
047D2Ah			
047D2Bh			
047D2Ch			
047D2Dh			
047D2Eh	CAN0 Mailbox 18: Time Stamp		XXXXh
047D2Fh			
047D30h	CAN0 Mailbox 19: Message Identifier	C0MB19	XXXX XXXXh
047D31h			
047D32h			
047D33h			
047D34h			
047D35h	CAN0 Mailbox 19: Data Length		XXh
047D36h	CAN0 Mailbox 19: Data Field		XXXX XXXX
047D37h			XXXX XXXXh
047D38h			
047D39h			
047D3Ah			
047D3Bh			
047D3Ch			
047D3Dh			
047D3Eh	CAN0 Mailbox 19: Time Stamp		XXXXh
047D3Fh			
047D40h	CAN0 Mailbox 20: Message Identifier	C0MB20	XXXX XXXXh
047D41h			
047D42h			
047D43h			
047D44h			
047D45h	CAN0 Mailbox 20: Data Length		XXh
047D46h	CAN0 Mailbox 20: Data Field		XXXX XXXX
047D47h			XXXX XXXXh
047D48h			
047D49h			
047D4Ah			
047D4Bh			
047D4Ch			
047D4Dh			
047D4Eh	CAN0 Mailbox 20: Time Stamp		XXXXh
047D4Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.81 SFR List (81)

Address	Register	Symbol	Reset Value
047D50h	CAN0 Mailbox 21: Message Identifier	C0MB21	XXXX XXXXh
047D51h			
047D52h			
047D53h			
047D54h			
047D55h	CAN0 Mailbox 21: Data Length		XXh
047D56h	CAN0 Mailbox 21: Data Field		XXXX XXXX
047D57h			XXXX XXXXh
047D58h			
047D59h			
047D5Ah			
047D5Bh			
047D5Ch			
047D5Dh			
047D5Eh	CAN0 Mailbox 21: Time Stamp		XXXXh
047D5Fh			
047D60h	CAN0 Mailbox 22: Message Identifier	C0MB22	XXXX XXXXh
047D61h			
047D62h			
047D63h			
047D64h			
047D65h	CAN0 Mailbox 22: Data Length		XXh
047D66h	CAN0 Mailbox 22: Data Field		XXXX XXXX
047D67h			XXXX XXXXh
047D68h			
047D69h			
047D6Ah			
047D6Bh			
047D6Ch			
047D6Dh			
047D6Eh	CAN0 Mailbox 22: Time Stamp		XXXXh
047D6Fh			
047D70h	CAN0 Mailbox 23: Message Identifier	C0MB23	XXXX XXXXh
047D71h			
047D72h			
047D73h			
047D74h			
047D75h	CAN0 Mailbox 23: Data Length		XXh
047D76h	CAN0 Mailbox 23: Data Field		XXXX XXXX
047D77h			XXXX XXXXh
047D78h			
047D79h			
047D7Ah			
047D7Bh			
047D7Ch			
047D7Dh			
047D7Eh	CAN0 Mailbox 23: Time Stamp		XXXXh
047D7Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.82 SFR List (82)

Address	Register	Symbol	Reset Value
047D80h	CAN0 Mailbox 24: Message Identifier	C0MB24	XXXX XXXXh
047D81h			
047D82h			
047D83h			
047D84h			
047D85h	CAN0 Mailbox 24: Data Length		XXh
047D86h	CAN0 Mailbox 24: Data Field		XXXX XXXX
047D87h			XXXX XXXXh
047D88h			
047D89h			
047D8Ah			
047D8Bh			
047D8Ch			
047D8Dh			
047D8Eh	CAN0 Mailbox 24: Time Stamp		XXXXh
047D8Fh			
047D90h	CAN0 Mailbox 25: Message Identifier	C0MB25	XXXX XXXXh
047D91h			
047D92h			
047D93h			
047D94h			
047D95h	CAN0 Mailbox 25: Data Length		XXh
047D96h	CAN0 Mailbox 25: Data Field		XXXX XXXX
047D97h			XXXX XXXXh
047D98h			
047D99h			
047D9Ah			
047D9Bh			
047D9Ch			
047D9Dh			
047D9Eh	CAN0 Mailbox 25: Time Stamp		XXXXh
047D9Fh			
047DA0h	CAN0 Mailbox 26: Message Identifier	C0MB26	XXXX XXXXh
047DA1h			
047DA2h			
047DA3h			
047DA4h			
047DA5h	CAN0 Mailbox 26: Data Length		XXh
047DA6h	CAN0 Mailbox 26: Data Field		XXXX XXXX
047DA7h			XXXX XXXXh
047DA8h			
047DA9h			
047DAAh			
047DABh			
047DACh			
047DADh			
047DAEh	CAN0 Mailbox 26: Time Stamp		XXXXh
047DAFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.83 SFR List (83)

Address	Register	Symbol	Reset Value
047DB0h	CAN0 Mailbox 27: Message Identifier	C0MB27	XXXX XXXXh
047DB1h			
047DB2h			
047DB3h			
047DB4h			
047DB5h	CAN0 Mailbox 27: Data Length		XXh
047DB6h	CAN0 Mailbox 27: Data Field		XXXX XXXX
047DB7h			XXXX XXXXh
047DB8h			
047DB9h			
047DBAh			
047DBBh			
047DBCh			
047DBDh			
047DBEh	CAN0 Mailbox 27: Time Stamp		XXXXh
047DBFh			
047DC0h	CAN0 Mailbox 28: Message Identifier	C0MB28	XXXX XXXXh
047DC1h			
047DC2h			
047DC3h			
047DC4h			
047DC5h	CAN0 Mailbox 28: Data Length		XXh
047DC6h	CAN0 Mailbox 28: Data Field		XXXX XXXX
047DC7h			XXXX XXXXh
047DC8h			
047DC9h			
047DCAh			
047DCBh			
047DCCh			
047DCDh			
047DCEh	CAN0 Mailbox 28: Time Stamp		XXXXh
047DCFh			
047DD0h	CAN0 Mailbox 29: Message Identifier	C0MB29	XXXX XXXXh
047DD1h			
047DD2h			
047DD3h			
047DD4h			
047DD5h	CAN0 Mailbox 29: Data Length		XXh
047DD6h	CAN0 Mailbox 29: Data Field		XXXX XXXX
047DD7h			XXXX XXXXh
047DD8h			
047DD9h			
047DDAh			
047DDBh			
047DDCh			
047DDDh			
047DDEh	CAN0 Mailbox 29: Time Stamp		XXXXh
047DDFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.84 SFR List (84)

Address	Register	Symbol	Reset Value
047DE0h	CAN0 Mailbox 30: Message Identifier	C0MB30	XXXX XXXXh
047DE1h			
047DE2h			
047DE3h			
047DE4h			
047DE5h	CAN0 Mailbox 30: Data Length		XXh
047DE6h	CAN0 Mailbox 30: Data Field		XXXX XXXX
047DE7h			XXXX XXXXh
047DE8h			
047DE9h			
047DEAh			
047DEBh			
047DECh			
047DEDh			
047DEEh	CAN0 Mailbox 30: Time Stamp		XXXXh
047DEFh			
047DF0h	CAN0 Mailbox 31: Message Identifier	C0MB31	XXXX XXXXh
047DF1h			
047DF2h			
047DF3h			
047DF4h			
047DF5h	CAN0 Mailbox 31: Data Length		XXh
047DF6h	CAN0 Mailbox 31: Data Field		XXXX XXXX
047DF7h			XXXX XXXXh
047DF8h			
047DF9h			
047DFAh			
047DFBh			
047DFCh			
047DFDh			
047DFEh	CAN0 Mailbox 31: Time Stamp		XXXXh
047DFFh			
047E00h	CAN0 Acceptance Mask Register 0	C0MKR0	XXXX XXXXh
047E01h			
047E02h			
047E03h			
047E04h	CAN0 Acceptance Mask Register 1	C0MKR1	XXXX XXXXh
047E05h			
047E06h			
047E07h			
047E08h	CAN0 Acceptance Mask Register 2	C0MKR2	XXXX XXXXh
047E09h			
047E0Ah			
047E0Bh			
047E0Ch	CAN0 Acceptance Mask Register 3	C0MKR3	XXXX XXXXh
047E0Dh			
047E0Eh			
047E0Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.85 SFR List (85)

Address	Register	Symbol	Reset Value
047E10h	CAN0 Acceptance Mask Register 4	C0MKR4	XXXX XXXXh
047E11h			
047E12h			
047E13h			
047E14h	CAN0 Acceptance Mask Register 5	C0MKR5	XXXX XXXXh
047E15h			
047E16h			
047E17h			
047E18h	CAN0 Acceptance Mask Register 6	C0MKR6	XXXX XXXXh
047E19h			
047E1Ah			
047E1Bh			
047E1Ch	CAN0 Acceptance Mask Register 7	C0MKR7	XXXX XXXXh
047E1Dh			
047E1Eh			
047E1Fh			
047E20h	CAN0 FIFO Receive ID Compare Register 0	C0FIDCR0	XXXX XXXXh
047E21h			
047E22h			
047E23h			
047E24h	CAN0 FIFO Receive ID Compare Register 1	C0FIDCR1	XXXX XXXXh
047E25h			
047E26h			
047E27h			
047E28h	CAN0 Mask Invalid Register	C0MKIVLR	XXXX XXXXh
047E29h			
047E2Ah			
047E2Bh			
047E2Ch	CAN0 Mailbox Interrupt Enable Register	C0MIER	XXXX XXXXh
047E2Dh			
047E2Eh			
047E2Fh			
047E30h			
047E31h			
047E32h			
047E33h			
047E34h			
047E35h			
047E36h			
047E37h			
047E38h			
047E39h			
047E3Ah			
047E3Bh			
047E3Ch			
047E3Dh			
047E3Eh			
047E3Fh			
047E40h to 047F1Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.86 SFR List (86)

Address	Register	Symbol	Reset Value
047F20h	CAN0 Message Control Register 0	C0MCTL0	00h
047F21h	CAN0 Message Control Register 1	C0MCTL1	00h
047F22h	CAN0 Message Control Register 2	C0MCTL2	00h
047F23h	CAN0 Message Control Register 3	C0MCTL3	00h
047F24h	CAN0 Message Control Register 4	C0MCTL4	00h
047F25h	CAN0 Message Control Register 5	C0MCTL5	00h
047F26h	CAN0 Message Control Register 6	C0MCTL6	00h
047F27h	CAN0 Message Control Register 7	C0MCTL7	00h
047F28h	CAN0 Message Control Register 8	C0MCTL8	00h
047F29h	CAN0 Message Control Register 9	C0MCTL9	00h
047F2Ah	CAN0 Message Control Register 10	C0MCTL10	00h
047F2Bh	CAN0 Message Control Register 11	C0MCTL11	00h
047F2Ch	CAN0 Message Control Register 12	C0MCTL12	00h
047F2Dh	CAN0 Message Control Register 13	C0MCTL13	00h
047F2Eh	CAN0 Message Control Register 14	C0MCTL14	00h
047F2Fh	CAN0 Message Control Register 15	C0MCTL15	00h
047F30h	CAN0 Message Control Register 16	C0MCTL16	00h
047F31h	CAN0 Message Control Register 17	C0MCTL17	00h
047F32h	CAN0 Message Control Register 18	C0MCTL18	00h
047F33h	CAN0 Message Control Register 19	C0MCTL19	00h
047F34h	CAN0 Message Control Register 20	C0MCTL20	00h
047F35h	CAN0 Message Control Register 21	C0MCTL21	00h
047F36h	CAN0 Message Control Register 22	C0MCTL22	00h
047F37h	CAN0 Message Control Register 23	C0MCTL23	00h
047F38h	CAN0 Message Control Register 24	C0MCTL24	00h
047F39h	CAN0 Message Control Register 25	C0MCTL25	00h
047F3Ah	CAN0 Message Control Register 26	C0MCTL26	00h
047F3Bh	CAN0 Message Control Register 27	C0MCTL27	00h
047F3Ch	CAN0 Message Control Register 28	C0MCTL28	00h
047F3Dh	CAN0 Message Control Register 29	C0MCTL29	00h
047F3Eh	CAN0 Message Control Register 30	C0MCTL30	00h
047F3Fh	CAN0 Message Control Register 31	C0MCTL31	00h

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.87 SFR List (87)

Address	Register	Symbol	Reset Value
047F40h	CAN0 Control Register	C0CTLR	0000 0101b
047F41h			0000 0000b
047F42h	CAN0 Status Register	C0STR	0000 0101b
047F43h			0000 0000b
047F44h	CAN0 Bit Configuration Register	C0BCR	00 0000h
047F45h			
047F46h			
047F47h	CAN0 Clock Select Register	C0CLKR	000X 0000b
047F48h	CAN0 Receive FIFO Control Register	C0RFCR	1000 0000b
047F49h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	XXh
047F4Ah	CAN0 Transmit FIFO Control Register	C0TFCR	1000 0000b
047F4Bh	CAN0 Transmit FIFO Pointer Control Register	C0TFPCR	XXh
047F4Ch	CAN0 Error Interrupt Enable Register	C0EIER	00h
047F4Dh	CAN0 Error Interrupt Factor Judge Register	C0EIFR	00h
047F4Eh	CAN0 Receive Error Count Register	C0RECR	00h
047F4Fh	CAN0 Transmit Error Count Register	C0TECR	00h
047F50h	CAN0 Error Code Store Register	C0ECSR	00h
047F51h	CAN0 Channel Search Support Register	C0CSSR	XXh
047F52h	CAN0 Mailbox Search Status Register	C0MSSR	1000 0000b
047F53h	CAN0 Mailbox Search Mode Register	C0MSMR	XXXX XX00b
047F54h	CAN0 Time Stamp Register	C0TSR	0000h
047F55h			
047F56h	CAN0 Acceptance Filter Support Register	C0AFSR	XXXXh
047F57h			
047F58h	CAN0 Test Control Register	C0TCR	00h
047F59h			
047F5Ah			
047F5Bh			
047F5Ch			
047F5Dh			
047F5Eh			
047F5Fh			
047F60h to 047FFFh			
048000h to 04FFFFh			

X: Undefined
Blanks are reserved. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings (1)

Symbol	Characteristic		Condition	Value	Unit
V_{CC}	Supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.0	V
AV_{CC}	Analog supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.0	V
V_I	Input voltage	XIN, $\overline{RESET}$, CNVSS, NSD, V_{REF}, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7		-0.3 to V_{CC} + 0.3	V
V_O	Output voltage	XOUT, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7		-0.3 to V_{CC} + 0.3	V
P_d	Power consumption		T_a = 25°C	500	mW
—	Operating temperature range			-40 to 125	°C
T_{stg}	Storage temperature range			-65 to 150	°C

Note:

1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5.2 Operating Conditions (1/6) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
V_{CC}	Digital supply voltage		3.0	5.0	5.5	V
AV_{CC}	Analog supply voltage			V_{CC}		V
V_{REF}	Reference voltage		3.0		V_{CC}	V
V_{SS}	Digital ground voltage			0		V
AV_{SS}	Analog ground voltage			0		V
dV_{CC}/dt	V_{CC} ramp up rate (V_{CC} < 2.0 V)		0.05			V/ms
V_{IH}	High level input voltage	XIN, $\overline{\text{RESET}}$, CNVSS, NSD	0.8 × V_{CC}		V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 (2), P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7	0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low level input voltage	XIN, $\overline{\text{RESET}}$, CNVSS, NSD	0		0.2 × V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 (2), P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7	0		0.3 × V_{CC}	V
T_{opr}	Operating temperature range	J version	-40		85	°C
		L version	-40		105	°C
		K version	-40		125	°C

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. V_{IH} and V_{IL} for P8_7 are specified for P8_7 as a programmable port. These values are not applicable to P8_7 as XCIN.

Table 5.3 Operating Conditions (2/6)
(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value (2)			Unit
			Min.	Typ.	Max.	
C_{VDC}	Decoupling capacitance for voltage regulator	Inter-pin voltage: 1.5 V	2.4		10.0	µF

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. This value should be satisfied with due consideration of every condition as follows: operating temperature, DC bias, aging, etc.

Table 5.4 Operating Conditions (3/6)
(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	High level peak output current (2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7			-10.0	mA
$I_{OH(avg)}$	High level average output current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7			-5.0	mA
$I_{OL(peak)}$	Low level peak output current (2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7			10.0	mA
$I_{OL(avg)}$	Low level average output current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7			5.0	mA

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. The following conditions should be satisfied:
   - The sum of $I_{OL(peak)}$ of ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14, and P15 is 80 mA or less.
   - The sum of $I_{OL(peak)}$ of ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 is 80 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P0, P1, P2, and P11 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P8_6, P8_7, P9, P10, P14, and P15 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P3, P4, P5, P12, and P13 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P6, P7, and P8_0 to P8_4 is -40 mA or less.
3. Average value within 100 ms.

Table 5.5 Operating Conditions (4/6)

(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
$f_{(XIN)}$	Main clock oscillator frequency	4		8	MHz
$f_{(XRef)}$	Reference clock frequency	2		4	MHz
$f_{(PLL)}$	PLL clock oscillator frequency	96		144	MHz
$f_{(Base)}$	Base clock frequency			64	MHz
$t_{c(Base)}$	Base clock cycle time	15.625			ns
$f_{(CPU)}$	CPU operating frequency			64	MHz
$t_{c(CPU)}$	CPU clock cycle time	15.625			ns
$f_{(BCLK)}$	Peripheral bus clock operating frequency			32	MHz
$t_{c(BCLK)}$	Peripheral bus clock cycle time	31.25			ns
$f_{(PER)}$	Peripheral clock source frequency			32	MHz
$f_{(XCIN)}$	Sub clock oscillator frequency		32.768	50	kHz

Note:
1. The device is operationally guaranteed under these operating conditions.

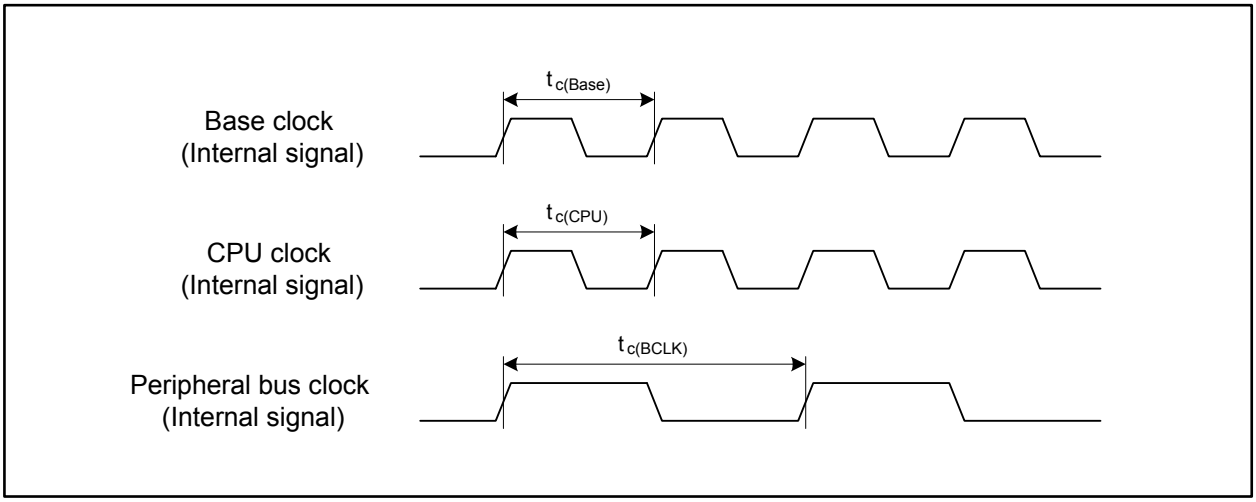


Figure 5.1 Clock Cycle Time

Table 5.6 Operating Conditions (5/6)

(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1, 2)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
$I_{IC(H)}$	High input injection current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_5, P7_7, P8_0 to P8_5, P9_1, P9_3 to P9_6, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7	$V_I > V_{CC}$			2	mA
$I_{IC(L)}$	Low input injection current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_5, P7_7, P8_0 to P8_5, P9_1, P9_3 to P9_6, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7	$V_I < V_{SS}$			-2	mA
$\Sigma\|I_{IC}\|$	Total injection current					20	mA

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. These conditions are applicable when each port is designated as input.

Table 5.7 Operating Conditions (6/6)
(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$V_{r(VCC)}$	Allowable ripple voltage	V_{CC} = 5.0 V			0.5	Vp-p
		V_{CC} = 3.0 V			0.3	Vp-p
$dV_{r(VCC)}/dt$	Ripple voltage gradient	V_{CC} = 5.0 V			±0.3	V/ms
		V_{CC} = 3.0 V			±0.3	V/ms
$f_{r(VCC)}$	Allowable ripple frequency				10	kHz

Note:
1. The device is operationally guaranteed under these operating conditions.

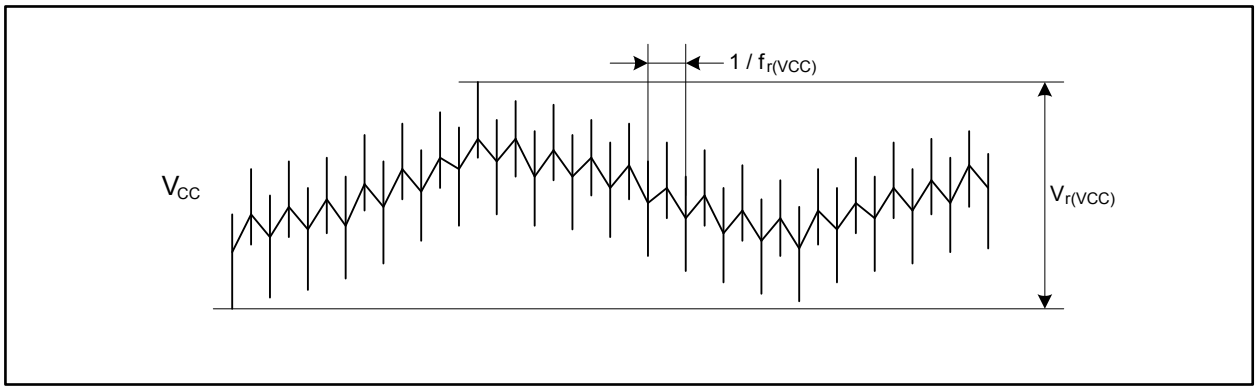


Figure 5.2 Ripple Waveform

Table 5.8 Flash Memory Electrical Characteristics
(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and Ta = T_{opr}, unless otherwise noted)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
—	Programming and erasure endurance of flash memory (1)	Program area	1000			times
		Data area	10000			times
—	4-word program time	Program area		150	900	µs
		Data area		300	1700	µs
—	Lock bit-program time	Program area		70	500	µs
		Data area		140	1000	µs
—	Block erasure time	4 Kbyte block		0.12	3.0	s
		32 Kbyte block		0.17	3.0	s
		64 Kbyte block		0.20	3.0	s
—	Data retention (2)	T_a = 55°C (3, 4)	20			years

Notes:
1. Program/erase definition
   This value represents the number of erasures per block.
   If the flash memory is programmed/erased n times, each block can be erased n times.
   i.e. If 4-word write is performed in 512 different addresses in the block A of 4 Kbyte and then the block is erased, it is considered the programming/erasure is performed just once.
   However a write in the same address more than once for one erasure is disabled (overwrite disabled).
2. The data retention time includes the periods when the supply voltage is not applied and no clock is provided.
3. This data retention includes 3000 hours in T_a = 125°C and 7000 hours in T_a = 85°C.
4. Contact a Renesas Electronics sales office regarding data retention time other than the above.

Table 5.9 E²dataFlash Electrical Characteristics
(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
—	Programming and erasure endurance of flash memory (1)		100000			times
—	Word program time			100	2000	µs
—	Block erasure time	32 byte block		15	200	ms
t_{PS}	Flash memory circuit start-up stabilization time			35	50	µs
—	Data retention (2)	T_a = 55°C (3, 4)	20			years

Notes:
1. Program/erase definition
   This value represents the number of erasure per block.
   If the flash memory is programmed/erased n times, each block can be erased n times.
   i.e. If a word write is performed in different 16 addresses in a block and then the block is erased, it is considered the programming/erasure is performed just once. However a write in the same address more than once for one erasure is disabled (overwrite disabled).
2. The data retention time includes the periods when the supply voltage is not applied and no clock is provided.
3. This data retention includes 3000 hours in T_a = 125°C and 7000 hours in T_a = 85°C.
4. Contact a Renesas Electronics sales office regarding data retention time other than the above.

Table 5.10 Power Supply Circuit Timing Characteristics
(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Internal power supply start-up stabilization time after the main power supply is turned on				2	ms

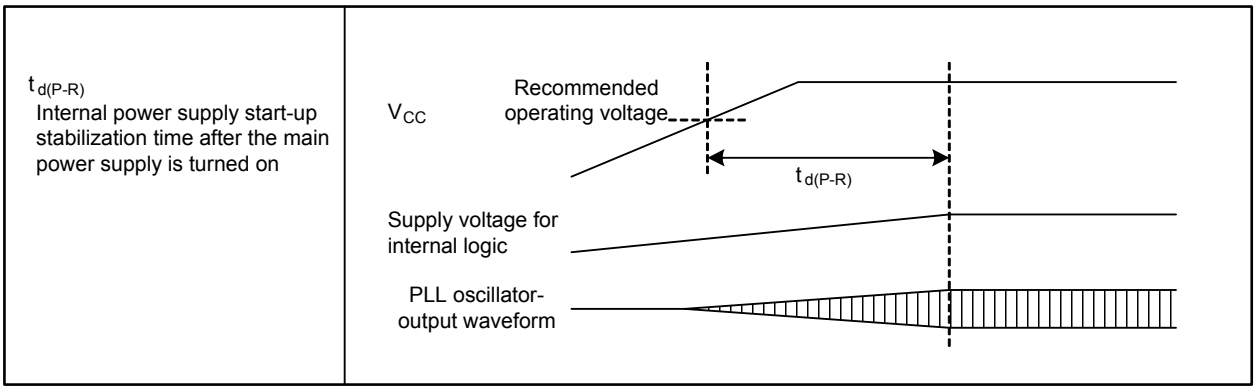


Figure 5.3 Power Supply Circuit Timing

Table 5.11 Electrical Characteristics of Voltage Regulator for Internal Logic (V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
V_{VDC1}	Output voltage			1.5		V

Table 5.12 Electrical Characteristics of Low Voltage Detector (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
ΔVdet	Detected voltage error				±0.2	V
Vdet(R)-Vdet(F)	Hysteresis width		0			V
—	Self-consuming current	V_{CC} = 5.0 V, low voltage detector enabled		4		μA
$t_{d(E-A)}$	Operation start time of low voltage detector				150	μs

Table 5.13 Electrical Characteristics of Oscillator (V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
$f_{SO(PLL)}$	PLL clock self-oscillation frequency		35	57	80	MHz
$\|\Delta f_{LOCK}\|$	Lock detection (1)				2	%
$\|\Delta f_{UNLOCK}\|$	Unlock detection (1)		2			%
$t_{LOCK(PLL)}$	PLL lock time (2, 3)	$f_{(XRef)}$ = 4 MHz			1	ms
$t_{jitter(p-p)}$	PLL jitter period (p-p)				2.0	ns
$f_{(OCO)}$	On-chip oscillator frequency		94	125	156	kHz

Notes:
1. This value is the deviation from target frequency.
2. This value is applicable only when the main clock oscillation is stable.
3. This value is the time until the PLF1 bit in the PLS register becomes 1.

Table 5.14 Electrical Characteristics of Clock Circuitry
(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
$t_{rec(WAIT)}$	Recovery time from wait mode to low power mode				225	µs
$t_{rec(STOP)}$	Recovery time from stop mode (1)				225	µs

Note:
1. This recovery time does not include the period until the main clock oscillator is stabilized. The CPU starts operating before the oscillator is stabilized.

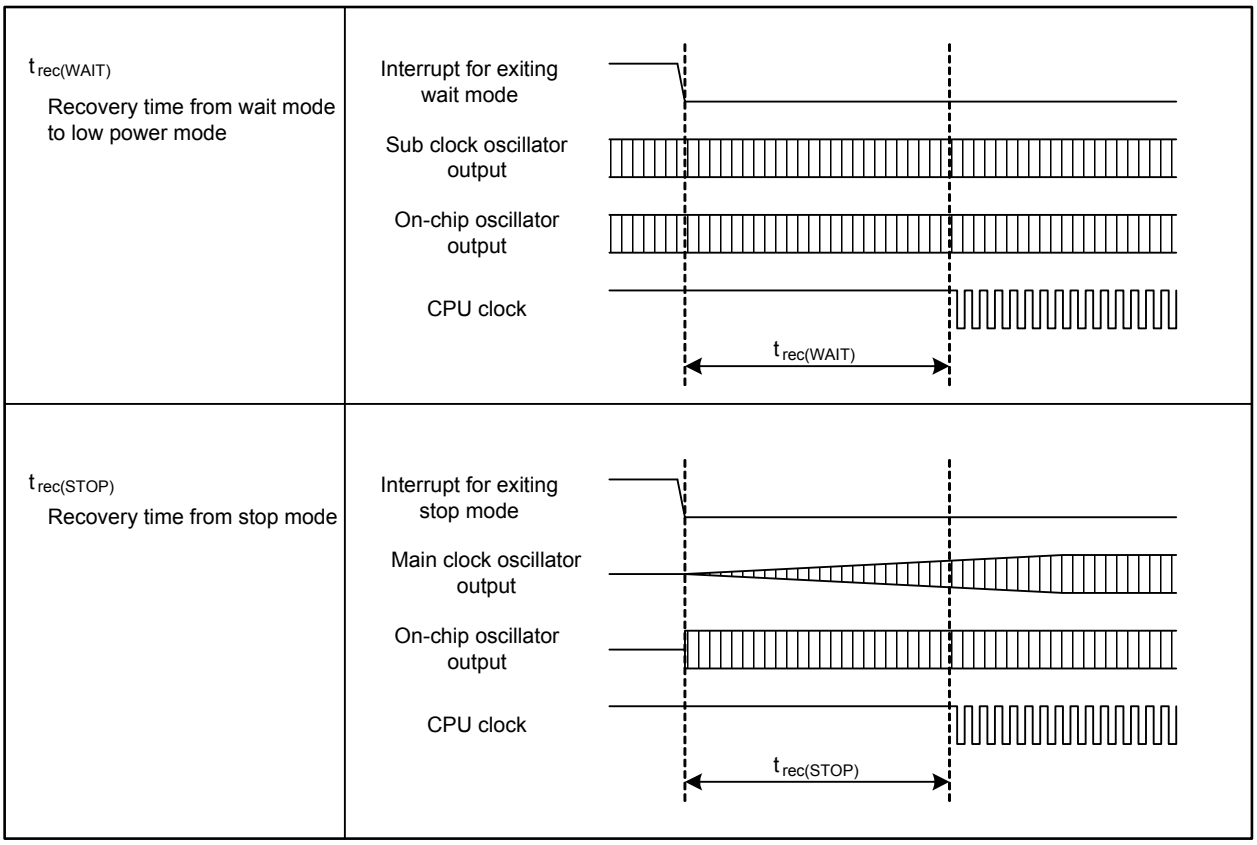


Figure 5.4 Clock Circuit Timing

Timing Requirements (V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and Ta = T_{opr}, unless otherwise noted)

Table 5.15 Flash Memory CPU Rewrite Mode Timing

Symbol	Characteristics	Value		Unit
		Min.	Max.	
t_{cR}	Read cycle time	200		ns
$t_{su(S-R)}$	Chip-select setup time for read	200		ns
$t_{h(R-S)}$	Chip-select hold time after read	0		ns
$t_{su(A-R)}$	Address setup time for read	200		ns
$t_{h(R-A)}$	Address hold time after read	0		ns
$t_{w(R)}$	Read pulse width	100		ns
t_{cW}	Write cycle time	200		ns
$t_{su(S-W)}$	Chip-select setup time for write	0		ns
$t_{h(W-S)}$	Chip-select hold time after write	30		ns
$t_{su(A-W)}$	Address setup time for write	0		ns
$t_{h(W-A)}$	Address hold time after write	30		ns
$t_{w(W)}$	Write pulse width	50		ns

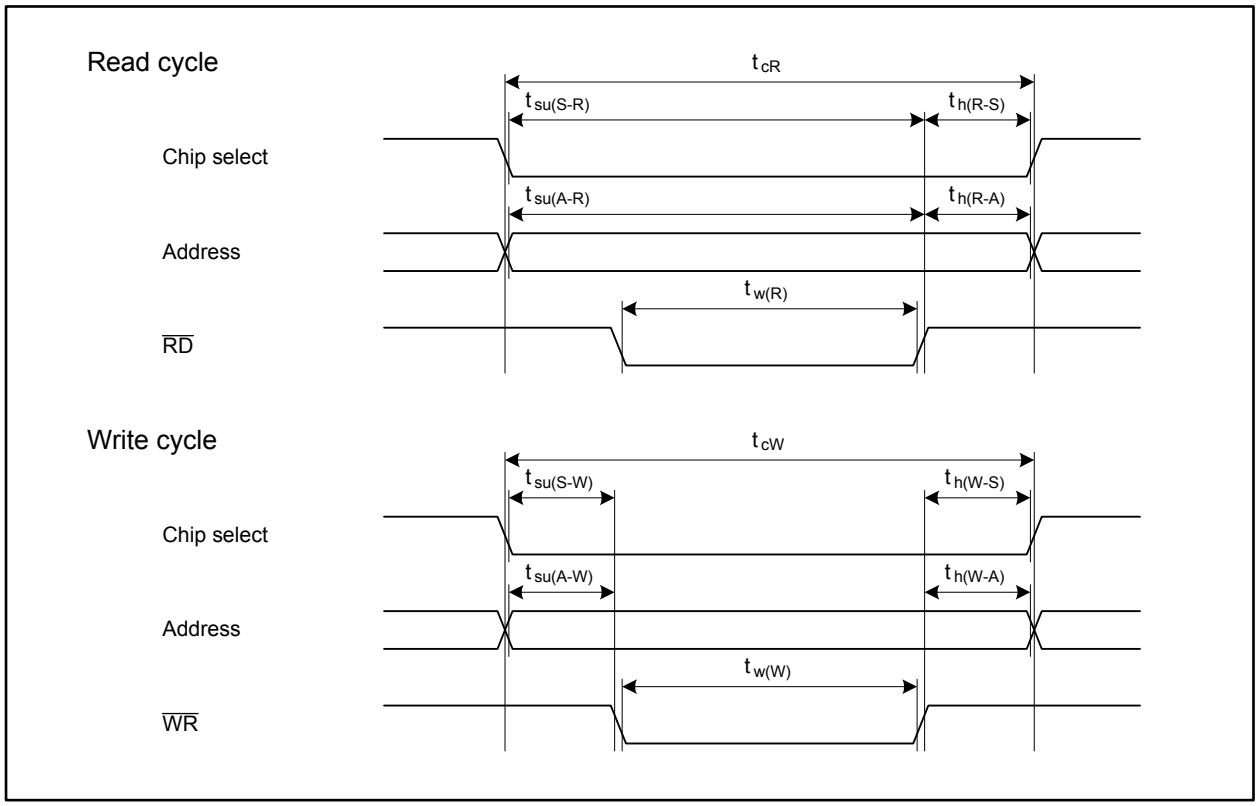


Figure 5.5 Flash Memory CPU Rewrite Mode Timing

V_{CC} = 5 V

Table 5.16 Electrical Characteristics (1/3)
(V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, T_a = T_{opr}, and $f_{(CPU)}$ = 64 MHz, unless otherwise noted)

Symbol	Characteristic		Measurement condition	Value			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7	I_{OH} = -5 mA	V_{CC} - 2.0		V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7	I_{OH} = -200 µA	V_{CC} - 0.3		V_{CC}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7	I_{OL} = 5 mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7	I_{OL} = 200 µA			0.45	V

V_{CC} = 5 V

Table 5.17 Electrical Characteristics (2/3)
(V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, T_a = T_{opr}, and $f_{(CPU)}$ = 64 MHz, unless otherwise noted)

Symbol	Characteristic		Measurement condition	Value			Unit
				Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	$\overline{NMI}$, $\overline{INT0}$ to $\overline{INT8}$, $\overline{KI0}$ to $\overline{KI3}$, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, $\overline{CTS0}$ to $\overline{CTS4}$, CLK0 to CLK4, RXD0 to RXD4, SCL0 to SCL2, SDA0 to SDA2, $\overline{SS0}$ to $\overline{SS2}$, SRXD0 to SRXD2, $\overline{ADTRG}$, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, IIO2_0 to IIO2_7, IIO3_0 to IIO3_7, UD0A, UD0B, UD1A, UD1B, $\overline{SCS0}$ to $\overline{SCS2}$, SSCK0 to SSCK2, SSI0 to SSI2, SSO0 to SSO2, LIN0_0IN to LIN0_3IN, LIN1_0IN to LIN1_3IN, CAN0IN to CAN3IN, $\overline{CAN0WU}$ to $\overline{CAN3WU}$			0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	High level input current	XIN, $\overline{RESET}$, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7	V_I = 5 V			1.0	µA
I_{IL}	Low level input current	XIN, $\overline{RESET}$, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7	V_I = 0 V			-1.0	µA
R_{PULLUP}	Pull-up resistor	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7	V_I = 0 V	30	50	170	kΩ
R_{fXIN}	Feedback resistor	XIN			1.5		MΩ
R_{fXCIN}	Feedback resistor	XCIN			15		MΩ

V_{CC} = 5 V

Table 5.18 Electrical Characteristics (3/3)
(V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement condition		Value			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current	In single-chip mode, output pins are left open and others are connected to V_{SS} XIN-XOUT Drive power: low XCIN-XCOUT Drive power: low	$f_{(CPU)}$ = 64 MHz, $f_{(BCLK)}$ = 32 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, PLL, Stopped: XCIN, OCO		43	70	mA
			$f_{(CPU)}$ = $f_{SO(PLL)}$/24 MHz, Active: PLL (self-oscillation), Stopped: XIN, XCIN, OCO		7		mA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(XIN)}$/256 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO		1.2		mA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown		220		µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(OCO)}$/4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown		230		µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(XIN)}$/256 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO, T_a = 25°C, Wait mode		960	1600	µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown, T_a = 25°C, Wait mode		8	140	µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(OCO)}$/4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown, T_a = 25°C, Wait mode		10	150	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 25°C		5	70	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 85°C			400	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 105°C			1200	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 125°C			2000	µA

V_{CC} = 5 V

Table 5.19 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = T_{opr}, and $f_{(BCLK)}$ = 32 MHz, unless otherwise noted)

Symbol	Characteristic	Measurement condition		Value			Unit
				Min.	Typ.	Max.	
—	Resolution	V_{REF} = V_{CC}				10	Bits
—	Absolute error	V_{REF} = V_{CC} = 5 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1			±3	LSB
			External op-amp connection mode			±7	LSB
INL	Integral non-linearity error	V_{REF} = V_{CC} = 5 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1			±3	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential non-linearity error					±1	LSB
—	Offset error					±3	LSB
—	Gain error					±3	LSB
R_{LADDER}	Resistor ladder	V_{REF} = V_{CC}		4		20	kΩ
t_{CONV}	Conversion time (10 bits)	ϕ_{AD} = 16 MHz, with sample and hold function		2.06			µs
		ϕ_{AD} = 16 MHz, without sample and hold function		3.69			µs
t_{CONV}	Conversion time (8 bits)	ϕ_{AD} = 16 MHz, with sample and hold function		1.75			µs
		ϕ_{AD} = 16 MHz, without sample and hold function		3.06			µs
t_{SAMP}	Sampling time	ϕ_{AD} = 16 MHz		0.188			µs
V_{IA}	Analog input voltage			0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	without sample and hold function		0.25		16	MHz
		with sample and hold function		1		16	MHz
$R_{PU(AST)}$	Pull-up resistor for open-circuit detection			5	10	15	kΩ
$R_{PD(AST)}$	Pull-down resistor for open-circuit detection			5	10	15	kΩ

V_{CC} = 5 V

Table 5.20 D/A Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute precision				1.0	%
t_S	Settling time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference input current	(1)			1.5	mA

Note:

1. One D/A converter is used. The DAi register (i = 0, 1) of the other unused converter is set to 00h. The resistor ladder for A/D converter is not considered.
   Even when the VCUT bit in the AD0CON1 register is set to 0 (V_{REF} disconnected), I_{VREF} is supplied.

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.21 External Clock Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(X)}$	External clock input period	125	250	ns
$t_{w(XH)}$	External clock input high level pulse width	50		ns
$t_{w(XL)}$	External clock input low level pulse width	50		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_w / t_c	External clock input duty	40	60	%

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.22 Timer A Input (Counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.23 Timer A Input (Gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.24 Timer A Input (External trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.25 Timer A Input (External trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.26 Timer A Input (Increment/decrement count switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input clock cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.27 Timer B Input (Counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time (one edge counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (one edge counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (one edge counting)	80		ns
$t_{c(TB)}$	TBiIN input clock cycle time (both edges counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (both edges counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (both edges counting)	80		ns

Table 5.28 Timer B Input (Pulse period measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

Table 5.29 Timer B Input (Pulse-width measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.30 Serial Interface

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input clock cycle time	200		ns
$t_{w(CKH)}$	CLKi input high level pulse width	80		ns
$t_{w(CKL)}$	CLKi input low level pulse width	80		ns
$t_{su(D-C)}$	RXDi input setup time	80		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.31 A/D Trigger Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(ADH)}$	$\overline{ADTRG}$ input high level pulse width Hardware trigger input high level pulse width	$\frac{3}{\phi_{AD}}$		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input low level pulse width Hardware trigger input high level pulse width	125		ns

Table 5.32 External Interrupt $\overline{INTi}$ Input

Symbol	Characteristic		Value		Unit
			Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high level pulse width (1)	Edge sensitive	250		ns
		Level sensitive	$t_{c(CPU)}$ + 200		ns
$t_{w(INL)}$	$\overline{INTi}$ input low level pulse width (1)	Edge sensitive	250		ns
		Level sensitive	$t_{c(CPU)}$ + 200		ns

Note:
1. The values are applied in case filtering function is disabled.

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.33 Serial Bus Interface

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$f_{(SSCK)}$	SSCKi frequency		4	MHz
$t_{c(SSCK)}$	SSCKi clock cycle time	250		ns
$t_{w(SSCKH)}$	SSCKi input high level pulse width	0.35 × $t_{c(SSCK)}$	0.6 × $t_{c(SSCK)}$	ns
$t_{w(SSCKL)}$	SSCKi input low level pulse width	0.35 × $t_{c(SSCK)}$	0.6 × $t_{c(SSCK)}$	ns
$t_{r(SSCK)}$	SSCKi input rising time		1	µs
$t_{f(SSCK)}$	SSCKi input falling time		1	µs
$t_{su(SCS-SSCK)}$	SCSi input setup time	$t_{c(BCLK)}$ + 50		ns
$t_{h(SSCK-SCS)}$	SCSi input hold time	$t_{c(BCLK)}$ + 50		ns
$t_{su(SSI-SSCK)}$	SSI input setup time	80		ns
$t_{h(SSCK-SSI)}$	SSI input hold time	10		ns
$t_{su(SSO-SSCK)}$	SSO input setup time	80		ns
$t_{h(SSCK-SSO)}$	SSO input hold time	20		ns

V_{CC} = 5 V

Switching Characteristics (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.34 Serial Interface

Symbol	Characteristic	Measurement condition	Value		Unit
			Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	Refer to Figure 5.6		80	ns
$t_{h(C-Q)}$	TXDi output hold time		0		ns

Table 5.35 Serial Bus Interface

Symbol	Characteristic	Measurement condition	Value		Unit
			Min.	Max.	
$t_{w(SSCKH)}$	SSCKi output high level pulse width	Refer to Figure 5.6	0.35 × $t_{c(SSCK)}$	0.6 × $t_{c(SSCK)}$	ns
$t_{w(SSCKL)}$	SSCKi output low level pulse width		0.35 × $t_{c(SSCK)}$	0.6 × $t_{c(SSCK)}$	ns
$t_{r(SSCK)}$	SSCKi output rising time			20	ns
$t_{f(SSCK)}$	SSCKi output falling time			20	ns
$t_{d(SCS-SSCK)}$	SSCKi output delay time for SCSi			0.5 × $t_{c(SSCK)}$ + 20	ns
$t_{d(SSCK-SCS)}$	SCSi output delay time for SSCKi		0.5 × $t_{c(SSCK)}$ - 20		ns
$t_{en(SCS-SSO)}$	SSOi output enable time			1.5 × $t_{c(BCLK)}$ + 100	ns
$t_{dis(SCS-SSO)}$	SSOi output disable time			1.5 × $t_{c(BCLK)}$ + 100	ns
$t_{en(SCS-SSI)}$	SSIi output enable time			1.5 × $t_{c(BCLK)}$ + 100	ns
$t_{dis(SCS-SSI)}$	SSIi output disable time			1.5 × $t_{c(BCLK)}$ + 100	ns
$t_{d(SSCK-SSO)}$	SSOi output delay time for SSCKi			30	ns
$t_{d(SSCK-SSI)}$	SSIi output delay time for SSCKi			85	ns
$t_{rec(SCS)}$	SCSi output high level period in continuous transmission			0.625 × $t_{c(SSCK)}$	ns

V_{CC} = 3.3 V

Table 5.36 Electrical Characteristics (1/3) (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, T_a = T_{opr}, and $f_{(CPU)}$ = 64 MHz, unless otherwise noted)

Symbol	Characteristic		Measurement condition	Value			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7	I_{OH} = -1 mA	V_{CC} - 0.6		V_{CC}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7	I_{OL} = 1 mA			0.5	V

V_{CC} = 3.3 V

Table 5.37 Electrical Characteristics (2/3) (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, T_a = T_{opr}, and $f_{(CPU)}$ = 64 MHz, unless otherwise noted)

Symbol	Characteristic		Measurement condition	Value			Unit
				Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	$\overline{NMI}$, $\overline{INT0}$ to $\overline{INT8}$, $\overline{KI0}$ to $\overline{KI3}$, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, $\overline{CTS0}$ to $\overline{CTS4}$, CLK0 to CLK4, RXD0 to RXD4, SCL0 to SCL2, SDA0 to SDA2, $\overline{SS0}$ to $\overline{SS2}$, SRXD0 to SRXD2, $\overline{ADTRG}$, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, IIO2_0 to IIO2_7, IIO3_0 to IIO3_7, UD0A, UD0B, UD1A, UD1B, $\overline{SCS0}$ to $\overline{SCS2}$, SSCK0 to SSCK2, SSI0 to SSI2, SSO0 to SSO2, LIN0_0IN to LIN0_3IN, LIN1_0IN to LIN1_3IN, CAN0IN to CAN3IN, $\overline{CAN0WU}$ to $\overline{CAN3WU}$		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	High level input current	XIN, $\overline{RESET}$, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7	V_I = 3.3 V			1.0	µA
I_{IL}	Low level input current	XIN, $\overline{RESET}$, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7	V_I = 0 V			-1.0	µA
R_{PULLUP}	Pull-up resistor	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7	V_I = 0 V	50	100	500	kΩ
R_{fXIN}	Feedback resistor	XIN			3		MΩ
R_{fXCIN}	Feedback resistor	XCIN			25		MΩ

V_{CC} = 3.3 V

Table 5.38 Electrical Characteristics (3/3)
(V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement condition		Value			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current	In single-chip mode, output pins are left open and others are connected to V_{SS} XIN-XOUT Drive power: low XCIN-XCOUT Drive power: low	$f_{(CPU)}$ = 64 MHz, $f_{(BCLK)}$ = 32 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, PLL, Stopped: XCIN, OCO		43	70	mA
			$f_{(CPU)}$ = $f_{SO(PLL)}$/24 MHz, Active: PLL (self-oscillation), Stopped: XIN, XCIN, OCO		7		mA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(XIN)}$/256 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO		670		µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown		180		µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(OCO)}$/4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown		190		µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(XIN)}$/256 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO, T_a = 25°C, Wait mode		500	900	µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown, T_a = 25°C, Wait mode		8	140	µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(OCO)}$/4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown, T_a = 25°C, Wait mode		10	150	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 25°C		5	70	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 85°C			400	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 105°C			1200	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 125°C			2000	µA

V_{CC} = 3.3 V

Table 5.39 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 3.0 to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_a = T_{opr}, and $f_{(BCLK)}$ = 32 MHz, unless otherwise noted)

Symbol	Characteristic	Measurement condition		Value			Unit
				Min.	Typ.	Max.	
—	Resolution	V_{REF} = V_{CC}				10	Bits
—	Absolute error	V_{REF} = V_{CC} = 3.3 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1			±5	LSB
			External op-amp connection mode			±7	LSB
INL	Integral non-linearity error	V_{REF} = V_{CC} = 3.3 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1			±5	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential non-linearity error	V_{REF} = V_{CC} = 3.3 V				±1	LSB
—	Offset error					±3	LSB
—	Gain error					±3	LSB
R_{LADDER}	Resistor ladder	V_{REF} = V_{CC}		4		20	kΩ
t_{CONV}	Conversion time (10 bits)	ϕ_{AD} = 10 MHz, with sample and hold function		3.3			µs
t_{CONV}	Conversion time (8 bits)	ϕ_{AD} = 10 MHz, with sample and hold function		2.8			µs
t_{SAMP}	Sampling time	ϕ_{AD} = 10 MHz		0.3			µs
V_{IA}	Analog input voltage			0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	without sample and hold function		0.25		10	MHz
		with sample and hold function		1		10	MHz
$R_{PU(AST)}$	Pull-up resistor for open-circuit detection			5	10	15	kΩ
$R_{PD(AST)}$	Pull-down resistor for open-circuit detection			5	10	15	kΩ

V_{CC} = 3.3 V

Table 5.40 D/A Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 3.0 to 3.6 V, V_{SS} = AV_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute precision				1.0	%
t_S	Settling time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference input current	(1)			1.0	mA

Note:
1. One D/A converter is used. The DAi register (i = 0, 1) of the other unused converter is set to 00h. The resistor ladder for A/D converter is not considered.
Even when the VCUT bit in the AD0CON1 register is set to 0 (V_{REF} disconnected), I_{VREF} is supplied.

V_{CC} = 3.3 V

Timing Requirements (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.41 External Clock Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(X)}$	External clock input period	125	250	ns
$t_{w(XH)}$	External clock input high level pulse width	50		ns
$t_{w(XL)}$	External clock input low level pulse width	50		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_w / t_c	External clock input duty	40	60	%

V_{CC} = 3.3 V

Timing Requirements (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.42 Timer A Input (Counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.43 Timer A Input (Gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.44 Timer A Input (External trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.45 Timer A Input (External trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.46 Timer A Input (Increment/decrement count switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input clock cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

V_{CC} = 3.3 V

Timing Requirements (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.47 Timer B Input (Counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time (one edge counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (one edge counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (one edge counting)	80		ns
$t_{c(TB)}$	TBiIN input clock cycle time (both edges counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (both edges counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (both edges counting)	80		ns

Table 5.48 Timer B Input (Pulse period measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

Table 5.49 Timer B Input (Pulse-width measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

V_{CC} = 3.3 V

Timing Requirements (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.50 Serial Interface

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input clock cycle time	200		ns
$t_{w(CKH)}$	CLKi input high level pulse width	80		ns
$t_{w(CKL)}$	CLKi input low level pulse width	80		ns
$t_{su(D-C)}$	RXDi input setup time	80		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.51 A/D Trigger Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(ADH)}$	$\overline{ADTRG}$ input high level pulse width Hardware trigger input high level pulse width	$\frac{3}{\phi_{AD}}$		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input low level pulse width Hardware trigger input high level pulse width	125		ns

Table 5.52 External Interrupt $\overline{INTi}$ Input

Symbol	Characteristic		Value		Unit
			Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high level pulse width (1)	Edge sensitive	250		ns
		Level sensitive	$t_{C(CPU)}$ + 200		ns
$t_{w(INL)}$	$\overline{INTi}$ input low level pulse width (1)	Edge sensitive	250		ns
		Level sensitive	$t_{C(CPU)}$ + 200		ns

Note:
1. The values are applied in case filtering function is disabled.

V_{CC} = 3.3 V

Timing Requirements (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.53 Serial Bus Interface

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$f_{(SSCK)}$	SSCKi frequency		4	MHz
$t_{c(SSCK)}$	SSCKi clock cycle time	250		ns
$t_{w(SSCKH)}$	SSCKi input high level pulse width	0.35 × $t_{c(SSCK)}$	0.6 × $t_{c(SSCK)}$	ns
$t_{w(SSCKL)}$	SSCKi input low level pulse width	0.35 × $t_{c(SSCK)}$	0.6 × $t_{c(SSCK)}$	ns
$t_{r(SSCK)}$	SSCKi input rising time		1	µs
$t_{f(SSCK)}$	SSCKi input falling time		1	µs
$t_{su(SCS-SSCK)}$	SCSi input setup time	$t_{c(BCLK)}$ + 50		ns
$t_{h(SSCK-SCS)}$	SCSi input hold time	$t_{c(BCLK)}$ + 50		ns
$t_{su(SSI-SSCK)}$	SSI input setup time	100		ns
$t_{h(SSCK-SSI)}$	SSI input hold time	10		ns
$t_{su(SSO-SSCK)}$	SSO input setup time	100		ns
$t_{h(SSCK-SSO)}$	SSO input hold time	20		ns

V_{CC} = 3.3 V

Switching Characteristics (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.54 Serial Interface

Symbol	Characteristic	Measurement condition	Value		Unit
			Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	Refer to Figure 5.6		80	ns
$t_{h(C-Q)}$	TXDi output hold time		0		ns

Table 5.55 Serial Bus Interface

Symbol	Characteristic	Measurement condition	Value		Unit
			Min.	Max.	
$t_{w(SSCKH)}$	SSCKi output high level pulse width	Refer to Figure 5.6	0.35 × $t_{c(SSCK)}$	0.6 × $t_{c(SSCK)}$	ns
$t_{w(SSCKL)}$	SSCKi output low level pulse width		0.35 × $t_{c(SSCK)}$	0.6 × $t_{c(SSCK)}$	ns
$t_{r(SSCK)}$	SSCKi output rising time			35	ns
$t_{f(SSCK)}$	SSCKi output falling time			35	ns
$t_{d(SCS-SSCK)}$	SSCKi output delay time for SCSi			0.5 × $t_{c(SSCK)}$ + 40	ns
$t_{d(SSCK-SCS)}$	SCSi output delay time for SSCKi		0.5 × $t_{c(SSCK)}$ - 40		ns
$t_{en(SCS-SSO)}$	SSOi output enable time			1.5 × $t_{c(BCLK)}$ + 100	ns
$t_{dis(SCS-SSO)}$	SSOi output disable time			1.5 × $t_{c(BCLK)}$ + 100	ns
$t_{en(SCS-SSI)}$	SSIi output enable time			1.5 × $t_{c(BCLK)}$ + 100	ns
$t_{dis(SCS-SSI)}$	SSIi output disable time			1.5 × $t_{c(BCLK)}$ + 100	ns
$t_{d(SSCK-SSO)}$	SSOi output delay time for SSCKi			50	ns
$t_{d(SSCK-SSI)}$	SSIi output delay time for SSCKi			120	ns
$t_{rec(SCS)}$	SCSi output high level period in continuous transmission			0.625 × $t_{c(SSCK)}$	ns

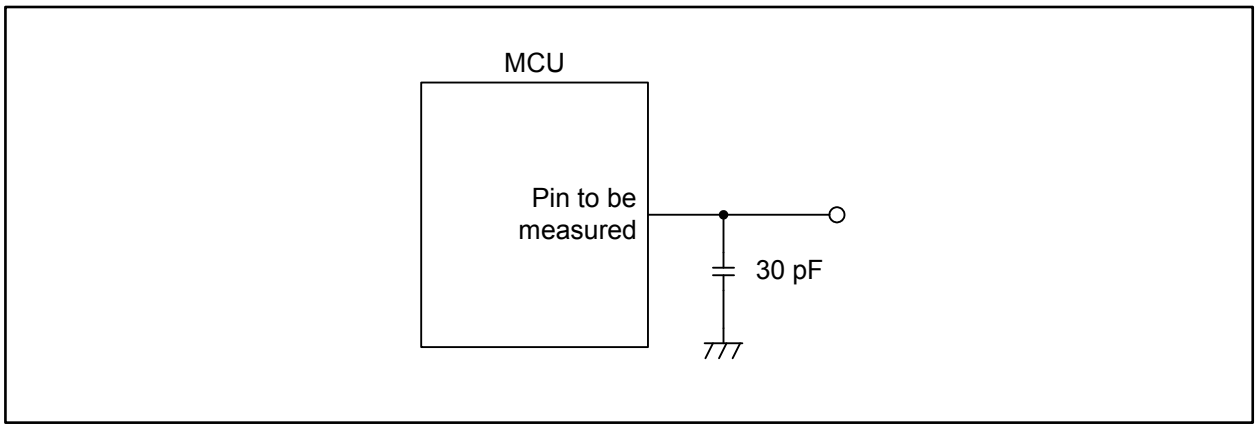


Figure 5.6 Switching Characteristic Measurement Circuit

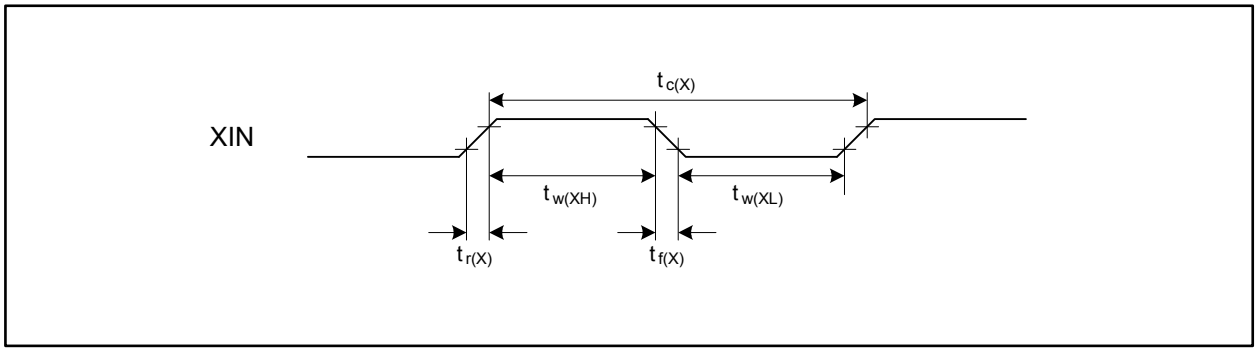


Figure 5.7 External Clock Input Timing

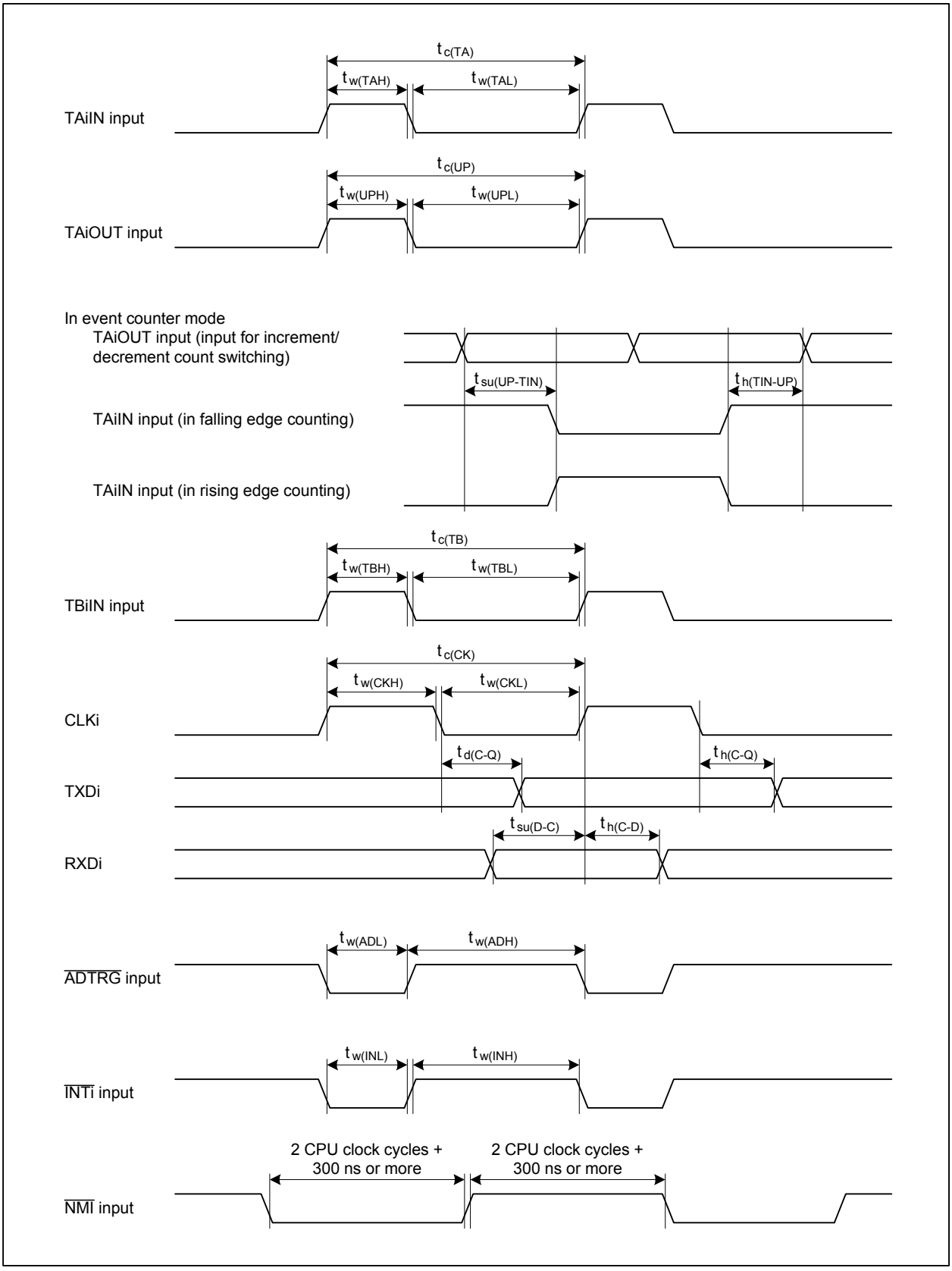


Figure 5.8 Timing of Peripheral Functions

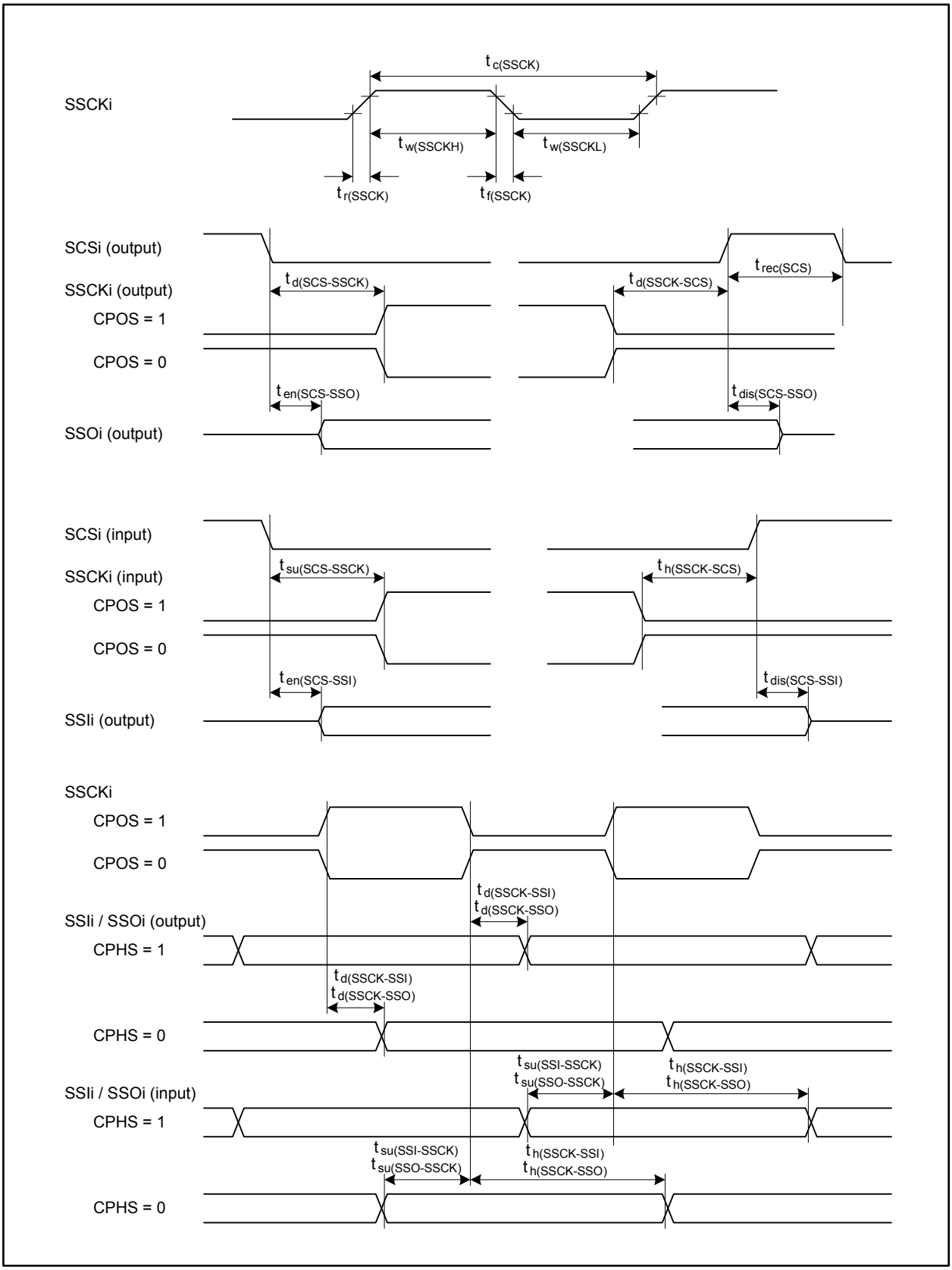
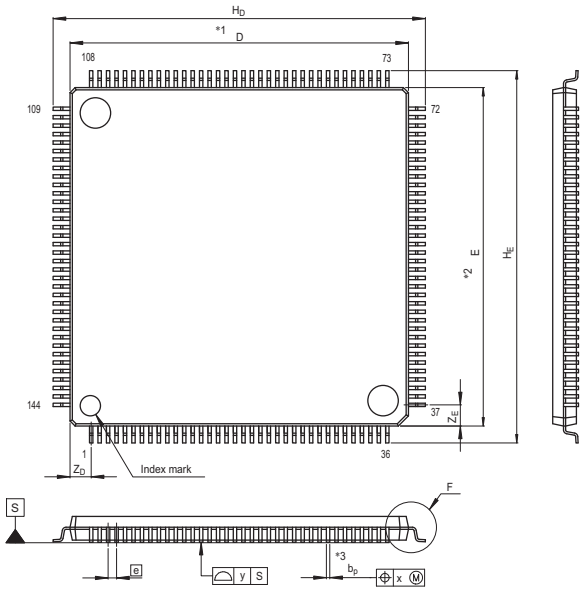
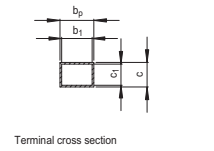


Figure 5.9 Timing of Serial Bus Interface

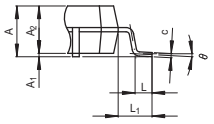
Appendix 1. Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Revision History	R32C/153 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.30	Feb 14, 2008	—	Initial release
1.02	Nov 30, 2009	—	Second edition released
			Chapter 1. Overview
		—	• Made minor text modifications to this chapter
		1	• Added “(MCUs)” to line 1 of **1.1**
		3	• Changed the following expressions in **Table 1.2**: “erase/program” to “program/erase”, “Read protection” to “Security protection”, “ID code check” to “ID code protect”, and “on-board flash re-programming” to “on-board flash programming”
		5	• Deleted hyphen before ROM number in **Figure 1.1**
		6	• Changed **Figure 1.2**
		7	• Modified “$\overline{K13}$” to “$\overline{K10}$” for pins 133 to 136 in **Figure 1.3** to “$\overline{KI3}$” to “$\overline{KI0}$”
		10	• Corrected a typo “LIN // CAN Module Pin” in **Table 1.6** to “LIN / CAN Module Pin”
		12-14	• Changed descriptions “Functional Category” and “Function” in **Tables 1.8 to 1.10** to “Function” and “Description”, respectively
			Chapter 2. Central Processing Unit
		—	• Made major text modifications to this chapter
		15, 16	• Changed description “Interrupt table register” in **Figure 2.1 and 2.1.6** to “Interrupt vector table base register”
			Chapter 3. Memory
		—	• Made major text modifications to this chapter
			Chapter 4. Special Function Registers
		20	• Changed hexadecimal format of reset values for registers CCR and FMCR in **Table 4.1** to binary
		21-22	• Changed the following expressions “DMAi Interrupt” and “Start/Stop Condition” in **Tables 4.2 to 4.3** to “DMAi Transfer Complete Interrupt” and “Start Condition/Stop Condition”, respectively
		26	• Deleted “6” from register name for register G2FS in **Table 4.7**
		29	• Changed binary format of reset values for U3RB and U4RB in **Table 4.10** to hexadecimal
		31	• Changed register symbols “G3TMi/G0POj” in **Table 4.12** to “G3TMi/G3POj”
		32	• Changed expression of register name “Xi Register Yi Register” and symbol “XiR, YiR” in **Table 4.13** to “Xi Register/Yi Register” and “XiR/YiR”, respectively
		37	• Changed hexadecimal format of reset values for registers PDi in **Table 4.18** to binary
		39	• Modified reset value for register PLS in **Table 4.20** to “1XXX XX00b”
		41	• Modified reset value for register IFS7 in **Table 4.22** to “XXXX XXX0b”
		41-43	• Modified register name “Port Pi_j Port Function Select Register” in **Tables 4.22 to 4.24** to “Port Pi_j Function Select Register”

Rev.	Date	Description	
		Page	Summary
		45	• Modified the following register names in **Table 4.26**: “DMAi Source Select Register 2” to “DMAi Request Source Select Register 2” and “DMAi Source Select Register 1” to “DMAi Request Source Select Register”; Changed expression “Wake-up/Interrupt Priority Level Control Register” to “Wake-up IPL Setting Register”
		46-47	• Modified “X” in reset values for unassigned bits to “0” for the following registers in **Tables 4.27 to 4.28**: LiCW, LiBRG, LiMD0, LiBRK, LiSPC, LiRFC, LiSC, LiTC, LiST, and LiEST
		47	• Corrected register symbol “L1FRC” in **Table 4.28** to “L1RFC”
		64, 78, 92, 106	• Modified reset value “00h” for C3CLKR in **Table 4.45**, C2CLKR in **Table 4.59**, C1CLKR in **Table 4.73**, and C0CLKR in **Table 4.87** to “000X 0000b”
		106	• Added addresses “047F60h to 047FFFh” and “048000h to 04FFFFh” to **Table 4.87**
			Chapter 5. Electrical Characteristics
		—	• Added initially
1.10	Sep 06, 2010	—	Third edition released
			This manual in general
		—	• Applied new Renesas templates and formats to the manual • Changed company name to “Renesas Electronics Corporation” and changed related descriptions due to business merger of Renesas Technology Corporation and NEC Electronics Corporation (under Chapters 1 and 5) • Modified expressions “version J”, “version L”, and “version K” to “J version”, “L version”, and “K version”, respectively (under Chapters 1 and 5)
			Chapter 1. Overview
		4	• Completed all “under development” phases in **Table 1.3**
		7	• Revised **Figure 1.3**
		12	• Modified expression “fC” in **Table 1.8** to “low speed clocks”
			Chapter 4. SFRs
		25, 28, 31	• Changed register name “Group i Timer Measurement Prescaler Register” in **Tables 4.6, 4.9, and 4.12** to “Group i Time Measurement Prescaler Register”
		32	• Modified expression “XY Control Register” in **Table 4.13** to “X-Y Control Register”
		34	• Changed register name “UART2 Transmission/Receive Mode Register” in **Table 4.15** to “UART2 Transmit/Receive Mode Register”; Changed hexadecimal format of reset values for registers TABSR, ONSF, and TRGSR to binary
		45	• Changed register name “External Interrupt Source Select Register i” in **Table 4.26** to “External Interrupt Request Source Select Register i”
		64, 78, 92, 106	• Modified register names “CANi Reception Error Count Register” and “CANi Transmission Error Count Register” in **Tables 4.45, 4.59, 4.73, and 4.87** to “CANi Receive Error Count Register” and “CANi Transmit Error Count Register”, respectively

Revision History	R32C/153 Group Datasheet

Rev.	Date	Description	
		Page	Summary
			Chapter 5. Electrical Characteristics
		—	• Changed expression “clock period” to “clock cycle time”
		116	• Changed typical and maximum values for “$f_{SO(PLL)}$” in **Table 5.13**; Added values for “$\|\Delta f_{LOCK}\|$” and “$\|\Delta f_{UNLOCK}\|$”
		118	• Changed expressions “$\overline{CS0}$” and “A23 to A0, $\overline{BC3}$ to $\overline{BC0}$” in **Figure 5.5** to “Chip select” and “Address”, respectively
			Appendix 1. Package Dimensions
		144	• Added a seating plane to the drawing of package dimension

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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