TGA4548-SM

17 - 20 GHz 10 W GaN Power Amplifier

Product Overview

Qorvo's TGA4548-SM is a high frequency, high power MMIC amplifier fabricated on Qorvo's production 0.15um GaN on SiC process (QGaN15). The TGA4548-SM operates from 17 – 20 GHz and typically provides 10 W saturated output power with power-added efficiency of 30% and large-signal gain of 22 dB. This combination of high frequency performance provides the flexibility designers are looking for to improve system performance while reducing size and cost. The TGA4548-SM also has an integrated power detector to support system diagnostics and other needs.

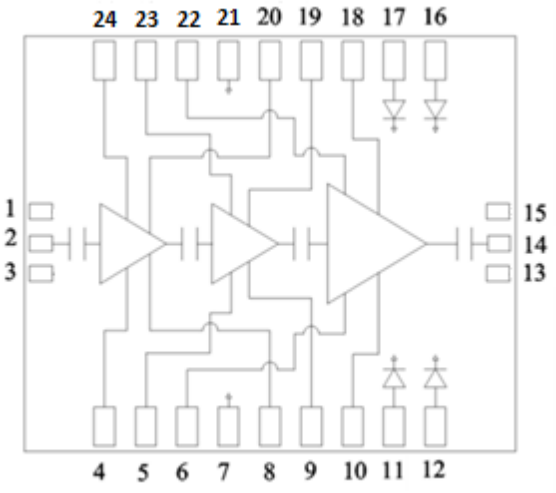
The TGA4548-SM is offered in a small 5x5.5 mm surface mount package, matched to 50Ω and has integrated DC blocking capacitors on both RF ports allowing for simple system integration. The frequency coverage and operational flexibility allows it support satellite communication as well as point to point data links.

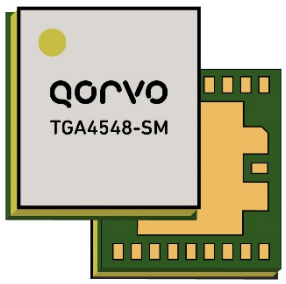
The TGA4548-SM is 100% DC and RF tested to ensure compliance to electrical specifications.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Functional Block Diagram





24-Lead 5.0 x 5.5 x 1.7 mm Package

Key Features

- Frequency Range: 17 – 20 GHz
- Power: 40 dBm Psat
- Small Signal Gain: 27 dB
- Large Signal Gain: 22 dB
- Integrated Power Detector
- PAE: 30% at P_{IN} = 12 dBm
- Bias: VD1 = VD2 = VD3 = +28 V, ID1 + ID2 + ID3 = 300 mA
- Package Dimensions: 5.0 x 5.5 x 1.7 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Applications

- Point-to-Point Radio
- Satellite Communications

Ordering Information

Part No.	ECCN	Description
TGA4548-SM-T/R	3A001.b.2.c	200 pieces on a 7" reel (standard)
TGA4548-SMS2	3A001.b.2.c	Waffle Tray with 4 pcs
TGA4548-SMEVB	EAR99	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-8 to 0 V
RF Input Power, CW, 50 Ω, T=25 °C	26 dBm
Dissipated Power (P_{DISS}), CW, 85°C	45 W
Storage Temperature	–55 to +150 °C
Mounting Temperature (30 seconds)	320 °C
Channel Temperature (T_{CH})	275 °C
Drain Current (I_{D1}), Top or Bottom	500 mA
Drain Current (I_{D2}), Top or Bottom	500 mA
Drain Current (I_{D3}), Top and Bottom	2 A
Forward Gate Current (I_{G1}), Top or Bottom	3 mA
Forward Gate Current (I_{G2}), Top or Bottom	12 mA
Forward Gate Current (I_{G3}), Top and Bottom	48 mA
Reference Power Detect (I_{ref})	4 mA
Power Detect Diode (I_{det})	4 mA

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_D)		+28		V
Operating Temp. Range	–40	+25	+85	°C
I_{DQ}		300		mA
V_G		–2.6		V
I_D drive (at +38dBm Pout)		930		mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

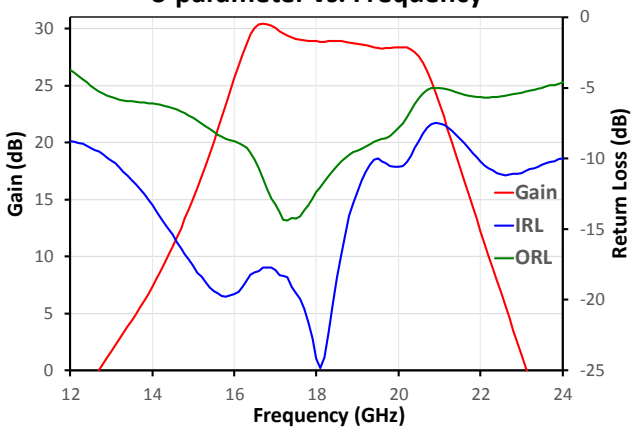
Parameter	Conditions [1]	Min	Typ	Max	Units
Operational Frequency Range		17		20	GHz
Small Signal Gain			27		dB
Input Return Loss			17		dB
Output Return Loss			10		dB
Output Power at Saturation, Psat			41		dBm
Power Added Efficiency, PAE	Pin = 12 dBm, 17.7 GHz Pin = 12 dBm, 18.5 GHz Pin = 12 dBm, 19.7 GHz		34 34 28		%
Third Order Intermodulation, IM3	Pout = +34 dBm/tone		–25		dBc
Gain Temperature Coefficient	T_{diff} = (85 – (–40)) °C		–0.054		dB/°C
Power Temperature Coefficient	T_{diff} = (85 – (–40)) °C, P_{in} = +5 dBm		–0.041		dBm/°C

Notes:
1. Test conditions unless otherwise noted: VD1 = VD2 = VD3 = 28V, ID1 + ID2 + ID3 = 300mA, VG1 = VG2 = VG3 = –2.6V typical, Temp = +25 °C, Z0 = 50 Ω

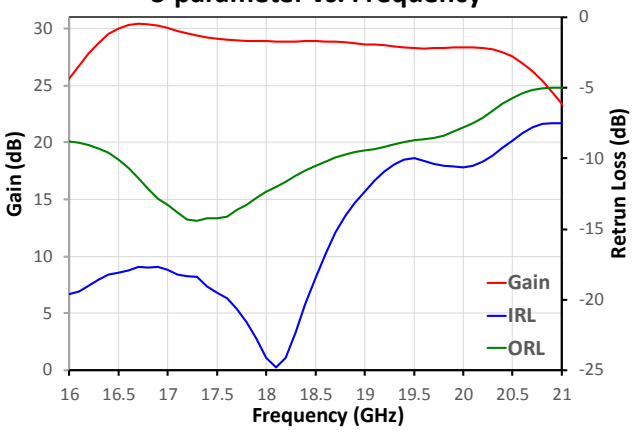
Performance Plots

Test conditions unless otherwise noted: VD1=VD2=VD3=28V, ID1+ID2+ID3=300mA, VG1=VG2=VG3=-2.6V typical, Temp = +25 °C, Z_0 = 50 Ω

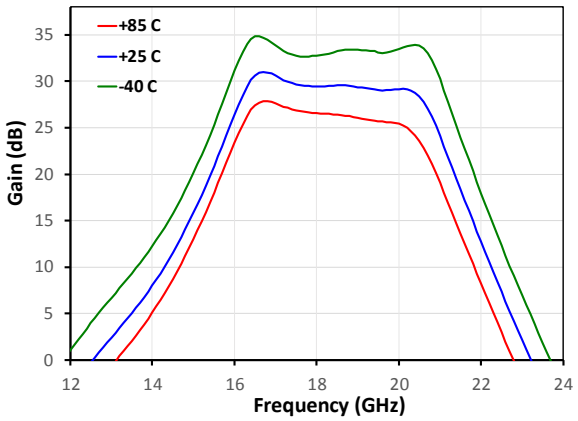
S-parameter vs. Frequency



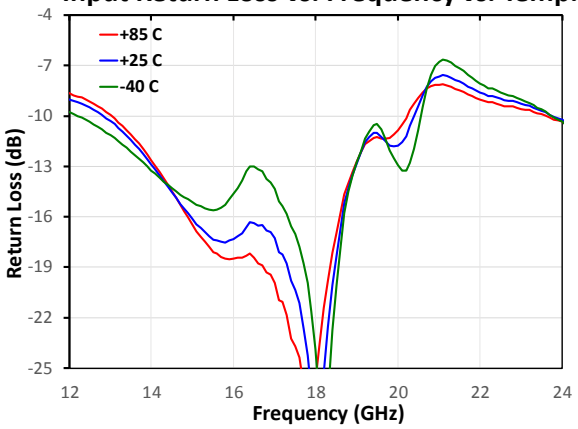
S-parameter vs. Frequency



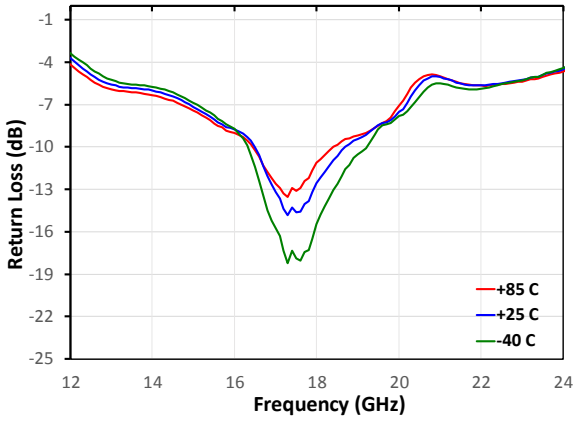
Gain vs. Frequency vs. Temp.



Input Return Loss vs. Frequency vs. Temp.



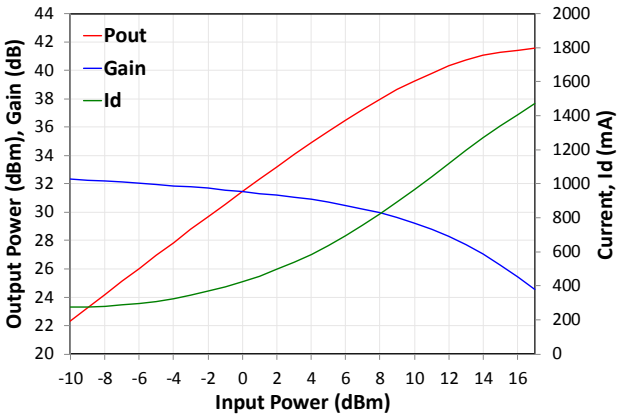
Output Return Loss vs. Frequency vs. Temp.



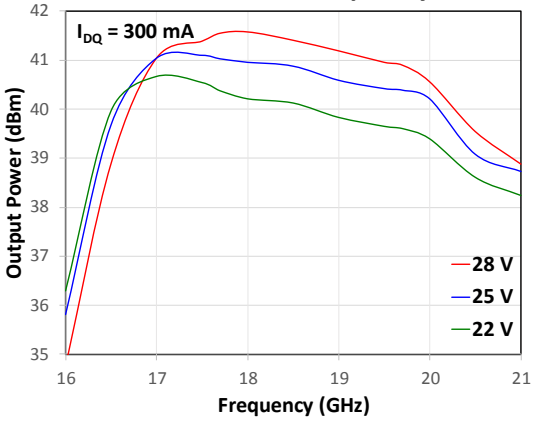
Performance Plots

Test conditions unless otherwise noted: VD1=VD2=VD3=28V, ID1+ID2+ID3=300mA, VG1=VG2=VG3=-2.6V typical, Temp = +25 °C, Z_0 = 50 Ω

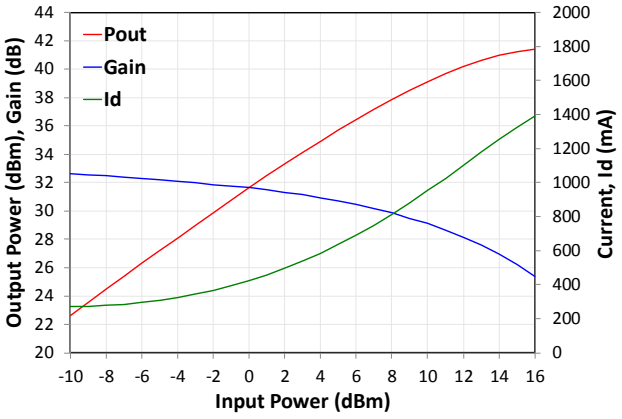
Pout, Gain, Id vs. Pin @ 17.7 GHz



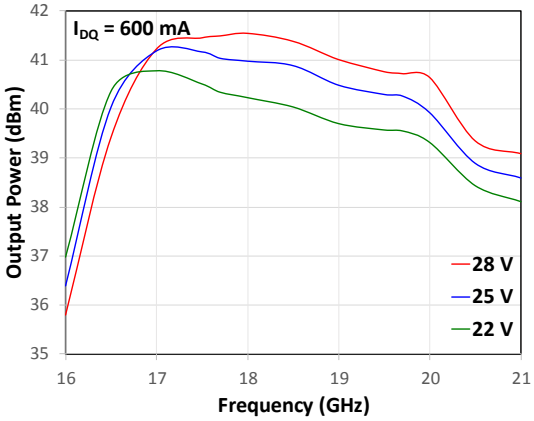
Psat vs. Vd vs. Frequency



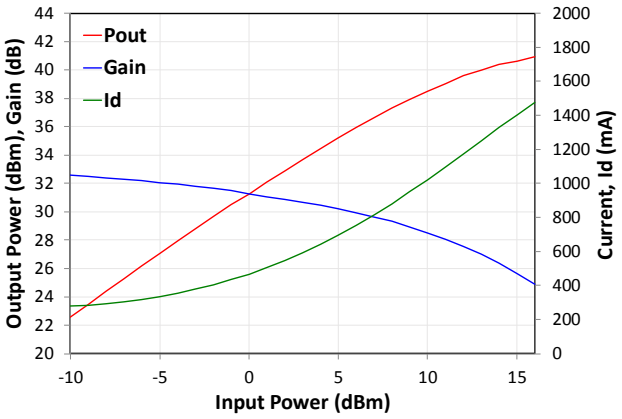
Pout, Gain, Id vs. Pin @ 18.5 GHz



Psat vs. Vd vs. Frequency



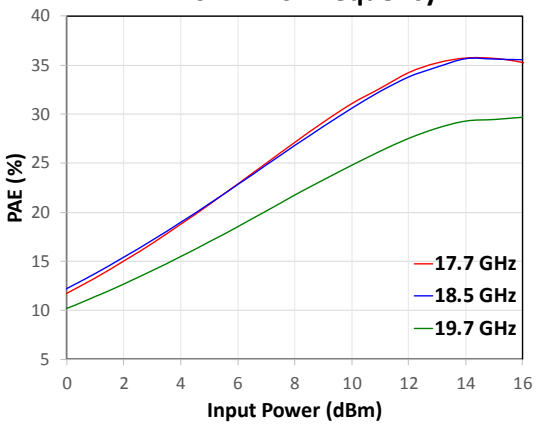
Pout, Gain, Id vs. Pin @ 19.7 GHz



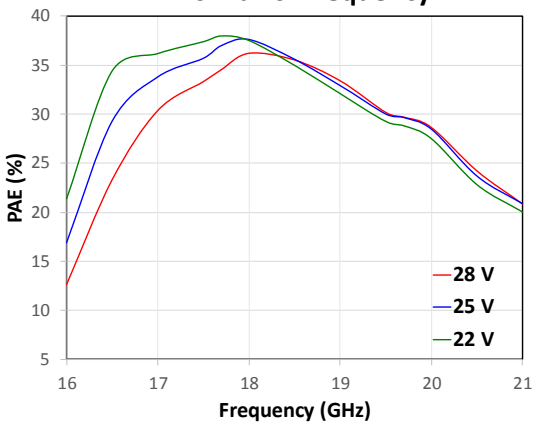
Performance Plots

Test conditions unless otherwise noted: VD1=VD2=VD3=28V, ID1+ID2+ID3=300mA, VG1=VG2=VG3=-2.6V typical, Temp = +25 °C, Z_0 = 50 Ω

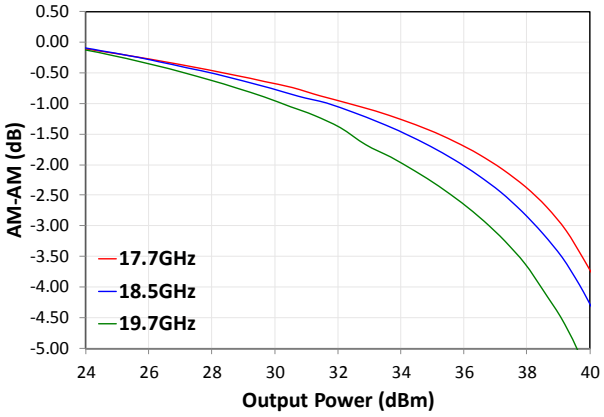
PAE vs. Pin vs. Frequency



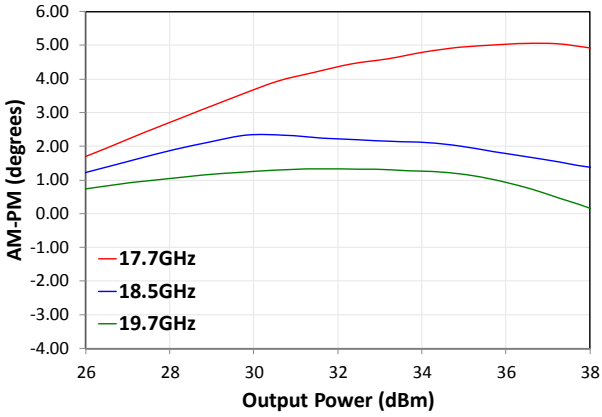
PAE vs. Vd vs. Frequency



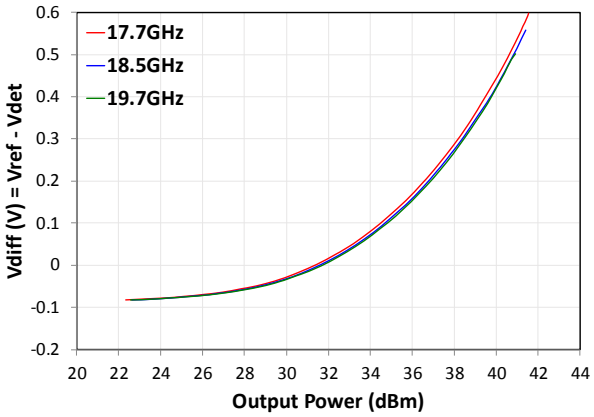
AM-AM vs. Pout vs. Frequency



AM-PM vs. Pout vs. Frequency



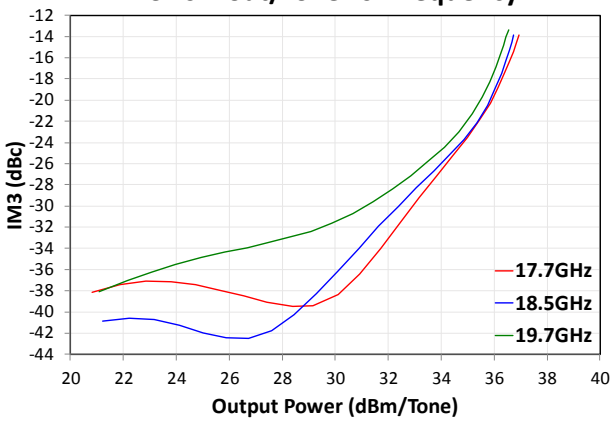
Power Detector vs. Pout vs. Frequency



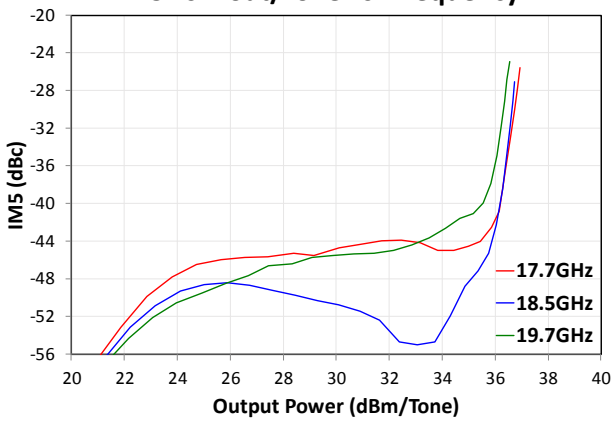
Performance Plots

Test conditions unless otherwise noted: VD1=VD2=VD3=28V, ID1+ID2+ID3=300mA, VG1=VG2=VG3=-2.6V typical, Temp = +25 °C, Z_0 = 50 Ω

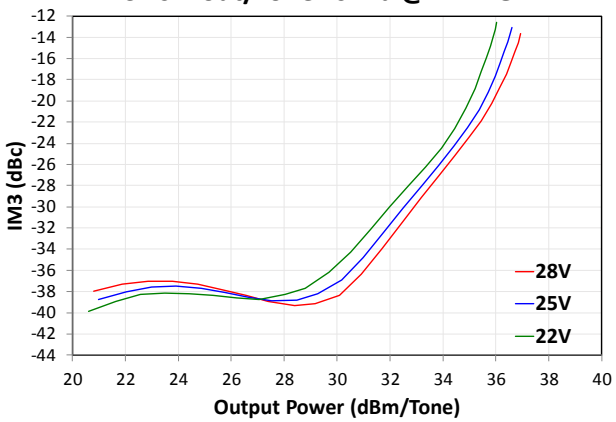
IM3 vs. Pout/Tone vs. Frequency



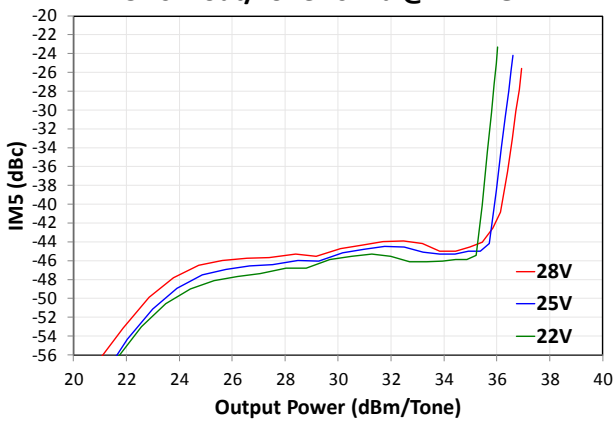
IM5 vs. Pout/Tone vs. Frequency



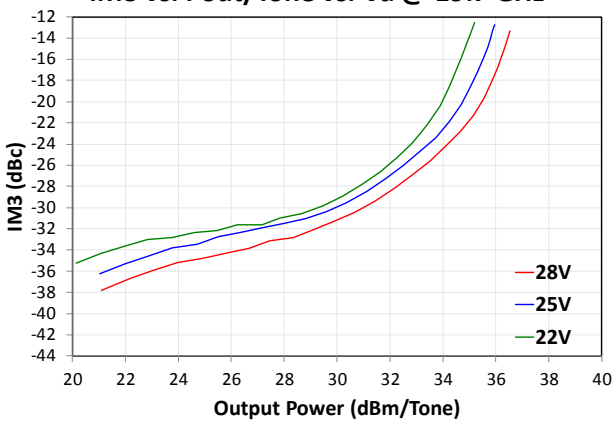
IM3 vs. Pout/Tone vs. Vd @ 17.7 GHz



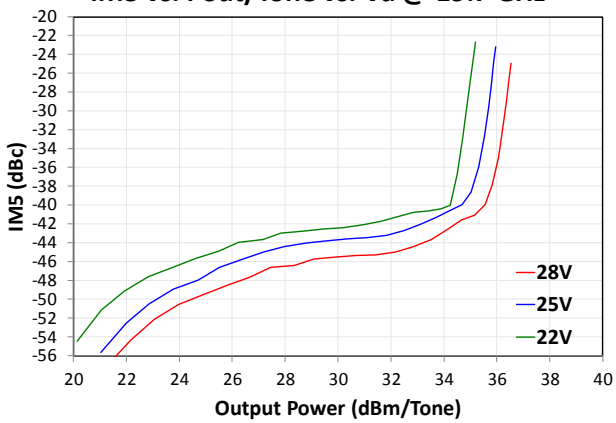
IM5 vs. Pout/Tone vs. Vd @ 17.7 GHz



IM3 vs. Pout/Tone vs. Vd @ 19.7 GHz



IM5 vs. Pout/Tone vs. Vd @ 19.7 GHz



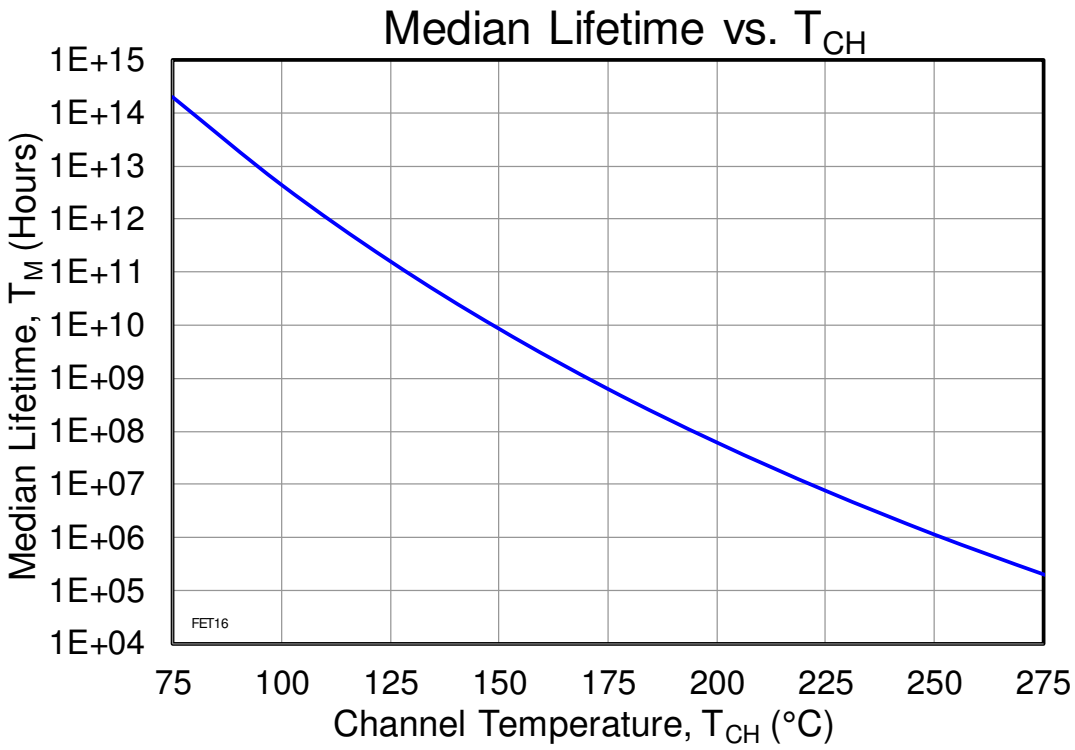
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	CW $T_{baseplate}$ = +85 °C, V_D = +28 V, I_D = 300 mA, P_{DISS} = 8.4 W	3.57	ºC/W
Channel Temperature, T_{CH} (I_{DQ})		115	°C
Median Lifetime (T_M)		5.7×10^{11}	Hrs
Thermal Resistance (θ_{JC}) (1)	CW $T_{baseplate}$ = +85 °C, V_D = +28 V, I_D = 1050 mA, P_{OUT} = 40 dBm, P_{DISS} = 19.4 W	3.61	ºC/W
Channel Temperature, T_{CH} (Under RF)		155	°C
Median Lifetime (T_M)		4.9×10^{9}	Hrs

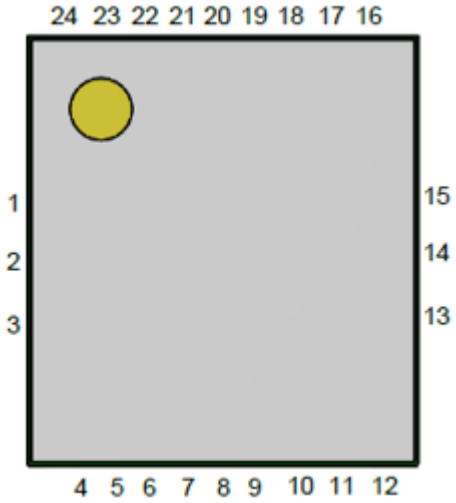
Notes:
1. Channel operating temperature will directly affect the device median lifetime (Tm). For maximum life, it is recommended that the channel temperatures be maintained at the lowest possible levels.

Median Lifetime

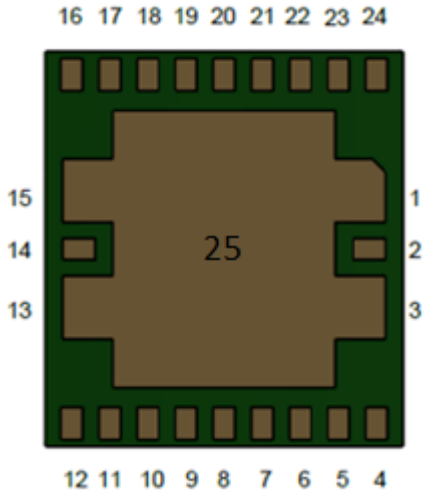
Test Conditions: V_D = +28 V; Failure Criteria is 10% reduction in I_{D_MAX}



Pad Configuration and Description



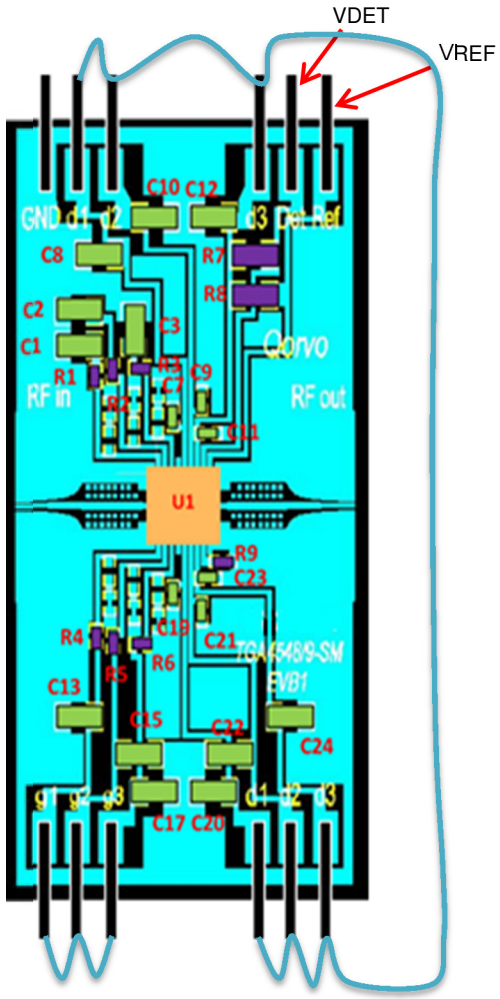
Top View



Bottom View

Pad No.	Label	Description
1, 3, 7, 13, 15, 21	GND	Ground. May be grounded on PCB.
2	RFIN	RF input, matched to 50Ω, AC coupled.
4, 24	VG1	Gate voltage. Bias network is required; can be biased from either pin, and non-biased pin can be left open; see Application Circuit on page 4 as an example.
5, 23	VG2	Gate voltage. Bias network is required; can be biased from either pin, and non-biased pin can be left open; see Application Circuit on page 4 as an example.
6, 22	VG3	Gate voltage. Bias network is required; can be biased from either pin, and non-biased pin can be left open; see Application Circuit on page 4 as an example.
8, 20	VD1	Drain voltage. Bias network is required; see Application circuit on page 4 as an example.
9, 19	VD2	Drain voltage. Bias network is required; see Application circuit on page 4 as an example.
10, 18	VD3	Drain voltage. Bias network is required; see Application circuit on page 4 as an example.
11, 17	VDET	Detector diode output voltage. Varies with RF output power.
12, 16	VREF	Reference diode output voltage
14	RFOUT	RF output, matched to 50Ω, AC coupled.
25	GND	Backside paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see Mounting Configuration on page 11 for suggested footprint.

Application Evaluation Board – TGA4548-SM

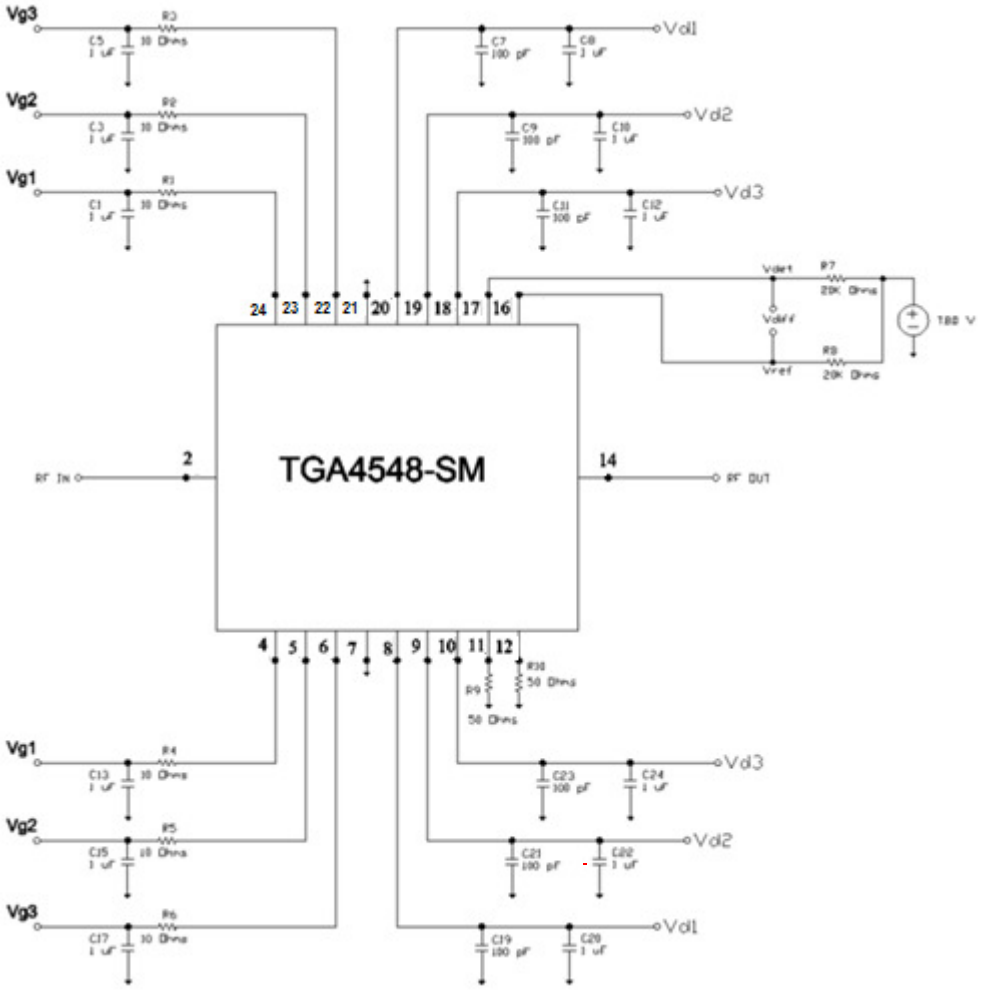


Notes:
1. Board Material is RO4003 0.008" thickness with ½ oz. copper cladding

Bill of Material – TGA4548-SM Evaluation board

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	17.7 – 19.7 GHz Power Amplifier	Qorvo	TGA4548-SM
C7, C9, C11, C19, C21, C23	100pF	Cap, 0402, 50 V, 5%, COG	various	
C1, C3, C5, C13, C15, C17	1uF	Cap, 0805, 50 V, 5%, X5R	various	
R1-R6	10Ω	Resistor, 0402, 5%, 1/16W, SMD	various	
R7, R8	20kΩ	Resistor, 0805, 5%, SMD	various	
R9	50Ω	Resistor, 0402, 5%, 1/16W, SMD	various	

Application Circuit



Notes:

1. VG1, VG2, and VG3 can be biased from either side, and the non-biased side can be left open. VD1, VD2, and VD3 must be biased from both sides.

Bias Up Procedure

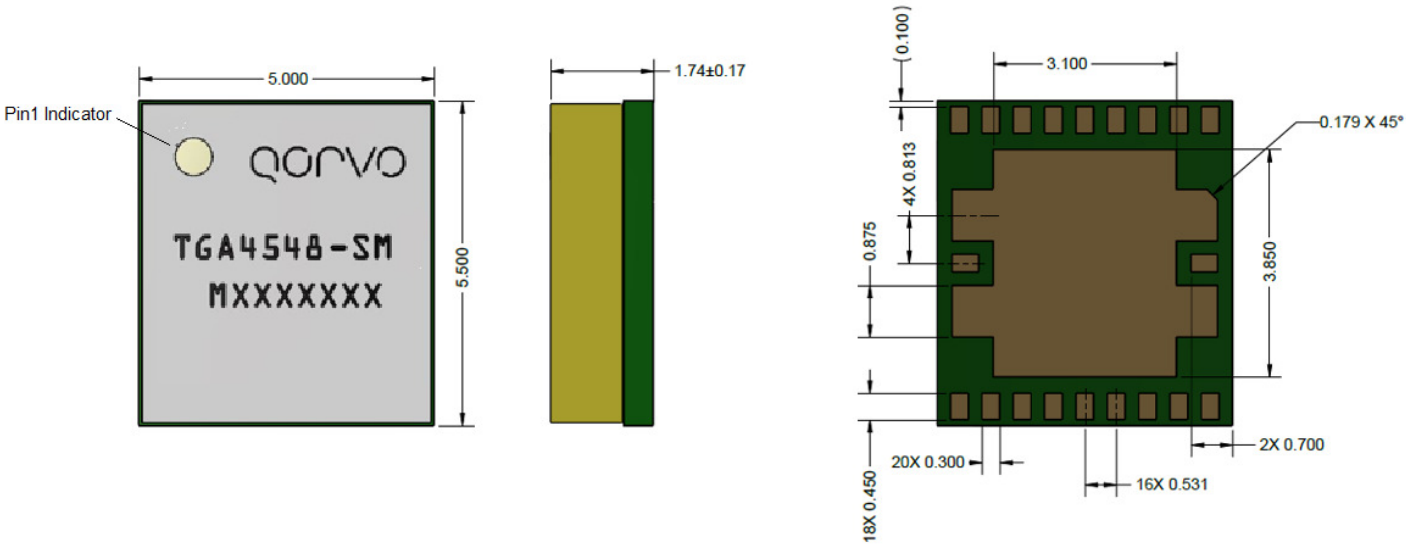
1. Set I_D limit to 3000 mA, I_G limit to 20 mA
2. Apply –5 V to V_G
3. Apply +28 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 300 mA (V_G ~ –2.3 V Typ.).
5. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to –5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

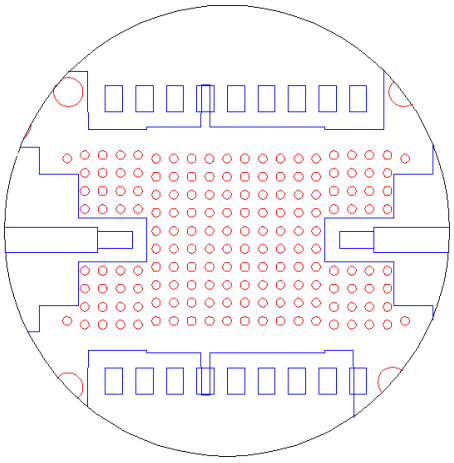
Package Marking and Dimensions

Marking: Part Number – TGA4548X-SM
Vendor and Lot Code – MXXXXXXX; "M" is the vendor code, XXXXXXX represents assembly lot number.



Notes:
This package is lead-free/RoHS-compliant with an embedded heat spreader, and the plating material on the leads is NiAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and tin-lead (maximum 245 °C reflow temperature) soldering processes.

PCB Mounting Pattern



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Ground vias are critical for the proper performance of this device. Vias should have a final plated thru diameter of .1524 mm (.006").
3. For best thermal performance, vias under the ground paddle should be copper filled.
4. The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	0B	ESDA / JEDEC JS-001-2012

Caution!
ESD-Sensitive Device

Solderability

Compatible with lead-free (260℃ max. reflow temp.) soldering process.
Solder profiles available upon request. Use of no-clean solder to avoid washing after soldering is recommended.

Contact plating: NiAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Important Notice

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