Blackfin® Embedded Processor

Preliminary Technical Data

ADSP-BF522C/ADSP-BF525C/ADSP-BF527C

FEATURES

Up to 600 MHz high-performance Blackfin processor
- **Two 16-bit MACs, two 40-bit ALUs, four 8-bit video ALUs, 40-bit shifter**
- **RISC-like register and instruction model for ease of programming and compiler-friendly support**
- **Advanced debug, trace, and performance monitoring**

tbd V to tbd V core V_{DD} with on-chip voltage regulation
1.8V, 2.5V, or 3.3V I/O operation
Embedded low power audio CODEC
289-ball MBGA package

MEMORY

132K bytes of on-chip memory:
- **48K bytes of instruction SRAM**
- **16K bytes of instruction SRAM/cache**
- **32K bytes of data SRAM**
- **32K bytes of data SRAM/cache**
- **4K bytes of scratchpad SRAM**

External memory controller with glueless support for SDRAM and asynchronous 8-bit and 16-bit memories
Nand flash controller
Flexible booting options from external flash, SPI and TWI memory or from SPI, TWI, and UART host devices
One-time programmable memory for security
Two dual-channel memory DMA controllers
Memory management unit providing memory protection

PERIPHERALS

Refer to the published ADSP-BF522/ADSP-BF525/ADSP-BF527 Revision PrB datasheet for additional peripherals

CODEC FEATURES

Stereo 24-bit A/D and D/A converters
DAC
- **100 dB (A-weighted) signal-to-noise ratio at 3.3 V**
- **95 dB (A-weighted) signal-to-noise ratio at 1.8 V**

ADC
- **90 dB (A-weighted) signal-to-noise ratio at 3.3 V**
- **85dB (A-weighted) signal-to-noise ratio at 1.8 V**

Audio sample rates
- **8 kHz, 44.1 kHz or 88.2 kHz–XTI/MCLK frequency 11.2896 MHz (256 × F_S) or 16.9344 MHz (384 × F_S)**
- **8 kHz, 32 kHz, 48 kHz or 96 kHz–XTI/MCLK frequency 12.288 MHz (256 × F_S) or 18.432 MHz (384 × F_S)**

Highly efficient headphone amplifier
Complete stereo/mono or microphone/line interface
Normal and USB modes programmed under software control
Low power
- **8 mW stereo playback (1.8 V all power supplies)**
- **20 mW record and playback (1.8 V all power supplies))**

Low supply voltages
- **1.8 V to 3.6 V analog supply range**
- **1.8 V to 3.6 V digital supply range**

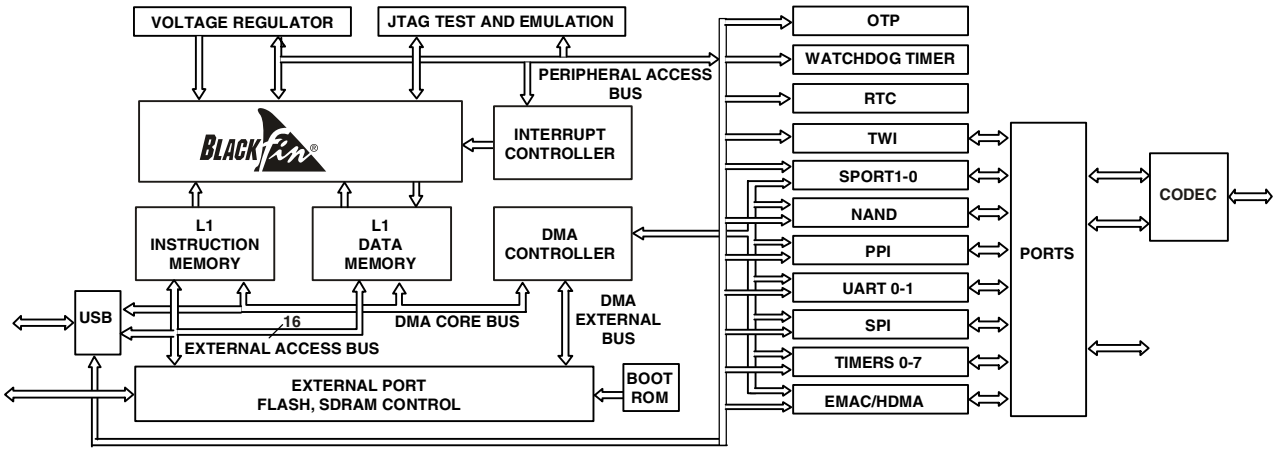

Figure 1. Functional Block Diagram

Rev. PrB

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REVISION HISTORY

6/07—Revision PrB: Changes from PrA to PrB

Corrects SS/PG and VRSEL 289-Ball Mini-BGA Ball Assignment (Alphabetically by Signal) 7

Corrects SS/PG and VRSEL 289-Ball Mini-BGA Ball Assignment (Numerically by Ball Number) 8

3/07—Revision PrA: Initial Version

GENERAL DESCRIPTION

This document describes the differences between the ADSP-BF522C/ADSP-BF525C/ADSP-BF527C and the ADSP-BF522/ADSP-BF525/ADSP-BF527 standard product. Please refer to the published ADSP-BF522/ADSP-BF525/ADSP-BF527 Revision PrC datasheet for general description and specifications. This document only describes the exceptions to that datasheet.

The ADSP-BF522C/ADSP-BF525C/ADSP-BF527C adds a stereo CODEC to the standard product and changes the package labeling.

STEREO CODEC

The CODEC in the ADSP-BF522C/ADSP-BF525C/ADSP-BF527C is a low power, high quality stereo audio CODEC for portable digital audio application. It features two 24-bit A/D converter channels and two 24-bit D/A converter channels.

In normal mode, the XMI/MCLK oscillator is set up according to the desired sample rates of the ADC and DAC. For ADC or DAC sampling rates of 8 kHz, 32 kHz, 48 kHz or 96 kHz, MCLK frequencies of either 12.288 MHz (256 × FS) or 18.432 MHz (384 × FS) can be used. For ADC or DAC sampling rates of 8 kHz, 44.1 kHz or 88.2 kHz, MCLK frequencies of either 11.2896 MHz (256 × FS) or 16.9344 MHz (384 × FS) can be used.

In USB mode, the XTI/MCLK frequency is only 12MHz allowing for ADC and DAC sampling rates of 8 kHz, 44.1 kHz or 88.2 kHz.

The CODEC can operate with power supplies as low as 1.8 V for the analog part and 1.8 V for digital port. The maximum voltage is 3.6 V for all power supplies.

The device is controlled by a 2- or 3-wire serial interface which provides access to all features including volume controls, mutes and extensive power management facilities.

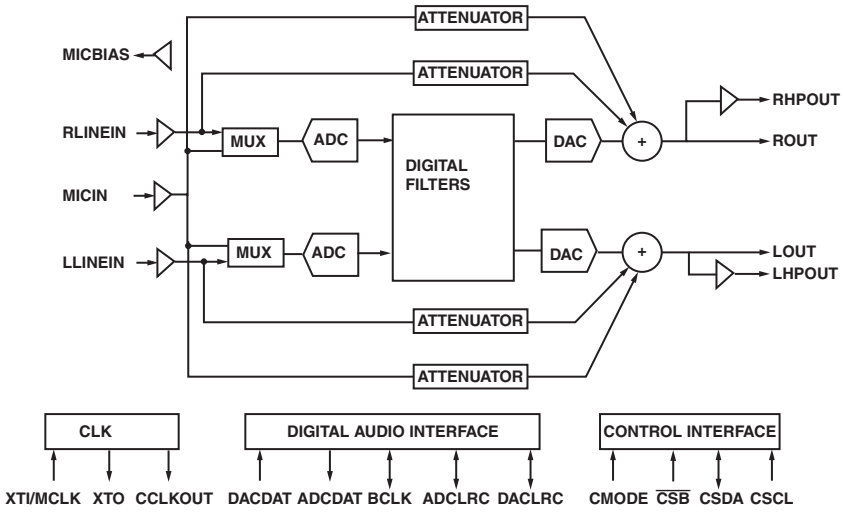

Figure 2. Audio CODEC Block Diagram

PIN DESCRIPTIONS

The ADSP-BF522C/ADSP-BF525C/ADSP-BF527C processor adds CODEC signals as listed in Table 1.

Table 1. Pin Descriptions

Pin Name	Type	Function	Pull-Up/Down
CCLKOUT	O	CODEC Clock Output	None
BCLK	I/O	CODEC Digital Audio Bit Clock	Internal Pull-down[1]
DACDAT	I	CODEC DAC Sample Rate Left/Right Clock	None
DACLRC	I/O	CODEC I/O DAC Sample Rate Left/Right Clock	Internal Pull-down[1]
ADCDAT	O	CODEC ADC Digital Audio Data Output	None
ADCLRC	I/O	CODEC ADC Sample Rate Left/Right Clock	Internal Pull-down[1]
CMODE	I	CODEC Control Interface Selection	Internal Pull-up[1]
$\overline{CSB}$	I	CODEC MPU Chip Select/MPU Interface Address Selection	Internal Pull-up[1]
CSDA	I/O	CODEC MPU Data Input	None
CSCL	I	CODEC MPU Clock	None
XTI/MCLK	I	CODEC Crystal Input/MPU Clock Input	None
XTO	O	CODEC Crystal Output	None
LHPOUT	O	CODEC Left Channel Headphone Output (Analog Output)	None
RHPOUT	O	CODEC Right Channel Headphone Output (Analog Output)	None
LOUT	O	CODEC Left Channel Line Output (Analog Output)	None
ROUT	O	CODEC Right Channel Line Output (Analog Output)	None
VMID	O	CODEC Mid-rail Reference Decoupling Point (Analog Output)	None
MICBIAS	O	CODEC Electret Microphone Bias (Analog Output)	None
MICIN	I	CODEC Microphone Input; (Analog Input, AC Coupled)	None
RLINEIN	I	CODEC Right Channel Line Input (Analog Input, AC Coupled)	None
LLINEIN	I	CODEC Left Channel Line Input (Analog Input, AC Coupled)	None
GND	P	CODEC Digital Core Ground	N/A
AVDD	P	CODEC Analog V_{DD}	N/A
AGND	P	CODEC Analog Ground	N/A
HPVDD	P	CODEC Headphone V_{DD} (Analog)	N/A
HPGND	P	CODEC Headphone Ground	N/A

[1] Pull-up/pull-down is only present when the control register interface ACTIVE = 0 to conserve power.

SPECIFICATIONS

Component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Typical	Max	Unit
CV_{DD}	Digital Core V_{DD}		1.8		3.6	V
AV_{DD}	Analog V_{DD}		1.8		3.6	V
HPV_{DD}	Headphone V_{DD} (Analog)		1.8		3.6	V
V_{ILC}	CODEC Low Level Input Voltage[1]				$0.3 \times CV_{DD}$	V
V_{IHC}	CODEC High Level Input Voltage[1]		$0.7 \times CV_{DD}$			V
V_{OLC}	CODEC Low Level Output Voltage[1]				$0.1 \times CV_{DD}$	V
V_{OHC}	CODEC Low Level Output Voltage[1]		$0.9 \times CV_{DD}$			V
T_J	Junction Temperature	289-Ball Chip Scale Ball Grid Array (Mini-BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+105	°C

[1] Parameter value applies to digital signal pins (ADCDAT, ADCLRC, BCLK, $\overline{CSB}$, CCLKOUT, CMODE, DACDAT, DACLRC, CSCL, CSDA, XTI/MCLK, XTO).

ELECTRICAL CHARACTERISTICS

Parameter		Conditions	Min	Typical	Max	Unit
Line Input to ADC						
SNR	Signal to Noise Ratio	A-weighted, 0 dB Gain @ F_S = 48 kHz	tbd	85		dB
SNR	Signal to Noise Ratio	A-weighted, 0 dB Gain @ F_S = 96 kHz		85		dB
DR	Dynamic Range	A-weighted, –60 dB Full Scale Input	tbd	88		dB
THD	Total Harmonic Distortion	–1 dB Input, 0 dB Gain		–76	tbd	dB
Microphone Input to ADC		0 dB Gain, F_S = 48 kHz, 40 kΩ Source Impedance				
SNR	Signal to Noise Ratio	A-weighted, 0 dB Gain		80		dB
DR	Dynamic Range	A-weighted, –60 dB Full Scale Input		70		dB
THD	Total Harmonic Distortion	0 dB Input, 0 dB Gain		–55		dB
Line Output for DAC Playback Only		Load = 10 kΩ, 50 pF				
SNR	Signal to Noise Ratio	A-weighted, 0 dB Gain @ F_S = 48 kHz	tbd	95		dB
SNR	Signal to Noise Ratio	A-weighted, 0 dB Gain @ F_S = 96 kHz		93		dB
DR	Dynamic Range	A-weighted, –60 dB Full Scale Input	tbd	90		dB
THD	Total Harmonic Distortion	1 kHz, 0 dB		–80	tbd	dB
THD	Total Harmonic Distortion	1 kHz, –3 dB		–90		dB
Analog Line Input to Line Output		Load = 10 k Ω, 50 pF, No Gain on Input, Bypass Mode				
SNR	Signal to Noise Ratio		tbd	90		dB
THD	Total Harmonic Distortion	1 kHz, 0 dB		–83	tbd	dB
THD	Total Harmonic Distortion	1 kHz, –3 dB		–92		dB
Stereo Headphone Output						
PO	Maximum Output Power	R_L = 32 Ω		9		mW
PO	Maximum Output Power	R_L = 16 Ω		18		mW
SNR	Signal to Noise Ratio	A-weighted	tbd	95		dB
THD	Total Harmonic Distortion	1 kHz, –5 dB, R_L = 32 Ω, Full Scale Input		–62	tbd	dB
THD	Total Harmonic Distortion	1 kHz,–2 dB, R_L = 32 Ω, Full Scale Input			tbd	dB
Microphone Input to Headphone Output Side Tone Mode						
SNR	Signal to Noise Ratio		tbd	90		dB

DIGITAL FILTER CHARACTERISTICS

Parameter	Conditions	Min	Typical	Max	Unit
ADC Filter					
Passband	±0.05 dB	tbd × F_S		tbd × F_S	
Passband	–6 dB		0.5 × F_S		
Passband Ripple				tbd	dB
Stopband		tbd × F_S			
Stopband Attenuation	F > 0.5465 × F_S	tbd			dB
High Pass Filter Corner Frequency	–3 dB		3.7		Hz
High Pass Filter Corner Frequency	–0.5 dB		10.4		Hz
High Pass Filter Corner Frequency	–0.1 dB		21.6		Hz
DAC Filter					
Passband	±0.03 dB	tbd × F_S		tbd × F_S	
Passband	–6 dB		0.5 × F_S		
Passband Ripple				tbd	dB
Stopband		tbd × F_S			
Stopband Attenuation	F > 0.5465 × F_S	tbd			dB

PACKAGE INFORMATION

The information presented in Figure 3 and Table 2 provides details about the package branding for the ADSP-BF522C/ADSP-BF525C/ADSP-BF527C processor. For a complete listing of product availability, see Ordering Guide on Page 12.

Figure 3. Product Information on Package

Table 2. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	Lead Free Option
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

289-BALL MINI-BGA PINOUT

Table 3 lists the mini-BGA pinout by signal mnemonic. Table 4 on Page 8 lists the mini-BGA pinout by ball number.

Table 3. 289-Ball Mini-BGA Ball Assignment (Alphabetically by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
ABE0/SDQM0	AB9	CSB	D23	GND	L14	PF5	B10	RESET	V22	VDDEXT	R17	VDDMEM	U8
ABE1/SDQM1	AC9	CSCL	B23	GND	L15	PF6	B12	RHPOUT	B21	VDDEXT	T17	VDDMEM	U9
ADCDAT	A16	CSDA	C23	GND	M9	PF7	B13	RLINEIN	F23	VDDEXT	U17	VDDMEM	U10
ADCLRC	A15	DACDAT	A18	GND	M10	PF8	B16	ROUT	G22	VDDINT	B5	VDDMEM	U11
ADDR1	AB8	DACLRC	A17	GND	M11	PF9	A20	RTXI	U23	VDDINT	H8	VDDMEM	U12
ADDR2	AC8	DATA0	Y1	GND	M12	PF10	B15	RTXO	V23	VDDINT	H9	VDDMEM	U13
ADDR3	AB7	DATA1	V2	GND	M13	PF11	B17	SA10	AC10	VDDINT	H10	VDDMEM	U14
ADDR4	AC7	DATA2	W1	GND	M14	PF12	B18	SCAS	AC11	VDDINT	H11	VDDMEM	U15
ADDR5	AC6	DATA3	U2	GND	M15	PF13	B19	SCKE	AB13	VDDINT	H12	VDDMEM	U16
ADDR6	AB6	DATA4	V1	GND	N9	PF14	A9	SCL	B22	VDDINT	H13	VDDOTP	AC12
ADDR7	AB4	DATA5	U1	GND	N10	PF15	A10	SDA	C22	VDDINT	H14	VDDRTC	W23
ADDR8	AB5	DATA6	T2	GND	N11	PG0	H2	SMS	AC13	VDDINT	H15	VDDUSB	W22
ADDR9	AC5	DATA7	T1	GND	N12	PG1	G1	SRAS	AB12	VDDINT	H16	VDDUSB	Y23
ADDR10	AC4	DATA8	R1	GND	N13	PG2	H1	SS/PG	AC20	VDDINT	J8	VMID	G23
ADDR11	AB3	DATA9	P1	GND	N14	PG3	F1	SWE	AB10	VDDINT	J16	VROUT	AC18
ADDR12	AC3	DATA10	P2	GND	N15	PG4	D1	TCK	L1	VDDINT	K8	VRSEL	AB22
ADDR13	AB2	DATA11	R2	GND	P9	PG5	D2	TDI	J1	VDDINT	K16	XTAL	P23
ADDR14	AC2	DATA12	N1	GND	P10	PG6	C2	TDO	K1	VDDINT	L8	XTI/MCLK	A22
ADDR15	AA2	DATA13	N2	GND	P11	PG7	B1	TMS	L2	VDDINT	L16	XTO	A21
ADDR16	W2	DATA14	M2	GND	P12	PG8	C1	TRST	K2	VDDINT	M8		
ADDR17	Y2	DATA15	M1	GND	P13	PG9	B2	USB_DM	AB21	VDDINT	M16		
ADDR18	AA1	EMU	J2	GND	P14	PG10	B4	USB_DP	AA22	VDDINT	N8		
ADDR19	AB1	EXT_WAKE	AC19	GND	P15	PG11	B3	USB_ID	Y22	VDDINT	N16		
AGND	G17	GND	A1	GND	R9	PG12	A2	USB_RSET	AC21	VDDINT	P8		
AGND	H22	GND	A23	GND	R10	PG13	A3	USB_VBUS	AB20	VDDINT	P16		
AMS0	AC17	GND	B6	GND	R11	PG14	A4	USB_VREF	AC22	VDDINT	R8		
AMS1	AB16	GND	J9	GND	R12	PG15	A5	USB_XTALIN	AB23	VDDINT	R16		
AMS2	AC16	GND	J10	GND	R13	PH0	A11	USB_XTALOUT	AA23	VDDINT	T8		
AMS3	AB15	GND	J11	GND	R14	PH1	A12	VDDEXT	G7	VDDINT	T9		
AOE	AC15	GND	J12	GND	R15	PH2	A13	VDDEXT	G8	VDDINT	T10		
ARDY	AC14	GND	J13	GND	T22	PH3	B14	VDDEXT	G9	VDDINT	T11		
ARE	AB17	GND	J14	GND	AC1	PH4	A14	VDDEXT	G10	VDDINT	T12		
AVDD	G16	GND	J15	GND	AC23	PH5	K23	VDDEXT	G11	VDDINT	T13		
AVDD	J22	GND	K9	LHPOUT	B20	PH6	K22	VDDEXT	G12	VDDINT	T14		
AWE	AB14	GND	K10	LLINEIN	E23	PH7	L23	VDDEXT	G13	VDDINT	T15		
BCLK	A19	GND	K11	LOUT	F22	PH8	L22	VDDEXT	G14	VDDINT	T16		
BMODE0	G2	GND	K12	MICBIAS	H23	PH9	T23	VDDEXT	G15	VDDMEM	J7		
BMODE1	F2	GND	K13	MICIN	J23	PH10	M22	VDDEXT	H7	VDDMEM	K7		
BMODE2	E1	GND	K14	NMI	U22	PH11	R22	VDDEXT	H17	VDDMEM	L7		
BMODE3	E2	GND	K15	OTPVPP	AB11	PH12	M23	VDDEXT	J17	VDDMEM	M7		
CCLKOUT	D22	GND	L9	PF0	A7	PH13	N22	VDDEXT	K17	VDDMEM	N7		
CLKBUF	AB19	GND	L10	PF1	B8	PH14	N23	VDDEXT	L17	VDDMEM	P7		
CLKIN	R23	GND	L11	PF2	A8	PH15	P22	VDDEXT	M17	VDDMEM	R7		
CLKOUT	AB18	GND	L12	PF3	B9	PPICLK/TMRCLK	A6	VDDEXT	N17	VDDMEM	T7		
CMODE	E22	GND	L13	PF4	B11	PPIFS1/TMR0	B7	VDDEXT	P17	VDDMEM	U7		

Table 4. 289-Ball Mini-BGA Ball Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	GND	B23	CSCL	H22	AGND	L22	PH8	P22	PH15	U22	NMI	AC5	ADDR9
A2	PG12	C1	PG8	H23	MICBIAS	L23	PH7	P23	XTAL	U23	RTXI	AC6	ADDR5
A3	PG13	C2	PG6	J1	TDI	M1	DATA15	R1	DATA8	V1	DATA4	AC7	ADDR4
A4	PG14	C22	SDA	J2	EMU	M2	DATA14	R2	DATA11	V2	DATA1	AC8	ADDR2
A5	PG15	C23	CSDA	J7	VDDMEM	M7	VDDMEM	R7	VDDMEM	V22	RESET	AC9	ABE1/SDQM1
A6	PPICLK/TMRCLK	D1	PG4	J8	VDDINT	M8	VDDINT	R8	VDDINT	V23	RTXO	AC10	SA10
A7	PF0	D2	PG5	J9	GND	M9	GND	R9	GND	W1	DATA2	AC11	SCAS
A8	PF2	D22	CCLKOUT	J10	GND	M10	GND	R10	GND	W2	ADDR16	AC12	VDDOTP
A9	PF14	D23	$\overline{CSB}$	J11	GND	M11	GND	R11	GND	W22	VDDUSB	AC13	SMS
A10	PF15	E1	BMODE2	J12	GND	M12	GND	R12	GND	W23	VDDRTC	AC14	ARDY
A11	PH0	E2	BMODE3	J13	GND	M13	GND	R13	GND	Y1	DATA0	AC15	AOE
A12	PH1	E22	CMODE	J14	GND	M14	GND	R14	GND	Y2	ADDR17	AC16	AMS2
A13	PH2	E23	LLINEIN	J15	GND	M15	GND	R15	GND	Y22	USB_ID	AC17	AMS0
A14	PH4	F1	PG3	J16	VDDINT	M16	VDDINT	R16	VDDINT	Y23	VDDUSB	AC18	VROUT
A15	ADCLRC	F2	BMODE1	J17	VDDEXT	M17	VDDEXT	R17	VDDEXT	AA1	ADDR18	AC19	EXT_WAKE
A16	ADCDAT	F22	LOUT	J22	AVDD	M22	PH10	R22	PH11	AA2	ADDR15	AC20	SS/PG
A17	DACLRC	F23	RLINEIN	J23	MICIN	M23	PH12	R23	CLKIN	AA22	USB_DP	AC21	USB_RSET
A18	DACDAT	G1	PG1	K1	TDO	N1	DATA12	T1	DATA7	AA23	USB_XTALOUT	AC22	USB_VREF
A19	BCLK	G2	BMODE0	K2	TRST	N2	DATA13	T2	DATA6	AB1	ADDR19	AC23	GND
A20	PF9	G7	VDDEXT	K7	VDDMEM	N7	VDDMEM	T7	VDDMEM	AB2	ADDR13		
A21	XTO	G8	VDDEXT	K8	VDDINT	N8	VDDINT	T8	VDDINT	AB3	ADDR11		
A22	XTI/MCLK	G9	VDDEXT	K9	GND	N9	GND	T9	VDDINT	AB4	ADDR7		
A23	GND	G10	VDDEXT	K10	GND	N10	GND	T10	VDDINT	AB5	ADDR8		
B1	PG7	G11	VDDEXT	K11	GND	N11	GND	T11	VDDINT	AB6	ADDR6		
B2	PG9	G12	VDDEXT	K12	GND	N12	GND	T12	VDDINT	AB7	ADDR3		
B3	PG11	G13	VDDEXT	K13	GND	N13	GND	T13	VDDINT	AB8	ADDR1		
B4	PG10	G14	VDDEXT	K14	GND	N14	GND	T14	VDDINT	AB9	ABE0/SDQM0		
B5	VDDINT	G15	VDDEXT	K15	GND	N15	GND	T15	VDDINT	AB10	SWE		
B6	GND	G16	AVDD	K16	VDDINT	N16	VDDINT	T16	VDDINT	AB11	OTPVPP		
B7	PPIFS1/TMR0	G17	AGND	K17	VDDEXT	N17	VDDEXT	T17	VDDEXT	AB12	SRAS		
B8	PF1	G22	ROUT	K22	PH6	N22	PH13	T22	GND	AB13	SCKE		
B9	PF3	G23	VMID	K23	PH5	N23	PH14	T23	PH9	AB14	AWE		
B10	PF5	H1	PG2	L1	TCK	P1	DATA9	U1	DATA5	AB15	AMS3		
B11	PF4	H2	PG0	L2	TMS	P2	DATA10	U2	DATA3	AB16	AMS1		
B12	PF6	H7	VDDEXT	L7	VDDMEM	P7	VDDMEM	U7	VDDMEM	AB17	ARE		
B13	PF7	H8	VDDINT	L8	VDDINT	P8	VDDINT	U8	VDDMEM	AB18	CLKOUT		
B14	PH3	H9	VDDINT	L9	GND	P9	GND	U9	VDDMEM	AB19	CLKBUF		
B15	PF10	H10	VDDINT	L10	GND	P10	GND	U10	VDDMEM	AB20	USB_VBUS		
B16	PF8	H11	VDDINT	L11	GND	P11	GND	U11	VDDMEM	AB21	USB_DM		
B17	PF11	H12	VDDINT	L12	GND	P12	GND	U12	VDDMEM	AB22	VRSEL		
B18	PF12	H13	VDDINT	L13	GND	P13	GND	U13	VDDMEM	AB23	USB_XTALIN		
B19	PF13	H14	VDDINT	L14	GND	P14	GND	U14	VDDMEM	AC1	GND		
B20	LHPOUT	H15	VDDINT	L15	GND	P15	GND	U15	VDDMEM	AC2	ADDR14		
B21	RHPOUT	H16	VDDINT	L16	VDDINT	P16	VDDINT	U16	VDDMEM	AC3	ADDR12		
B22	SCL	H17	VDDEXT	L17	VDDEXT	P17	VDDEXT	U17	VDDEXT	AC4	ADDR10		

Table 5. Thermal Characteristics (BC-289)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	tbd	°C/W
θ_{JMA}	1 linear m/s air flow	tbd	°C/W
θ_{JMA}	2 linear m/s air flow	tbd	°C/W
θ_{JB}		tbd	°C/W
θ_{JC}		tbd	°C/W

Figure 5 shows the top view of the mini-BGA ball configuration. Figure 4 shows the bottom view of the mini-BGA ball configuration.

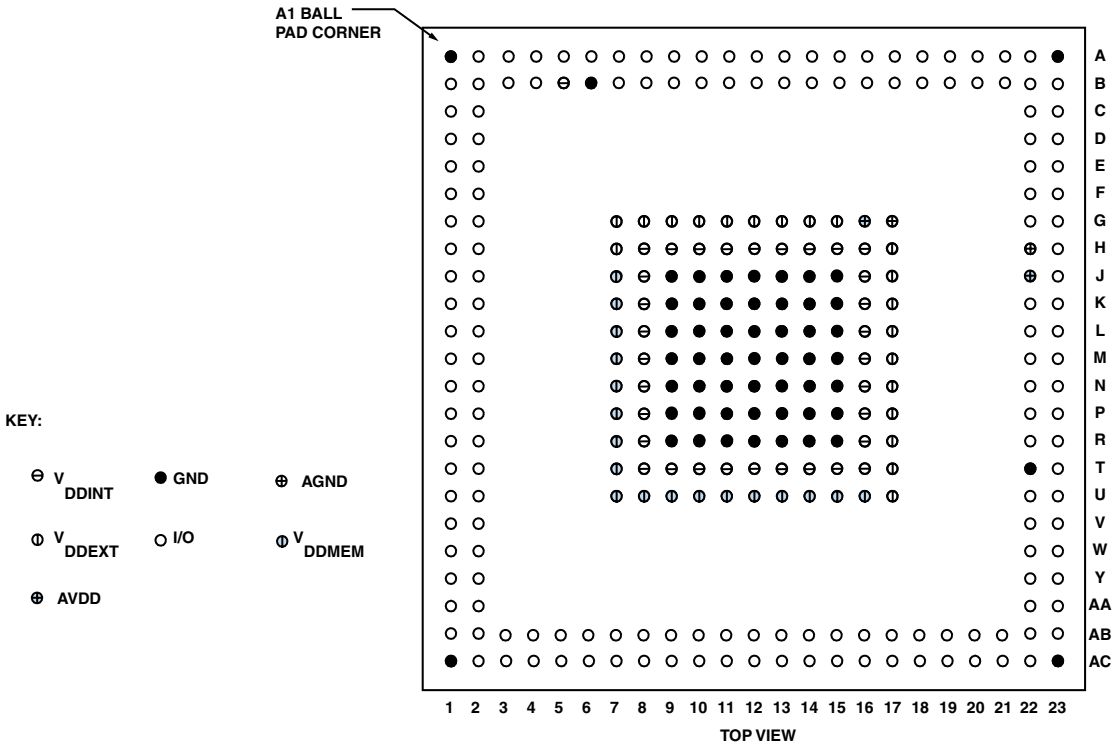

Figure 4. 289-Ball Mini-BGA Ball Configuration (Top View)

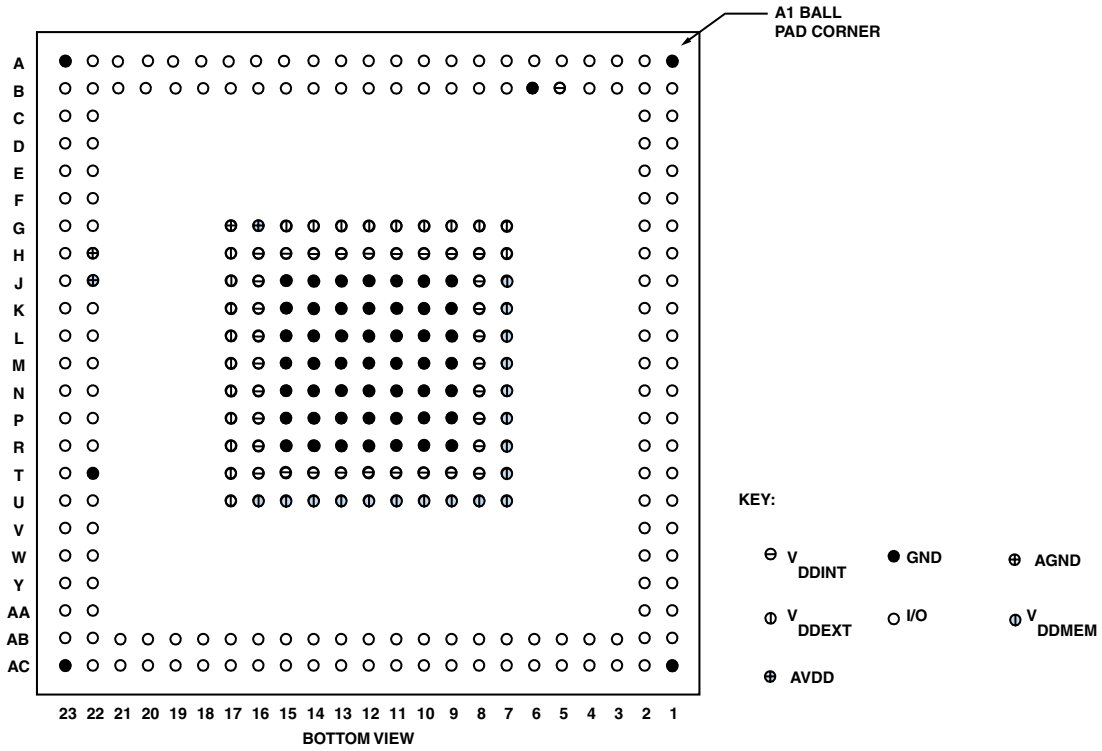

Figure 5. 289-Ball Mini-BGA Ball Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in the outline dimension figures are shown in millimeters.

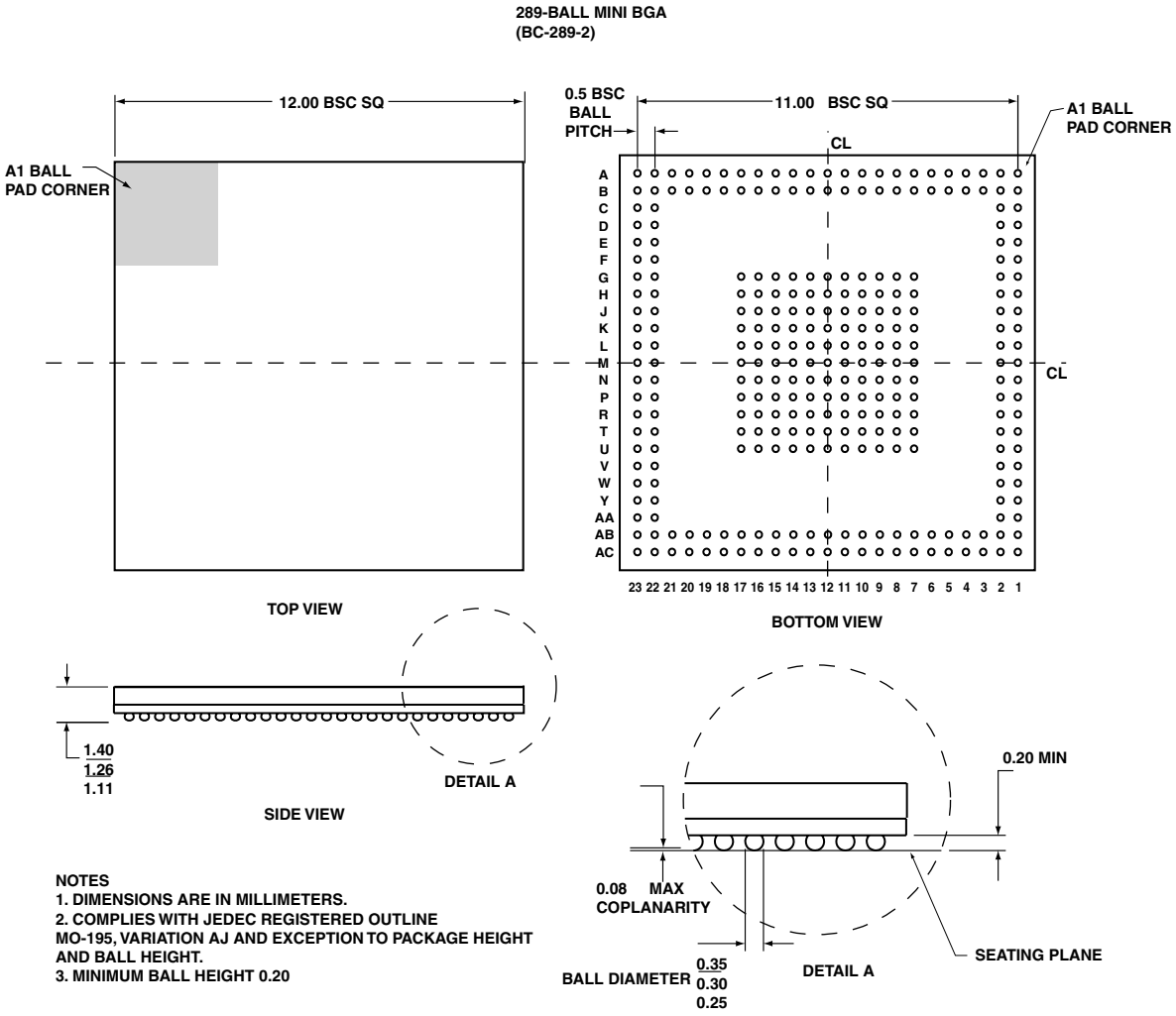

Figure 6. 289-Ball Chip Scale Package Ball Grid Array (Mini-BGA)

SURFACE MOUNT DESIGN

Table 6 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Table 6. BGA Data for Use with Surface Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
289-Ball Chip Scale Package Ball Grid Array (Mini-BGA)	Solder Mask Defined	0.26 mm diameter	0.35 mm diameter

ORDERING GUIDE

Model	Temperature Range[1]	Package Description	Package Option	Instruction Rate (Max)	Operating Voltage (Nom)
ADSPBF527KBCZENGC1	0°C to +70°C	289-Ball Chip Scale Package Ball Grid Array (Mini-BGA)	BC-289	600 MHz	tbd V internal, 1.8 V or 3.3 V I/O

[1] Referenced temperature is ambient temperature.

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