



# W83194AR-We

## 200MHZ CLOCK FOR WHITNEY CHIPSET

### 1.0 GENERAL DESCRIPTION

The W83194AR-We is a Clock Synthesizer for Intel Whitney chipset. W83194AR-We provides all clocks required for high-speed RISC or CISC microprocessor and also provides 64 different frequencies of CPU, SDRAM, PCI, 3V66, IOAPIC clocks frequency setting. All clocks are externally selectable with smooth transitions.

The W83194AR-We provides I<sup>2</sup>C serial bus interface to program the registers to enable or disable each clock outputs and provides 0.5% and 0.75% center type spread spectrum to reduce EMI.

The W83194AR-We accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50± 5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

### 2.0 PRODUCT FEATURES

- 2 CPU clocks
- 9 SDRAM clocks for 2 DIMMs
- 8 PCI synchronous clocks.
- Optional single or mixed supply:  
(VddR = VddP=VddS = Vdd48 = Vdd3 = 3.3V, VddA=VddC=2.5V)
- Skew form CPU to PCI clock -1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.8 to 200MHz
- I<sup>2</sup>C 2-Wire serial interface and I<sup>2</sup>C read back
- 0.5% and 0.75% center type spread spectrum
- Programmable registers to enable/stop each output and select modes  
(mode as Tri-state or Normal )
- Two 48 MHz pins for USB
- 24 MHz for super I/O
- 48-pin SSOP package

## 3.0 PIN CONFIGURATION

REFX2/*FS3	1	48	VddLAPIC
VddR	2	47	IOAPIC
Xin	3	46	VddLCPU
Xout	4	45	CPUCLK0
Vss	5	44	CPUCLK1
Vdd3	6	43	VssC
3V66-0	7	42	VddS
3V66-1	8	41	SDRAM 0
Vss3	9	40	SDRAM 1
PCICLK0/ *FS0	10	39	SDRAM 2
PCICLK1/ FS1#	11	38	VssS
PCICLK2/*FS2	12	37	SDRAM 3
VssP	13	36	SDRAM 4
PCICLK3/ *APIC_SEL	14	35	SDRAM 5
PCICLK4	15	34	VddS
VddP	16	33	SDRAM 6
PCICLK5	17	32	SDRAM 7
PCICLK6	18	31	SDRAM 8
PCICLK7	19	30	VssS
Vss48	20	29	PD#
48MHz_0	21	28	*SDCLK
48MHz_1/ FS4#	22	27	VddA
*SIO_SEL/24_48MHz	23	26	VssA
Vdd48	24	25	*SDATA

**PRELIMINARY****4.0 PIN DESCRIPTION**

IN - Input

OUT - Output

I/O - Bi-directional Pin

# - Active Low

\* - Internal 250kΩ pull-up

**4.1 Crystal I/O**

SYMBOL	PIN	I/O	FUNCTION
Xin	3	IN	Crystal input with internal loading capacitors(36pF) and feedback resistors.
Xout	4	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors(36pF).

**4.2 CPU, SDRAM, PCI, IOAPIC Clock Outputs**

SYMBOL	PIN	I/O	FUNCTION
CPUCLK [0:1]	45,44	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU and Chipset.
PD#	29	IN	Power Down mode when driven low.
IOAPIC	47	OUT	Clock outputs synchronous with PCI clock and powered by VddA.
SDRAM [ 0:8]	41,40, 39,37,36,35,33, 32,31	OUT	SDRAM clock outputs.
PCICLK0/ *FS0	10	I/O	3.3V 33MHz PCI clock during normal operation. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks(Default=1).
PCICLK1/ FS1#	11	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks(Default=0).
PCICLK2/ *FS2	12	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks(Default=1).
PCICLK3/*APIC_SEL	14	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for APIC_SEL at initial power up for H/W selecting the output frequency of IOAPIC clock (Default=1).
PCICLK [ 4:7 ]	15,17,18,19	OUT	Low skew (< 250ps) PCI clock outputs.
3V66 [0:1]	7,8	OUT	3.3V output clocks for the chipset.

**4.3 I<sup>2</sup>C Control Interface**

SYMBOL	PIN	I/O	FUNCTION
*SDATA	25	I/O	Serial data of I <sup>2</sup> C 2-wire control interface with internal pull-up resistor.
*SDCLK	28	IN	Serial clock of I <sup>2</sup> C 2-wire control interface with internal pull-up resistor.

**4.4 Fixed Frequency Outputs**

SYMBOL	PIN	I/O	FUNCTION
REFX2 / *FS3	3	I/O	14.318MHz reference clock. This REF output is the stronger buffer for ISA bus loads. Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks (Default=1).
*SIO_SEL/24_48MHz	23	I/O	24MHz or 48MHz output clock. Latched input for SIO_SEL at initial power up for the output frequency of 24MHz(HIGH) and 48MHz(LOW) clocks.
48MHz_0	21	O	48MHz output for USB during normal operation.
48MHz_1/ FS4#	22	I/O	48MHz / Latched input for FS4 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks (Default=0).

**4.5 Power Pins**

SYMBOL	PIN	FUNCTION
VddL	48	Power supply for CPU & IOAPIC, 2.5V or 3.3V.
Vdd48	24	Power supply for 48MHz output, 3.3V.
Vdd3	6	Power supply for 3V_66 output, 3.3V.
VddP	16	Power supply for PCICLK, 3.3V.
VddR	2	Power supply for REFX2, 3.3V.
VddS	42,34	Power supply for SDRAM[0:8], nominal 3.3V.
VddA	27	Power for I2C CLK and DATA.
Vss	5,9,13,20,26,30,38,43	Circuit Ground.

### 5.0 FREQUENCY SELECTION BY HARDWARE

FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	CPU /SDRAM	3V66 (MHz)	PCI(MHz)	IOAPIC (MHz) APIC_SEL=1	IOAPIC (MHz) APIC_SEL=0
0	0	0	0	0	83.3	124.95	2/3	83.30	41.65	20.83	41.65
0	0	0	0	1	90	90	1	60.00	30.00	15.00	30.00
0	0	0	1	0	75	112.5	2/3	75.00	37.50	18.75	37.50
0	0	0	1	1	72	108	2/3	72.00	36.00	18.00	36.00
0	0	1	0	0	89.07	133.6	2/3	89.07	44.53	22.27	44.53
0	0	1	0	1	95.25	95.25	1	63.50	31.75	15.88	31.75
0	0	1	1	0	121	121	1	80.67	40.33	20.17	40.33
0	0	1	1	1	124	124	1	82.67	41.33	20.67	41.33
0	1	0	0	0	119	119	1	79.33	39.67	19.83	39.67
0	1	0	0	1	114	114	1	76.00	38.00	19.00	38.00
0	1	0	1	0	110	110	1	73.33	36.67	18.33	36.67
0	1	0	1	1	105	105	1	70.00	35.00	17.50	35.00
0	1	1	0	0	66.8	100.2	2/3	66.80	33.40	16.70	33.40
0	1	1	0	1	100.2	100.2	1	66.80	33.40	16.70	33.40
0	1	1	1	0	133.6	133.6	1	66.80	33.40	16.70	33.40
0	1	1	1	1	133.6	100.2	4/3	66.80	33.40	16.70	33.40
1	0	0	0	0	135	101.25	4/3	67.50	33.75	16.88	33.75
1	0	0	0	1	125	125	1	83.33	41.67	20.83	41.67
1	0	0	1	0	127	127	1	84.67	42.33	21.17	42.33
1	0	0	1	1	130	130	1	86.67	43.33	21.67	43.33
1	0	1	0	0	140	140	1	70.00	35.00	17.50	35.00
1	0	1	0	1	136	136	1	68.00	34.00	17.00	34.00
1	0	1	1	0	166	166.00	1	83.00	41.50	20.75	41.50
1	0	1	1	1	155	155	1	77.50	38.75	19.38	38.75
1	1	0	0	0	150	112.5	4/3	75.00	37.50	18.75	37.50
1	1	0	0	1	117	117	1	78.00	39.00	19.50	39.00
1	1	0	1	0	107	107	1	71.33	35.67	17.83	35.67
1	1	0	1	1	100.9	100.9	1	67.27	33.63	16.82	33.63
1	1	1	0	0	145	108.75	4/3	72.50	36.25	18.13	36.25
1	1	1	0	1	140	105	4/3	70.00	35.00	17.50	35.00
1	1	1	1	0	138	103.5	4/3	69.00	34.50	17.25	34.50
1	1	1	1	1	137	102.75	4/3	68.50	34.25	17.13	34.25

## 6.0 SERIAL CONTROL 0REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ....) will be valid and acknowledged.

### Frequency Table Setting by I2C (SEL5 ~ SEL0)

SSE L5	SS EL4	SS EL3	SS EL2	SS EL1	SS EL0	CPU (MHz)	SDRAM (MHz)	CPU/S DRAM	3V66 (MHz)	PCI(M Hz)	IOAPIC (MHz) APIC_SEL=1	IOAPIC (MHz) APIC_SEL=0
0	0	0	0	0	0	83.3	124.95	2/3	83.30	41.65	20.83	41.65
0	0	0	0	0	1	90	90	1	60.00	30.00	15.00	30.00
0	0	0	0	1	0	75	112.5	2/3	75.00	37.50	18.75	37.50
0	0	0	0	1	1	72	108	2/3	72.00	36.00	18.00	36.00
0	0	0	1	0	0	89.07	133.6	2/3	89.07	44.53	22.27	44.53
0	0	0	1	0	1	95.25	95.25	1	63.50	31.75	15.88	31.75
0	0	0	1	1	0	121	121	1	80.67	40.33	20.17	40.33
0	0	0	1	1	1	124	124	1	82.67	41.33	20.67	41.33
0	0	1	0	0	0	119	119	1	79.33	39.67	19.83	39.67
0	0	1	0	0	1	114	114	1	76.00	38.00	19.00	38.00
0	0	1	0	1	0	110	110	1	73.33	36.67	18.33	36.67
0	0	1	0	1	1	105	105	1	70.00	35.00	17.50	35.00
0	0	1	1	0	0	66.8	100.2	2/3	66.80	33.40	16.70	33.40
0	0	1	1	0	1	100.2	100.2	1	66.80	33.40	16.70	33.40
0	0	1	1	1	0	133.6	133.6	1	66.80	33.40	16.70	33.40
0	0	1	1	1	1	133.6	100.2	4/3	66.80	33.40	16.70	33.40
0	1	0	0	0	0	135	101.25	4/3	67.50	33.75	16.88	33.75
0	1	0	0	0	1	125	125	1	83.33	41.67	20.83	41.67
0	1	0	0	1	0	127	127	1	84.67	42.33	21.17	42.33
0	1	0	0	1	1	130	130	1	86.67	43.33	21.67	43.33
0	1	0	1	0	0	140	140	1	70.00	35.00	17.50	35.00
0	1	0	1	0	1	136	136	1	68.00	34.00	17.00	34.00
0	1	0	1	1	0	166	166.00	1	83.00	41.50	20.75	41.50
0	1	0	1	1	1	155	155	1	77.50	38.75	19.38	38.75
0	1	1	0	0	0	150	112.5	4/3	75.00	37.50	18.75	37.50
0	1	1	0	0	1	117	117	1	78.00	39.00	19.50	39.00
0	1	1	0	1	0	107	107	1	71.33	35.67	17.83	35.67
0	1	1	0	1	1	100.9	100.9	1	67.27	33.63	16.82	33.63
0	1	1	1	0	0	145	108.75	4/3	72.50	36.25	18.13	36.25
0	1	1	1	0	1	140	105	4/3	70.00	35.00	17.50	35.00
0	1	1	1	1	0	138	103.5	4/3	69.00	34.50	17.25	34.50
0	1	1	1	1	1	137	102.75	4/3	68.50	34.25	17.13	34.25

## PRELIMINARY

SSE L5	SS EL4	SS EL3	SS EL2	SS EL1	SS EL0	CPU (MHz)	SDRAM (MHz)	CPU/S DRAM	3V66 (MHz)	PCI(M Hz)	IOAPIC (MHz) APIC_SEL=1	IOAPIC (MHz) APIC_SEL=0
1	0	0	0	0	0	136	102.00	4/3	68.00	34.00	17.00	34.00
1	0	0	0	0	1	138	138.00	1	69.00	34.50	17.25	34.50
1	0	0	0	1	0	139	104.25	4/3	69.50	34.75	17.38	34.75
1	0	0	0	1	1	141	141.00	1	70.50	35.25	17.63	35.25
1	0	0	1	0	0	142	142.00	1	71.00	35.50	17.75	35.50
1	0	0	1	0	1	142	106.50	4/3	71.00	35.50	17.75	35.50
1	0	0	1	1	0	143	143.00	1	71.50	35.75	17.88	35.75
1	0	0	1	1	1	143	107.25	4/3	71.50	35.75	17.88	35.75
1	0	1	0	0	0	144	144.00	1	72.00	36.00	18.00	36.00
1	0	1	0	0	1	144	108.00	4/3	72.00	36.00	18.00	36.00
1	0	1	0	1	0	146	146	1	73.00	36.50	18.25	36.50
1	0	1	0	1	1	146	109.50	4/3	73.00	36.50	18.25	36.50
1	0	1	1	0	0	147	147	1	73.50	36.75	18.38	36.75
1	0	1	1	0	1	147	110.25	4/3	73.50	36.75	18.38	36.75
1	0	1	1	1	0	148	148.00	1	74.00	37.00	18.50	37.00
1	0	1	1	1	1	148	111.00	4/3	74.00	37.00	18.50	37.00
1	1	0	0	0	0	149	111.75	4/3	74.50	37.25	18.63	37.25
1	1	0	0	0	1	152	152.00	1	76.00	38.00	19.00	38.00
1	1	0	0	1	0	153	114.75	4/3	76.50	38.25	19.13	38.25
1	1	0	0	1	1	156	156.00	1	78.00	39.00	19.50	39.00
1	1	0	1	0	0	157	117.75	4/3	78.50	39.25	19.63	39.25
1	1	0	1	0	1	158	158.00	1	79.00	39.50	19.75	39.50
1	1	0	1	1	0	159	119.25	4/3	79.50	39.75	19.88	39.75
1	1	0	1	1	1	160	160.00	1	80.00	40.00	20.00	40.00
1	1	1	0	0	0	162	121.5	4/3	81.00	40.50	20.25	40.50
1	1	1	0	0	1	164	164.00	1	82.00	41.00	20.50	41.00
1	1	1	0	1	0	170	170.00	1	85.00	42.50	21.25	42.50
1	1	1	0	1	1	175	175	1	87.5	43.75	21.88	43.75
1	1	1	1	0	0	180	90	2	60	30	15	30
1	1	1	1	0	1	185	92.5	2	61.67	30.83	15.42	30.83
1	1	1	1	1	0	190	126.67	3/2	63.33	31.67	15.83	31.67
1	1	1	1	1	1	200.4	133.60	3/2	66.80	33.40	16.70	33.40

## 6.1 Register 0: Control Register

Bit	@PowerUp	Pin	Description
7	0	-	Reserved
6	1	1	REF2X(Active / Inactive)
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Reserved
2	1	23	24_48MHz(Active / Inactive)
1	1	21,22	48MHz_0, 48MHz_1(Active / Inactive)
0	1	31	SDRAM8(Active / Inactive)

## 6.2 Register 1 : SDRAM Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	32	SDRAM7 (Active / Inactive)
6	1	33	SDRAM6 (Active / Inactive)
5	1	35	SDRAM5 (Active / Inactive)
4	1	36	SDRAM4 (Active / Inactive)
3	1	37	SDRAM3 (Active / Inactive)
2	1	39	SDRAM2 (Active / Inactive)
1	1	40	SDRAM1 (Active / Inactive)
0	1	41	SDRAM0 (Active / Inactive)

## 6.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	19	PCICLK7 (Active / Inactive)
6	1	18	PCICLK6 (Active / Inactive)
5	1	17	PCICLK5 (Active / Inactive)
4	1	15	PCICLK4 (Active / Inactive)
3	1	14	PCICLK3 (Active / Inactive)
2	1	13	PCICLK2 (Active / Inactive)
1	1	11	PCICLK1 (Active / Inactive)
0	1	10	PCICLK0 (Active / Inactive)



## PRELIMINARY

**6.4 Register 3: CPU Clock Register (1 = Active, 0 = Inactive)**

Bit	@PowerUp	Pin	Description
7	X	-	FS0#
6	1	7	3V66_0(Active / Inactive)
5	1	8	3V66_1(Active / Inactive)
4	X	-	FS1#
3	1	47	IOAPIC(Active / Inactive)
2	1	44	CPUCLK1 (Active / Inactive)
1	1	43	CPUCLK0 (Active / Inactive)
0	X	-	FS2#

**6.5 Register 4: Control Register (1 = Active, 0 = Inactive)**

Bit	@PowerUp	Pin	Description
7	0	-	SSEL3 (Frequency table selection by software via I <sup>2</sup> C )
6	0	-	SSEL2 ( Frequency table selection by software via I <sup>2</sup> C )
5	0	-	SSEL1 ( Frequency table selection by software via I <sup>2</sup> C )
4	0	-	SSEL0 ( Frequency table selection by software via I <sup>2</sup> C )
3	0	-	0 = Selection by hardware 1 = Selection by software I <sup>2</sup> C - Bit (1,2, 4:6)
2	0	-	SSEL4 (Frequency table selection by software via I <sup>2</sup> C )
1	0	-	SSEL5 (Frequency table selection by software via I <sup>2</sup> C )
0	0	-	Reserved

**6.6 Register 5: Control Register (1 = Active, 0 = Inactive)**

Bit	@PowerUp	Pin	Description
7	0	-	0 = $\pm 0.5\%$ Center type Spread Spectrum Modulation 1 = $\pm 0.75\%$ Center type Spread Spectrum Modulation
6	1	-	SKEW2(SDRAM to CPU Skew programming bit)
5	0	-	SKEW1(SDRAM to CPU Skew programming bit)
4	0	-	SKEW0(SDRAM to CPU Skew programming bit)
3	X	-	FS3#
2	X	-	FS4#
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	X	-	APIC_SEL#

PRELIMINARY

**6.7 Register 6: Winbond Chip ID Register (Read Only)**

Bit	@PowerUp	Pin	Description
7	1	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	1	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	0	-	Winbond Chip ID
0	0	-	Winbond Chip ID

**6.8 Register 7: Winbond Chip ID Register (Read Only)**

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Version ID
1	0	-	Winbond Version ID
0	1	-	Winbond Version ID

## 7.0 SPECIFICATIONS

### 7.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vdd , V <sub>IN</sub>	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
T <sub>STG</sub>	Storage Temperature	- 65°C to + 150°C
T <sub>B</sub>	Ambient Temperature	- 55°C to + 125°C
T <sub>A</sub>	Operating Temperature	0°C to + 70°C

### 7.2 Electrical Characteristics---Input/Output

Vddq1=Vddq2 = Vddq3 = Vddq4 =3.3V, VddL1 =VddL2= 2.5V , T <sub>A</sub> = 0° C to +70° C						
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Low Voltage	V <sub>IL</sub>	Vss-0.3		0.8	V <sub>dc</sub>	
Input High Voltage	V <sub>IH</sub>	2.0		Vdd+0.3	V <sub>dc</sub>	
Input Low Current	I <sub>IL</sub>	-5			μA	No pull-up resistors
Input Low Current	I <sub>IL</sub>	-200			μA	Pull-up resistors
Input High Current	I <sub>IH</sub>	-5		5	μA	
Input Capacitance	C <sub>IN</sub>			5	pF	Logic inputs
	C <sub>OUT</sub>			6	pF	Output capacitance
	C <sub>INX</sub>	27		45	pF	Xin and Xout
Operating Supply Current	I <sub>dd3</sub>			100	MA	CPU = 66.6 MHz PCI = 33.3 Mhz with load
Power Down Supply Current	I <sub>dd2</sub>			600	μA	
Settling Time	T <sub>s</sub>			3	mS	From first crossing to 1% target freq.
Delay	t <sub>PZH</sub> , t <sub>PZH</sub>	1		10	nS	Output enable delay
	t <sub>PLZ</sub> , t <sub>PZH</sub>	1		10	nS	Output enable delay

### 7.3 Electrical Characteristics of CPU Clock

V<sub>dd</sub>=2.5V +/- 5%; C<sub>L</sub>=10-20pF

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R <sub>DSP</sub>	13.5		40	Ohm	
Output Impedance	R <sub>DSN</sub>	13.5		40	Ohm	
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> =1mA
Output High Voltage	V <sub>OH</sub>	2.0			V	I <sub>OH</sub> =-1mA
Output Low Current	I <sub>OL</sub>	27		30	MA	
Output High Current	I <sub>OH</sub>	-27		-27	MA	
Pull-Up Current Min	I <sub>OH(min)</sub>	-27			MA	V <sub>out</sub> = 1.0 V
Pull-Up Current Max	I <sub>OH(max)</sub>			-27	MA	V <sub>out</sub> = 2.0V
Rise/Fall Time Min Between 0.4 V and 2.0 V	T <sub>RF(min)</sub>	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	T <sub>RF(max)</sub>			1.6	ns	20pF Load
Duty Cycle	Dt	45		55	%	V <sub>T</sub> =1.25V
Skew	T <sub>SK</sub>			175	ps	V <sub>T</sub> =1.25V
Jitter	T <sub>sc-c</sub>			250	ps	V <sub>T</sub> =1.25V

### 7.4 Electrical Characteristics of 3V66 Clock

V<sub>dd</sub>=3.3V +/- 5%; C<sub>L</sub>=10-30pF

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R <sub>DSP</sub>	15		55	Ohm	
Output Impedance	R <sub>DSN</sub>	15		55	Ohm	
Output Low Voltage	V <sub>OL</sub>			0.55	V	I <sub>OL</sub> =1mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> =-1mA
Output Low Current	I <sub>OL</sub>	30		38	MA	
Output High Current	I <sub>OH</sub>	-33		-33	MA	
Rise/Fall Time Min Between 0.4 V and 2.0 V	T <sub>RF(min)</sub>	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	T <sub>RF(max)</sub>			1.6	ns	20pF Load
Duty Cycle	Dt	45		55	%	V <sub>T</sub> =1.5V
Skew	T <sub>SK</sub>			175	ps	V <sub>T</sub> =1.5V
Jitter	T <sub>sc-c</sub>			500	ps	V <sub>T</sub> =1.5V

## 7.5 Electrical Characteristics of SDRAM Clock

Vdd=3.3V +/- 5%; C<sub>L</sub>=20-30pF

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R <sub>DSP</sub>	13.5		40	Ohm	
Output Impedance	R <sub>DSN</sub>	13.5		40	Ohm	
Output Low Voltage	V <sub>OL</sub>			0.45	V	I <sub>OL</sub> =1mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> =-1mA
Output Low Current	I <sub>OL</sub>	54		54	MA	
Output High Current	I <sub>OH</sub>	-54		-45	MA	
Rise/Fall Time Min Between 0.4 V and 2.0 V	T <sub>RF(min)</sub>	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	T <sub>RF(max)</sub>			1.6	ns	20pF Load
Duty Cycle	Dt	45		55	%	V <sub>T</sub> =1.5V
Skew	T <sub>SK</sub>			250	ps	V <sub>T</sub> =1.5V
Jitter	T <sub>SC-C</sub>			250	ps	V <sub>T</sub> =1.5V

## 7.6 Electrical Characteristics of PCI Clock

Vdd=3.3V +/- 5%; C<sub>L</sub>=10-30pF

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R <sub>DSP</sub>	15		55	Ohm	
Output Impedance	R <sub>DSN</sub>	15		55	Ohm	
Output Low Voltage	V <sub>OL</sub>			0.55	V	I <sub>OL</sub> =1mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> =-1mA
Output Low Current	I <sub>OL</sub>	30		38	MA	
Output High Current	I <sub>OH</sub>	-33		-33	MA	
Rise/Fall Time Min Between 0.4 V and 2.0 V	T <sub>RF(min)</sub>	0.5			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	T <sub>RF(max)</sub>			2.0	ns	20pF Load
Duty Cycle	Dt	45		55	%	V <sub>T</sub> =1.5V
Skew	T <sub>SK</sub>			500	ps	V <sub>T</sub> =1.5V
Jitter	T <sub>SC-C</sub>			500	ps	V <sub>T</sub> =1.5V

**PRELIMINARY****7.7 Electrical Characteristics of 48MHz, REF Clock**V<sub>dd</sub>=3.3V +/- 5%; C<sub>L</sub>=10-20pF

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R <sub>DSP</sub>	20		55	Ohm	
Output Impedance	R <sub>DSN</sub>	20		55	Ohm	
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> =1mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> =-1mA
Output Low Current	I <sub>OL</sub>	29		27	MA	
Output High Current	I <sub>OH</sub>	-29		-23	MA	
RiseTime	T <sub>R</sub>		1.8	4	ns	10pF Load
Fall Time	T <sub>F</sub>		1.7	4	ns	20pF Load
Duty Cycle	Dt	45		55	%	V <sub>T</sub> =1.5V
Skew	T <sub>SK</sub>			500	ps	V <sub>T</sub> =1.5V
Jitter	T <sub>sc-c</sub>			1000	ps	V <sub>T</sub> =1.5V

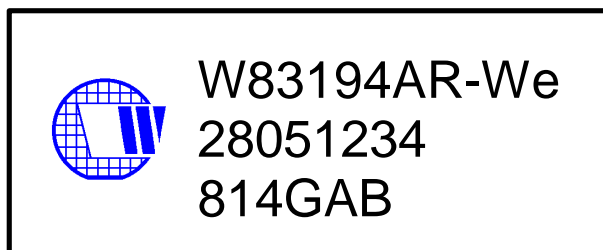


## PRELIMINARY

### 8.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194AR-We	48 PIN SSOP	Commercial, 0°C to +70°C

### 9.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194AR-We

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

814: packages made in '98, week 14

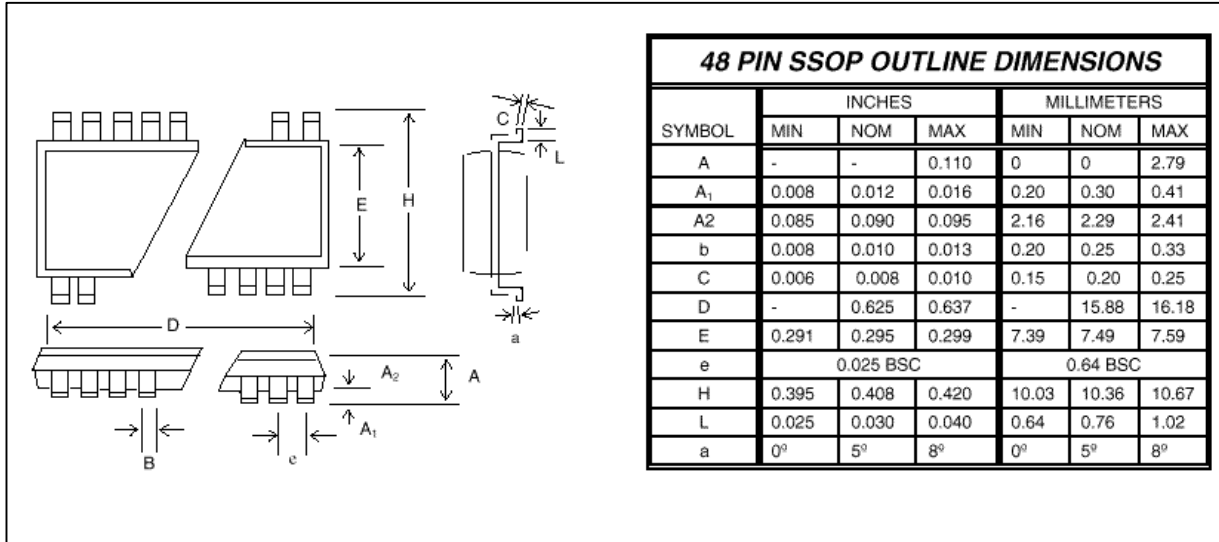
G: assembly house ID; O means OSE, G means GR

A: Internal use code

B: IC revision

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## 10.0 PACKAGE DRAWING AND DIMENSIONS



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