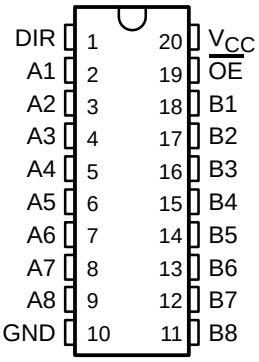
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds JESD 22**
  **– 2000-V Human-Body Model (A114-A)**

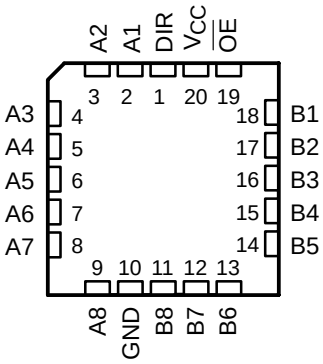
## description

These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

**SN54BCT245 . . . J OR W PACKAGE**
**SN74BCT245 . . . DB, DW, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54BCT245 . . . FK PACKAGE**
**(TOP VIEW)**




**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | PDIP – N | Tube | SN74BCT245N | SN74BCT245N |
| | SOIC – DW | Tube | SN74BCT245DW | BCT245 |
| | | Tape and reel | SN74BVT245DWR | |
| | SOP – NS | Tape and reel | SN74BCT245NSR | BCT245 |
| | SSOP – DB | Tape and reel | SN74BCT245DBR | BT245 |
| | TSSOP – PW | Tape and reel | SN74BCT245PWR | BT245 |
| –55°C to 125°C | CDIP – J | Tube | SNJ54BCT245J | SNJ54BCT245J |
| | CFP – W | Tube | SNJ54BCT245W | SNJ54BCT245W |
| | LCCC – FK | Tube | SNJ54BCT245FK | SNJ54BCT245FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

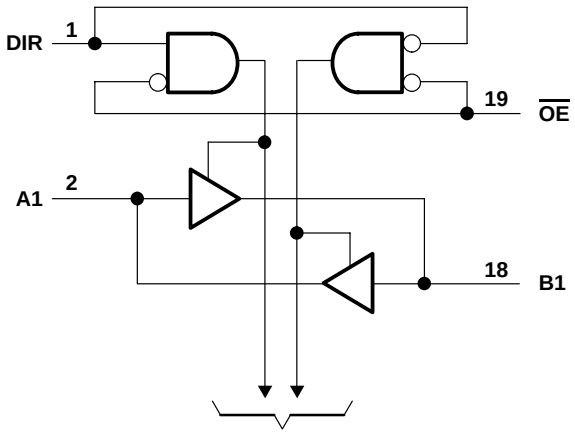
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**FUNCTION TABLE**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

## logic diagram (positive logic)




**To Seven Other Channels**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$: Control inputs (see Note 1) . . . . . –0.5 V to 7 V
I/O ports (see Note 1) . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ . . . . . –0.5 V to $V_{CC}$
Current into any output in the low state, $I_O$: SN54BCT245 . . . . . 96 mA
SN74BCT245 . . . . . 128 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
PW package . . . . . 83°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | SN54BCT245 | | | SN74BCT245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | –18 | | | –18 | mA |
| $I_{OH}$ | High-level output current | A port | | | –3 | | | –3 | mA |
| | | B port | | | –12 | | | –15 | |
| $I_{OL}$ | Low-level output current | A port | | | 20 | | | 24 | mA |
| | | B port | | | 48 | | | 64 | |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | 0 | | 70 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54BCT245 | | | SN74BCT245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | A port | $V_{CC}$ = 4.5 V | $I_{OH}$ = –1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | $I_{OH}$ = –3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | B port | $V_{CC}$ = 4.5 V | $I_{OH}$ = –3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | | | $I_{OH}$ = –12 mA | 2 | 3.2 | | | | | |
| | | | $I_{OH}$ = –15 mA | | | | 2 | 3.1 | | |
| $V_{OL}$ | A port | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| | B port | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | 0.38 | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | 0.42 | 0.55 | |
| $I_I$ | A or B port | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| | Control input | | | | | 0.1 | | | 0.1 | |
| $I_{IH}$‡ | A or B port | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 70 | | | 70 | µA |
| | Control input | | | | | 20 | | | 20 | |
| $I_{IL}$‡ | A or B port | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | –0.65 | | | –0.65 | mA |
| | Control input | | | | | –1.2 | | | –1.2 | |
| $I_{OS}$§ | A port | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | –60 | | –150 | –60 | | –150 | mA |
| | B port | | | –100 | | –225 | –100 | | –225 | |
| $I_{CCL}$ | A to B | $V_{CC}$ = 5.5 V | | | 57 | 90 | | 57 | 90 | mA |
| $I_{CCH}$ | A to B | $V_{CC}$ = 5.5 V | | | 36 | 57 | | 36 | 57 | mA |
| $I_{CCZ}$ | | $V_{CC}$ = 5.5 V | | | 10 | 15 | | 10 | 15 | mA |
| $C_i$ | Control input | $V_{CC}$ = 5 V, | $V_I$ = 2.5 V or 0.5 V | | 7 | | | 7 | | pF |
| $C_{io}$ | A to B | $V_{CC}$ = 5 V, | $V_O$ = 2.5 V or 0.5 V | | 9 | | | 9 | | pF |
| | B to A | | | | 12 | | | 12 | | |

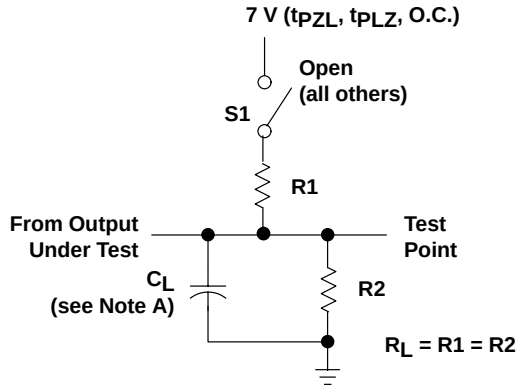
† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

## switching characteristics (see Figure 1)

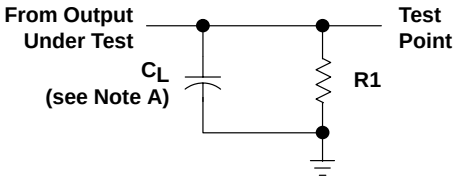
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | ′BCT245 | | | SN54BCT245 | | SN74BCT245 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 1 | 4.4 | 6 | 1 | 7.2 | 1 | 7 | ns |
| $t_{PHL}$ | | | 1.5 | 4.8 | 6.6 | 1.5 | 7.6 | 1.5 | 7 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 1.5 | 8 | 9.4 | 1.5 | 11.2 | 1.5 | 10.9 | ns |
| $t_{PZL}$ | | | 1.5 | 8 | 10.2 | 1.5 | 11.8 | 1.5 | 11.6 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 1.5 | 5.8 | 8.3 | 1.5 | 9.7 | 1.5 | 9.3 | ns |
| $t_{PLZ}$ | | | 1.5 | 5.1 | 7.8 | 1.5 | 9.6 | 1.5 | 9.1 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

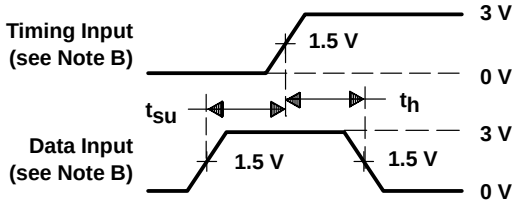
## PARAMETER MEASUREMENT INFORMATION



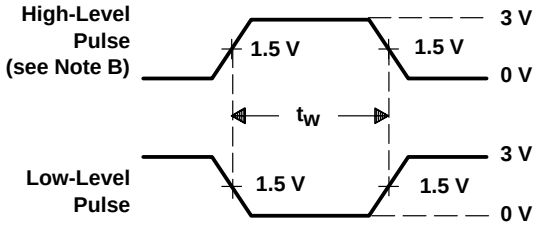

LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



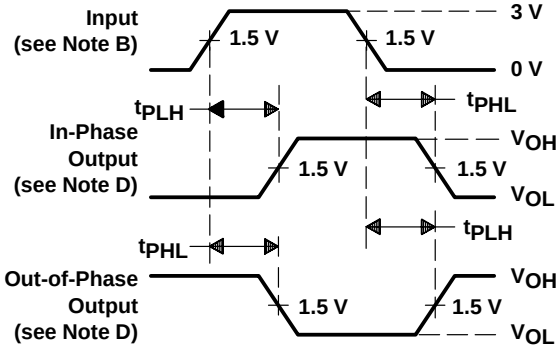

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



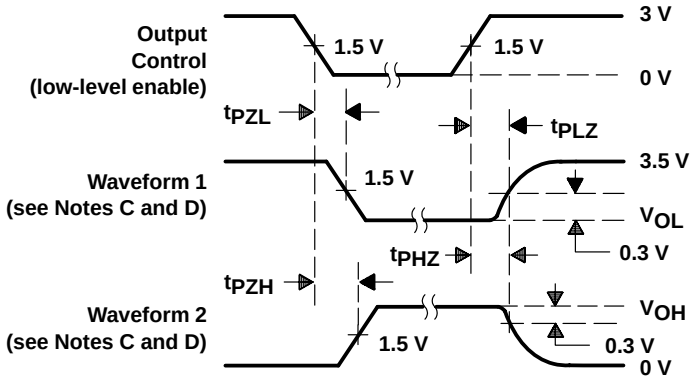

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

**Figure 1. Load Circuit and Voltage Waveforms**

## TYPICAL CHARACTERISTICS†

Figures 2 through 5 show the typical power dissipation for an SN74BCT245 over variations in outputs switching, output frequency, and capacitive load.

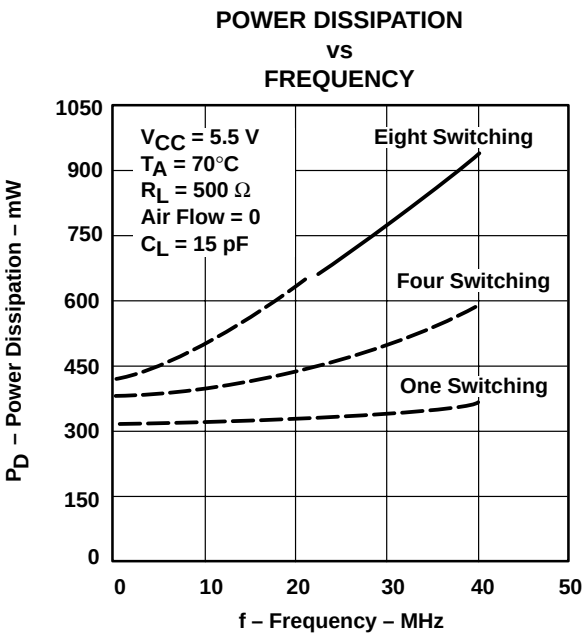



**Figure 2**

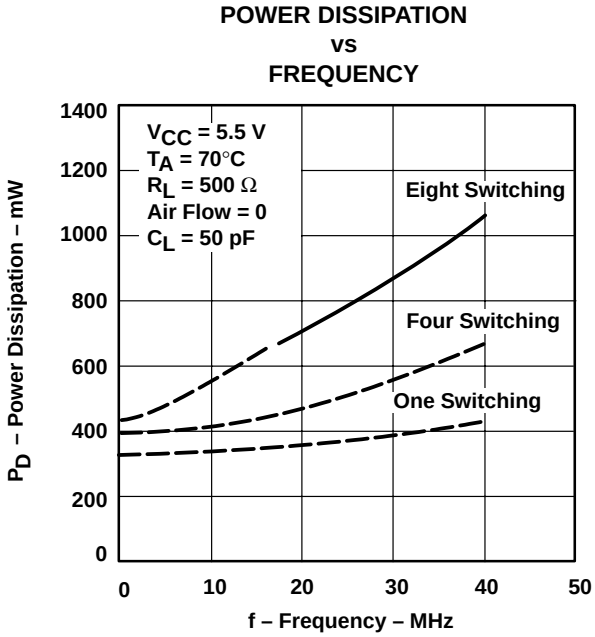



**Figure 3**

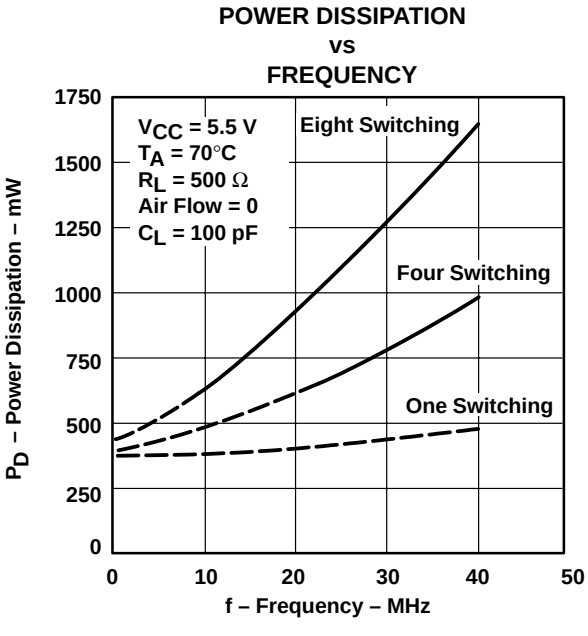



**Figure 4**

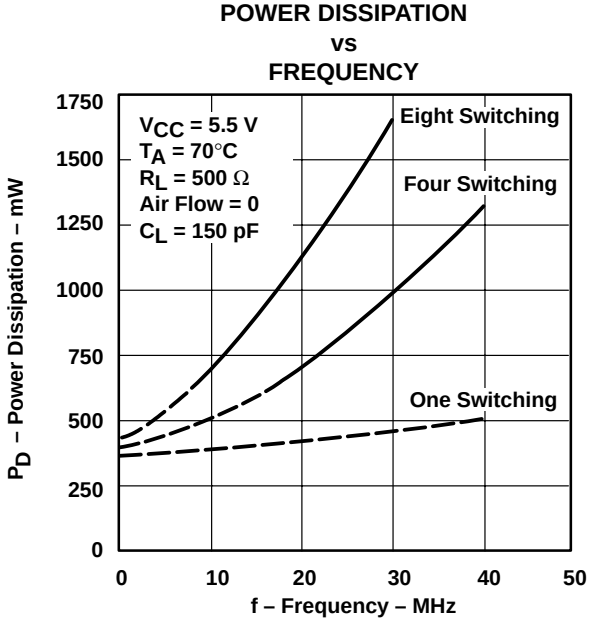



**Figure 5**

† The dashed lines are for the DB package only.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| 5962-9051401M2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-9051401MRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| 5962-9051401MSA | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| SN74BCT245DBLE | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI |
| SN74BCT245DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245DBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245DBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74BCT245NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74BCT245NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245NSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245PWE4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245PWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245PWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT245PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SNJ54BCT245FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54BCT245J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ54BCT245W | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

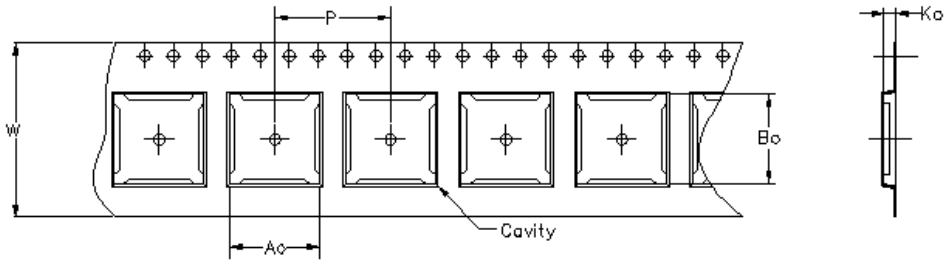
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

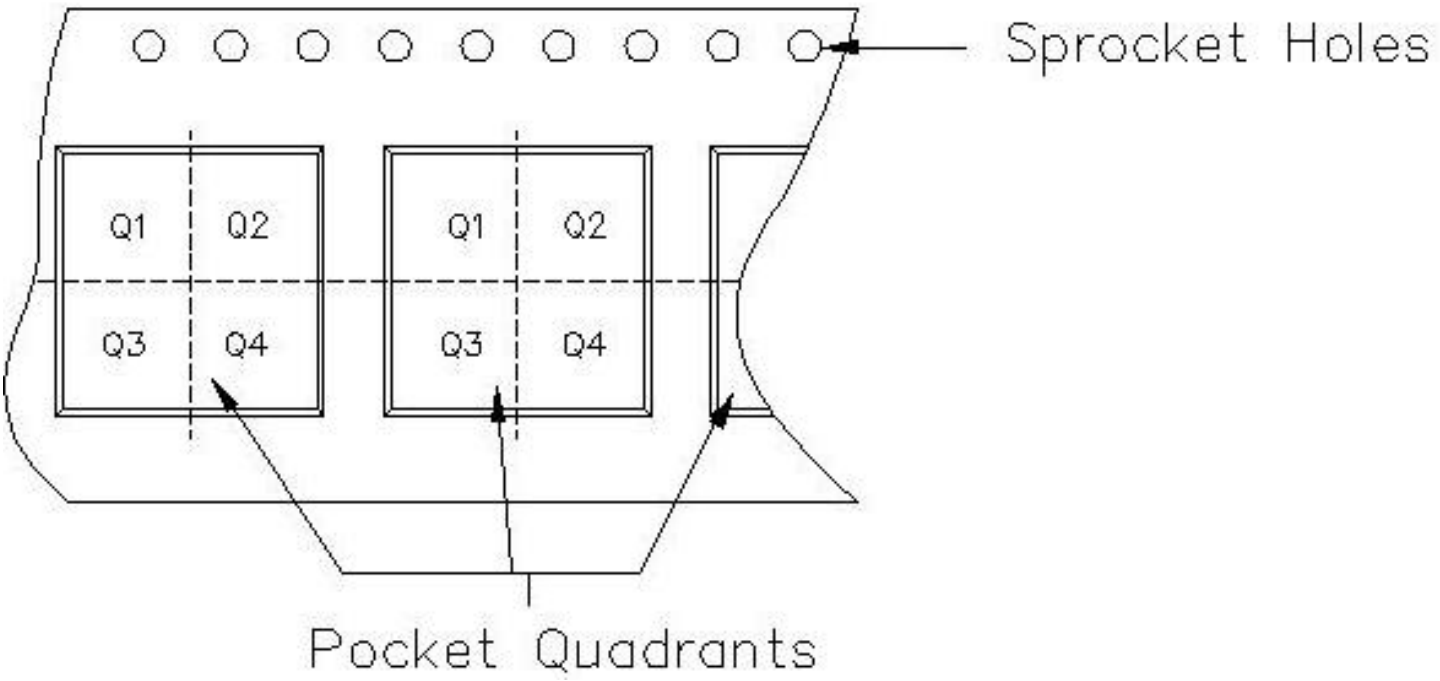
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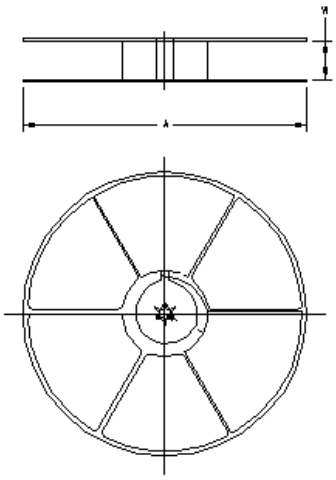

Carrier tape design is defined largely by the component lentgh, width, and thickness.

| |
|---|
| Ao = Dimension designed to accommodate the component width. |
| Bo = Dimension designed to accommodate the component length. |
| Ko = Dimension designed to accommodate the component thickness. |
| W = Overall width of the carrier tape. |
| P = Pitch between successive cavity centers. |



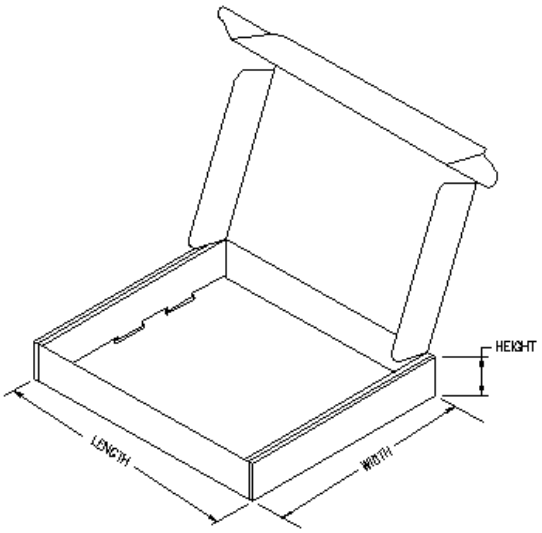

**TAPE AND REEL INFORMATION**

| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74BCT245DBR | DB | 20 | MLA | 330 | 16 | 8.2 | 7.5 | 2.5 | 12 | 16 | Q1 |
| SN74BCT245DWR | DW | 20 | MLA | 330 | 24 | 10.8 | 13.0 | 2.7 | 12 | 24 | Q1 |
| SN74BCT245NSR | NS | 20 | MLA | 330 | 24 | 8.2 | 13.0 | 2.5 | 12 | 24 | Q1 |
| SN74BCT245PWR | PW | 20 | MLA | 330 | 16 | 6.95 | 7.1 | 1.6 | 8 | 16 | Q1 |



## TAPE AND REEL BOX INFORMATION

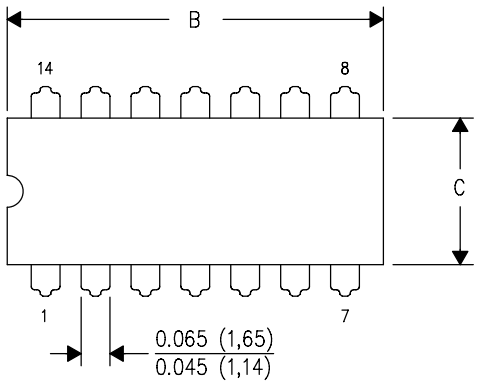
| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|
| SN74BCT245DBR | DB | 20 | MLA | 342.9 | 336.6 | 28.58 |
| SN74BCT245DWR | DW | 20 | MLA | 333.2 | 333.2 | 31.75 |
| SN74BCT245NSR | NS | 20 | MLA | 333.2 | 333.2 | 31.75 |
| SN74BCT245PWR | PW | 20 | MLA | 342.9 | 336.6 | 28.58 |


HEIGHT
LENGTH
WIDTH

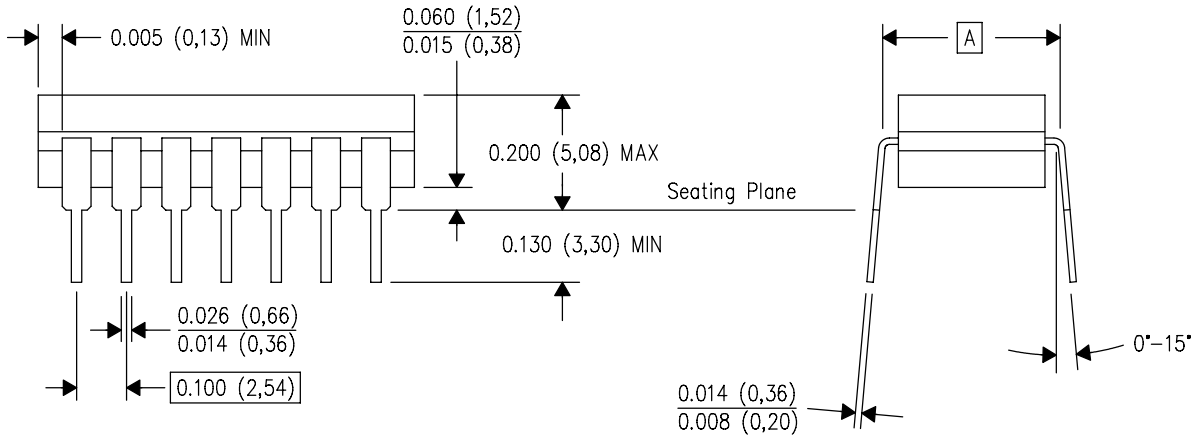
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE



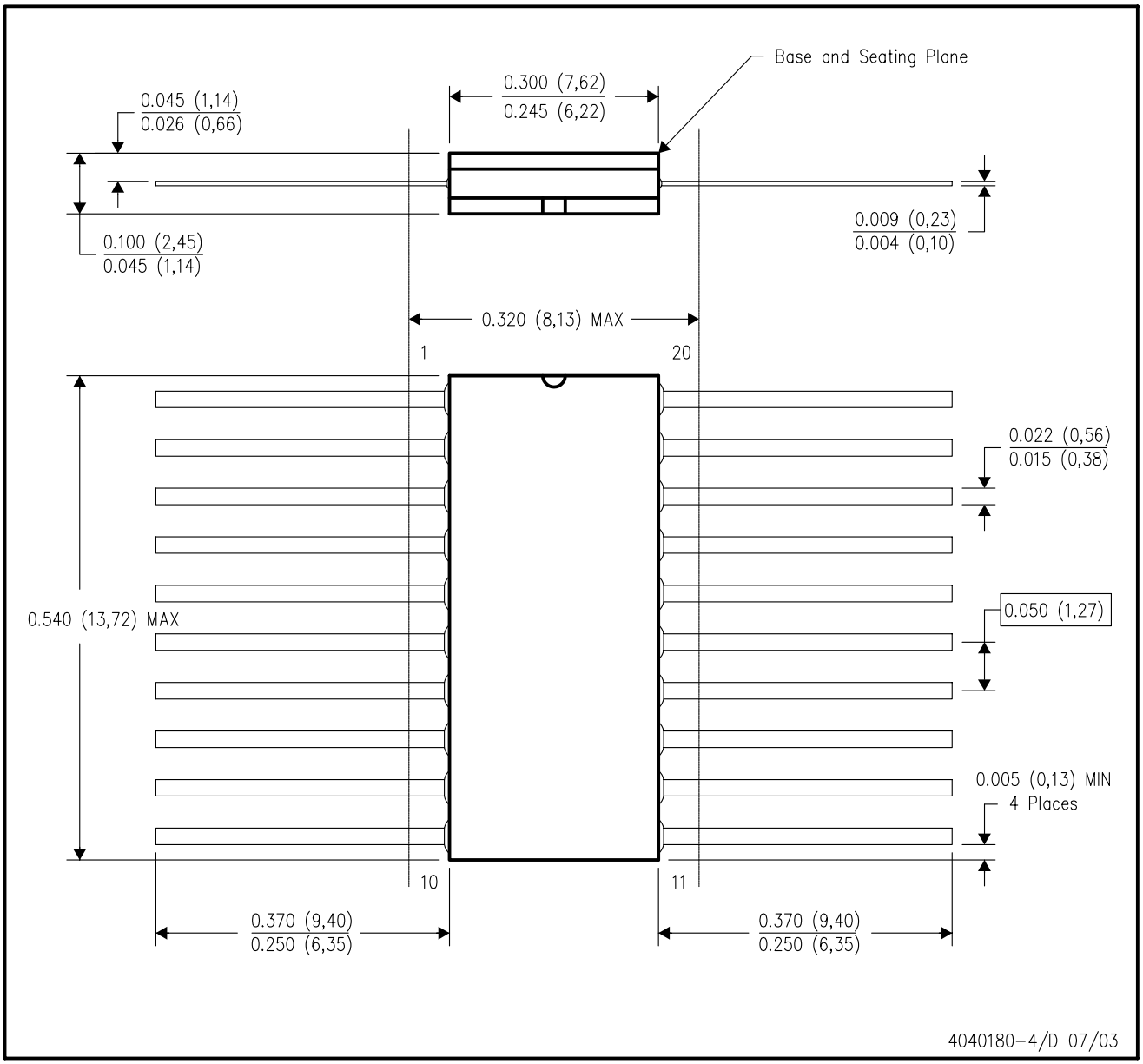

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

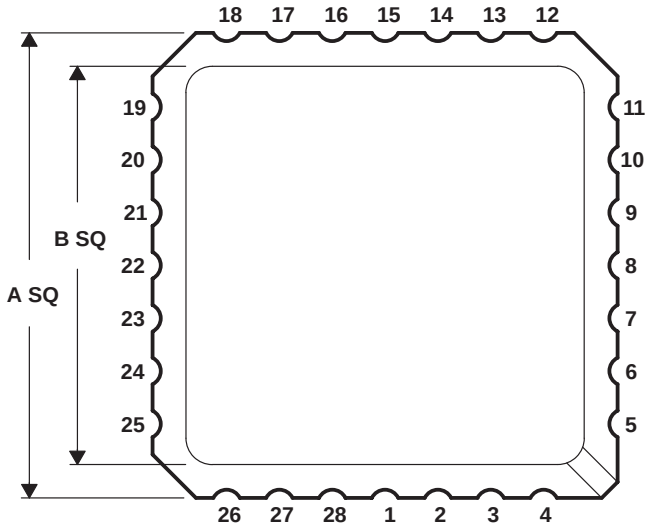
## W (R–GDFP–F20) CERAMIC DUAL FLATPACK



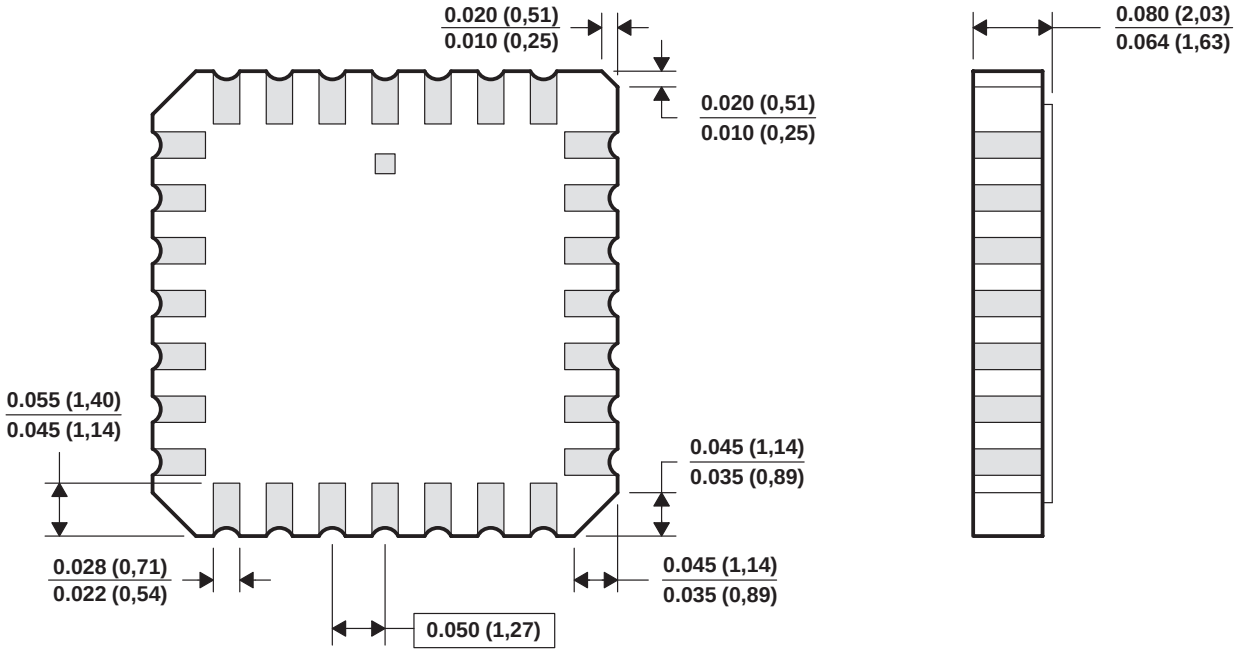

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

**FK (S-CQCC-N**)** **LEADLESS CERAMIC CHIP CARRIER**

**28 TERMINAL SHOWN**




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.739 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



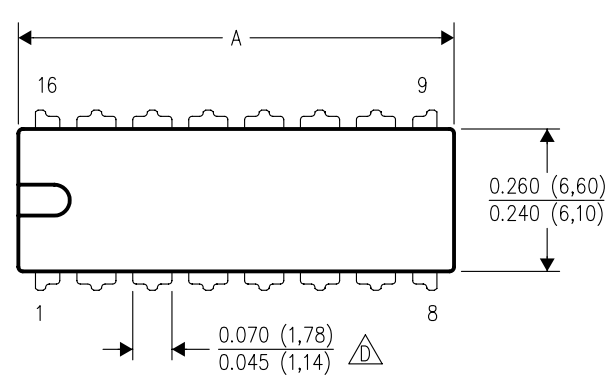

**4040140/D 10/96**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

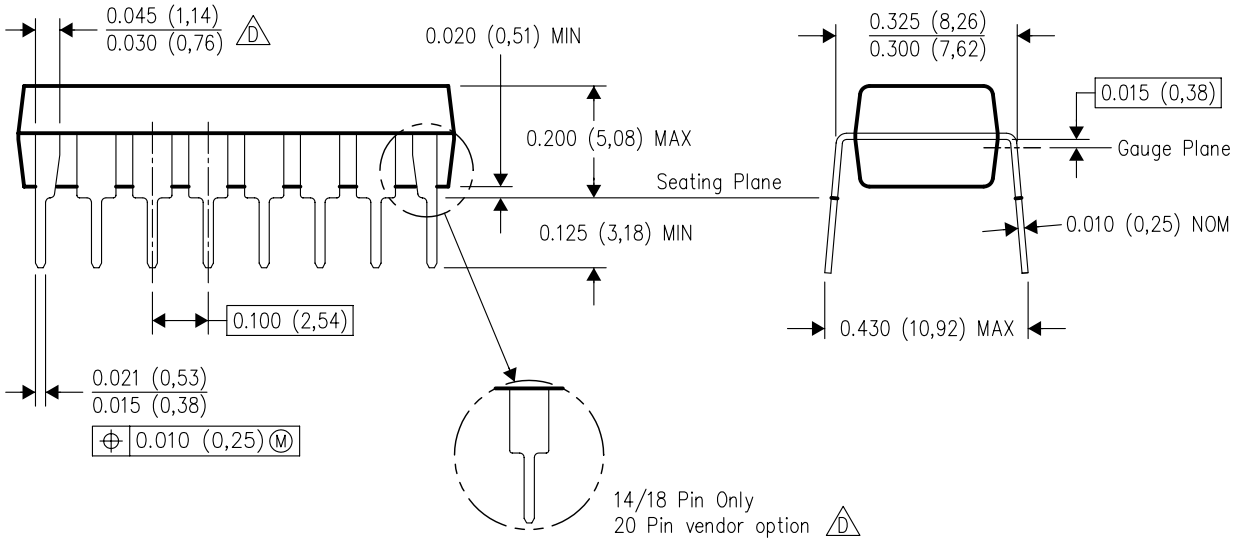
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



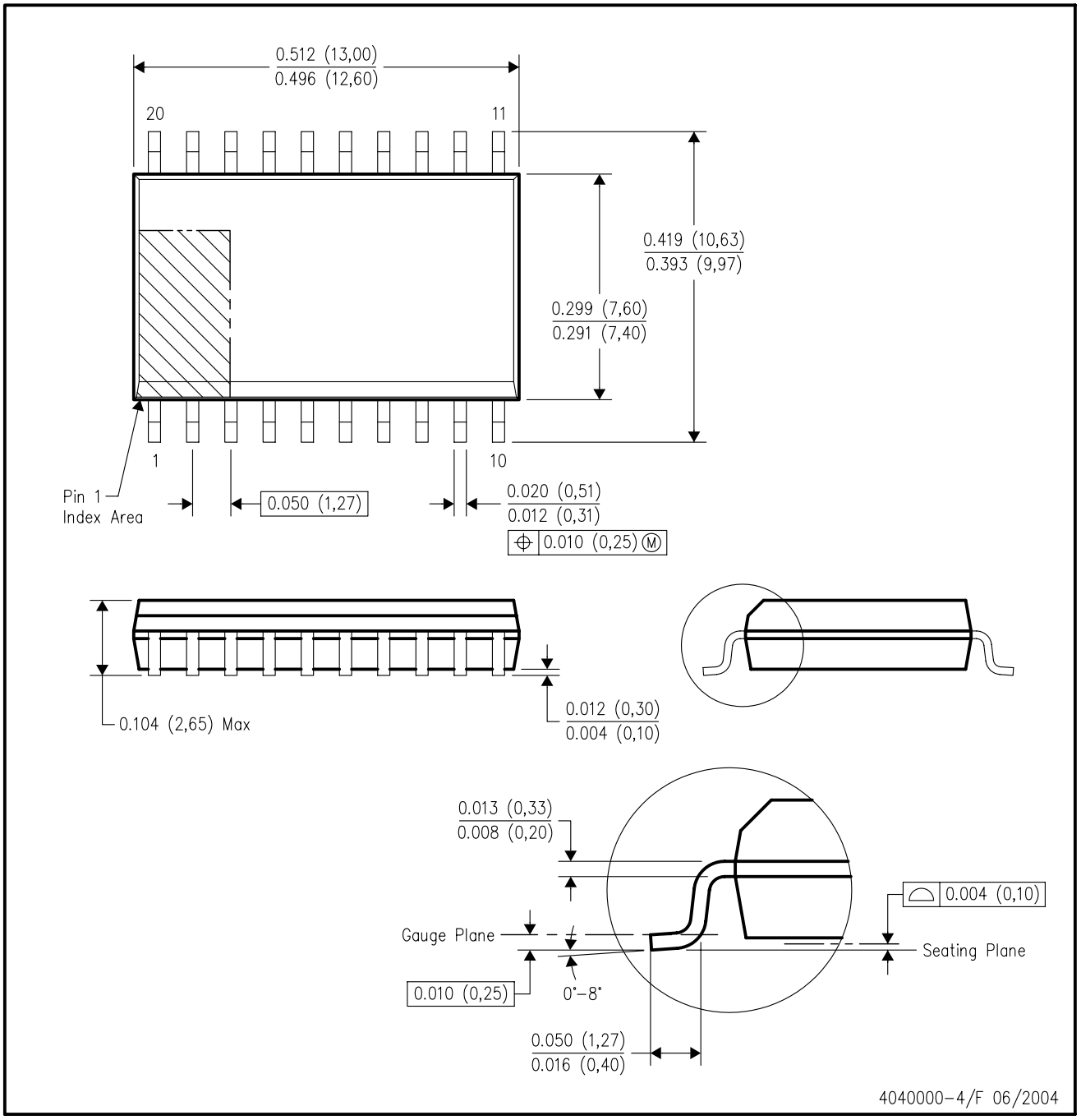

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE

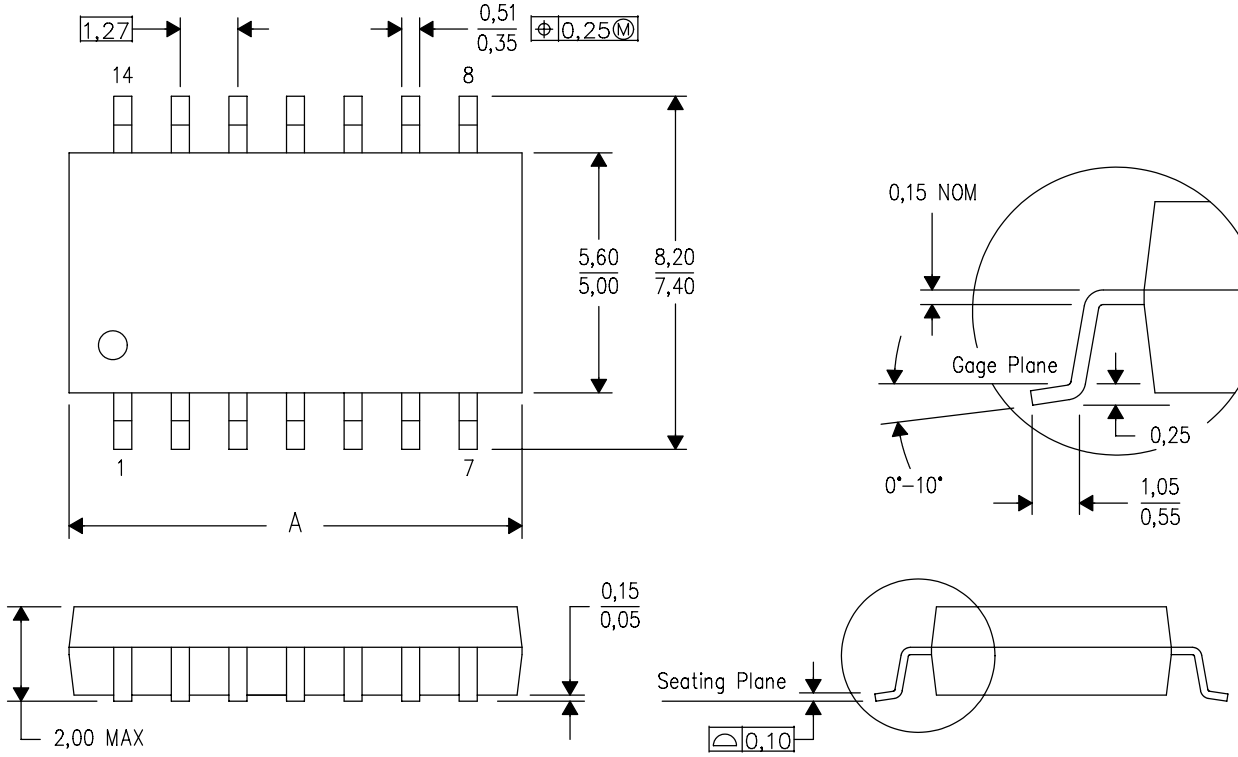



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

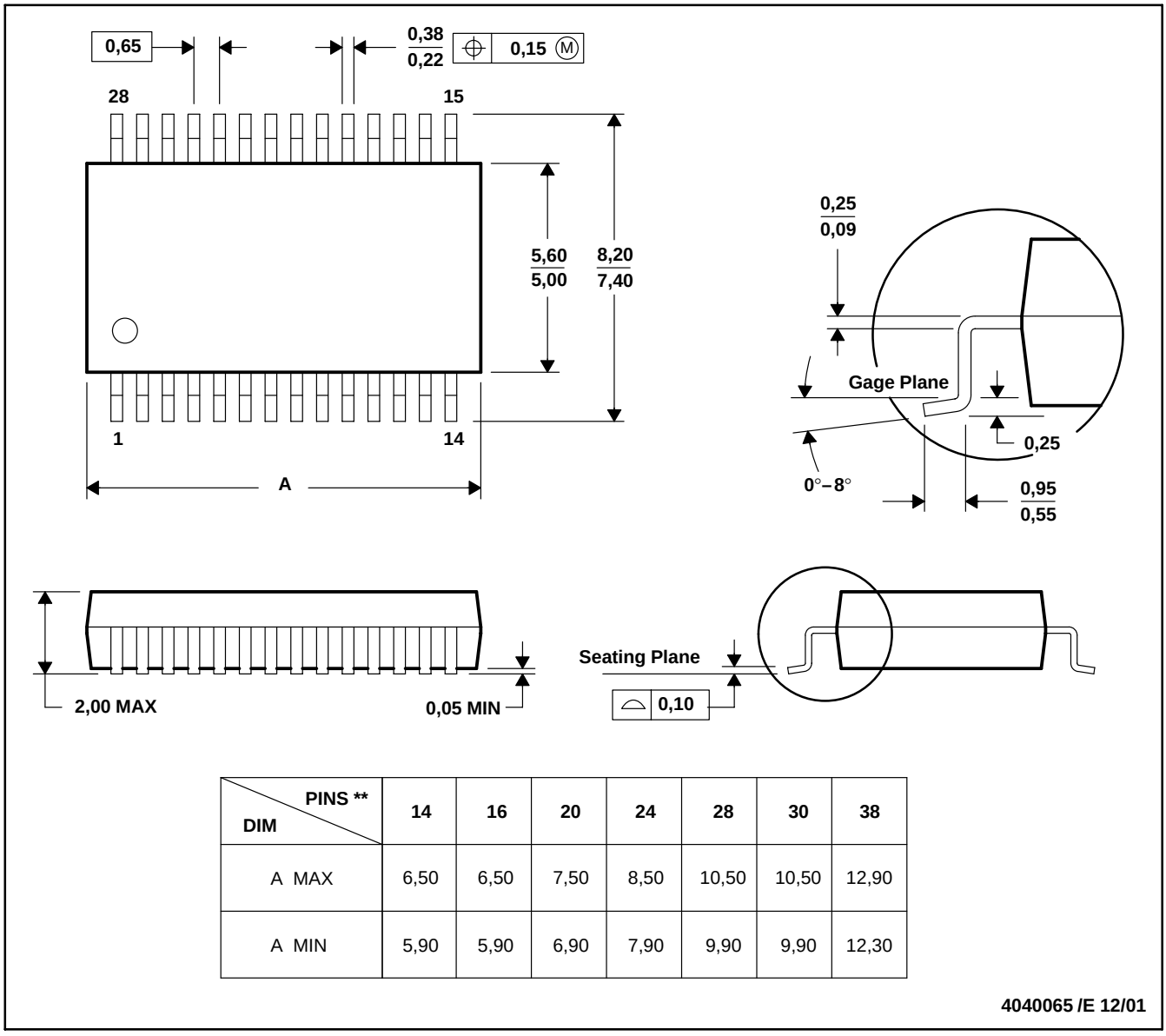
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**



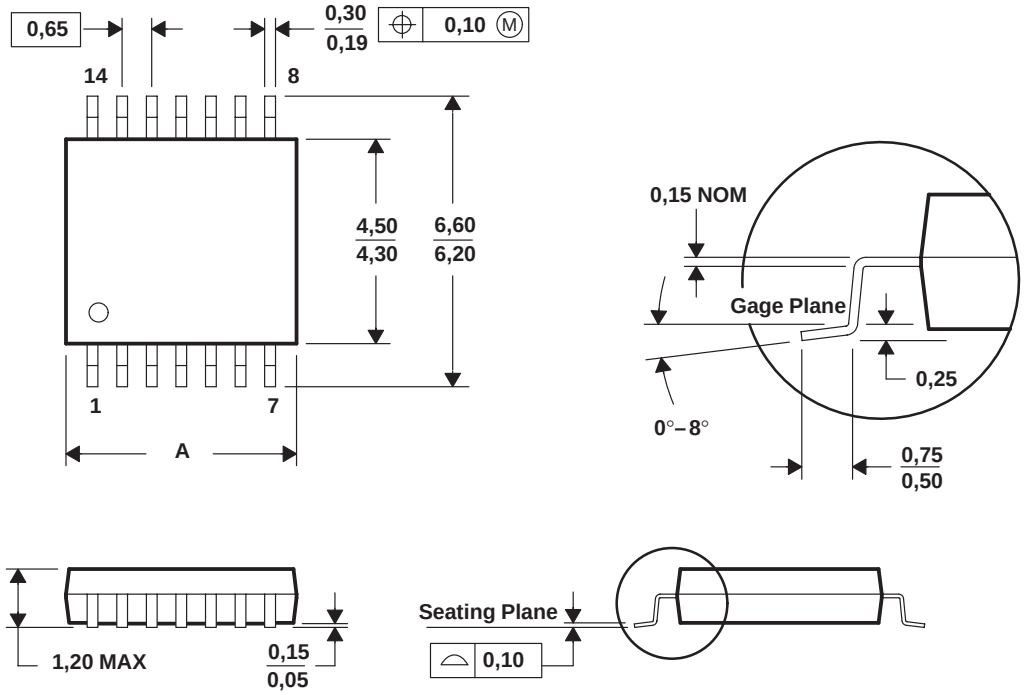

| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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