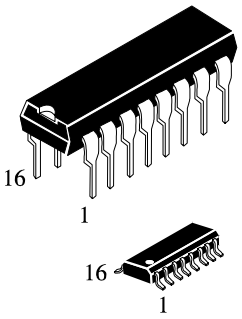
1-OF-8 DECODER/DEMULTIPLEXER

High-Speed Silicon-Gate CMOS

The IN74ACT138 is identical in pinout to the LS/ALS138, HC/HCT138. The IN74ACT138 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The IN74ACT138 decodes a three-bit Address to one-of-eight active-lot outputs. This device features three Chip Select inputs, two active-low and one active-high to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA; 0.1 μA @ 25°C
- Outputs Source/Sink 24 mA



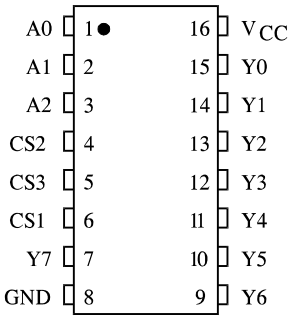
N SUFFIX
PLASTIC

D SUFFIX
SOIC

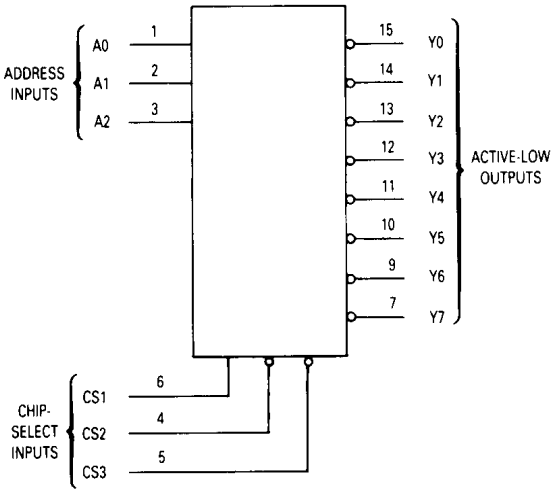
ORDERING INFORMATION

IN74ACT138N Plastic
IN74ACT138D SOIC
T_A = -40° to 85° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16 =V_{CC}
PIN 8 = GND

FUNCTION TABLE

Inputs						Outputs							
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level (steady state)
L = low level (steady state)
X = don't care

INTEGRAL

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_J	Junction Temperature (PDIP)		140	°C
T_A	Operating Temperature, All Package Types	-40	+85	°C
I_{OH}	Output Current - High		-24	mA
I_{OL}	Output Current - Low		24	mA
t_r, t_f	Input Rise and Fall Time * V_{CC} =4.5 V (except Schmitt Inputs) V_{CC} =5.5 V	0 0	10 8.0	ns/V

* V_{IN} from 0.8 V to 2.0 V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limits 25 °C	Guaranteed Limits -40°C to 85°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V	4.5 5.5	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V	4.5 5.5	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$I_{OUT} \leq$ -50 μA	4.5 5.5	4.4 5.4	4.4 5.4	V
		*V_{IN}=V_{IH} or V_{IL} I_{OH}=-24 mA I_{OH}=-24 mA	4.5 5.5	3.86 4.86	3.76 4.76	
V_{OL}	Maximum Low-Level Output Voltage	$I_{OUT} \leq$ 50 μA	4.5 5.5	0.1 0.1	0.1 0.1	V
		*V_{IN}= V_{IH} or V_{IL} I_{OL}=24 mA I_{OL}=24 mA	4.5 5.5	0.36 0.36	0.44 0.44	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	5.5	±0.1	±1.0	μA
ΔI_{CCT}	Additional Max. I_{CC}/Input	V_{IN}=V_{CC} - 2.1 V	5.5		1.5	mA
I_{OLD}	+Minimum Dynamic Output Current	V_{OLD}=1.65 V Max	5.5		75	mA
I_{OHD}	+Minimum Dynamic Output Current	V_{OHD}=3.85 V Min	5.5		-75	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND	5.5	8.0	80	μA

* All outputs loaded; thresholds on input associated with output under test.
+Maximum test duration 2.0 ms, one output loaded at a time.

AC ELECTRICAL CHARACTERISTICS(V_{CC}=5.0 V ± 10%, C_L=50pF,Input t_r=t_f=3.0 ns)

Symbol	Parameter	Guaranteed Limits				Unit
		25 °C		-40°C to 85°C		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay, Input A to Output Y (Figure 1)	1.5	10.5	1.5	11.5	ns
t_{PHL}	Propagation Delay, Input A to Output Y (Figure 1)	1.5	10.5	1.5	11.5	ns
t_{PLH}	Propagation Delay, CS2 or CS3 to Output Y (Figure 3)	2.5	11.5	2.0	12.5	ns
t_{PHL}	Propagation Delay, CS2 or CS3 to Output Y (Figure 3)	2.0	11.5	2.0	12.5	ns
t_{PLH}	Propagation Delay, CS1 to Output Y (Figure 2)	2.5	12.0	2.0	13.0	ns
t_{PHL}	Propagation Delay, CS1 to Output Y (Figure 2)	2.0	10.5	1.5	11.5	ns
C_{IN}	Maximum Input Capacitance	4.5		4.5		pF

		Typical @25°C,V_{CC}=5.0 V	
C_{PD}	Power Dissipation Capacitance	60	pF

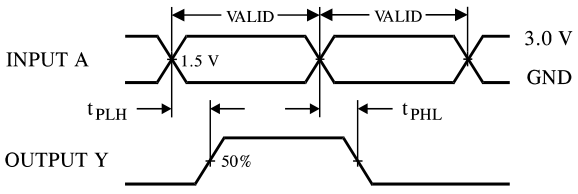


Figure 1. Switching Waveforms

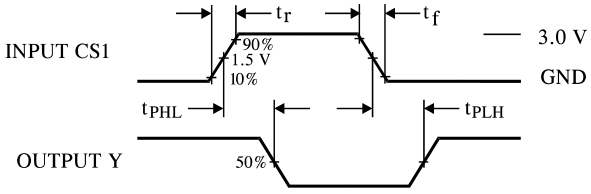


Figure 2. Switching Waveforms

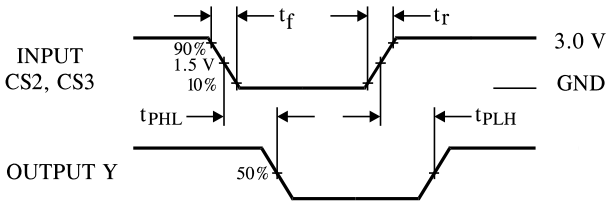


Figure 3. Switching Waveforms

INTEGRAL

EXPANDED LOGIC DIAGRAM

