# FAN5068

## DDR-1/DDR-2 plus ACPI Regulator Combo

### Features

- PWM regulator for VDDQ (2.5V or 1.8V)
- Linear LDO regulator generates VTT = VDDQ/2, 1.5A Peak sink/source capability
- 1 independent programable ULDO controllers driving external N-Channel MOSFET
- ACPI drive and control for 5V DUAL generation
- 3.3V Internal LDO for 3V-ALW generation
- 300kHz fixed frequency switching
- $R_{DS(ON)}$ current sensing or optional current sense resistor for precision over-current detect
- Internal Synchronous Boot diode
- Power Good signal for all voltages
- Input Under-Voltage Lock-Out (UVLO)
- Thermal Shutdown
- Latched Multi-Fault Protection
- 24-pin 5x5mm MLP package

### Applications

- DDR-1/DDR-2 VDDQ and VTT voltage generation with ACPI support
- Desktop PC's
- Servers

### General Description

The FAN5068 DDR memory regulator combines a high-efficiency PWM controller to generate the supply voltage, VDDQ, and a linear regulator to generate VTT, the termination voltage. Synchronous rectification provides high-efficiency over a wide range of load currents. Efficiency is further enhanced by using the low-side MOSFET's $R_{DS(ON)}$ to sense current instead of a series sense resistor.

In S3 mode, only the VDDQ switcher and the 3.3V regulators remain on while the VTT and ULDO regulators are shut off. To avoid "glitching" the VDDQ output during the transition from S3 to S0, the three linear regulators use the SS capacitor to limit their slew rates, thereby limiting the surge current from the VDDQ output. PGOOD becomes true in S0 only when all 3 regulators have achieved stable outputs.

In S5 (EN = 0), the 3.3V internal LDO stays on, while the other regulators are powered down.

The VDDQ PWM regulator is a sampled current mode control with external compensation to achieve fast load transient response and provide system design optimization.

The VTT regulator derives its reference and takes its power from the VDDQ PWM regulator output using a precision internal voltage divider to set its output at 1/2 of VDDQ. The VTT termination regulator is capable of sourcing or sinking at least 1.5A peak current.

## Block Diagrams

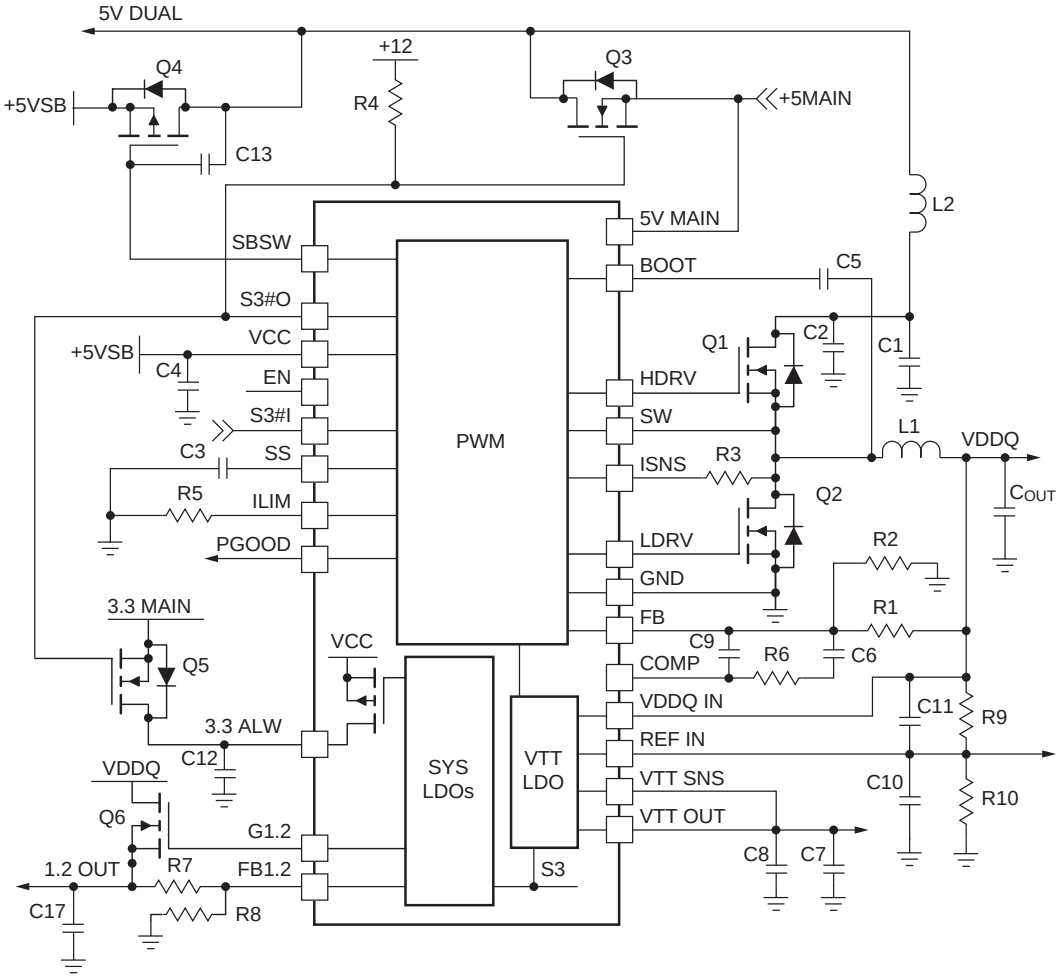



**Figure 1. DDR/ACPI System Regulation Schematic**

The components selected are for a 15A ouput on VDDQ.

**Table 1. BOM for Figure 1**

| Description | Qty | Ref. | Vendor | Part Number |
|---|---|---|---|---|
| See notes below | | COUT | | |
| See notes below | | C1, C12, C17 | | |
| Capacitor 1uF, 10%, 16VDC, X7R, 1206 | 2 | C2, C4 | KEMET | C1206C105K4RACTU |
| Capacitor 10nF, 10%, 100VDC, X7R, 0805 | 1 | C3 | Panasonic | ECJ-2VB2A103K |
| Capacitor 2.2nF, 10%, 50V, X7R, 0805 | 1 | C6 | AVX | 08055C222KAT2A |
| Capacitor 33pF, 10%, 50VDC, NPO, 0805 | 1 | C9 | Panasonic | ECJ-2VC1H330J |
| Capacitor 10nF, 10%, 100VDC, X7R, 0805 | 2 | C10, C11 | Panasonic | ECJ-2VB2A103K |
| Capacitor 220nF, 20%, 10VDC, X5R, 0603 | 1 | C5 | AVX | 06033D224MAT |
| Capacitor 100nF, 10%, 25VDC, X7R, 0805 | 1 | C8 | Kemet | C0805C104K3RACTU |
| Inductor 1.8uH, 3.24mΩ, 16 Amps, 20%, 0.5" | 1 | L1 | Inter-Technical | SC5018-1R8M |
| Inductor 0.39uH, 2.8mΩ, 15 Amps, 20%, 0.25" | 1 | L2 | Inter-Technical | SC7232-R39M |
| MOSFET N-CH, 8.8mΩ, 30V, 50A, D-PAK, FSID: FDD6296 | 1 | Q1 | Fairchild | FDD6296 |

**Table 1. BOM for Figure 1** (continued)

| Description | Qty | Ref. | Vendor | Part Number |
|---|---|---|---|---|
| MOSFET N-CH, 6mΩ, 30V, 75A, D-PAK, FSID: FDD6606 | 1 | Q2 | Fairchild | FDD6606 |
| MOSFET N-CH, 32mΩ, 20V, 21A, D-PAK, FSID: FDD6530A | 3 | Q3, Q6, Q5 | Fairchild | FDD6530A |
| MOSFET P-CH, 35mΩ, -20V, -5.5A, SSOT-6, FSID: FDC602P | 1 | Q4 | Fairchild | FDC602P |
| Resistor 1.82kΩ, 1%, 0805 | 4 | R1, R2, R9, R10 | Yageo | 9C08052A1821FKHFT |
| Resistor 56kΩ, 1%, 0805 | 1 | R5 | Any | |
| Resistor 60.4kΩ, 1%, 0805 | 1 | R6 | Any | |
| Resistor 3.01kΩ, 1%, 0603 | 1 | R7 | | |
| Resistor 9.09kΩ, 1%, 0603 | 1 | R8 | | |
| Resistor 10kΩ, 1%, 0805 | 1 | R4 | Any | |
| Resistor 1kΩ, 1%, 0805 | 1 | R3 | Any | |
| IC System Regulator, MLP 24-Pin 5X5mm | 1 | U2 | Fairchild | FAN5068 |

## Bypass Capacitor Notes:

Input capacitor C1 is typically chosen based on the ripple current requirements. COUT is typically selected based on both current ripple rating and ESR requirement. See AN-6006 for these calculations.

C17 and C12 selection will be largely determined by ESR and load transient response requirements. In each case, the number of capacitors required depends on the capacitor technology chosen. Oscons can meet the requirements with less space, but higher cost than using low ESR electrolytics (like Rubycon MBZ).

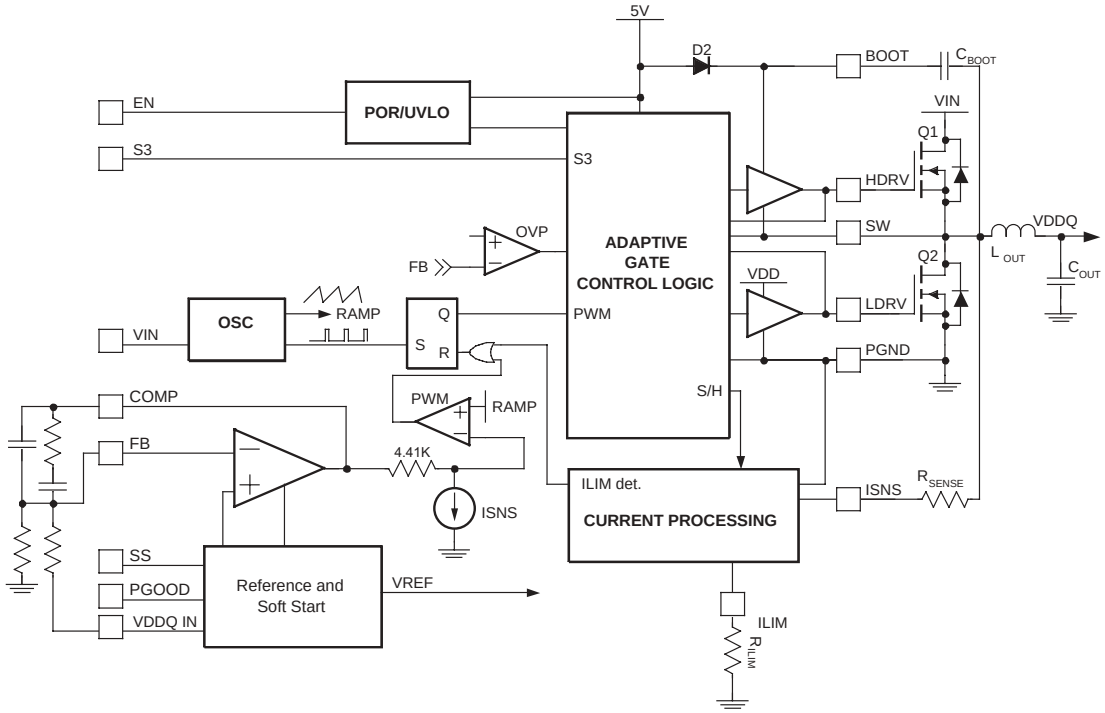



**Figure 2. PWM Modulator Block Diagram**

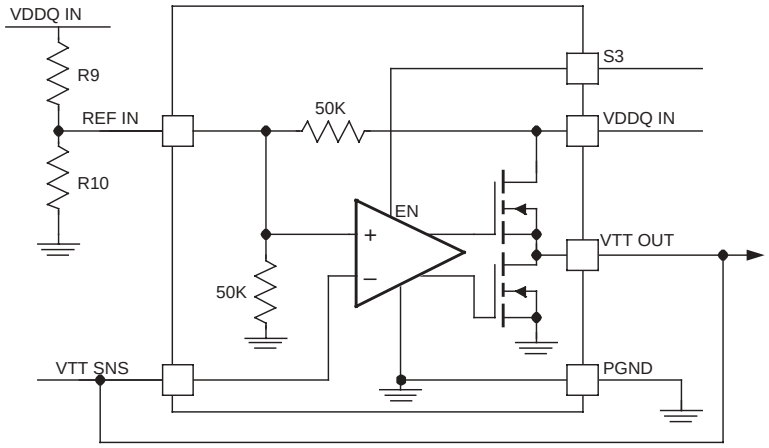
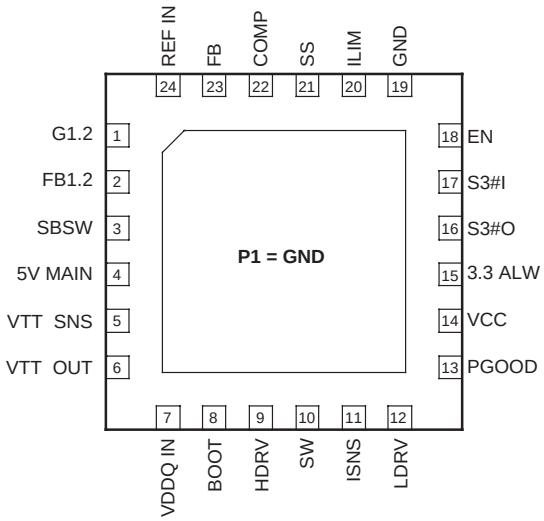



**Figure 3. VTT Regulator Block Diagram**

## Pin Configuration




**FAN5068MP 5x5 mm MLP-24 Package ($\theta_{JA}$ = 38°C/W, $\theta_{JC}$ = 1.4°C/W)***
Note: Connect P1 pad to GND.

## Pin Definitions

| Pin # | Pin Name | Pin Function Description |
|---|---|---|
| 1 | G1.2 | **Gate Drive for the 1.2V LDO**. Turned off (low) in S3 and S5 modes. |
| 2 | FB1.2 | **Feedback for the 1.2V LDO Output**. Tie to a voltage higher than 0.9V to disable this regulator. |
| 3 | SBSW | **Standby Switch**. Drives the P-Channel MOSFET to power 5V DUAL from 5VSB when in S3. Goes high in S0 and S5. |
| 4 | 5V MAIN | **5V MAIN**. When this pin is below 4.5V, transition from S3 to S0 is inhibited. |
| 5 | VTT SNS | **VTT Remote Sense Input**. |
| 6 | VTT OUT | **VTT Regulator Power Output**. |
| 7 | VDDQ IN | **VDDQ Input from PWM**. Connect to PWM output voltage. This is the VTT Regulator power input. |

*Test method as per JEDEC Specification JESD51-5

## Pin Definitions (continued)

| Pin # | Pin Name | Pin Function Description |
|---|---|---|
| 8 | BOOT | **Boot**. Positive supply for the upper MOSFET driver. Connect as shown in Figure 1. IC contains a boot diode to VCC. |
| 9 | HDRV | **High-Side Drive**. High-side (upper) MOSFET driver output. Connect to gate of high-side MOSFET. |
| 10 | SW | **Switching Node**. Return for the high-side MOSFET driver and a current sense input. Connect to source of high-side MOSFET and low-side MOSFET drain. |
| 11 | ISNS | **Current Sense Input**. Monitors the voltage drop across the lower MOSFET or external sense resistor for current feedback. |
| 12 | LDRV | **Low-Side Drive**. The low-side (lower) MOSFET driver output. Connect to gate of low-side MOSFET. |
| 13 | PGOOD | **Power Good Flag**. An open-drain output that will pull LOW when FB is outside of a ±10% range of the 0.9V reference and the LDO outputs are > 80% or < 110% of its reference. PGOOD goes low when S3 is high. The power good signal from the PWM regulator enables the VTT regulator and the LDO controller. |
| 14 | VCC | **VCC**. The IC takes its bias power from this pin. Also used for gate drive power. The IC is held in standby until this pin is above 4.35V (UVLO threshold). |
| 15 | 3.3 ALW | **3.3V LDO Output**. Internal LDO output. Turned off in S0, on in S5 or S3 modes. |
| 16 | S3#O | **S3# Output**. Open-drain output which pulls the gates of two N-Channel blocking MOSFETs low in S5 and S3. This pin goes high (open) in S0 mode. |
| 17 | S3#I | **S3 Input**. When LOW, turns off the VTT and 1.2V LDO regulators and turns on the 3.3V regulator. Also causes S3#O to pull low to turn off blocking switch Q3 as shown in Figure 1. PGOOD is low when S3#I is LOW. |
| 18 | EN | **ENABLE**. Typically tied to S5#. When this pin is low, the IC is in a low quiescent current state, all regulators are off and S3#O is low. |
| 19 | GND | **GROUND** for the IC are tied to this pin and also connected to P1. |
| 20 | ILIM | **Current Limit**. A resistor from this pin to GND sets the current limit. |
| 21 | SS | **Soft Start**. A capacitor from this pin to GND programs the slew rate of the converter during initialization as well as sets the initial slew rate of the LDO controllers when transitioning from S3 to S0. This pin is charged/discharged with a 5µA current source during initialization, and charged with 50µA during PWM soft-start. |
| 22 | COMP | **Output of the PWM error amplifier**. Connect compensation network between this pin and FB. |
| 23 | FB | **VDDQ Feedback**. The feedback from PWM output. Used for regulation as well as PGOOD, under-voltage, and over-voltage protection and monitoring. |
| 24 | REF IN | **VTT Reference**. Input which provides the reference for the VTT regulator. A precision internal divider from VDDQ IN is provided. |

## Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| VCC | | | 6.5 | V |
| BOOT, SW, ISNS, HDRV, S3#O | | | 28 | V |
| BOOT to SW | | | 6.5 | V |
| All Other Pins | –0.3 | | VCC+0.3 | V |
| Junction Temperature ($T_J$) | –20 | | 150 | °C |
| Storage Temperature | –65 | | 150 | °C |
| Lead Soldering Temperature, 10 seconds | | | 300 | °C |
| I(VTT) Peak (Duration < 2ms) | | | 1.5 | A |
| I(VTT) RMS | | | 1 | A |

## Recommended Operating Conditions

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Supply Voltage VCC | | 4.5 | 5 | 5.5 | V |
| I(3.3 ALW) | | | | 1.25 | A |
| Ambient Temperature ($T_A$) | | –10 | | 85 | °C |

## Electrical Specifications

Recommended operating conditions, component values per Figure 1 unless otherwise noted.

| Parameter | | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Power Supplies** | | | | | | |
| VCC Current: | S0 | LDRV, HDRV Open, FB forced above regulation point, I(VTT) = 0, EN = 1, S3#I = 1 | | 15 | 24 | mA |
| | S3 | EN = 1, S3#I = LOW, I(3.3) < 10mA | | 15 | 24 | mA |
| | S5 | EN = 0, I(3.3) = 0 | | 2 | 4 | mA |
| VCC UVLO Threshold | | Rising VCC | 4.0 | 4.2 | 4.4 | V |
| | | Falling | 3.9 | 4.05 | 4.2 | V |
| | | Hysteresis | | 0.150 | | V |
| 5V MAIN UVLO Threshold | | Rising | 4.3 | 4.4 | 4.6 | V |
| | | Falling | 3.9 | 4.1 | 4.2 | V |
| | | Hysteresis | | 0.300 | | V |
| **Oscillator** | | | | | | |
| Frequency | | | 255 | 300 | 345 | kHz |
| Ramp Amplitude, pk–pk | | | | 1.8 | | V |
| Ramp Offset | | | | 0.5 | | V |
| **Reference and Soft Start** | | | | | | |
| Internal Reference Voltage | | | 0.891 | 0.900 | 0.909 | V |
| Soft Start current ($I_{SS}$) | | Initial ramp after power-up | | 4.5 | | µA |
| | | During PWM / LDO soft start | | 48 | | |
| SS Discharge on-resistance | | EN = 0 | | 150 | | Ω |

## Electrical Specifications (continued)

Recommended operating conditions, component values per Figure 1 unless otherwise noted.

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| SS Complete Threshold | | | 1.5 | | V |
| SS Complete Hysteresis | | | 50 | | mV |
| **PWM Converter** | | | | | |
| Load Regulation | $I_{OUT}$ from 0 to 16A | –2 | | +2 | % |
| FB Bias Current | | 0.75 | 1 | 1.25 | µA |
| Under-Voltage Shutdown | As % of set point.<br>2µs noise filter | 65 | 75 | 80 | % |
| $I_{SNS}$ Over-Current threshold | $R_{ILIM}$ = 56kΩ | 145 | 170 | 195 | µA |
| Over-Voltage threshold | As % of set point | 110 | 115 | 120 | % |
| **PWM Output Driver** | | | | | |
| HDRV Output Resistance | Sourcing | | 1.8 | 3 | Ω |
| | Sinking | | 1.8 | 3 | Ω |
| LDRV Output Resistance | Sourcing | | 1.8 | 3 | Ω |
| | Sinking | | 1.2 | 2 | Ω |
| **PGOOD (Power Good Output) and Control pins. VDDQ output** | | | | | |
| Lower Threshold | As % of set point, 2µs noise filter | 86 | | 92 | % |
| Upper Threshold | As % of set point, 2µs noise filter | 108 | | 115 | % |
| PGOOD Output Low | $I_{PGOOD}$ = 1.5mA | | | 0.5 | V |
| Leakage Current | $V_{PULLUP}$ = 5V | | | 1 | µA |
| **VTT Regulator** | | | | | |
| VDDQ IN Current | S0 mode, $I_{VTT}$ = 0 | | 35 | 70 | mA |
| VREF IN to VTT Differential Output Voltage | $I_{VTT}$ = 0, $T_A$ = 25°C<br>$I_{VTT}$ = ± 1.25A (pulsed) | –20<br>–40 | | 20<br>40 | mV |
| Internal Divider Gain | | 0.493 | 0.498 | 0.503 | V/V |
| VTT Current limit | Pulsed (300ms max.), $T_A$ = 25°C | ±1.5 | ±3 | ±4 | A |
| VTT Leakage Current | S3#I = LOW | –20 | | 20 | mA |
| VTT SNS input resistance | VTT = 0.9V | | 110 | | kΩ |
| VTT PGOOD | Measured at VTT SNS | 80 | | 110 | % VTT REF |
| Drop-Out Voltage | ITT = ± 1.5A | –0.8 | | 0.8 | V |
| **1.2V LDO** | | | | | |
| Regulation | I(1.2) from 0 to 5A | 1.17 | 1.2 | 1.23 | V |
| Drop-Out Voltage | I(1.2) ≤ 5A, $R_{DS(ON)}$ < 50mΩ | | | 0.3 | V |
| External Gate Drive | VCC = 4.75V | | | 4.5 | V |
| Gate Drive Source Current | | | 1.2 | | mA |
| Gate Drive Sink Current | | | 1.2 | | mA |
| External Gate Drive | VCC = 4.75V | | | 4.5 | V |
| FB1.2 PGOOD threshold | | | | 0.80 | V |
| **3.3V LDO** | | | | | |
| Regulation | I(3.3) from 0 to 1.25A, VCC > 4.75V | 3.2 | 3.3 | 3.4 | V |
| Drop-Out Voltage | I(3.3) ≤ 1.25A | | | 1.5 | V |

## Electrical Specifications (continued)

Recommended operating conditions, component values per Figure 1 unless otherwise noted.

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **Control Functions** | | | | | |
| S3#I, EN Input Threshold | | 1.0 | 1.25 | 1.55 | V |
| S3#I EN Input Current | | –1 | | 1 | µA |
| Over-Temperature Shutdown | | | 150 | | °C |
| Over-Temperature Hysteresis | | | 25 | | °C |
| S3#O Output Low $R_{DS(ON)}$ | | | 170 | 300 | Ω |
| S3#O Output High Leakage | V(S3#O) = 12V | | 4 | 10 | µA |
| SBSW Output Low Resistance | 5V MAIN OK | | 125 | 200 | Ω |
| SBSW Sink current (note 1) | 5V MAIN < UVLO | | 500 | | nA |
| SBSW Output High (note 2) | | | 820 | 1200 | Ω |

# Circuit Description

## Overview

The FAN5068 provides 5 functions:

1. A general purpose PWM regulator, typically used to generate VDDQ for DDR memory.
2. A low-dropout linear VTT regulator capable of sinking and sourcing 1.5A peak.
3. An adjustable Ultra Low Drop Out (ULDO) controller which, in conjunction with an external N-Channel power MOSFET, provides a programmable low voltage output. The power source for this output is typically the VDDQ output and is used to provide the 1.2V GTL processor FSB termination voltage.
4. Control for generating a 5V DUAL voltage using an external N-channel to supply power from 5V MAIN in S0, and an external P-Channel to provide power from 5V Standby (5VSB) in S3.
5. An internal LDO which regulates "3.3V Always" in S3 mode from VCC(VSB). In S3, this regulator is capable of 1.25A peak currents with average currents limited by the thermal design of the PCB.

At initial power-up, or when transitioning from S5, the PWM regulator will be disabled until 5V MAIN is above its UVLO threshold.

**Table 2. ACPI States**

| STATE | S3#I | EN (S5#) | S3#O | SBSW | VDDQ | VTT | G1.2 LDO | 3.3 ALW LDO |
|---|---|---|---|---|---|---|---|---|
| **S5** | X | L | L | H | OFF | OFF | OFF | ON |
| **S3** | L | H | L | L | ON | OFF | OFF | ON |
| **S0** | H | H | H | H | ON | ON | ON | OFF |

| STATE | 3.3 ALW | 5V Dual |
|---|---|---|
| **S5** | LDO | OFF |
| **S3** | LDO | +5VSB |
| **S0** | Q5 (MAIN) | +5 MAIN |

## Regulator Sequencing

The VCC pin provides power to all logic and analog control functions of the regulator including:

1. Power for the 3.3V regulator
2. LDRV gate driver current
3. HDRV boot diode charging current.
4. The regulator analog control and logic

This pin must be decoupled with a ceramic capacitor (4.7µF or larger recommended) as close as possible to the VCC pin. After VCC is above UVLO, the start-up sequence begins as shown in Figure 6.

**T1 to T3:** After initial power-up, the IC will ignore all logic inputs for a time period (T3-T1) of about:

$$T3 - T1 = \frac{6.4 \times C_{SS}}{5} \quad (1)$$

where T3-T1 is in ms if $C_{SS}$ is in nF. At T2 (about 2/3 of the way from T1 to T3), the 3.3V-ALW LDO is in regulation. The 3.3V LDO's slew rate is limited by the discharge slope of CSS. If 3.3V MAIN has come up prior to this time, the 3.3V-ALW node will already be pre-charged through the body diode of Q5 (see Figure 1).

**T3 to T4:** The IC will start VDDQ only if 5V MAIN is above its UVLO threshold (5V MAIN OK). Provided 5V MAIN is up before T3, the IC waits about 100µs before initiating soft-start on VDDQ to allow CSS time to fully discharge. The IC is in "SLEEP" or S5 state when EN is low. In S5, only the 3.3V LDO is on. If the IC is in S5 at T4, CSS will be held to 0V.

**T4 to T5:** After VDDQ is stablized (when CSS is at about 1.3V) an internal VDDQ OK is generated which will allow the 1.2V LDO and the VTT LDO to start. To ensure that the VDDQ output is not subjected to large transient currents during S3 to S0 transition, the VTT and 1.2V LDO slew rates are limited by the slew rate of the SS cap until the LDO is in regulation. In addition, the VTT regulator is current limited. After VDDQ OK becomes true, CSS will be held to 1.2V until S3#I goes high.

**S0 to S3:** The system signals this transition by dropping the S3#I signal. When this occurs, S3#O goes low, and the 3.3V LDO turns on. The 1.2V LDO and the VTT LDO are turned off, and CSS is discharged to 2V. SBSW pulls low to turn on the P-Channel 5V DUAL switch.

**S3 to S0:** The system signals this transition by raising the S3#I signal. S0 mode is not entered until 5V MAIN OK. Then the following occurs:

S3#O releases
SBSW pulls high to turn off the P-Channel switch
The 3.3V LDO turns off
The 1.2V LDO and the VTT LDO are turned on and, and CSS is allowed to charge up

In most systems, the ATX power supply is enabled when S3#I goes from high. At that point, 5V and 3.3V MAIN will start to rise. The FAN5068 waits until 5V MAIN is above 4.5V to turn on Q3 and Q5. This can cause about a 10% "bump" in both 5V DUAL and 3.3V ALW when Q3 and Q5 turn on, since at that point, 5V MAIN and 3.3V MAIN are at 90% of their regulation value.

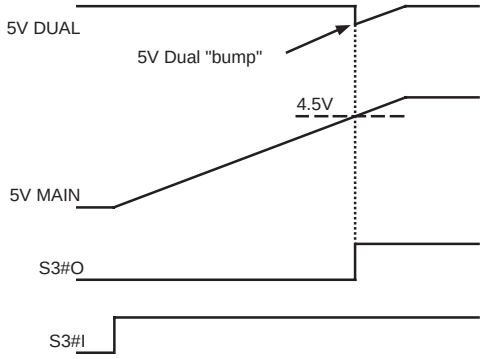



**Figure 4. S3 to S0 Transition: 5V DUAL**

To eliminate the "bump", add delay to the 5V MAIN pin as shown below. The 5V MAIN pin on the FAN5068 does not supply power to the IC, it is only used to monitor the voltage level of the 5V MAIN supply, and therefore is a high impedance input.

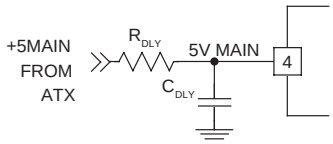



**Figure 5. Adding Delay to 5V MAIN**

Another method to eliminate the potential for this "bump" is to use the PWR_OK to drive the 5V MAIN pin. Some systems cannot tolerate the long delay for PWR_OK (>100ms) to assert, hence the solution in figure 5 may be preferrable.

**S5 to S3:** During S5 to S3 transition, the IC will pull SBSW low with a 500nA current sink to limit inrush in Q4 if 5V MAIN is below its UVLO threshold. At that time, 5V DUAL is discharged. The limited gate drive controls the inrush current through Q4 as it charges C1 (capacitance on 5V Dual). Depending on the $C_{GD}$ of Q4, the current available from 5VSB, and the size of C1, C13 may be omitted.

$$I_{Q4(INRUSH)} = \frac{C1 \bullet 5 \times 10^{-7}}{C13 + C_{GD(Q4)}} \quad (2)$$

If 5V MAIN is above its UVLO threshold, SBSW will be pulled down with an impedance of about 2K. VDDQ will not start until 5V MAIN OK is true.

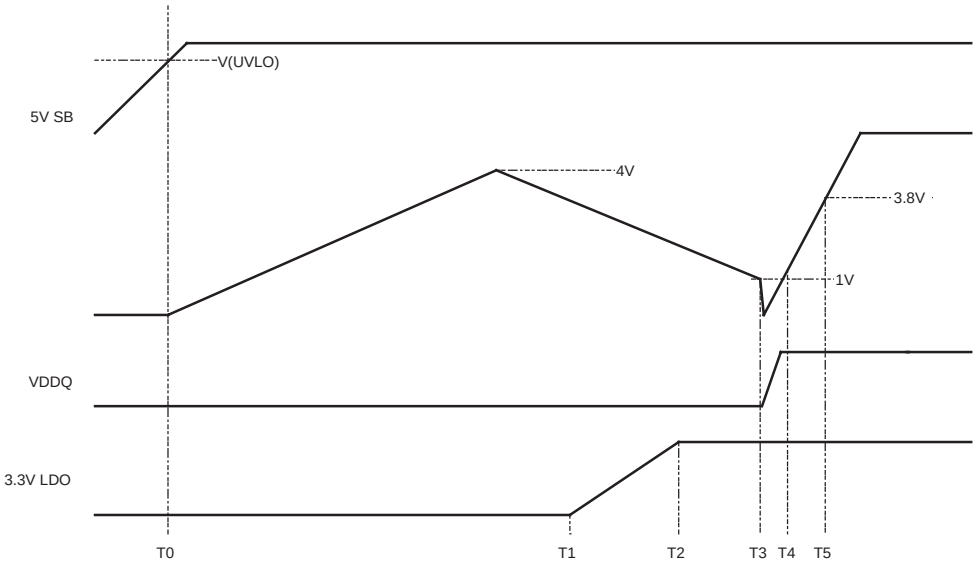



**Figure 6. Start-up Sequence into S0.**

## PWM Regulator

A PSPICE model and spreadsheet calculator are available for the VDDQ PWM regulator to select external components and verify loop stability. The topics covered below provide the explanation behind the calculations in the spreadsheet.

### Setting the output voltage

The output voltage of the PWM regulator can be set in the range of 0.9V to 90% of its power input by an external resistor divider.

The internal reference is 0.9V. The output is divided down by an external voltage divider to the FB pin (for example, R1 and R2 in Figure 1). There is also a 1µA precision (±5%) current sourced out of FB to ensure that if the pin is open, VDDQ will remain low. The output voltage therefore is:

$$\frac{0.9V}{R2} = \frac{V_{OUT} - 0.9V}{R1} + 1\mu A \quad (3a)$$

To minimize noise pickup on this node, keep the resistor to GND (R2) below 2k. We selected R2 at 1.82k and solved for R1.

$$R1 = \frac{R2 \bullet (V_{OUT} - 0.9)}{0.9 - 1\mu A} = 1.816k \approx 1.82k \quad (3b)$$

The synchronous buck converter is optimized for 5V operation. The PWM modulator uses an average current mode control for simplified feedback loop compensation.

### Oscillator

The oscillator frequency is 300kHz. The internal PWM ramp is reset on the rising clock edge.

### PWM Soft Start

When the PWM regulator is enabled the circuit will wait until the VDDQ IN pin is below 100mV to ensure that the soft-start cycle does not begin with a large residual voltage on the PWM regulator output.

When the PWM regulator is disabled, 50Ω is turned on from VDDQ IN to PGND to discharge the output.

The voltage at the positive input of the error amplifier is limited to $V_{CSS}$ which is charged with a 50µA current source. Once CSS has charged to 0.9V, the output voltage will be in regulation.

The time it takes SS to reach 0.9V is:

$$T_{0.9} = \frac{0.9 \times C_{SS}}{50} \quad (4)$$

where $T_{0.9}$ is in ms if $C_{SS}$ is in nF.

CSS charges another 400mV before the PWM regulator's latched faults are enabled. When CSS reaches 2.5V, the VTT and 1.2V LDO will begin their soft-start ramps. After the VTT and 1.2V LDO regulators are in regulation, PGOOD is then allowed to go HIGH (open). UVLO on VCC will discharge SS and reset the IC.

To prevent large duty cycles and high currents during the beginning of the PWM soft-start, the input to the PWM comparator is also clamped by CSS. This clamping action has no practical effect on operation of the circuit after CSS has passed about 0.4V.

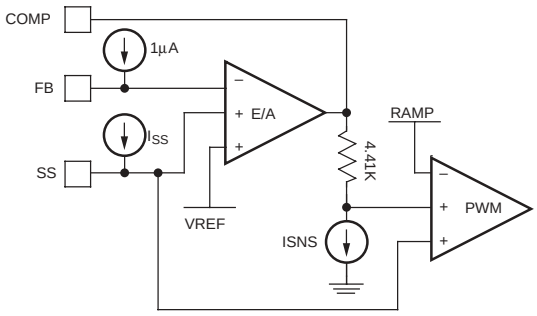



**Figure 7. SS Clamp and FB Open Protection**

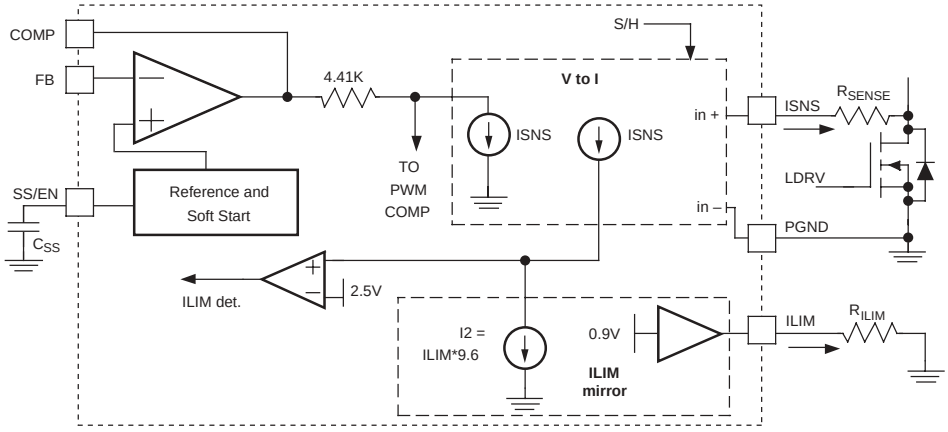



**Figure 8. Current Limit / Summing Circuits**

## Current Processing Section

The following discussion refers to Figure 8.

The current through $R_{SENSE}$ resistor (ISNS) is sampled shortly after Q2 is turned on. That current is held, and summed with the output of the error amplifier. This effectively creates a current mode control loop. $R_{SENSE}$ sets the gain in the current feedback loop. For stable operation, the voltage induced by the current feedback at the PWM comparator input should be set to 30% of the ramp amplitude at maximum load currrent and line voltage. The following expression estimates the recommended value of $R_{SENSE}$ as a function of the maximum load current ($I_{LOAD(MAX)}$) and the value of the MOSFET's $R_{DS(ON)}$.:

$$R_{SENSE} = \frac{I_{LOAD(MAX)} \bullet R_{DS(ON)} \bullet 4.1k}{30\% \bullet 0.125 \bullet V_{IN(MAX)}} - 100 \qquad (5)$$

RSENSE must, however, be kept higher than:

$$R_{SENSE(MIN)} = \frac{I_{LOAD(MAX)} \bullet R_{DS(ON)}}{150\mu A} - 100 \qquad (6)$$

## Setting the Current Limit

An ISNS is compared to the current established when a 0.9 V internal reference drives the ILIM pin. $R_{ILIM}$, the $R_{DS(ON)}$ of Q2, and $R_{SENSE}$ determine the current limit:

$$R_{ILIM} = \frac{9.6}{I_{LIMIT}} \times \frac{(100 + R_{SENSE})}{R_{DS(ON)}} \qquad (7)$$

Where ILIMIT is the peak inductor current. Since the tolerance on the current limit is largely dependent on the ratio of the external resistors it is fairly accurate if the voltage drop on the Switching Node side of $R_{SENSE}$ is an accurate representation of the load current. When using the MOSFET as the sensing element, the variation of $R_{DS(ON)}$ causes proportional variation in the ISNS. This value not only varies from device to device, but also has a typical junction temperature coefficient of about 0.4%/°C (consult the MOSFET datasheet for actual values), so the actual current limit set point will decrease propotional to increasing MOSFET die temperature. A factor of 1.6 in the current limit setpoint should compensate for all MOSFET $R_{DS(ON)}$ variations, assuming the MOSFET's heat sinking will keep its operating die temperature below 125°C.

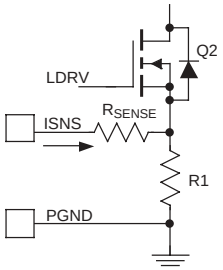



**Figure 9. Improving Current Sensing Accuracy**

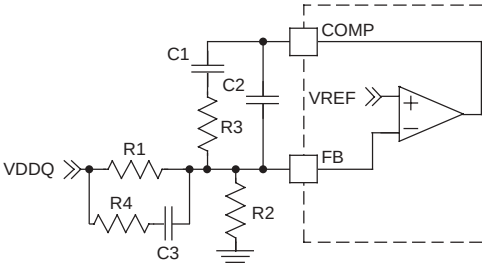



**Figure 10. Compensation Network**

More accurate sensing can be achieved by using a resistor (R1) instead of the $R_{DS(ON)}$ of the FET as shown in Figure 9. This approach causes higher losses, but yields greater accuracy. R1 is a low value (e.g. 10mΩ) resistor.

Current limit ($I_{LIMIT}$) should be set sufficiently high as to allow inductor current to rise in response to an output load transient. Typically, a factor of 1.3 is sufficient. In addition, since $I_{LIMIT}$ is a peak current cut-off value, we will need to multiply $I_{LOAD(MAX)}$ by the inductor ripple current (we'll use 20%).

$$I_{LIMIT} > I_{LOAD(MAX)} * 1.6 * 1.3 * 1.2 \quad (8)$$

## Gate Driver Section

The Adaptive gate control logic translates the internal PWM control signal into the MOSFET gate drive signals providing necessary amplification, level shifting and shoot-through protection. Also, it has functions that help optimize the IC performance over a wide range of operating conditions. Since MOSFET switching time can vary dramatically from type to type and with the input voltage, the gate control logic provides adaptive dead time by monitoring the gate-to-source voltages of both upper and lower MOSFETs. The lower MOSFET drive is not turned on until the gate-to-source voltage of the upper MOSFET has decreased to less than approximately 1 volt. Similarly, the upper MOSFET is not turned on until the gate-to-source voltage of the lower MOSFET has decreased to less than approximately 1 volt. This allows a wide variety of upper and lower MOSFETs to be used without a concern for simultaneous conduction, or shoot-through.

There must be a low-resistance, low-inductance path between the driver pin and the MOSFET gate for the adaptive dead-time circuit to work properly. Any delay along that path will subtract from the delay generated by the adaptive dead-time circit and shoot-through may occur.

## Frequency Loop Compensation

The loop is compensated using a feedback network around the error amplifier, which is a voltage output op amp.

Figure 10 shows a complete type 3 compensation network. A type 2 compensation configuration eliminates R4 and C3 and is shown in Figure 1. Since the FAN5068 architecture employs summing current mode, type 2 compensation can be used for most applications. For critical applications that require wide loop-bandwidth, and use very low ESR output capacitors, type 3 compensation may be required. The PSPICE model and spreadsheet calculator can be used to calculate these component values.

## PGOOD Signal

PGOOD monitors the status of the PWM output as well as the VTT and 1.2V LDO regulators. PGOOD remains low unless all of the conditions below are met:

1. S3#I is HIGH
2. SS is above 4V
3. Fault latch is cleared
4. FB is between 90% and 110% of VREF
5. VTT and LDO 1.2 are in regulation

## Protection

The converter output is monitored and protected against extreme overload, short circuit, over-voltage and under-voltage conditions.

An internal “Fault Latch” is set for any fault intended to shut down the IC. When the “Fault Latch” is set, the IC will discharge VOUT by driving LDRV high until VDDQ IN < 0.5V. LDRV will then go low until VDDQ IN > 0.8V. This behavior will discharge the output without causing undershoot (negative output voltage).

To discharge the output capacitors, a 50Ω load resistor is switched in from VDDQ IN to PGND whenever the IC is in fault condition, or when EN is low. After a latched fault, operation can be restored by recycling power or by toggling the EN pin.

## Under-Voltage Shutdown

If FB stays below the under-voltage threshold for 2µs, the “Fault latch” is set. This fault is prevented from setting the fault latch during PWM soft-start (SS < 1.3V).

### Over-Current Sensing

If the circuit's current limit signal (“ILIM det” as shown in Figure 8) is high at the beginning of a clock cycle, a pulse-skipping circuit is activated and HDRV is inhibited. The circuit continues to pulse skip in this manner for the next 8 clock cycles. If at any time from the 9$^{th}$ to the 16$^{th}$ clock cycle, the “ILIM det” is again reached, the fault latch is set. If “ILIM det” does not occur between cycle 9 and 16, normal operation is restored and the over-current circuit resets itself.

This fault is prevented from setting the fault latch during soft-start (SS < 1.3V).

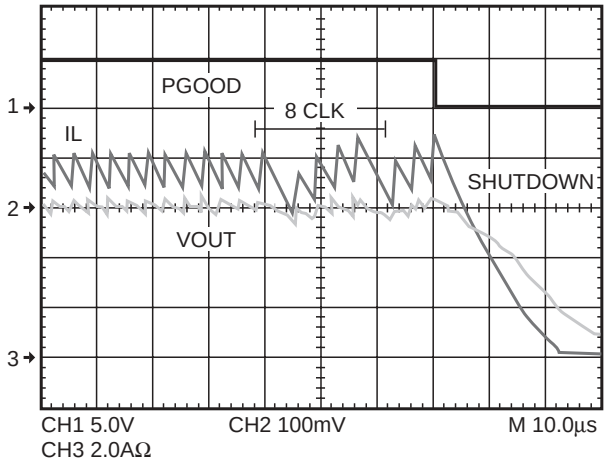



**Figure 11. Over-Current Protection Waveforms**

### OVP / HS Fault / FB short to GND detection:

A **HS Fault** is detected when there is more than 0.5V from SW to PGND 350ns after LDRV reaches 4V (same time as the current sampling time).

**OVP Fault Detection** occurs if FB > 115% VREF for 16 clock cycles.

During soft-start, the output voltage could potentially “run away” if either the FB pin is shorted to GND or R1 is open. This fault will be detected if the following condition persists for more than 14 µs during soft-start.

1. VDDQ IN (PWM output voltage) > 1V and
2. FB < 100mV

Any of these 3 faults will set the fault latch. These 3 faults can set the fault latch during the SS time (SS < 1.3V).

To ensure that FB pin open will not cause a destructive condition, a 1µA current source ensures that the FB pin will be high if open. This will cause the regulator to keep the output low, and eventually result in an Under-voltage fault shutdown (after PWM SS complete).

### Over-Temperature Protection

The chip incorporates an over temperature protection circuit that shuts the chip down when a die temperature of about 160°C is reached. Normal operation is restored at when the die temperature falls below 125°C with internal Power On Reset asserted, resulting in a full soft-start cycle. To accomplish this, the over-temperature comparator should discharge the SS pin.

## VTT Regulator Section (Figure 3)

The VTT regulator includes an internal resistor divider (50k for each resistor) from the output of the PWM regulator. If the REF IN pin is left open, the divider will produce a voltage that is 50% of VDDQ IN.

The VTT regulator is enabled when S3#I is HIGH and the PWM regulator’s internal PGOOD signal is true. The VTT regulator also includes its own PGOOD signal which is high when VTT SNS > 90% of REF IN.

## LDO Controller

The LDO controller is typically used to provide 1.2V for the Front-side bus GTL termination. Drop-out voltage for this regulator will depend on the RDS(ON) of the external N-Channel MOSFET pass element that is selected. Gate drive comes from VCC and can pull up to within 0.5V of VCC line. With 1.2V output, the enhancement voltage for the MOSFET is: VENH = 4.75 - 0.5 - 1.2 = 3.05V. Therefore, a low enhancement voltage MOSFET should be used for the pass element.

The LDO controller contains a soft-start circuit which limits its output slew rate when it powers up. The LDO's output voltage ($V_{1.2}$) is established with the following equation (reference designators are from Figure 1.):

$$V_{1.2} = 0.9 \times \left(1 + \frac{R7}{R8}\right) \quad (9)$$

## Design and Component Selection Guidelines

The spreadsheet calculator, which is part of AN-6006 can be used to calculate all external component values for the FAN5068. As an initial step, define:

1. Output voltage
2. Maximum VDDQ load current
3. Maximum load transient current and maximum allowable output drop during load transient
4. RDS(ON) of the low-side MOSFET (Q2)
5. Maximum allowable output ripple

## Power MOSFET Selection

For a complete treatment of MOSFET selection and efficiency calculations, see:

AN-6005: *Synchronous buck MOSFET loss calculations with Excel model.*

Losses in a MOSFET are the sum of its switching ($P_{SW}$) and conduction ($P_{COND}$) losses.

In typical applications, the FAN5068 converter's output voltage is low with respect to its input voltage, therefore the Lower MOSFET (Q2) is conducting the full load current for most of the cycle. Q2 should be therefore be selected to minimize conduction losses, thereby selecting a MOSFET with low $R_{DS(ON)}$.

In contrast, the high-side MOSFET (Q1) has a much shorter duty cycle, and its conduction loss will therefore have less of an impact. Q1, however, sees most of the switching losses, so Q1's primary selection criteria should be gate charge.

## High-Side Losses:

Figure 12 shows a MOSFET's switching interval, with the upper graph being the voltage and current on the Drain to Source and the lower graph detailing $V_{GS}$ vs. time with a constant current charging the gate. The x-axis therefore is also representative of gate charge ($Q_G$). $C_{ISS} = C_{GD} + C_{GS}$, and it controls t1, t2, and t4 timing. $C_{GD}$ receives the current from the gate driver during t3 (as $V_{DS}$ is falling). The gate charge ($Q_G$) parameters on the lower graph are either specified or can be derived from MOSFET datasheets.

Assuming switching losses are about the same for both the rising edge and falling edge, Q1's switching losses, occur during the shaded time when the MOSFET has voltage across it and current through it.

These losses are given by:

$$P_{UPPER} = P_{SW} + P_{COND}$$

$$P_{SW} = \left(\frac{V_{DS} \times I_L}{2} \times 2 \times t_S\right) F_{SW} \quad (10a)$$

$$P_{COND} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT}^{\ 2} \times R_{DS(ON)} \quad (10b)$$

where:

$P_{UPPER}$ is the upper MOSFET's total losses, and $P_{SW}$ and $P_{COND}$ are the switching and conduction losses for a given MOSFET. $R_{DS(ON)}$ is at the maximum junction temperature ($T_J$). $t_S$ is the switching period (rise or fall time) and is t2+t3 (Figure 12).

The driver's impedance and $C_{ISS}$ determine t2 while t3's period is controlled by the driver's impedance and $Q_{GD}$. Since most of $t_S$ occurs when $V_{GS} = V_{SP}$ we can use a constant current assumption for the driver to simplify the calculation of $t_S$:

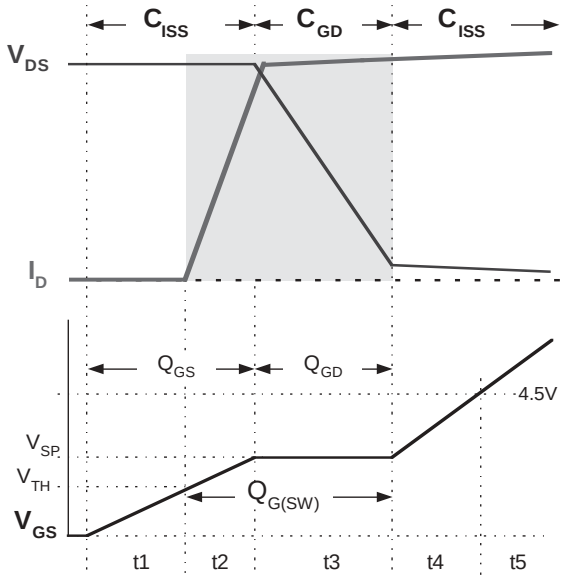



**Figure 12. Switching Losses and QG**

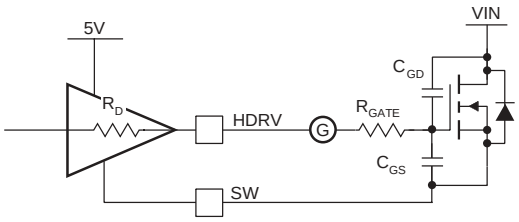



**Figure 13. Drive Equivalent Circuit**

$$t_S = \frac{Q_{G(SW)}}{I_{DRIVER}} \approx \frac{Q_{G(SW)}}{\left(\frac{VCC - V_{SP}}{R_{DRIVER} + R_{GATE}}\right)} \quad (11)$$

Most MOSFET vendors specify $Q_{GD}$ and $Q_{GS}$. $Q_{G(SW)}$ can be determined as: $Q_{G(SW)} = Q_{GD} + Q_{GS} - Q_{TH}$ where $Q_{TH}$ is the gate charge required to get the MOSFET to it's threshold ($V_{TH}$). For the high-side MOSFET, $V_{DS}$ = VIN, which can be as high as 20V in a typical portable application. Care should also be taken to include the delivery of the MOSFET's gate power ($P_{GATE}$) in calculating the power dissipation required for the FAN5068:

$$P_{GATE} = Q_G \times VCC \times F_{SW} \quad (12)$$

where $Q_G$ is the total gate charge to reach VCC.

### Low-Side Losses

Q2, however, switches on or off with its parallel shottky diode conducting, therefore $V_{DS} \approx 0.5V$. Since $P_{SW}$ is proportional to $V_{DS}$, Q2's switching losses are negligible and we can select Q2 based on $R_{DS(ON)}$ only.

Conduction losses for Q2 are given by:

$$P_{COND} = (1 - D) \times I_{OUT}^{2} \times R_{DS(ON)} \quad (13)$$

where $R_{DS(ON)}$ is the $R_{DS(ON)}$ of the MOSFET at the highest operating junction temperature and

$$D = \frac{V_{OUT}}{V_{IN}}$$

is the minimum duty cycle for the converter. Since $D_{MIN} <$ 20% for portable computers, (1-D) ≈ 1 produces a conservative result, further simplifying the calculation.

The maximum power dissipation ($P_{D(MAX)}$) is a function of the maximum allowable die temperature of the low-side MOSFET, the $\theta_{J\text{-}A}$, and the maximum allowable ambient temperature rise:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{J-A}} \quad (14)$$

$\theta_{J\text{-}A}$, depends primarily on the amount of PCB area that can be devoted to heat sinking (see FSC app note AN-1029 for SO-8 MOSFET thermal information).

## PCB Design Guidelines:

Below is a summary of recommendations for PCB layout when using MLP packages:

1. PCB lead finger pad should be designed 0.2-0.5mm longer than the package terminal length for good filleting.
2. Non Solder Mask Defined (NSMD) pads are recommended over SMD pads due to the tighter tolerance on copper etching than solder masking.
3. For Good thermal performance it is recommended to use 4 layer PCB's with vias to effectively remove heat from the device.
4. For a 5X5 die size, it is recommended to use 0.3-0.33mm size holes in the middle.
5. Vias should be plugged to prevent voids being formed between the exposed pad and PCB thermal pad due to solder escaping by the capillary effect. This can be avoided by tenting the via during the solder mask process. The via solder mask diameter should be 100µm larger than the via hole diameter.

### PCB Layout General Guidelines

Switching converters, even during normal operation, produce short pulses of current which could cause substantial ringing and be a source of EMI if layout constrains are not observed.

There are two sets of critical components in a DC-DC converter. The switching power components process large amounts of energy at high rate and are noise generators. The low power components responsible for bias and feedback functions are sensitive to noise.

A multi-layer printed circuit board is recommended. Dedicate one solid layer for a ground plane. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels.

Notice all the nodes that are subjected to high dV/dt voltage swing such as SW, HDRV and LDRV, for example. All surrounding circuitry will tend to couple the signals from these nodes through stray capacitance. Do not oversize copper traces connected to these nodes. Do not place traces connected to the feedback components adjacent to these traces.

Keep the wiring traces from the IC to the MOSFET gate and source as short as possible and capable of handling peak currents of 2A. Minimize the area within the gate-source path to reduce stray inductance and eliminate parasitic ringing at the gate.

Locate small critical components like the soft-start capacitor and current sense resistors as close as possible to the respective pins of the IC.

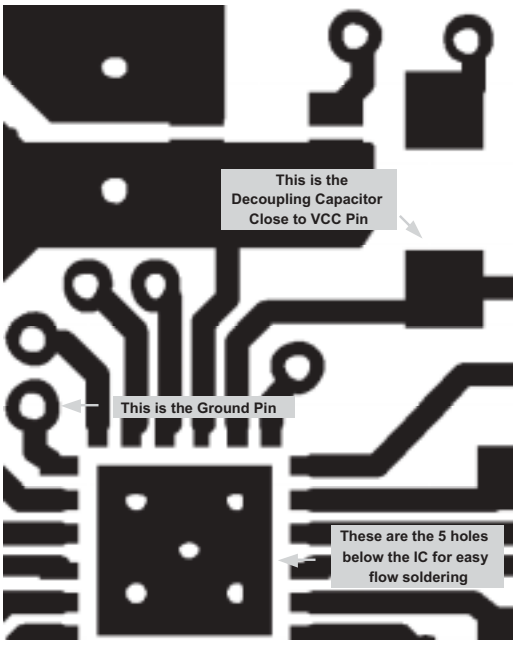
### Specific Layout recommendations

All component designators reference Figure 1. Layout examples refer to the FAN5068 EVAL board, available through your Fairchild Semiconductor representative.

1. All currents flow in a closed path. All routing should ensure that the currents are returned to their source of origin by the shortest possible path without creating unnecessary loops.
2. A Multi layer (4 layers or more) PCB facilitates the use of a complete Ground layer which acts as very low impedance return path for both the control and power return currents. This ground plane will also increase the noise immunity of the control circuit by providing a shield against radiated disturbances. In the Eval board layout Layer 2 is reserved for the GND plane.
3. VCC of the controller should be de-coupled with a ceramic capacitor (C4) very close to the pin. If it is possible, the capacitor could be connected across the VCC (#14) and the GND (#19) pins on top copper. Pin 19 should also connect to the GND plane with a via at the pin. If a short top-copper connection for C4 is not possible the capacitor should be close to the VCC pin with

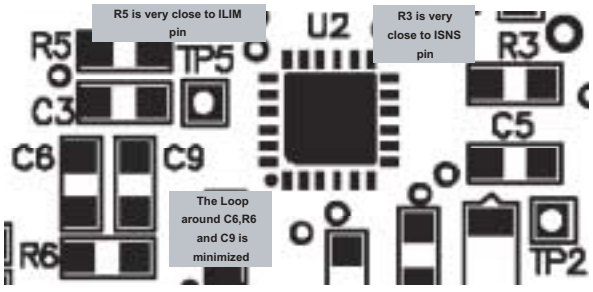
the other side connected to the ground plane through a via. If there is a significant amount of noise on VCC pin, L-C decoupling at the VCC pin can be used to attenuate the noise.

4. The pad under the IC is for power ground return. This pad needs to be directly connected to the ground plane by vias under the IC as mentioned above. Do not connect this pad to Pin #19 through the top copper, as this is the analog ground at the IC.

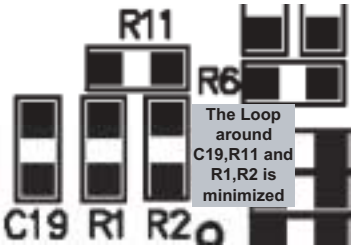



5. Use copper planes for power and GND wherever possible to reduce trace resistance and inductance as well.

6. Resistors should be as close to the IC pins as possible to prevent noise pickup due to radiated and adjacent high dV/dT signals. Avoid routing sense signals near the gate drive, SW node, boot, or other high dV/dT nodes. Particular care should be taken to place R3 (ISNS resistor) as close as possible to pin 11



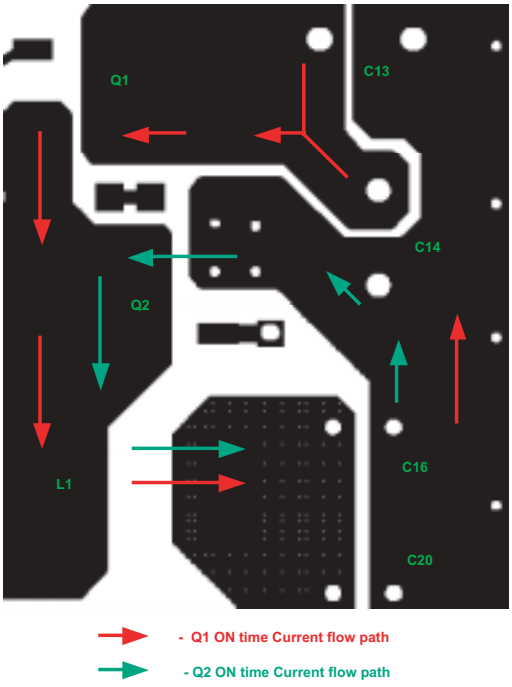

7. The closed path (loop) around the feedback components should be minimized to avoid noise pickup. These components will need to be close to the feedback pin. R2, R10 and C10 should be returned to pin 19 or to the GND plane as close to pin 19 as possible and away from other current on the GND plane.



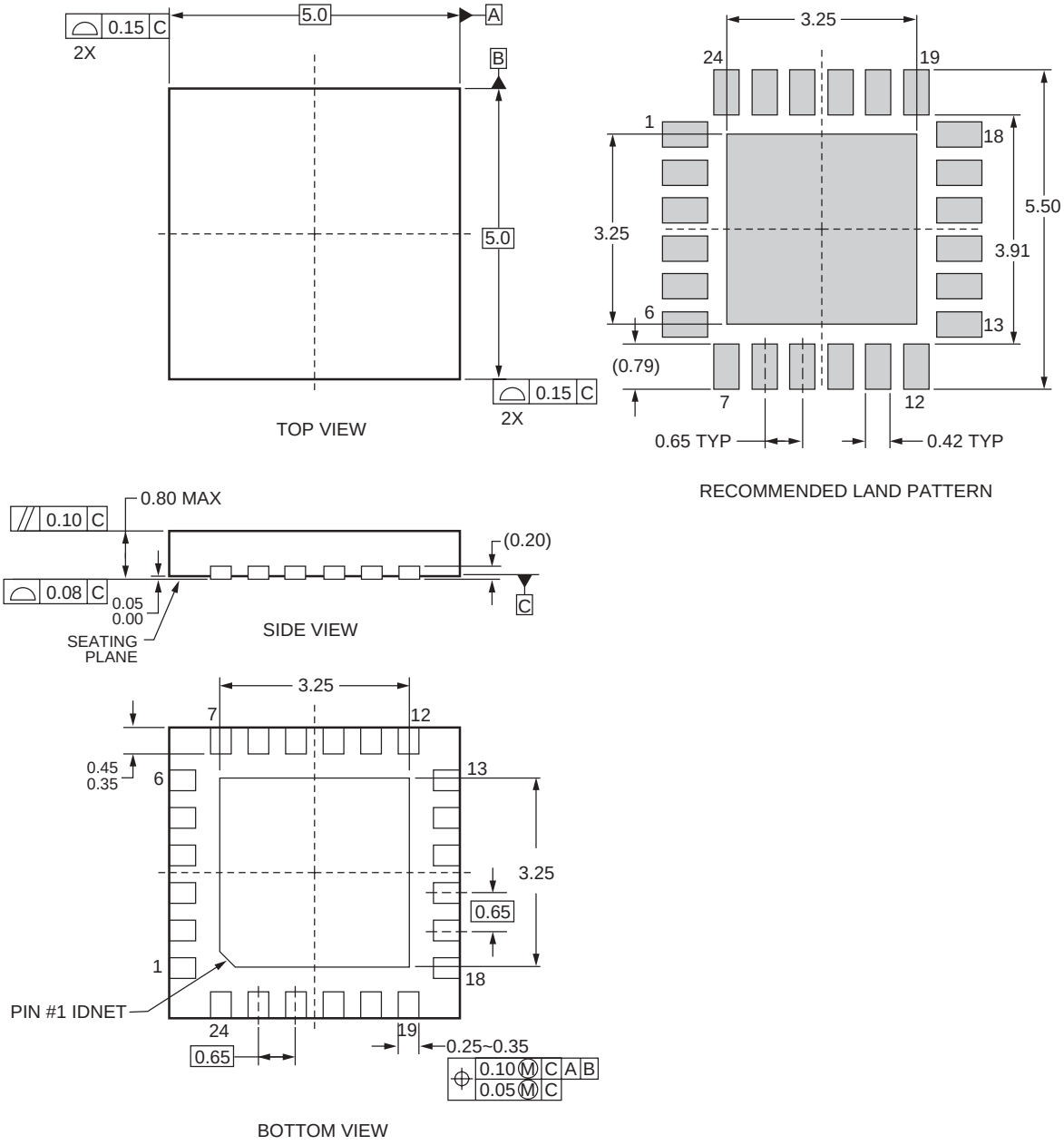

8. Minimize the path length for the boot cap formed by SW, C5 and pin 8.

9. Use thick trace widths for Q1 and Q2 gate drive signals to minimize their resistance and inductances. Top copper should be used to route the gate drive traces if possible, especially Q1 Gate to HDRV.

10. Power Plane Routing: The Power Plane routing for traces carrying higher currents as in the VDDQ output, need to be routed carefully. The loop from C2 (5V Dual high frequency bypass cap) to the source of Q2 needs to be minimized to minimize ringing on SW and Q1 drain. The loop formed by COUT to the source of the Q2 also needs to be minimized to keep the ringing on the switch node low. Basically what we are trying to achieve by doing this is to reduce the loop inductance and thereby minimizing the energy in the stray inductance.



# Dimensional Outline Drawing




Notes:
A) Conforms to JEDEC registration number MO-220, variation WHHC, dated Aug/2002.
B) Dimensions are in millimeters.
C) Dimensions and tolerances per asme Y14.5-1994.

## Ordering Information

| Part Number | Temperature Range | Package | Packing |
|---|---|---|---|
| FAN5068MPX | -10°C to 85°C | MLP-24 5x5 mm | Tape and Reel |

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.


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