Single-Ended, Analog-Input 24-Bit, 96-kHz Stereo A/D Converter

FEATURES

- **24-Bit Delta-Sigma Stereo A/D Converter**
- **Single-Ended Voltage Input: 3 Vp-p**
- **Oversampling Decimation Filter:**
  - **Oversampling Frequency: ×64**
  - **Pass-Band Ripple: ±0.05 dB**
  - **Stop-Band Attenuation: –65 dB**
  - **On-Chip High-Pass Filter: 0.91 Hz (48 kHz)**
- **High Performance:**
  - **THD+N: –93 dB (Typical)**
  - **SNR: 99 dB (Typical)**
  - **Dynamic Range: 99 dB (Typical)**
- **PCM Audio Interface With SPI Control:**
  - **Master/Slave Mode Selectable**
  - **Data Formats: 24-Bit Left-Justified, 24-Bit I^2S**
- **Multiple Functions with SPI Control:**
  - **Power Down**
  - **Mute with Fade-Out and Fade-In**
  - **Polarity Control**
- **Analog Antialias LPF Included**
- **Sampling Rate: 16–96 kHz**
- **System Clock: 256 f_S, 384 f_S, 512 f_S**
- **Dual Power Supplies:**
  - **5-V for Analog**
  - **3.3-V for Digital**
- **Package: 14-Pin TSSOP**

APPLICATIONS

- **DVD Recorder**
- **Digital TV**
- **AV Amplifier/Receiver**
- **MD Player**
- **CD Recorder**
- **Multitrack Receiver**
- **Electric Musical Instrument**

DESCRIPTION

The PCM1807 is high-performance, low-cost, single-chip stereo analog-to-digital converter with single-ended analog voltage input. The PCM1807 uses a delta-sigma modulator with 64-times oversampling and includes a digital decimation filter and high-pass filter that removes the dc component of the input signal. For various applications, the PCM1807 supports master and slave mode and two data formats in serial audio interface.

The PCM1807 has many functions which are controlled through SPI serial-control port: power down, fade-in and fade-out, polarity control, etc.

The PCM1807 is suitable for wide variety of cost-sensitive consumer applications where good performance and operation with a 5-V analog supply and 3.3-V digital supply is required. The PCM1807 is fabricated using a highly advanced CMOS process and is available in a small, 14-pin TSSOP package.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	PCM1807
Analog supply voltage, V_{CC}	–0.3 V to 6.5 V
Digital supply voltage, V_{DD}	–0.3 V to 4 V
Ground voltage differences, AGND, DGND	±0.1 V
Digital input voltage, LRCK, BCK, DOUT	–0.3 V to (V_{DD} + 0.3 V) < 4 V
Digital input voltage, MD, MC, MS, SCKI	–0.3 V to 6.5 V
Analog input voltage, $V_{IN}L$, $V_{IN}R$, V_{REF}	–0.3 V to (V_{CC} + 0.3 V) < 6.5 V
Input current (any pins except supplies)	±10 mA
Ambient temperature under bias, T_A	–40°C to 125°C
Storage temperature, T_{stg}	–55°C to 150°C
Junction temperature, T_J	150°C
Lead temperature (soldering)	260°C, 5 s
Package temperature (reflow, peak)	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Analog supply voltage, V_{CC}		4.5	5	5.5	V
Digital supply voltage, V_{DD}		2.7	3.3	3.6	V
Analog input voltage, full scale (–0 dB)	V_{CC} = 5 V		3		Vp-p
Digital input logic family			TTL compatible		
Digital input clock frequency, system clock		4.096		49.152	MHz
Digital input clock frequency, sampling clock		16		96	kHz
Digital output load capacitance				20	pF
Operating free-air temperature, T_A		–40		85	°C

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 512 f_S, 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			24		Bits
DATA FORMAT						
	Audio data interface format			I^2S, left-justified		
	Audio data bit length			24		Bits
	Audio data format			MSB-first, 2s complement		
f_S	Sampling frequency		16	48	96	kHz
	System clock frequency	256 f_S	4.096	12.288	24.576	MHz
		384 f_S	6.144	18.432	36.864	
		512 f_S	8.192	24.576	49.152	
INPUT LOGIC						
V_{IH} (1)	Input logic level		2		V_{DD}	VDC
V_{IL} (1)			0		0.8	
V_{IH} (2) (3)			2		5.5	
V_{IL} (2) (3)			0		0.8	
I_{IH} (2)	Input logic current	$V_{IN} = V_{DD}$			±10	μA
I_{IL} (2)		V_{IN} = 0 V			±10	
I_{IH} (1) (3)		$V_{IN} = V_{DD}$		65	100	
I_{IL} (1) (3)		V_{IN} = 0 V			±10	
OUTPUT LOGIC						
V_{OH} (4)	Output logic level	I_{OUT} = –4 mA	2.8			VDC
V_{OL} (4)		I_{OUT} = 4 mA			0.5	
DC ACCURACY						
	Gain mismatch, channel-to-channel			±1	±3	% of FSR
	Gain error			±3	±6	% of FSR
DYNAMIC PERFORMANCE (5)						
THD+N	Total harmonic distortion + noise	V_{IN} = –0.5 dB, f_S = 48 kHz		–93	–87	dB
		V_{IN} = –0.5 dB, f_S = 96 kHz (6)		–87		
		V_{IN} = –60 dB, f_S = 48 kHz		–37		
		V_{IN} = –60 dB, f_S = 96 kHz (6)		–39		
	Dynamic range	f_S = 48 kHz, A-weighted	95	99		dB
		f_S = 96 kHz, A-weighted (6)		101		
S/N	Signal-to-noise ratio	f_S = 48 kHz, A-weighted	95	99		dB
		f_S = 96 kHz, A-weighted (6)		101		
	Channel separation	f_S = 48 kHz	93	97		dB
		f_S = 96 kHz (6)		91		
ANALOG INPUT						
	Input voltage			0.6 V_{CC}		Vp-p
	Center voltage (V_{REF})			0.5 V_{CC}		V
	Input impedance			60		kΩ
	Antialiasing filter frequency response	–3 dB		1.3		MHz

(1) Pins 7, 8: LRCK, BCK (Schmitt-trigger input, with 50-kΩ typical pulldown resistor, in slave mode)
(2) Pin 6: SCKI (Schmitt-trigger input, 5-V tolerant)
(3) Pins 10–12: MD, MC, MS (Schmitt-trigger input, with 50-kΩ typical pulldown resistor, 5-V tolerant)
(4) Pins 7–9: LRCK, BCK (in master mode), DOUT
(5) Analog performance specifications are tested using a System Two™ audio measurement system by Audio Precision™ with 400-Hz HPF and 20-kHz LPF in RMS mode.
(6) f_S = 96 kHz, system clock = 256 f_S.

ELECTRICAL CHARACTERISTICS (continued)

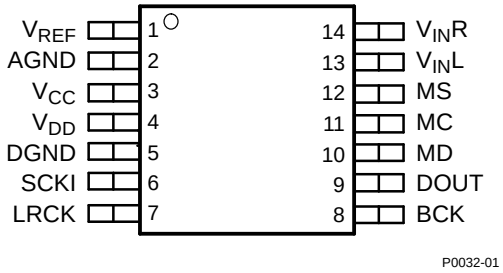
All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 512 f_S, 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL FILTER PERFORMANCE						
	Pass band				0.454 f_S	
	Stop band		0.583 f_S			
	Pass-band ripple				±0.05	dB
	Stop-band attenuation		–65			dB
	Delay time			17.4/f_S		
	HPF frequency response	–3 dB		0.019 f_S/1000		
POWER SUPPLY REQUIREMENTS						
V_{CC}	Voltage range		4.5	5	5.5	VDC
V_{DD}			2.7	3.3	3.6	
I_{CC}	Supply current (7)			8.6	11	mA
		Powered down (8)		1		µA
I_{DD}		f_S = 48 kHz		5.9	8	mA
		f_S = 96 kHz (9)		10.2		mA
		Powered down (8)		80		µA
	Power dissipation	Operatng, f_S = 48 kHz		62	81	mW
		Operatng, f_S = 96 kHz (9)		77		
		Powered down (8)		270		µW
TEMPERATURE RANGE						
T_A	Operation temperature		–40		85	°C
θ_{JA}	Thermal resistance			170		°C/W

(7) Minimum load on LRCK (pin 7), BCK (pin 8), DOUT (pin 9)
(8) By setting PDWN or SRST bit through serial control port. Halt SCKI, BCK, LRCK.
(9) f_S = 96 kHz, system clock = 256 f_S.

PIN ASSIGNMENTS

PW PACKAGE
(TOP VIEW)



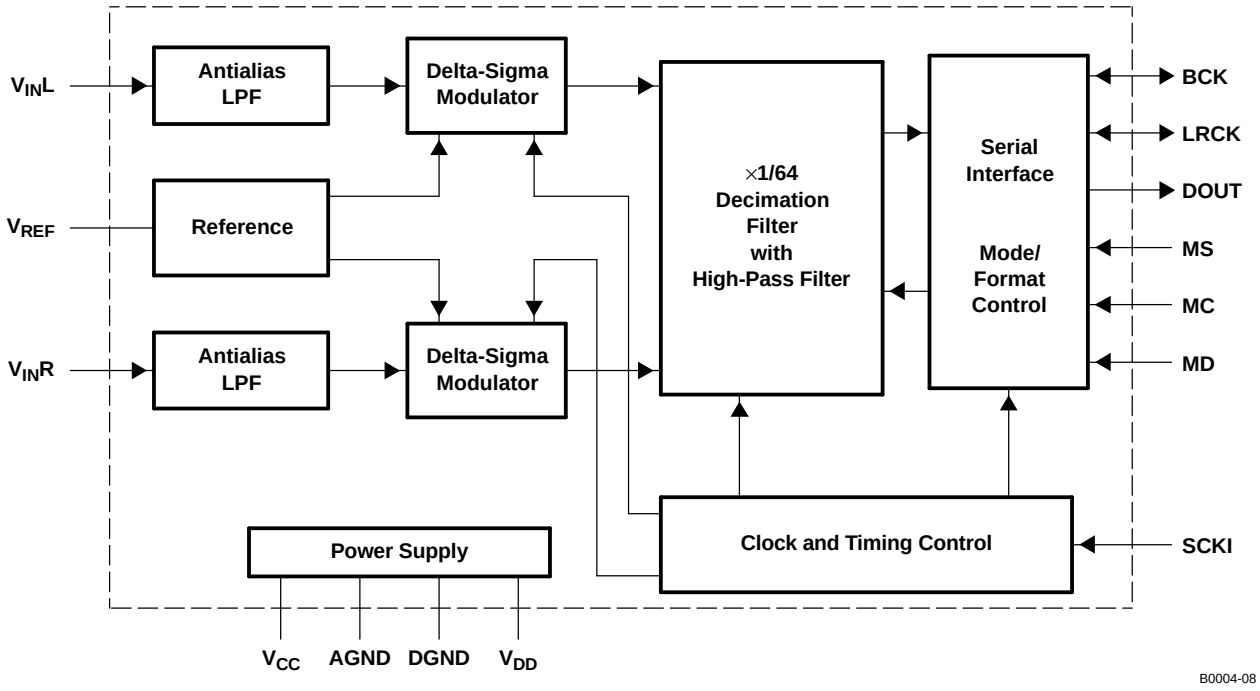
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TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	PIN		
AGND	2	–	Analog GND
BCK	8	I/O	Audio data bit clock input/output (1)
DGND	5	–	Digital GND
DOUT	9	O	Audio data digital output
LRCK	7	I/O	Audio data latch enable input/output (1)
MC	11	I	Mode control clock input (2)
MD	10	I	Mode control data input (2)
MS	12	I	Mode control select input (2)
SCKI	6	I	System clock input; 256 f_S, 384 f_S or 512 f_S (3)
V_{CC}	3	–	Analog power supply, 5-V
V_{DD}	4	–	Digital power supply, 3.3-V
$V_{IN}L$	13	I	Analog input, L-channel
$V_{IN}R$	14	I	Analog input, R-channel
V_{REF}	1	–	Reference voltage decoupling (= 0.5 V_{CC})

(1) Schmitt-trigger input with internal pulldown (50-kΩ, typical)
(2) Schmitt-trigger input with internal pulldown (50-kΩ, typical), 5-V tolerant
(3) Schmitt-trigger input, 5-V tolerant

Functional Block Diagram



TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 512 f_S, 24-bit data, unless otherwise noted.

DECIMATION FILTER FREQUENCY RESPONSE

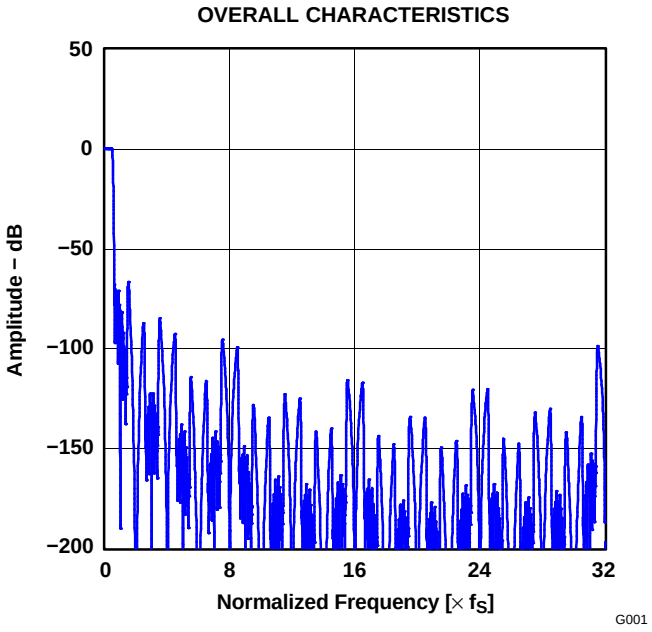


Figure 1.

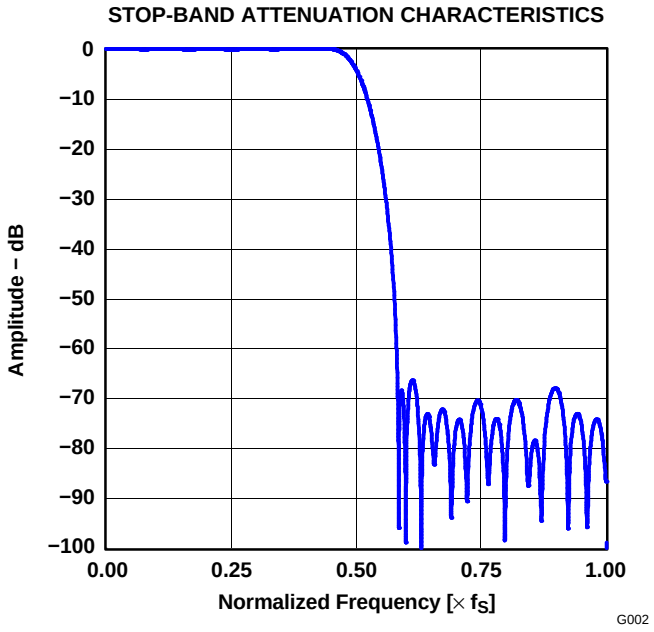


Figure 2.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (Continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 512 f_S, 24-bit data, unless otherwise noted.

DECIMATION FILTER FREQUENCY RESPONSE (Continued)

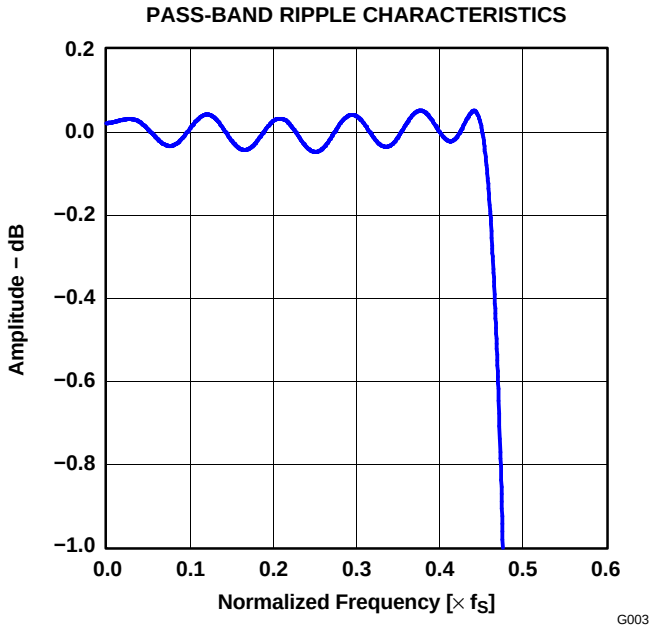


Figure 3.

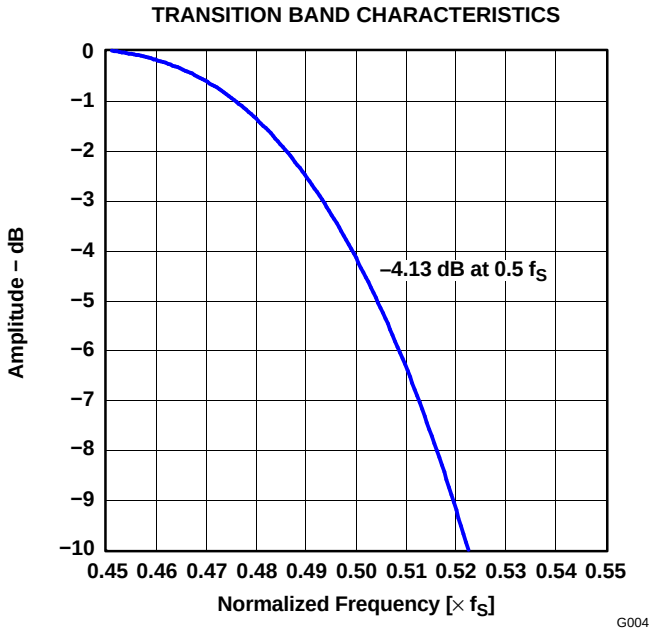


Figure 4.

HIGH-PASS FILTER FREQUENCY RESPONSE

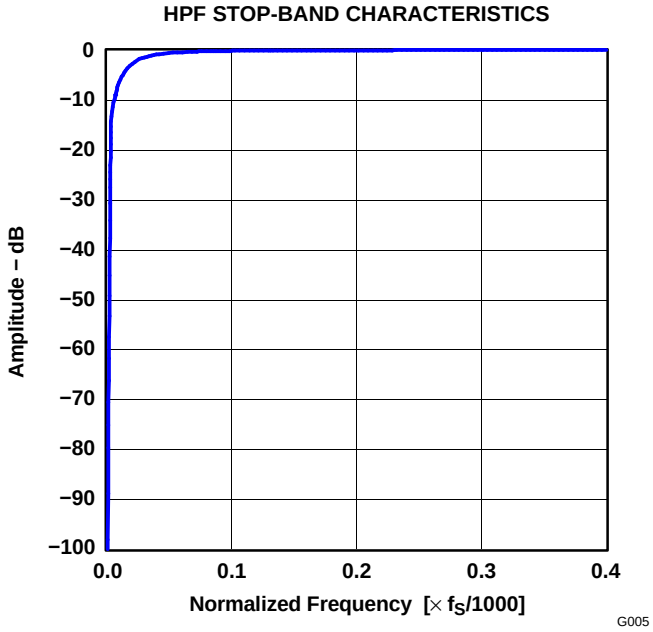


Figure 5.

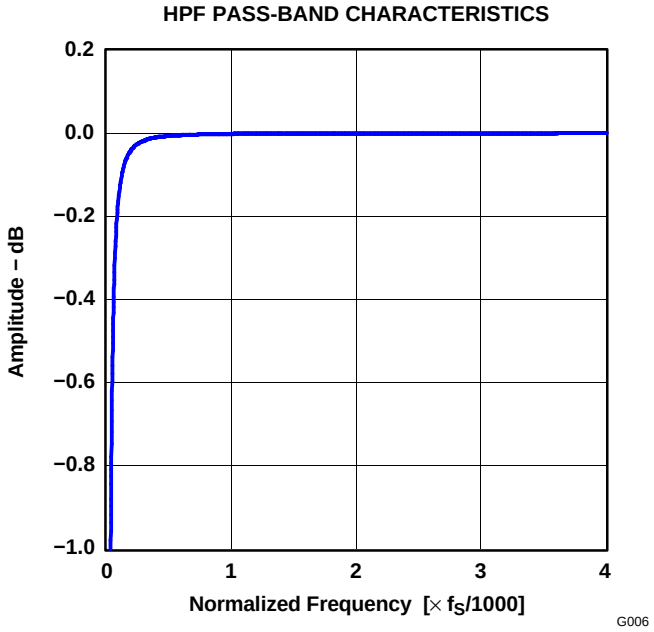


Figure 6.

TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 512 f_S, 24-bit data, unless otherwise noted.

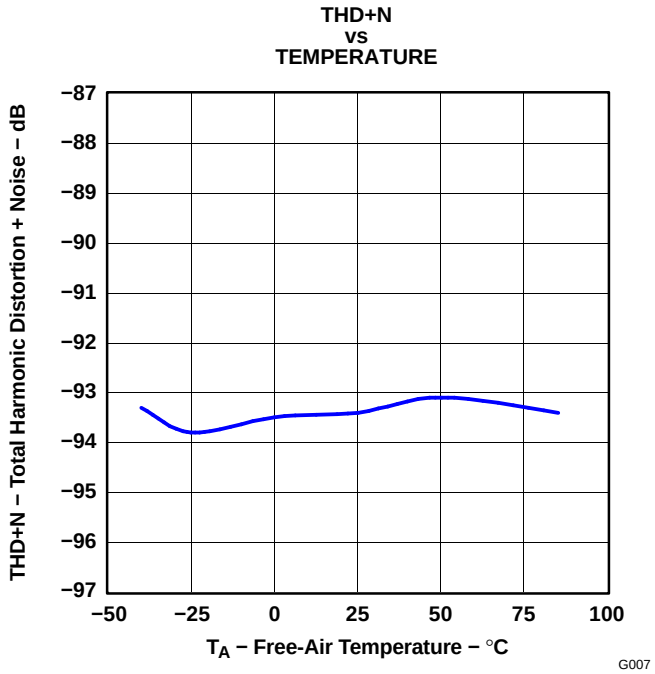


Figure 7.

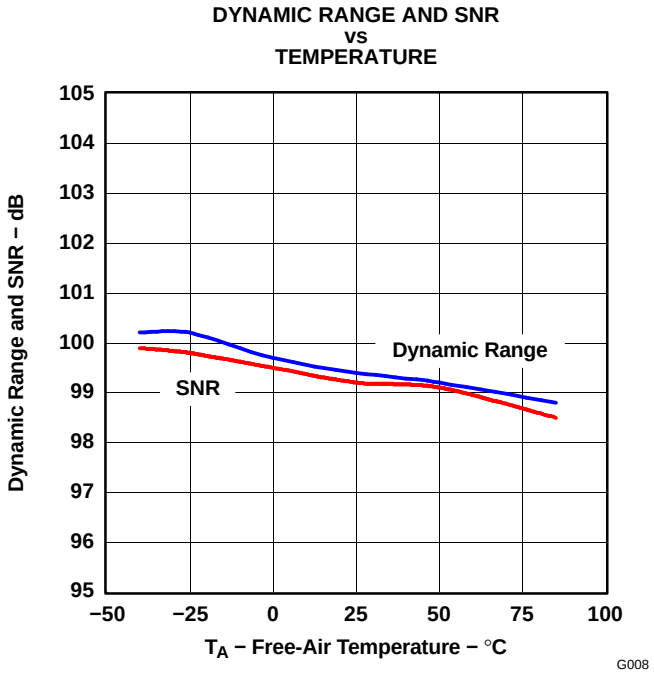


Figure 8.

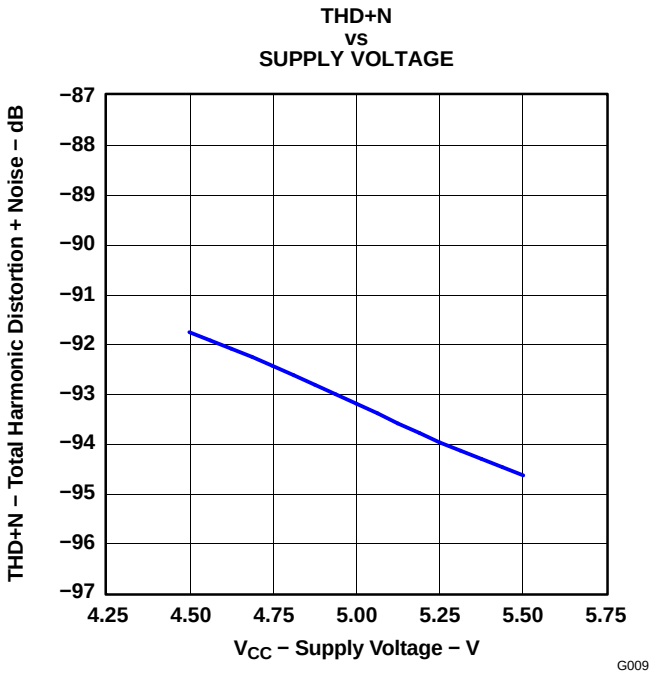


Figure 9.

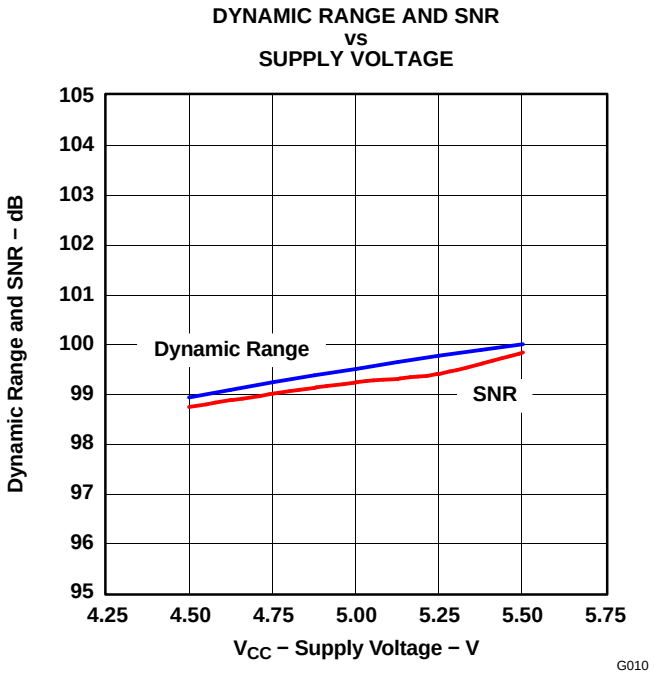


Figure 10.

TYPICAL PERFORMANCE CURVES (Continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 512 f_S, 24-bit data, unless otherwise noted.

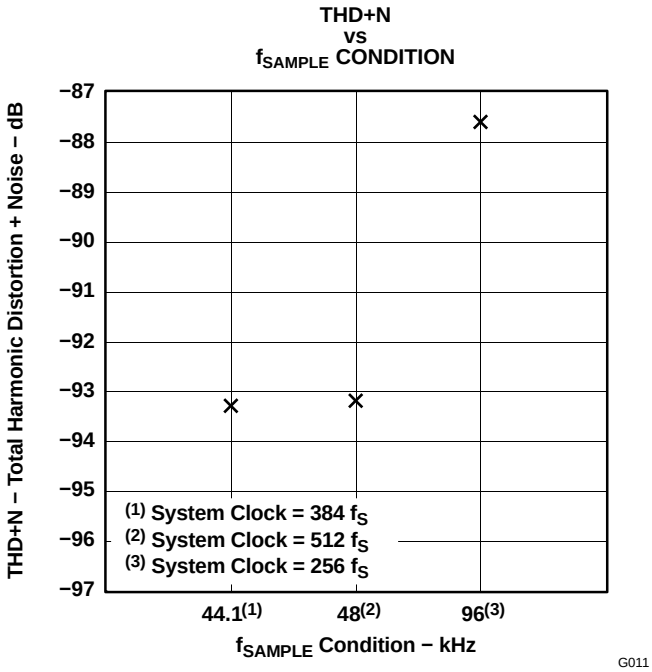


Figure 11.

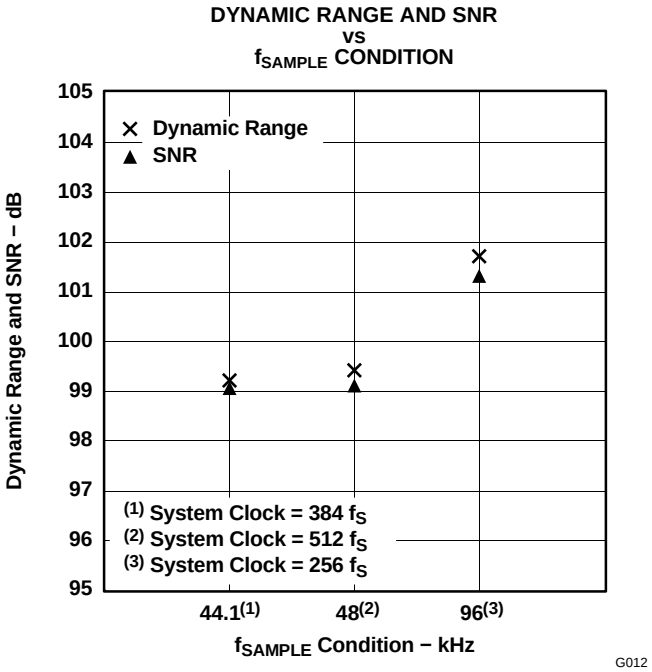


Figure 12.

OUTPUT SPECTRUM

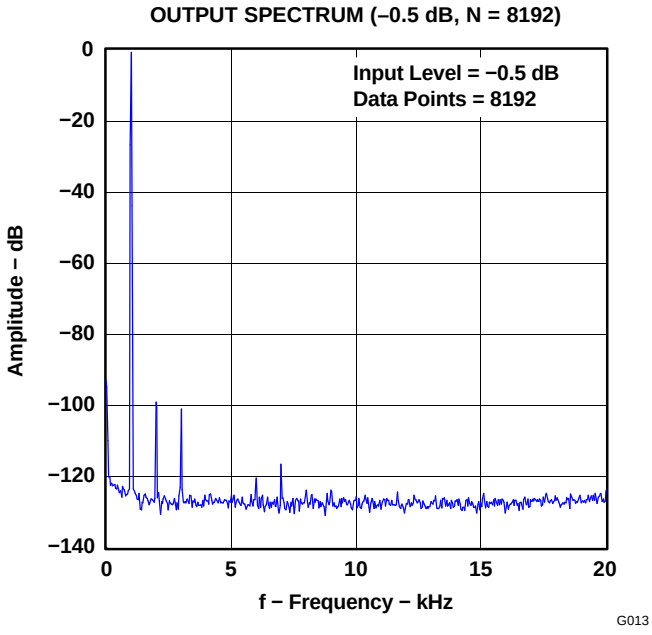


Figure 13.

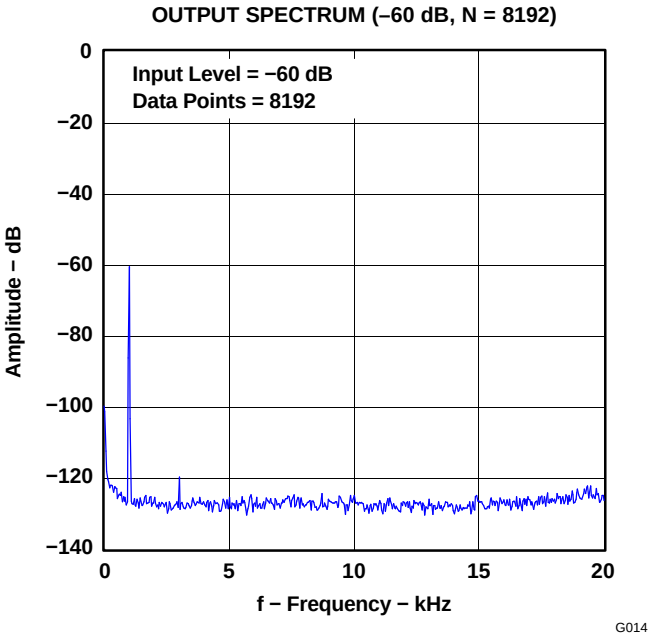


Figure 14.

TYPICAL PERFORMANCE CURVES (Continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 512 f_S, 24-bit data, unless otherwise noted.

OUTPUT SPECTRUM (Continued)

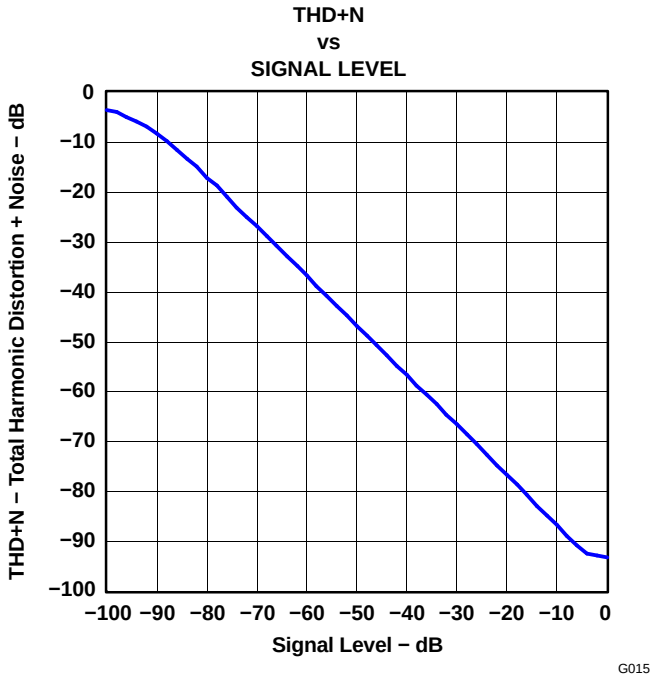


Figure 15.

SUPPLY CURRENT

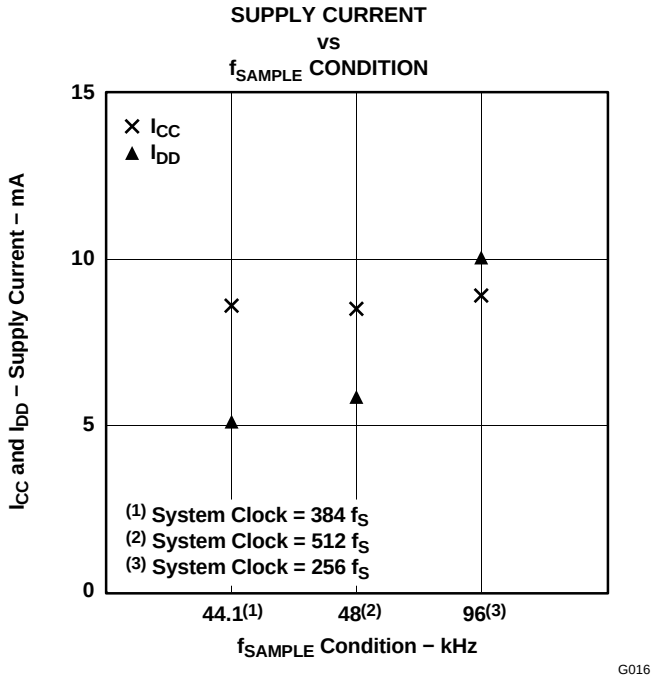


Figure 16.

SYSTEM CLOCK

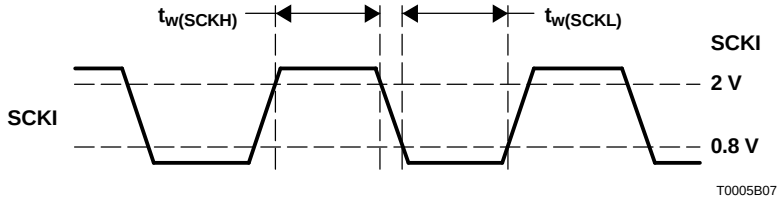
The PCM1807 supports 256 f_S, 384 f_S and 512 f_S as system clock, where f_S is the audio sampling frequency. The system clock must be supplied on SCKI (pin 6).

The PCM1807 has a system clock detection circuit which automatically senses if the system clock is operating at 256 f_S, 384 f_S, or 512 f_S in slave mode. In master mode, the system clock frequency must be controlled through the serial control port, which uses MD (pin 10), MC (pin 11), and MS (pin 12). The system clock is divided down automatically to generate frequencies of 128 f_S and 64 f_S, which are used to operate the digital filter and the delta-sigma modulator, respectively.

Table 1 shows some typical relationships between sampling frequency and system clock frequency, and Figure 17 shows system clock timing.

Table 1. Sampling Frequency and System Clock Frequency

SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)		
	256 f_S	384 f_S	512 f_S
16	4.096	6.144	8.192
32	8.192	12.288	16.384
44.1	11.2896	16.9344	22.5792
48	12.288	18.432	24.576
64	16.384	24.576	32.768
88.2	22.5792	33.8688	45.1584
96	24.576	36.864	49.152



SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{w(SCKH)}$	System clock pulse duration, HIGH	8		ns
$t_{w(SCKL)}$	System clock pulse duration, LOW	8		ns

Figure 17. System Clock Timing

FADE-IN AND FADE-OUT FUNCTIONS

The PCM1807 has fade-in and fade-out functions on DOUT (pin 9) to avoid pop noise, and the functions come into operation in some cases as described in several following sections. The level changes from 0 dB to mute or mute to 0 dB are performed using calculated pseudo S-shaped characteristics with zero-cross detection. Because of the zero-cross detection, the time needed for the fade in and fade out depends on the analog input frequency (f_{in}). It takes $48/f_{in}$ until processing is completed. If there is no zero cross during $8192/f_S$, DOUT is faded in or out by force during $48/f_S$ (TIME OUT). Figure 18 illustrates the fade-in and fade-out operation processing.

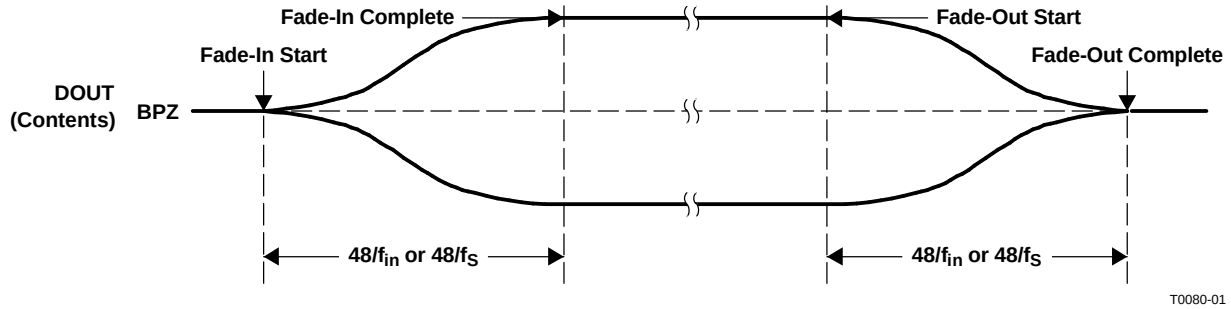


Figure 18. Fade-In and Fade-Out Operations

POWER ON

The PCM1807 has an internal power-on-reset circuit, and initialization (reset) is performed automatically when the power supply (V_{DD}) exceeds 2.2 V (typical). While V_{DD} < 2.2 V (typical), and for 1024 system-clock counts after V_{DD} > 2.2 V (typical), the PCM1807 stays in the reset state and the digital output is forced to zero. The digital output is valid after the reset state is released and the time of $8960/f_S$ has elapsed. Because the fade-in operation is performed, it takes additional time of $48/f_{in}$ or $48/f_S$ until the data corresponding to the analog input signal is obtained. Figure 19 illustrates the power-on timing and the digital output.

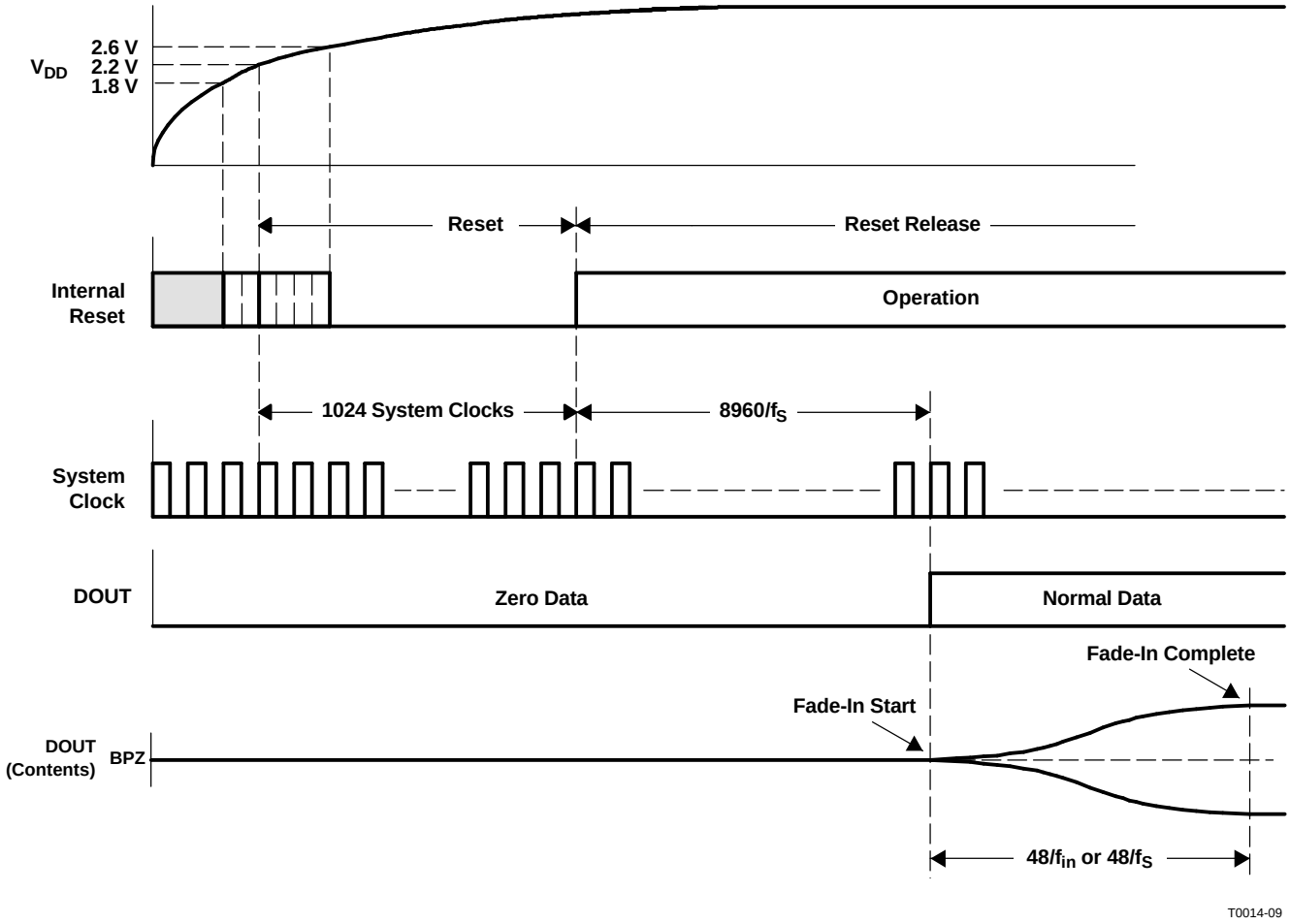


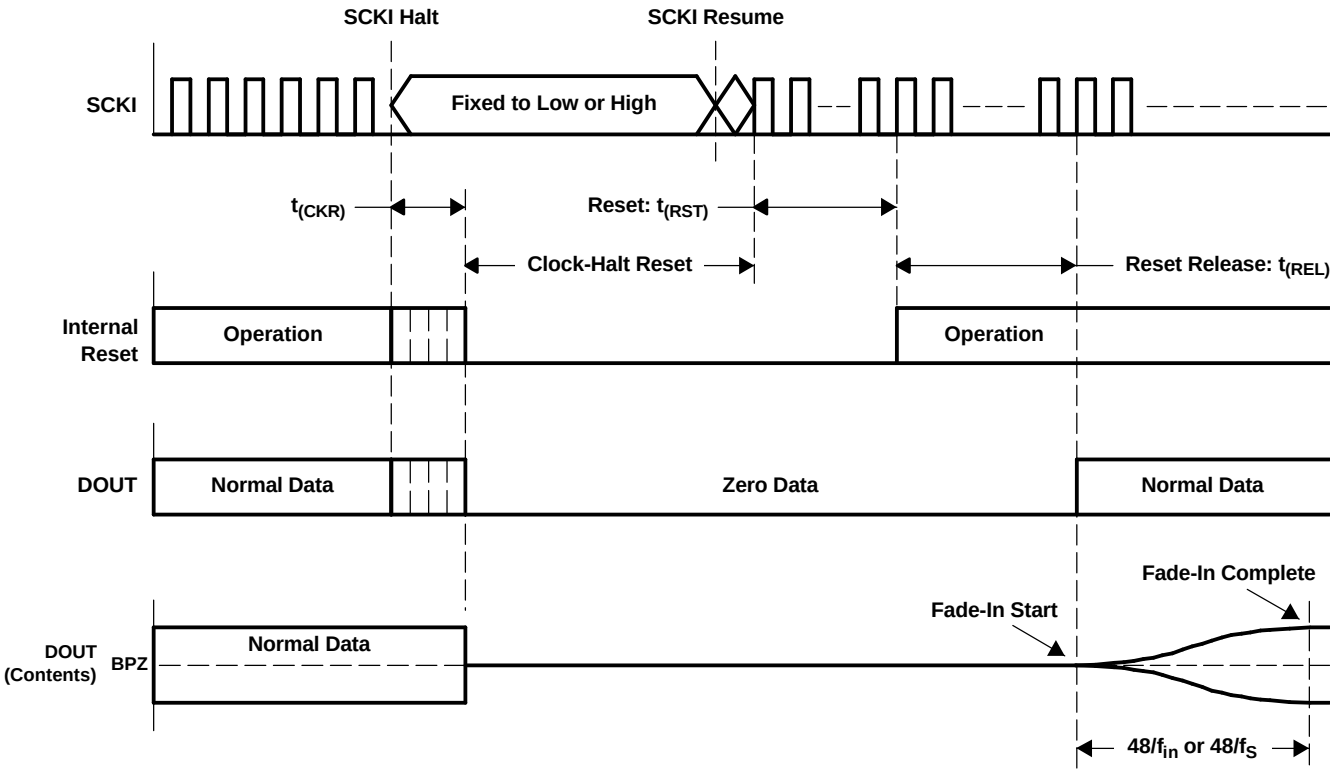
Figure 19. Power-On Timing

CLOCK-HALT RESET FUNCTIONS

The PCM1807 has a reset function, which is triggered by halting SCKI (pin 6) in both master and slave modes. The function is available anytime after power on. Reset and power down are performed automatically 4 µs (minimum) after SCKI is halted. While the clock-halt reset is asserted, the PCM1807 stays in the reset and power-down mode, and DOUT is forced to zero. Also, all registers except the mode control registers are reset once. If minimization of power dissipation is required, the PDWN bit must be set to HIGH prior to halting SCKI through the serial control port as described in the *SPI Serial Control Port for Mode Control* section. SCKI must be supplied to release the reset and power-down mode. The digital output is valid after the reset state is released and the time of 1024 SCKI + 8960/f_S has elapsed. Because the fade-in operation is performed, it takes additional time of 48/f_{in} or 48/f_S until the level corresponding to the analog input signal is obtained. Figure 20 illustrates the clock-halt reset timing.

To avoid ADC performance degradation, BCK (pin 8) and LRCK (pin 7) are required to synchronize with SCKI within 4480/f_S after SCKI is resumed. If it takes more than 4480/f_S for BCK and LRCK to synchronize with SCKI, SCKI should be masked until the synchronization is formed again, taking care of glitch and jitter. See the typical circuit connection diagram, Figure 31

To avoid ADC performance degradation, the clock-halt reset also should be asserted when f_S, SCKI, MD[1:0], FMT bits, etc., are changed on the fly.



SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{(CKR)}$	Delay time from SCKI halt to internal reset	4		µs
$t_{(RST)}$	Delay time from SCKI resume to reset release		1024 SCKI	µs
$t_{(REL)}$	Delay time from reset release to DOUT output		8960/f_S	µs

Figure 20. Clock-Halt Reset Timing

SERIAL AUDIO DATA INTERFACE

The PCM1807 interfaces the audio system through LRCK (pin 7), BCK (pin 8), and DOUT (pin 9).

INTERFACE MODE

The PCM1807 supports master mode and slave mode as interface modes, which are selected by MD1 and MD0. MD1 and MD0 are controlled through the serial control port as shown in Table 2.

In master mode, the PCM1807 provides the timing of serial audio data communications between the PCM1807 and the digital audio processor or external circuit. While in slave mode, the PCM1807 receives the timing for data transfer from an external controller.

Table 2. Interface Modes

MD1	MD0	INTERFACE MODE
0	0	Slave mode (256 f_S, 384 f_S, 512 f_S autodetection) (default)
0	1	Master mode (512 f_S)
1	0	Master mode (384 f_S)
1	1	Master mode (256 f_S)

Master mode

In master mode, BCK and LRCK work as output pins, and these pins are controlled by timing which is generated in the clock circuit of the PCM1807. The frequency of BCK is fixed at 64 BCK/frame.

Slave mode

In slave mode, BCK and LRCK work as input pins. The PCM1807 accepts 64 BCK/frame or 48 BCK/frame format (only for a 384 f_S system clock), not 32 BCK/frame format.

DATA FORMAT

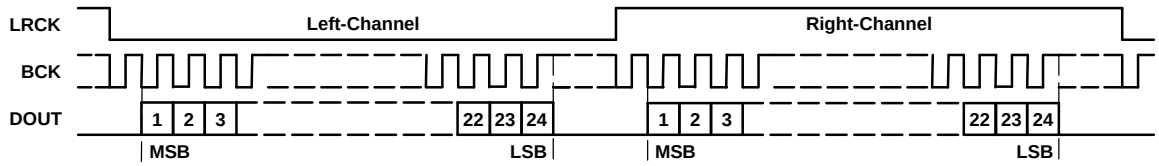
The PCM1807 supports two audio data formats in both master and slave modes. The data formats are selected by FMT, which is controlled through the serial control port as shown in Table 3. Figure 21 illustrates the data formats in slave mode and master mode.

Table 3. Data Format

FORMAT NO.	FMT	FORMAT
0	0	I^2S, 24-bit (default)
1	1	Left-justified, 24-bit

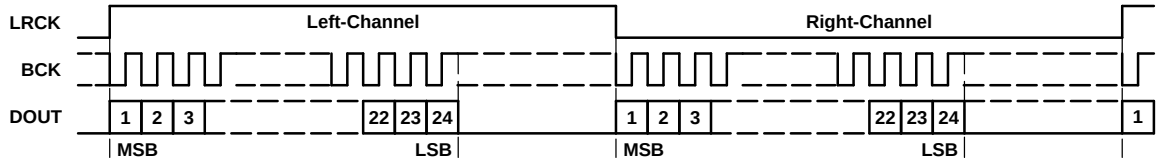
FORMAT 0: FMT = 0

24-Bit, MSB-First, I²S



FORMAT 1: FMT = 1

24-Bit, MSB-First, Left-Justified

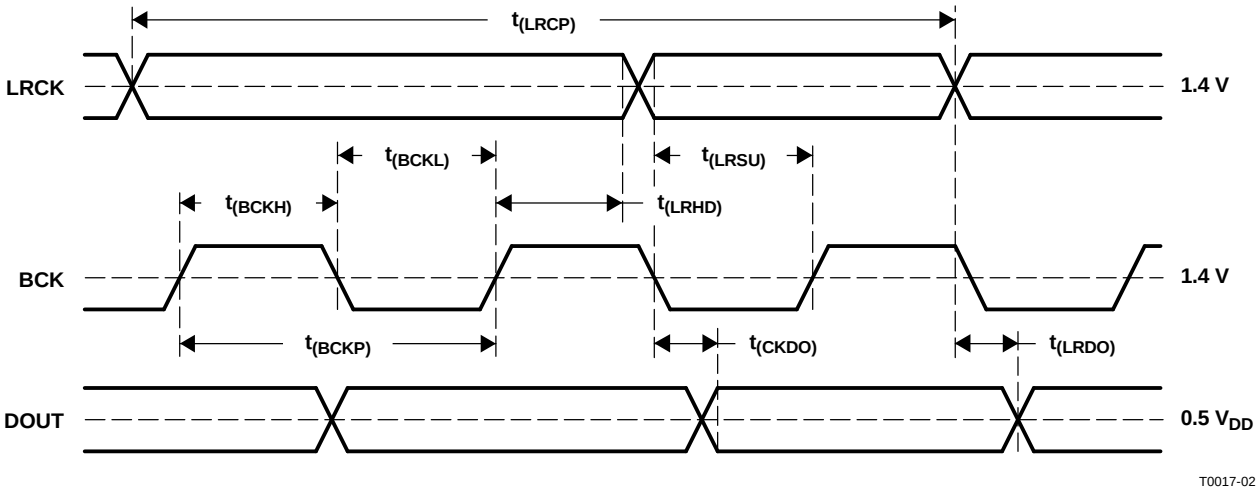


T0016-14

Figure 21. Audio Data Format (LRCK and BCK Work as Inputs in Slave Mode and as Outputs in Master Mode)

INTERFACE TIMING

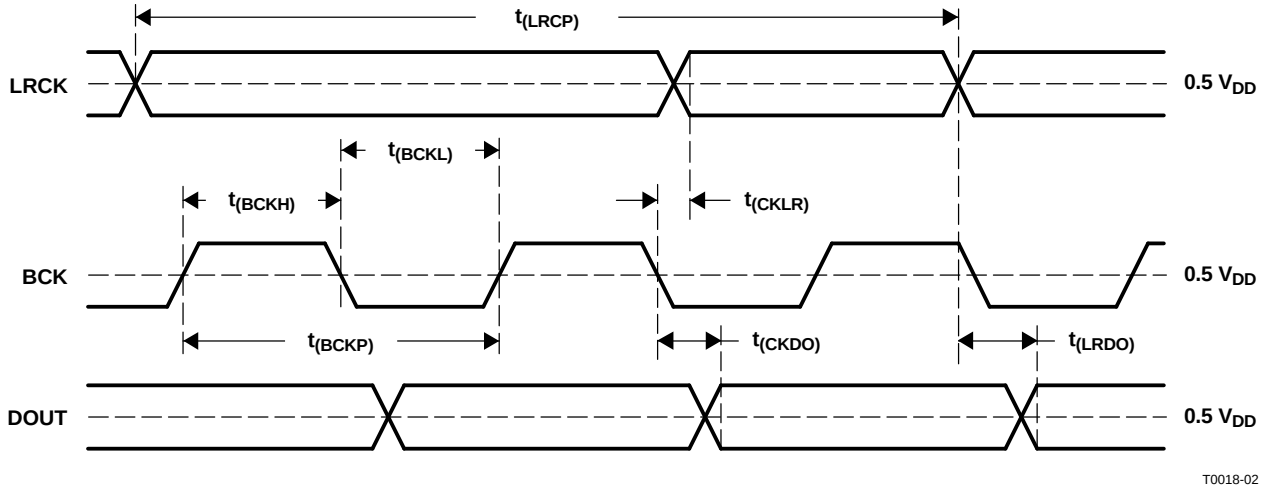
Figure 22 and Figure 23 illustrate the interface timing in slave mode and master mode, respectively.



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	$1/(64\ f_S)$			ns
$t_{(BCKH)}$	BCK pulse duration, HIGH	$1.5 \times t_{SCKI}$			ns
$t_{(BCKL)}$	BCK pulse duration, LOW	$1.5 \times t_{SCKI}$			ns
$t_{(LRSU)}$	LRCK setup time to BCK rising edge	50			ns
$t_{(LRHD)}$	LRCK hold time to BCK rising edge	10			ns
$t_{(LRCP)}$	LRCK period	10			µs
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10		40	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10		40	ns

NOTE: Timing measurement reference level is 1.4 V for input and 0.5 V_{DD} for output. Load capacitance of DOUT is 20 pF. t_{SCKI} is the SCKI period.

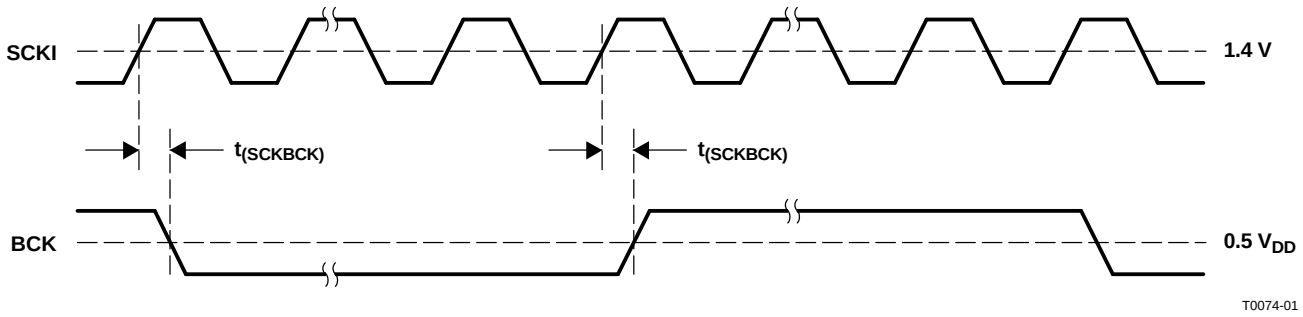
Figure 22. Audio Data Interface Timing (Slave Mode: LRCK and BCK Work as Inputs)



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	150	1/(64 f_S)	1000	ns
$t_{(BCKH)}$	BCK pulse duration, HIGH	65		600	ns
$t_{(BCKL)}$	BCK pulse duration, LOW	65		600	ns
$t_{(CKLR)}$	Delay time, BCK falling edge to LRCK valid	–10		20	ns
$t_{(LRCP)}$	LRCK period	10	1/f_S	65	µs
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10		20	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10		20	ns

NOTE: Timing measurement reference level is 0.5 V_{DD}. Load capacitance of all signals is 20 pF.

Figure 23. Audio Data Interface Timing (Master Mode: LRCK and BCK Work as Outputs)



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(SCKBCK)}$	Delay time, SCKI rising edge to BCK edge	5		30	ns

NOTE: Timing measurement reference level is 1.4 V for input and 0.5 V_{DD} for output. Load capacitance of BCK is 20 pF. This timing is applied when SCKI frequency is less than 25 MHz.

Figure 24. Audio Clock Interface Timing (Master Mode: BCK Works as Output)

SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM

In slave mode, the PCM1807 operates under LRCK, synchronized with system clock SCKI. The PCM1807 does not require a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ±6 BCKs for 64 BCK/frame (±5 BCKs for 48 BCK/frame) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within $1/f_S$ and digital output is forced to zero data (BPZ code) until resynchronization between LRCK and SCKI is established.

In the case of changes less than ±5 BCKs for 64 BCK/frame (±4 BCKs for 48 BCK/frame), resynchronization does not occur and the previously described digital output control and discontinuity do not occur.

Figure 25 illustrates the digital output response for loss of synchronization and resynchronization. During undefined data, the PCM1807 can generate some noise in the audio signal. Also, the transition of normal data to undefined data creates a discontinuity in the digital output data, which can generate some noise in audio signal. The digital output is valid after resynchronization completes and the time of $32/f_S$ has elapsed. Because the fade-in operation is performed, it takes additional time of $48/f_{in}$ or $48/f_S$ until the level corresponding to the analog input signal is obtained. If synchronization is lost during the fade-in or fade-out operation, the operation stops and DOUT is forced to zero data immediately. The fade-in operation resumes from mute after the time of $32/f_S$ following resynchronization.

It is recommended to set the PDWN bit to HIGH once through the serial control port to get stable analog performance when the sampling rate, interface mode, or data format is changed.

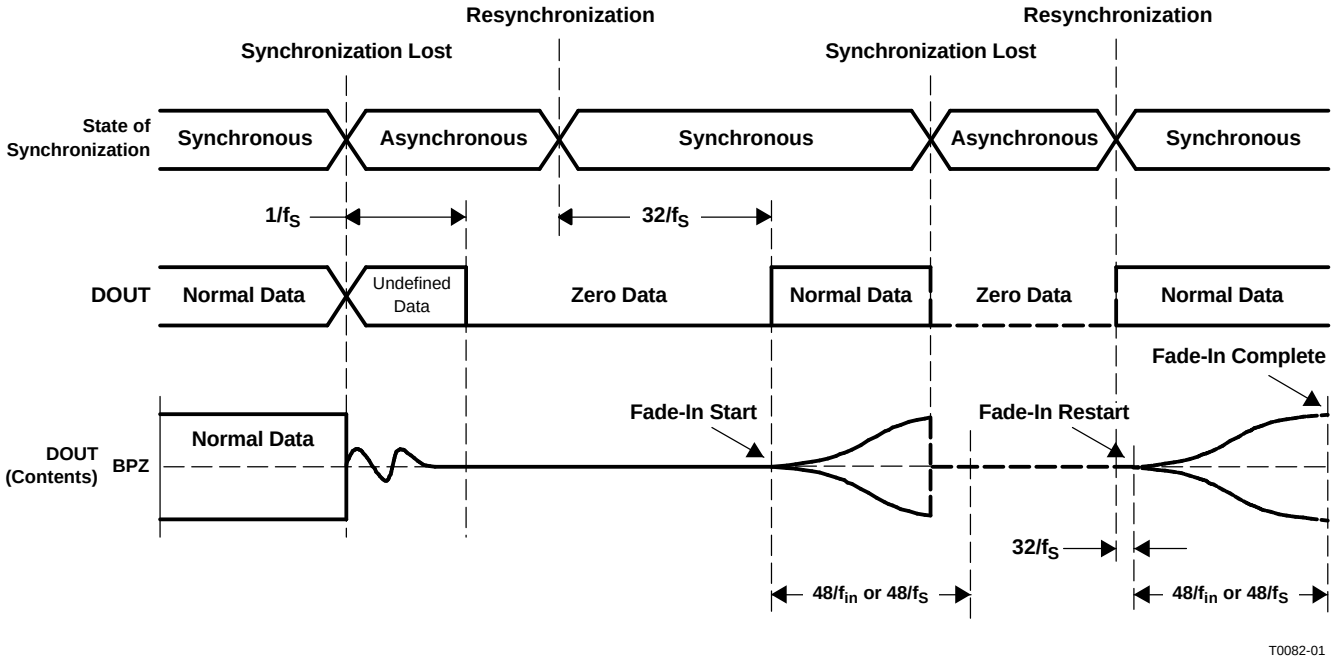


Figure 25. ADC Digital Output for Loss of Synchronization and Resynchronization

FUNCTION CONTROL

The PCM1807 has the following functions which can be controlled through the serial control port. When the LRCK (f_S), SCKI, MD[1:0], or FMT bit is changed on the fly, a clock-halt reset or an immediate reset by PDWN or SRST via the serial control port is recommended to obtain stable analog performance.

MUTE

The MUTE bit controls fade-in and fade-out operation for DOUT. When the MUTE bit is set from 0 to 1, the fade-out operation provides step-down digital attenuation to prevent a pop noise. When the MUTE bit is set from 1 to 0, the fade-in operation provides a step-up digital gain to prevent a pop noise. The digital output of DOUT behaves as shown in Figure 18.

Table 4. Mute On/Off Control

MUTE	MUTE CONTROL
0	Normal operation (default)
1	Mute on

POLARITY CONTROL

By setting PREV = 1, the PCM1807 inverts the data on DOUT relative to that of the analog signal on $V_{IN}L/V_{IN}R$ (pin 13/pin 14). Because the inversion occurs immediately after the PREV bit changes, pop noise can be generated at the change. It is recommended that MUTE or PDWN be asserted before using PREV.

Table 5. Polarity Control

PREV	POLARITY CONTROL
0	Normal operation (default)
1	Invert

MODE CONTROL REGISTER RESET

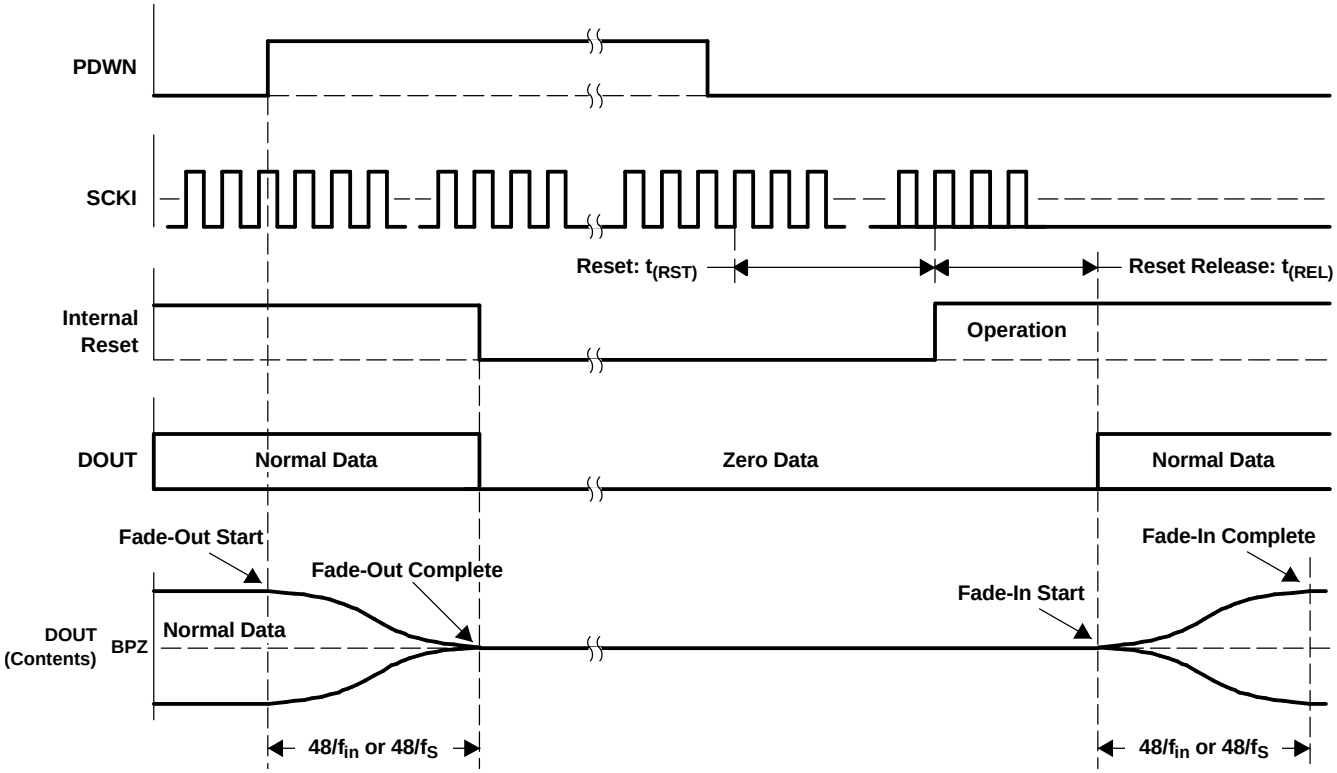
The MRST bit is used to reset the mode control register to the default setting.

Table 6. Mode Control Register Reset

MRST	MODE CONTROL REGISTER RESET
0	Set default value
1	Normal operation (default)

POWER DOWN

The PDWN bit controls the operation of the PCM1807. During power-down mode, both supply current for the analog section and clock signal for the digital section are shut down, and DOUT is forced to zero. Also, all registers except the mode control registers are reset once. The PCM1807 minimizes power dissipation during the power-down mode. When the PCM1807 takes power down or power up, fade-out or fade-in which is shown in Figure 18 is asserted, respectively. The system clock must be input until the fade-out process completes and prior to PDWN deassertion. The digital output is valid after the reset state is released and the time of 1024 SCKI + 8960/f_S has elapsed. Because the fade-in operation is processed, it takes additional time of 48/f_{in} or 48/f_S until the level corresponding to the analog input signal is obtained. Figure 26 illustrates DOUT behavior on the power-down and power-up sequence by PDWN.



SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{(RST)}$	Delay time from SCKI resume to reset release		1024 SCKI	µs
$t_{(REL)}$	Delay time from reset release to DOUT output		8960/f_S	µs

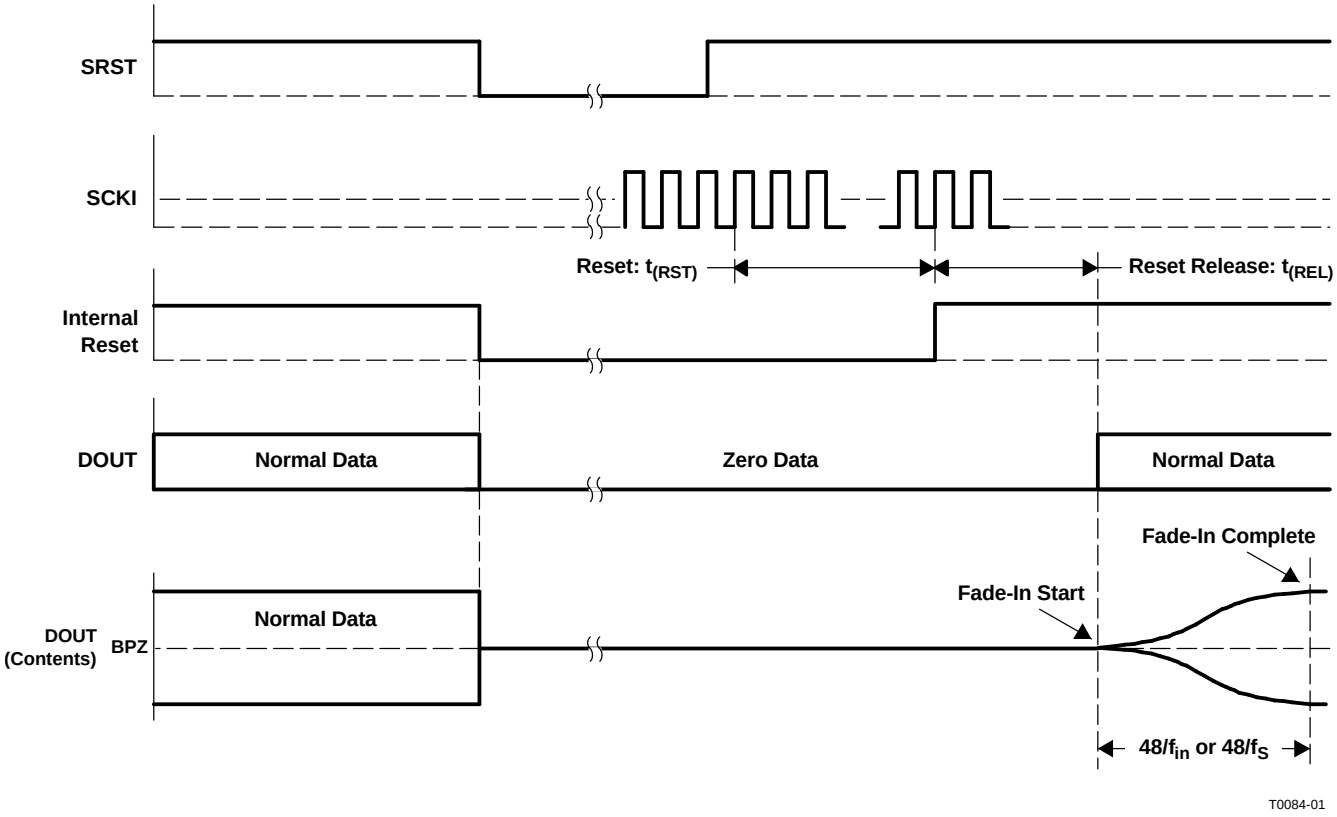
Figure 26. Power Up/Power Down Sequence by PDWN

Table 7. Power-Down Control

PDWN	POWER DOWN
0	Normal operation (default)
1	Power-down mode

SYSTEM RESET

The SRST bit controls the entire ADC operation except fade-out. DOUT is forced to zero immediately and the PCM1807 goes into power-down state. Also, all registers except the mode control register are reset once. The PCM1807 minimizes power dissipation during the power-down state. When the PCM1807 powers up, the digital output is valid after the reset state is released and the time of 1024 SCKI + 8960/f_S has elapsed. Because the fade-in operation is performed, it takes additional time of 48/f_{in} or 48/f_S until the level corresponding to the analog input signal is obtained. Figure 27 illustrates DOUT behavior during the power-down and power-up sequences by SRST.



SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{(RST)}$	Delay time from SCKI resume to reset release		1024 SCKI	µs
$t_{(REL)}$	Delay time from reset release to DOUT output		8960/f_S	µs

Figure 27. Power-Up/Power-Down Sequence by SRST

Table 8. System Reset Control

SRST	SYSTEM RESET
0	System reset
1	Normal operation (default)

SPI SERIAL CONTROL PORT FOR MODE CONTROL

The user-programmable built-in functions of the PCM1807 can be controlled through the serial control port with SPI format. All operations for the serial control port use 16-bit data words. Figure 28 shows the control data word format. The most-significant bit must be set to 0. Seven bits, labeled IDX[6:0], set the register index (or address) for the write operations. The least-significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 29 shows the functional timing diagram for writing to the serial control port. MS (pin 12) is held at a logic-1 state until a register is to be written. To start the register write cycle, MS is set to logic-0. Sixteen clocks are then provided on MC (pin 11), corresponding to the 16 bits of the control data word on MD (pin 10). After the 16th clock cycle has completed, the data is latched into the indexed-mode control register in the write operation. To write subsequent data, MS must be set to 1 once.

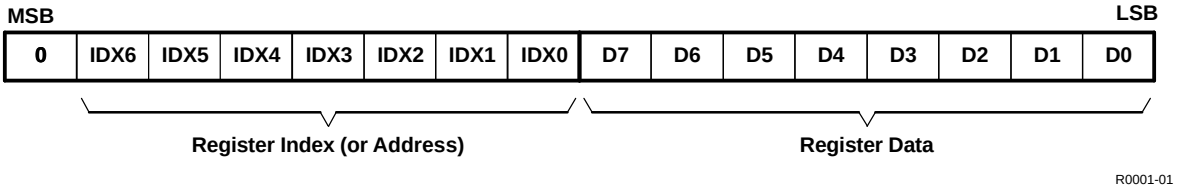


Figure 28. Control Data Word Format for MD

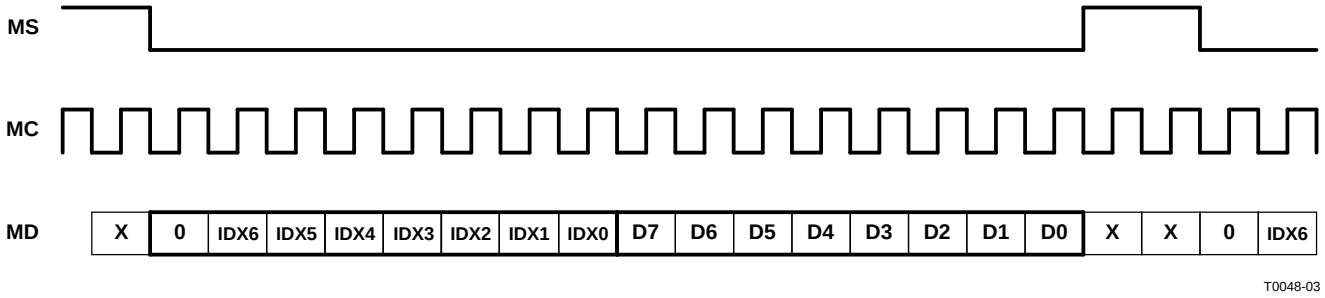
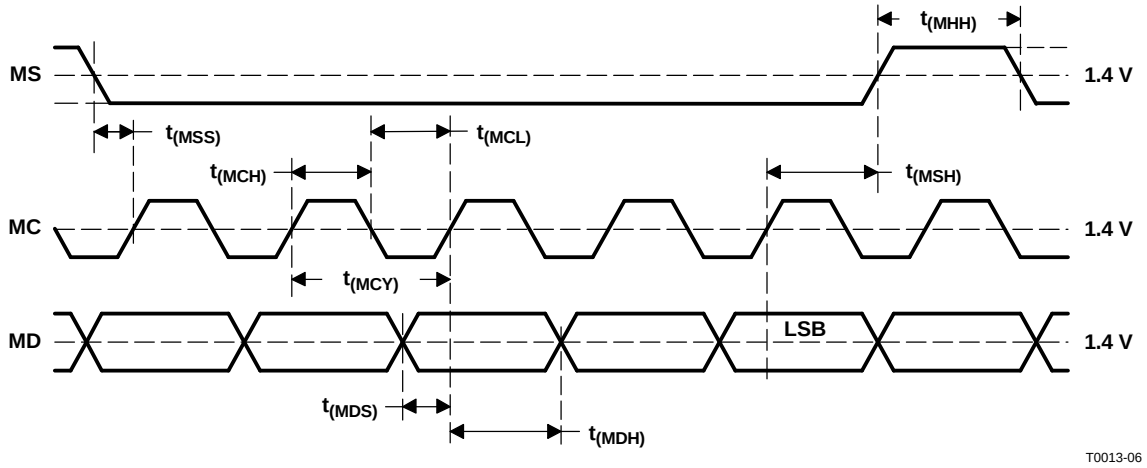


Figure 29. Serial Control Format

CONTROL INTERFACE TIMING REQUIREMENTS

Figure 30 illustrates a detailed timing diagram for the serial control port. These timing parameters are critical for proper control port operation.



SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{(MCY)}$	MC pulse cycle time	100		ns
$t_{(MCL)}$	MC low-level time	40		ns
$t_{(MCH)}$	MC high-level time	40		ns
$t_{(MHH)}$	MS high-level time	t_{MCY}		ns
$t_{(MSS)}$	MS falling edge to MC rising edge	15		ns
$t_{(MSH)}$	MS hold time (1)	15		ns
$t_{(MDH)}$	MD hold time	15		ns
$t_{(MDS)}$	MD setup time	15		ns

(1) MC rising edge to MS rising edge for the MC pulse corresponding to the LSB of MD

Figure 30. Control Interface Timing

MODE CONTROL REGISTER

The user-programmable mode control functions and the mode control register bit map are shown in Table 9 and Table 10.

Table 9. User-Programmable Mode Controls

FUNCTION	RESET DEFAULT	REGISTER	BIT(S)
Mode control register reset	Normal operation	49	MRST
System reset	Normal operation	49	SRST
Audio interface mode control	Slave mode	49	MD[1:0]
Audio interface format control	I^2S, 24-bit	49	FMT
Power-down control	Normal operation	49	PDWN
DOUT data polarity selection	Normal operation	49	PREV
DOUT data mute control	Normal operation	49	MUTE

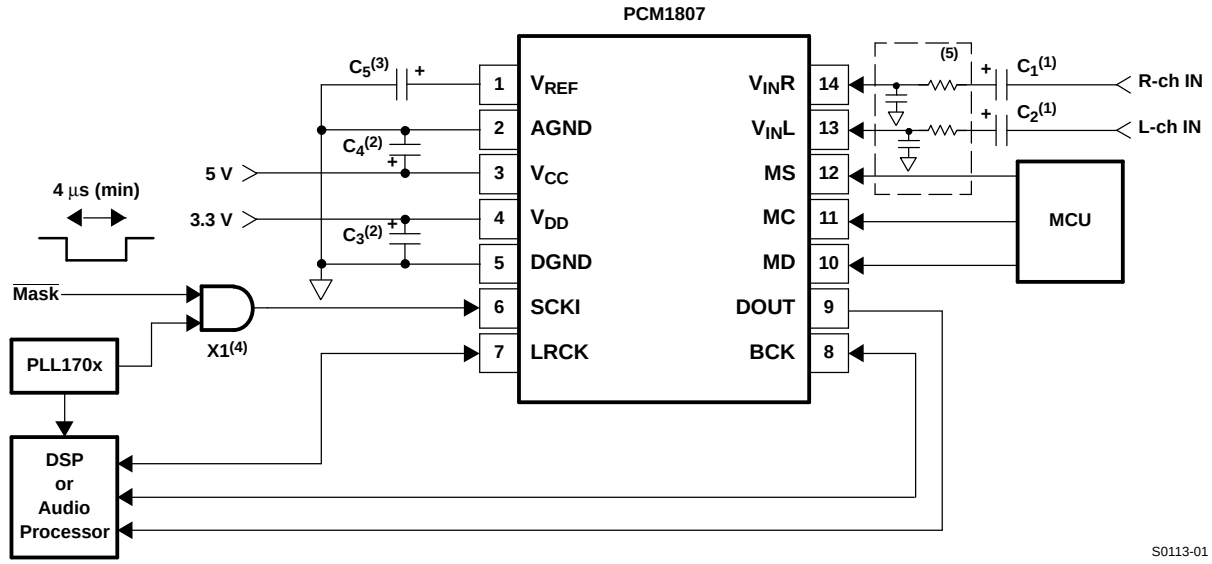
Table 10. Mode Control Register Bit Map

IDX (B14–B8)	REGIS-TER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
31h	49	0	0	1	1	0	0	0	1	MRST	SRST	MD1	MD0	FMT	PDWN	PREV	MUTE

APPLICATION INFORMATION

TYPICAL CIRCUIT CONNECTION DIAGRAM

Figure 31 is typical circuit connection diagram. The antialiasing low-pass filters are integrated on the analog inputs, $V_{IN}L$ and $V_{IN}R$. If the performance of these filters is not adequate for an application, appropriate external antialiasing filters are needed. A passive RC filter (100 Ω and 0.01 µF to 1 kΩ and 1000 pF) generally is used.



(1) C1, C2: A 1-µF electrolytic capacitor gives 2.7 Hz (τ = 1 µF × 60 kΩ) cutoff frequency for the input HPF in normal operation and requires a power-on settling time with a 60-ms time constant in the power-on initialization period.

(2) C3, C4: Bypass capacitors, 0.1-µF ceramic and 10-µF electrolytic, depending on layout and power supply

(3) C5: 0.1-µF ceramic and 10-µF electrolytic capacitors are recommended.

(4) X1: X1 masks the system clock input when using the clock-halt reset function with external control.

(5) Optional external antialiasing filter could be required, depending on the application.

Figure 31. Typical Circuit Connection Diagram

BOARD DESIGN AND LAYOUT CONSIDERATIONS

V_{CC}, V_{DD} PINS

The digital and analog power supply lines to the PCM1807 should be bypassed to the corresponding ground pins with both 0.1-µF ceramic and 10-µF electrolytic capacitors as close to the pins as possible to maximize the dynamic performance of the ADC.

AGND, DGND PINS

To maximize the dynamic performance of the PCM1807, the analog and digital grounds are not internally connected. These grounds should have low impedance to avoid digital noise feedback into the analog ground. They should be connected directly to each other under the PCM1807 package to reduce potential noise problems.

$V_{IN}L$, $V_{IN}R$ PINS

$V_{IN}L$ and $V_{IN}R$ are single-ended inputs. The antialias low-pass filters are integrated on these inputs to remove the noise outside the audio band. If the performance of these filters is not adequate for an application, appropriate external antialiasing filters are required. A passive RC filter (100 Ω and 0.01 µF to 1 kΩ and 1000 pF) is generally used.

APPLICATION INFORMATION (continued)

V_{REF} PIN

To ensure low source impedance of the ADC references, 0.1-μF ceramic and 10-μF electrolytic capacitors are recommended between V_{REF} and AGND. These capacitors should be located as close as possible to the V_{REF} pin to reduce dynamic errors on the ADC references.

DOUT PIN

The DOUT pin has a large load-drive capability, but if the DOUT line is long, locating a buffer near the PCM1807 and minimizing load capacitance is recommended to minimize the digital-analog crosstalk and maximize the dynamic performance of the ADC.

SYSTEM CLOCK

The quality of the system clock can influence dynamic performance, as the PCM1807 operates based on a system clock. Therefore, it may be necessary to consider the system clock duty, jitter, and the time difference between system clock transition and BCK or LRCK transition in slave mode.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PCM1807PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1807PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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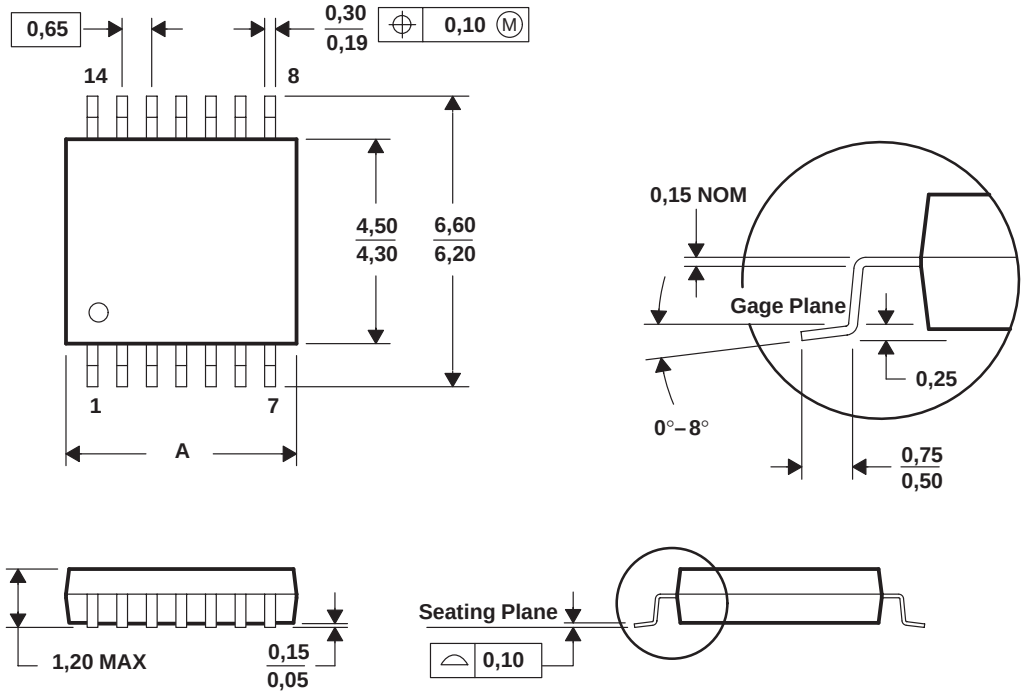
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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