



LC²MOS Precision 5 V/3 V Quad SPST Switches

ADG511/ADG512/ADG513

FEATURES

- +3 V, +5 V or ± 5 V Power Supplies
- Ultralow Power Dissipation ($<0.5 \mu\text{W}$)
- Low Leakage ($<100 \text{ pA}$)
- Low On Resistance ($<50 \Omega$)
- Fast Switching Times
- Low Charge Injection
- TTL/CMOS Compatible
- 16-Lead DIP or SOIC Package

APPLICATIONS

- Battery-Powered Instruments
- Single Supply Systems
- Remote Powered Equipment
- 5 V Supply Systems
- Computer Peripherals such as Disk Drives
- Precision Instrumentation
- Audio and Video Switching
- Automatic Test Equipment
- Precision Data Acquisition
- Sample Hold Systems
- Communication Systems
- Compatible with ± 5 V Supply DACs and ADCs such as AD7840/AD7848, AD7870/AD7871/AD7872/AD7874/AD7875/AD7876/AD7878

GENERAL DESCRIPTION

The ADG511, ADG512 and ADG513 are monolithic CMOS ICs containing four independently selectable analog switches. These switches feature low, well-controlled on resistance and wide analog signal range, making them ideal for precision analog signal switching.

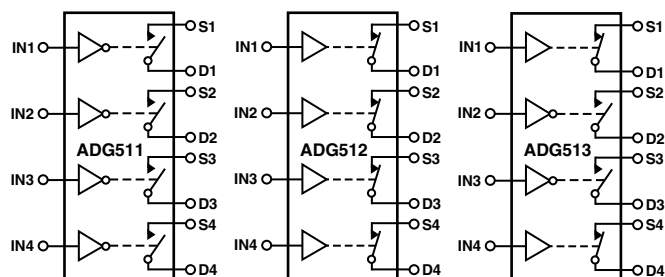
These switch arrays are fabricated using Analog Devices' advanced linear compatible CMOS (LC²MOS) process which offers the additional benefits of low leakage currents, ultralow power dissipation and low capacitance for fast switching speeds with minimum charge injection. These features make the ADG511, ADG512 and ADG513 the optimum choice for a wide variety of signal switching tasks in precision analog signal processing and data acquisition systems.

The ability to operate from single +3 V, +5 V or ± 5 V bipolar supplies make the ADG511, ADG512 and ADG513 perfect for use in battery-operated instruments, 4–20 mA loop systems and with the new generation of DACs and ADCs from Analog Devices. The use of 5 V supplies and reduced operating currents give much lower power dissipation than devices operating from ± 15 V supplies.

REV. C

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

The ADG511, ADG512 and ADG513 contain four independent SPST switches. The ADG511 and ADG512 differ only in that the digital control logic is inverted. The ADG511 switch is turned on with a logic low on the appropriate control input, while a logic high is required for the ADG512. The ADG513 contains two switches whose digital control logic is similar to that of the ADG511 while the logic is inverted in the remaining two switches.

PRODUCT HIGHLIGHTS

- 5 Volt Single Supply Operation**
The ADG511/ADG512/ADG513 offers high performance, including low on resistance and wide signal range, fully specified and guaranteed with +3 V, ± 5 V as well as +5 V supply rails.
- Ultralow Power Dissipation**
CMOS construction ensures ultralow power dissipation.
- Low R_{ON}**
- Break-Before-Make Switching**
Switches are guaranteed to have break-before-make operation. This allows multiple outputs to be tied together for multiplexer applications without the possibility of momentary shorting between channels.

ADG511/ADG512/ADG513—SPECIFICATIONS¹

Dual Supply ($V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted)

Parameter	B Versions		T Version		Unit	Test Conditions/Comments
	25°C	-40°C to +85°C	25°C	-55°C to +125°C		
ANALOG SWITCH						
Analog Signal Range		V_{DD} to V_{SS}		V_{DD} to V_{SS}	V	
R_{ON}	30	50	30	50	Ω typ Ω max	$V_D = \pm 3.5\text{ V}$, $I_S = -10\text{ mA}$; $V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	± 0.025 ± 0.1	± 2.5	± 0.025 ± 0.1	± 2.5	nA typ nA max	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ $V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$; Test Circuit 2
Drain OFF Leakage I_D (OFF)	± 0.025 ± 0.1	± 2.5	± 0.025 ± 0.1	± 2.5	nA typ nA max	$V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$; Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.05 ± 0.2	± 5	± 0.05 ± 0.2	± 5	nA typ nA max	$V_D = V_S = \pm 4.5\text{ V}$; Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current I_{INL} or I_{INH}	0.005	± 0.1	0.005	± 0.1	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
DYNAMIC CHARACTERISTICS²						
t_{ON}	200	375	200	375	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = \pm 3\text{ V}$; Test Circuit 4
t_{OFF}	120	150	120	150	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = \pm 3\text{ V}$; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG513 Only)	100		100		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_{S1} = V_{S2} = 3\text{ V}$; Test Circuit 5
Charge Injection	11		11		pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 10\text{ nF}$; Test Circuit 6
OFF Isolation	68		68		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 8
C_S (OFF)	9		9		pF typ	$f = 1\text{ MHz}$
C_D (OFF)	9		9		pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	35		35		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS						
V_{DD}		+4.5/5.5		+4.5/5.5	V min/max	
V_{SS}		-4.5/-5.5		-4.5/-5.5	V min/max	
I_{DD}	0.0001	1	0.0001	1	μA typ μA max	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ Digital Inputs = 0 V or 5 V
I_{SS}	0.0001	1	0.0001	1	μA typ μA max	

NOTES

¹Temperature ranges are as follows: B Versions -40°C to +85°C; T Version -55°C to +125°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply ($V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted)

Parameter	B Versions		T Version		Unit	Test Conditions/Comments
	25°C	−40°C to +85°C	25°C	−55°C to +125°C		
ANALOG SWITCH						
Analog Signal Range		0 V to V _{DD}		0 V to V _{DD}	V	
R _{ON}	45	75	45	75	Ω typ Ω max	V _D = 3.5 V, I _S = −10 mA; V _{DD} = 4.5 V
LEAKAGE CURRENTS						
Source OFF Leakage I _S (OFF)	±0.025 ±0.1	±2.5	±0.025 ±0.1	±2.5	nA typ nA max	V _{DD} = 5.5 V V _D = 4.5/1 V, V _S = 1/4.5 V; Test Circuit 2
Drain OFF Leakage I _D (OFF)	±0.025 ±0.1	±2.5	±0.025 ±0.1	±2.5	nA typ nA max	V _D = 4.5/1 V, V _S = 1/4.5 V; Test Circuit 2
Channel ON Leakage I _D , I _S (ON)	±0.05 ±0.2	±5	±0.05 ±0.2	±5	nA typ nA max	V _D = V _S = 4.5 V/1 V; Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V _{INH}		2.4		2.4	V min	
Input Low Voltage, V _{INL}		0.8		0.8	V max	
Input Current I _{INL} or I _{INH}	0.005	±0.1	0.005	±0.1	μA typ μA max	V _{IN} = V _{INL} or V _{INH}
DYNAMIC CHARACTERISTICS ²						
t _{ON}	250	500	250	500	ns typ ns max	R _L = 300 Ω, C _L = 35 pF; V _S = 2 V; Test Circuit 4
t _{OFF}	50	100	50	100	ns typ ns max	R _L = 300 Ω, C _L = 35 pF; V _S = 2 V; Test Circuit 4
Break-Before-Make Time Delay, t _D (ADG513 Only)	200		200		ns typ	R _L = 300 Ω, C _L = 35 pF; V _{S1} = V _{S2} = 2 V; Test Circuit 5
Charge Injection	16		16		pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 10 nF; Test Circuit 6
OFF Isolation	68		68		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; Test Circuit 8
C _S (OFF)	9		9		pF typ	f = 1 MHz
C _D (OFF)	9		9		pF typ	f = 1 MHz
C _D , C _S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						
V _{DD}		4.5/5.5		4.5/5.5	V min/max	
I _{DD}	0.0001	1	0.0001	1	μA typ μA max	V _{DD} = 5.5 V Digital Inputs = 0 V or 5 V

NOTES

¹Temperature ranges are as follows: B Versions -40°C to +85°C; T Version -55°C to +125°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply ($V_{DD} = 3.3\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, GND = 0 V, unless otherwise noted)

NOTES

¹Temperature range is as follows: B Version -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

V _{DD} to V _{SS}	44 V
V _{DD} to GND	–0.3 V to +25 V
V _{SS} to GND	+0.3 V to –25 V
Analog, Digital Inputs ²	V _{SS} – 2 V to V _{DD} + 2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Extended (T Version)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Cerdip Package, Power Dissipation	900 mW
θ _{JA} Thermal Impedance	76°C/W
Lead Temperature, Soldering (10 sec)	300°C

Plastic Package, Power Dissipation	470 mW
θ _{JA} Thermal Impedance	117°C/W
Lead Temperature, Soldering (10 sec)	260°C
SOIC Package, Power Dissipation	600 mW
θ _{JA} Thermal Impedance	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG511/ADG512/ADG513 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

Model ¹	Temperature Range ²	Package Option ³
ADG511BN	–40°C to +85°C	N-16
ADG511BR	–40°C to +85°C	R-16A
ADG511ABR ⁴	–40°C to +85°C	R-16A
ADG511TQ ⁴	–55°C to +125°C	Q-16
ADG512BN	–40°C to +85°C	N-16
ADG512BR	–40°C to +85°C	R-16A
ADG512ABR ⁴	–40°C to +85°C	R-16A
ADG513BN	–40°C to +85°C	N-16
ADG513BR	–40°C to +85°C	R-16A
ADG513ABR ⁴	–40°C to +85°C	R-16A

NOTES

¹For availability of MIL-STD-883, Class B processed parts, contact factory.

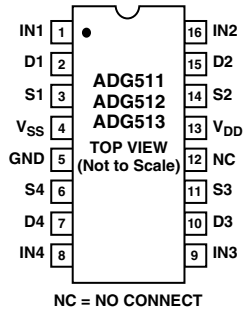
²3.3 V specifications apply over 0°C to 70°C temperature range.

³N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); Q = Cerdip.

⁴Trench isolated latch-up proof parts. See Trench Isolation section.

ADG511/ADG512/ADG513

PIN CONFIGURATION (DIP/SOIC)



Truth Table (ADG511/ADG512)

ADG511 In	ADG512 In	Switch Condition
0	1	ON
1	0	OFF

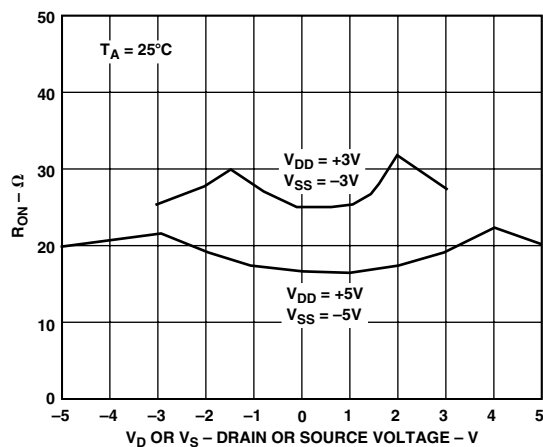
Truth Table (ADG513)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

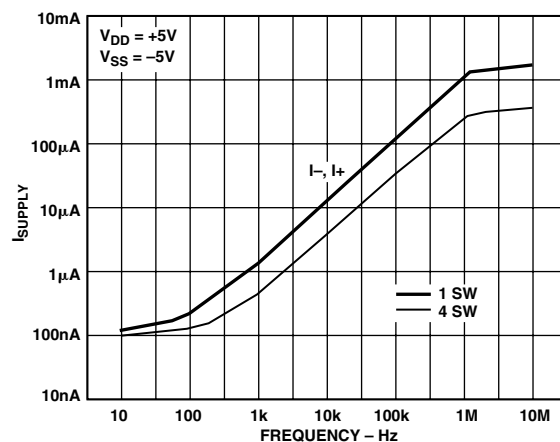
TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
V_{SS}	Most Negative Power Supply Potential in dual supplies. In single supply applications, it may be connected to GND.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
R_{ON}	Ohmic Resistance between D and S.
I_S (OFF)	Source Leakage Current with the switch "OFF."
I_D (OFF)	Drain Leakage Current with the switch "OFF."
I_D, I_S (ON)	Channel Leakage Current with the switch "ON."
V_D (V_S)	Analog Voltage on terminals D, S.
C_S (OFF)	"OFF" Switch Source Capacitance.
C_D (OFF)	"OFF" Switch Drain Capacitance.
C_D, C_S (ON)	"ON" Switch Capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_D	"OFF" or "ON" time measured between the 90% points of both switches when switching from one address state to another.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.

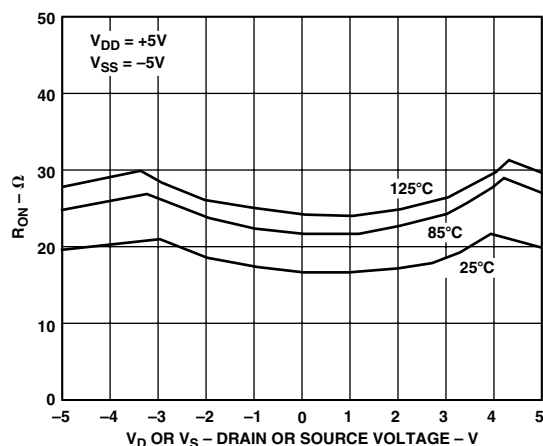
Typical Performance Characteristics—ADG511/ADG512/ADG513



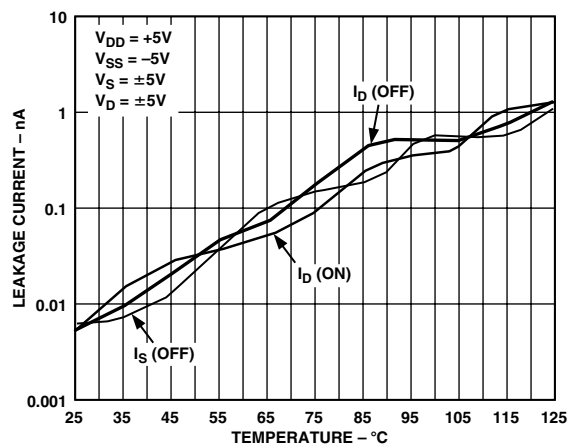
TPC 1. On Resistance as a Function of V_D (V_S) Dual Supplies



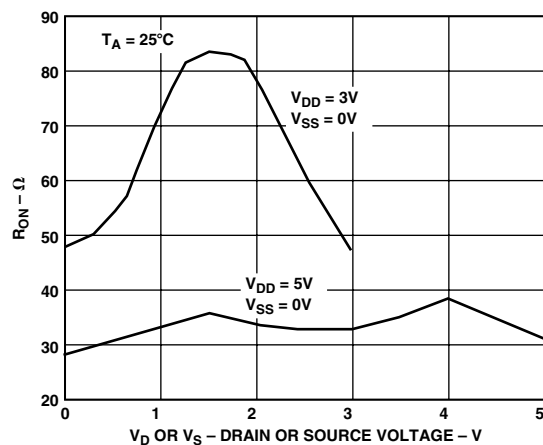
TPC 4. Supply Current vs. Input Switching Frequency



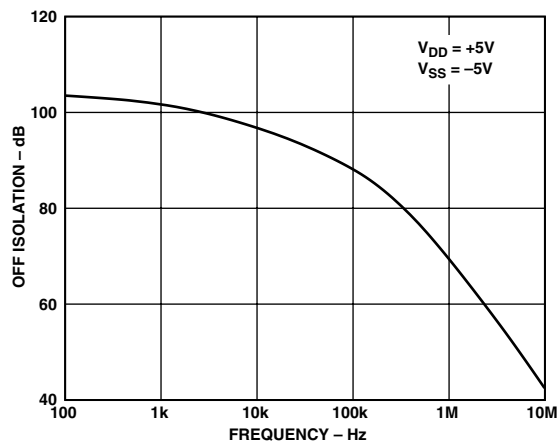
TPC 2. On Resistance as a Function of V_D (V_S) for Different Temperatures



TPC 5. Leakage Currents as a Function of Temperature

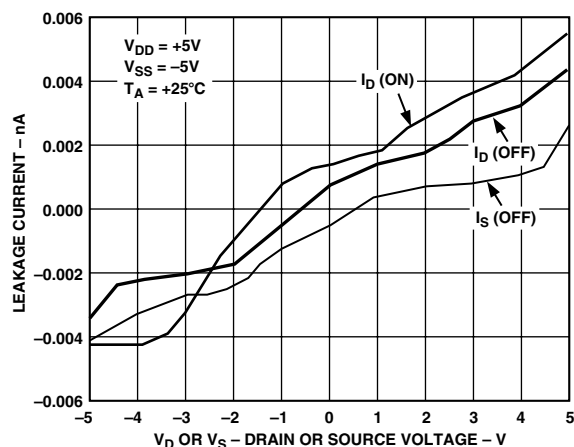


TPC 3. On Resistance as a Function of V_D (V_S) Single Supply

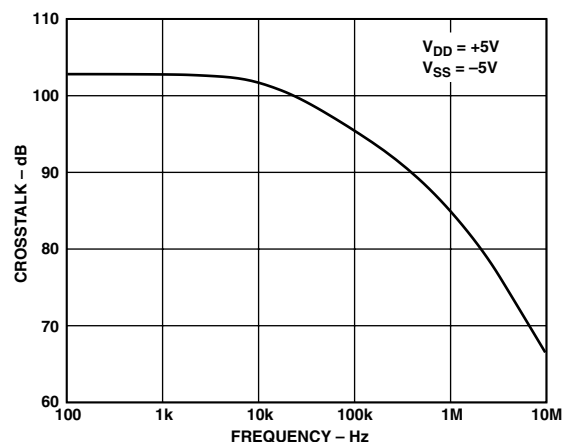


TPC 6. Off Isolation vs. Frequency

ADG511/ADG512/ADG513



TPC 7. Leakage Currents as a Function of V_D (V_S)



TPC 8. Crosstalk vs. Frequency

APPLICATION

Figure 1 illustrates a precise sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an OP07. During the track mode, SW1 is closed and the output V_{OUT} follows the input signal V_{IN} . In the hold mode, SW1 is opened and the signal is held by the hold capacitor C_H .

Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG511/ADG512/ADG513 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a poly-styrene hold capacitor. The droop rate for the circuit shown is typically $15 \mu V/\mu s$.

A second switch, SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp OP07, which will minimize charge injection effects. Pedestal error is also reduced by the compensation

network R_C and C_C . This compensation network also reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the ± 3 V input range. The acquisition time is $2.5 \mu s$ while the settling time is $1.85 \mu s$.

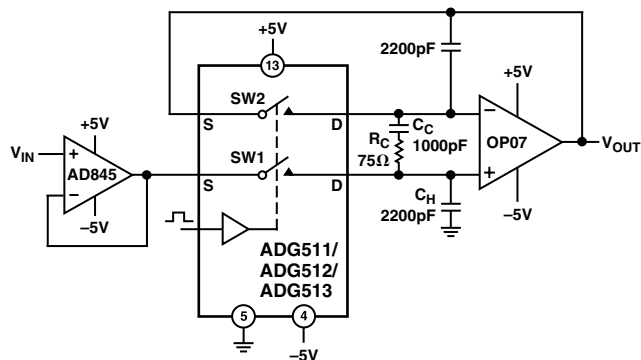


Figure 1. Accurate Sample-and-Hold

TRENCH ISOLATION

The MOS devices that make up the ADG511A/ADG512A/ADG513A are isolated from each other by an oxide layer (trench) (see Figure 2). When the NMOS and PMOS devices are not electrically isolated from each other, there exists the possibility of "latch-up" caused by parasitic junctions between CMOS transistors. Latch-up is caused when P-N junctions that are normally reverse biased, become forward biased, causing large currents to flow. This can be destructive.

CMOS devices are normally isolated from each other by *Junction Isolation*. In Junction Isolation the N and P wells of the CMOS transistors form a diode that is reverse biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A Silicon-Controlled Rectifier (SCR)-type circuit is formed by the two transistors, causing a significant amplification of the current that, in turn, leads to latch-up. With Trench Isolation, this diode is removed; the result is a latch-up-proof circuit.

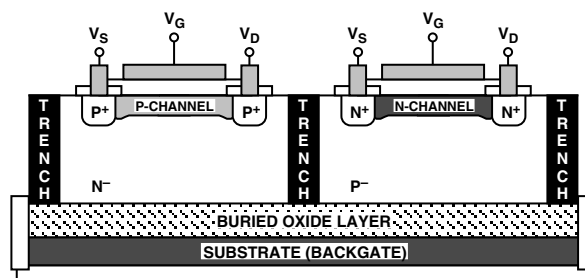
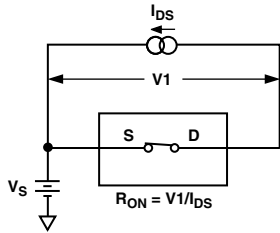
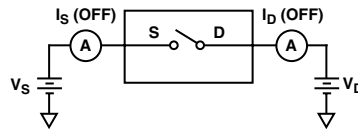


Figure 2. Trench Isolation

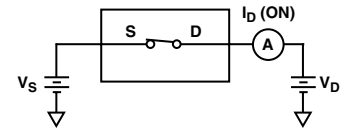
Test Circuits



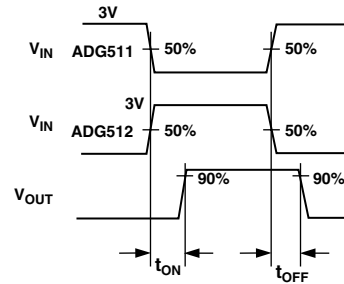
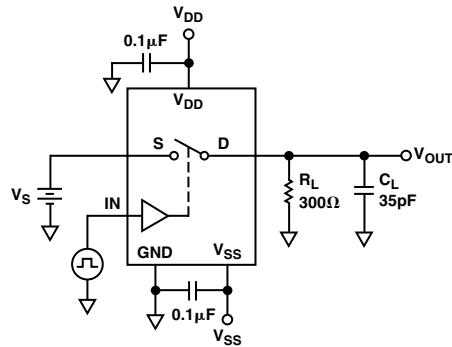
Test Circuit 1. On Resistance



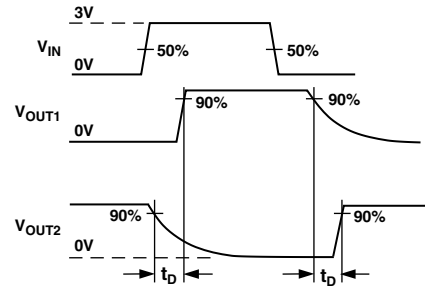
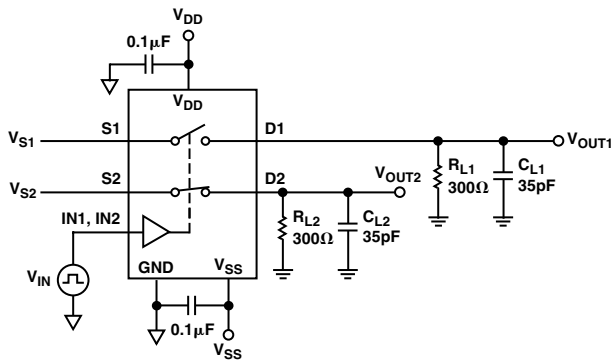
Test Circuit 2. Off Leakage



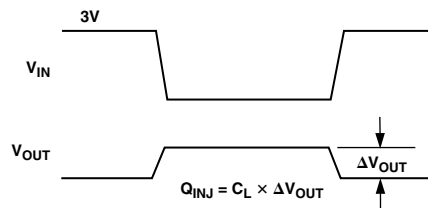
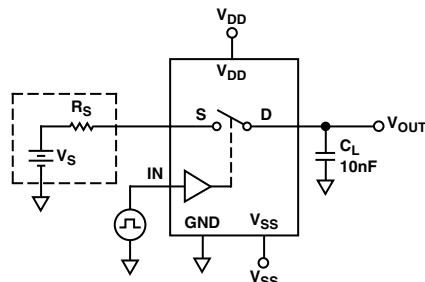
Test Circuit 3. On Leakage



Test Circuit 4. Switching Times

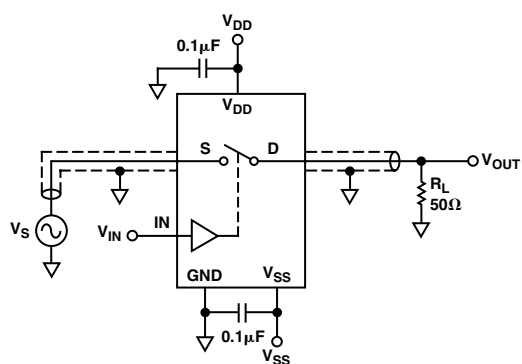


Test Circuit 5. Break-Before-Make Time Delay

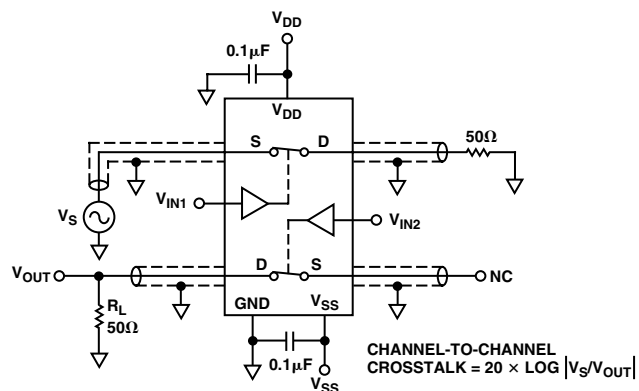


Test Circuit 6. Charge Injection

ADG511/ADG512/ADG513



Test Circuit 7. Off Isolation



Test Circuit 8. Channel-to-Channel Crosstalk

Dimensions shown in inches and (mm).

ADG511/ADG512/ADG513—Revision History

Location	Page
Data Sheet changed from REV. B to REV. C.	
Changes to Specifications table, Dual Supply, and Notes: “T Versions” made singular	2
Changes to Specifications table, Single Supply, and Notes: “T Versions” made singular	3
Change to Ordering Guide: Removed one line	5

C00036b-0-5/01(C)

PRINTED IN U.S.A.