Dual 3A Current Sharing 2.5MHz High Efficiency Synchronous Buck Regulator

ISL78236

The ISL78236 is a dual output 3A/3A integrated FET buck regulator for point-of-load power applications. The supply voltage range is from 2.8V to 6V, allowing for the use of a single Li+ cell, three NiMH cells or a regulated 3V/5V bus input. It is optimized for regulating output voltages down to 1.2V. Each channel provides an output current up to 3A which can be combined to form a single 6A output in current sharing mode. The two channels operate 180° out-of-phase to reduce input RMS current and EMI.

The ISL78236 integrates a pair of low ON-resistance P-channel and N-channel internal MOSFETs to maximize efficiency and minimize external component count. It can operate up to 100% duty cycle to maximize operating life as battery voltage drops out. When supplying 3A on each channel, the 100% duty cycle operation limits the dropout voltage to less than 250mV. Other features include internal digital soft-start, independent channel enable for power sequencing, overcurrent protection, and thermal shutdown.

The ISL78236 is offered in a 24 Ld 4mmx4mm QFN package with 1mm maximum height. The complete converter occupies less than 1.5cm^2 area.

The ISL78236 is AEC - Q100 qualified and is rated for the automotive temperature range (-40°C to +105°C).

Features

- Dual 3A/3A independent outputs
- 2.5MHz synchronous buck regulator with internal MOSFETs up to 95% efficiency
- 2% voltage reference accuracy over-temperature
- 6A current sharing mode operation
- Internal or external compensation
- Peak current limiting and hiccup mode short circuit protection
- Reverse overcurrent protection
- Over-temperature protection shutdown
- AEC - Q100 qualified

Applications

- DSP and embedded processor power supply
- Infotainment system power
- Automotive point of load power

Related Literature

- AN1927, “ISL78236DUALEVAL1Z Dual 3A Low Quiescent Current High Efficiency Synchronous Buck Regulator”
- AN1928, “ISL78236CRSHEVAL1Z Current Sharing 6A Low Quiescent Current High Efficiency Synchronous Buck Regulator”

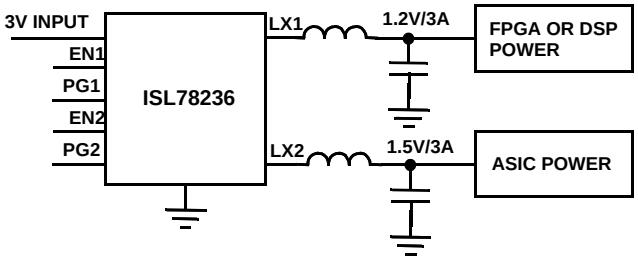


FIGURE 1. TYPICAL APPLICATION BLOCK DIAGRAM: DUAL OUTPUT 3A/3A BUCK REGULATOR

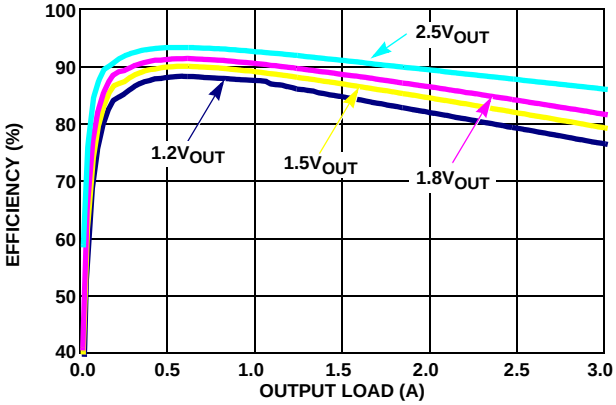


FIGURE 2. EFFICIENCY vs LOAD CURRENT, V_{IN} = 3.3V, T_A = +25°C

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Typical Applications

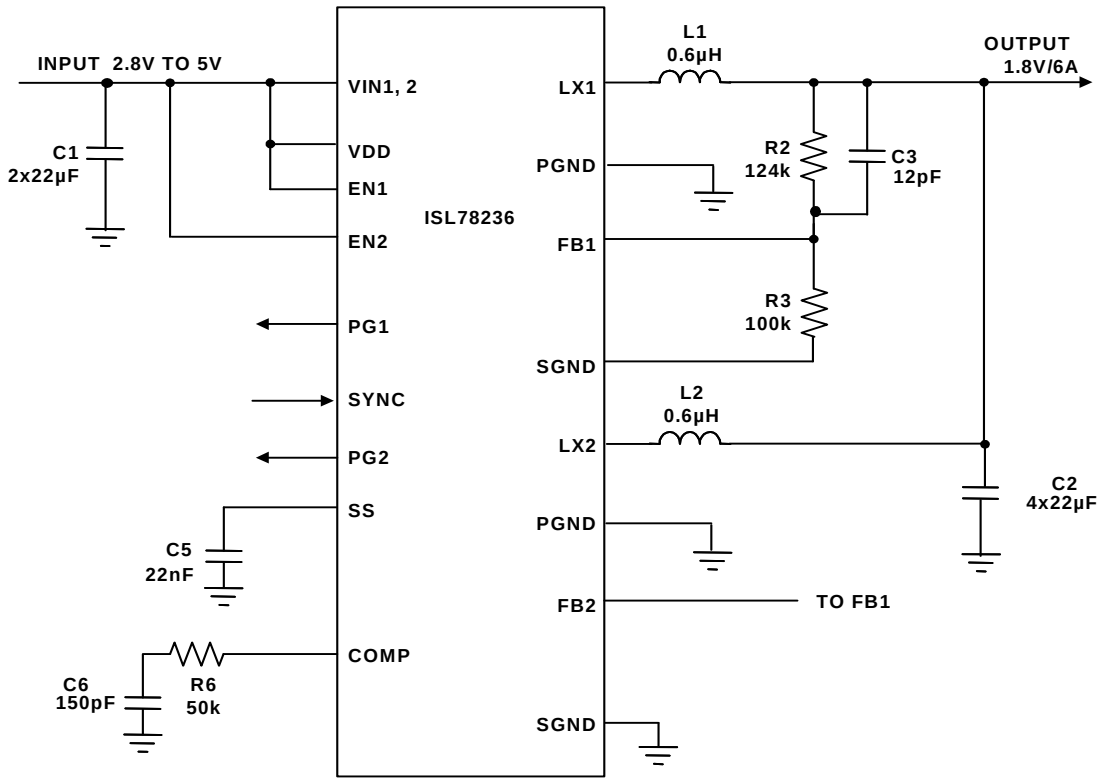


FIGURE 3. TYPICAL APPLICATION DIAGRAM - SINGLE 6A

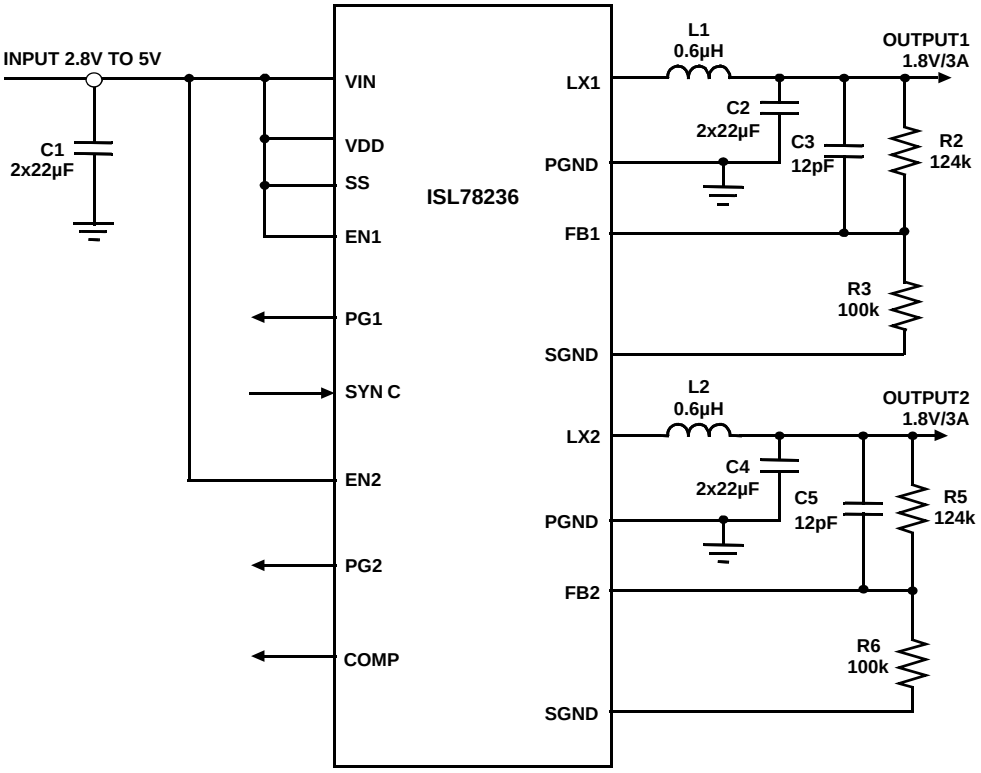


FIGURE 4. TYPICAL APPLICATION DIAGRAM - DUAL 3A OUTPUTS

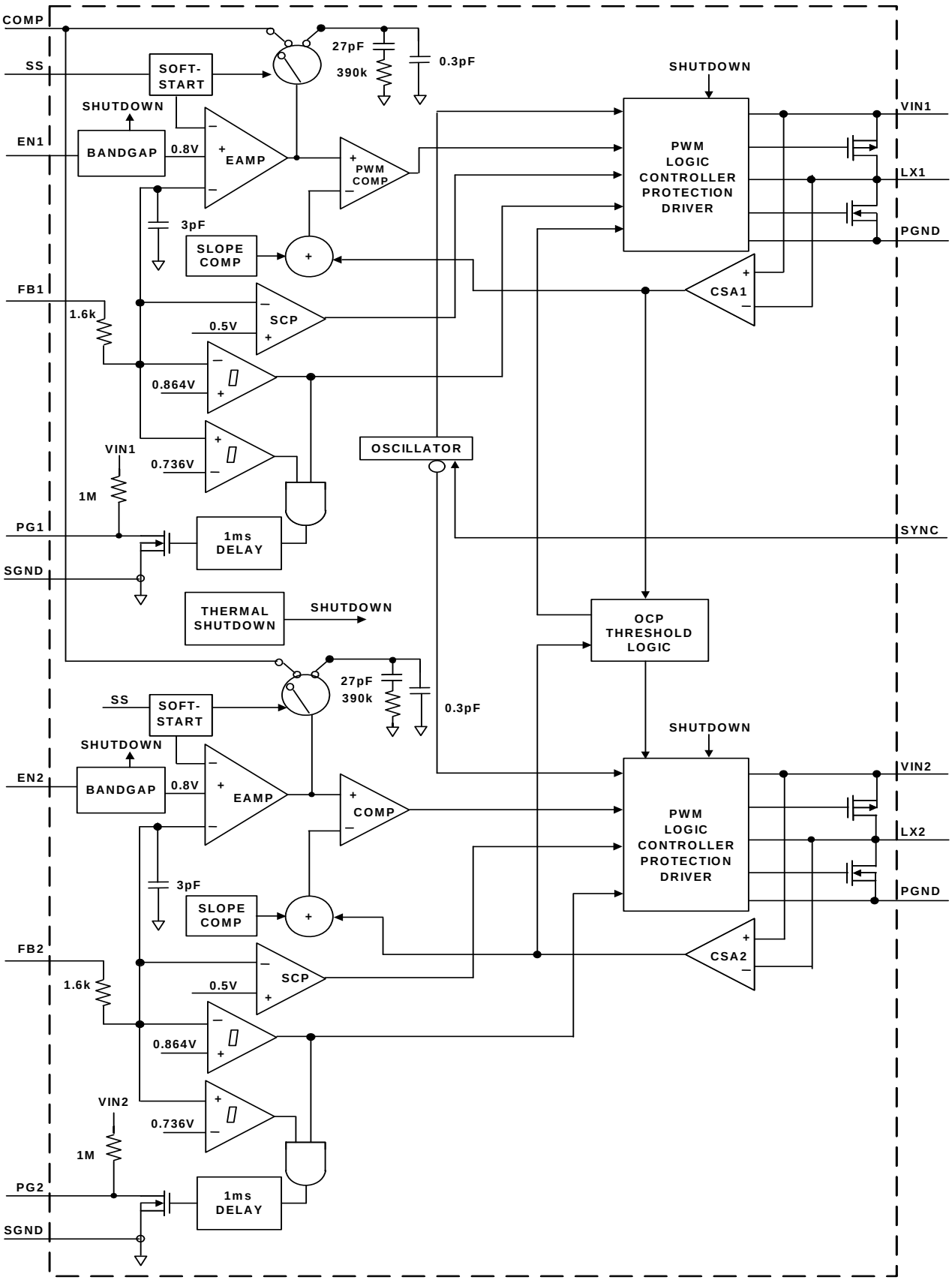
TABLE 1. COMPONENT VALUE SELECTION FOR DUAL OUTPUT OPERATION

V_{OUT}	1.2V	1.5V	1.8V	2.5V	3.3V
C1	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF
C2	4x22µF	4X22µF	4x22µF	4x22µF	4x22µF
L1 (or L2)	0.5~1.1µH	0.5~1.1µH	0.5~1.68µH	0.5~1.68µH	0.5~2.2µH
R2 (or R5)	50k	87.5k	124k	212.5k	312.5k
R3 (or R6)	100k	100k	100k	100k	100k

TABLE 2. COMPONENT VALUE SELECTION FOR CURRENT SHARING OPERATION

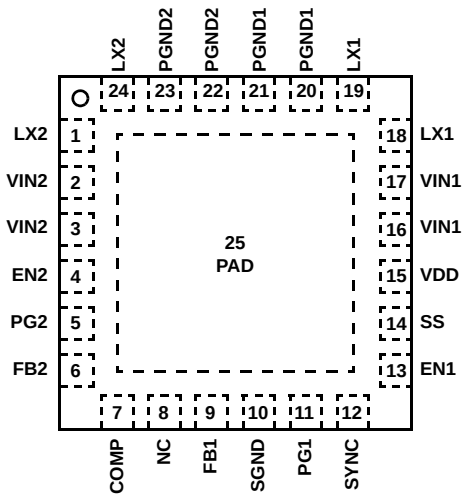
V_{OUT}	1.2V	1.5V	1.8V	2.5V	3.3V
C1	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF
C2 (or C4)	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF
L1 (or L2)	0.5~1.1µH	0.5~1.1µH	0.5~1.68µH	0.5~1.68µH	0.5~2.2µH
R2	50k	87.5k	124k	212.5k	312.5k
R3	100k	100k	100k	100k	100k
R6	33k	31k	30k	29k	28k
C6	180pF	150pF	150pF	150pF	150pF

Block Diagram



Pin Configuration

ISL78236
(24 LD QFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 24	LX2	Switching node connection for Channel 2.
4	EN2	Regulator Channel 2 enable pin. Enable the output, VOUT2, when driven to high. Shutdown VOUT2 and discharge output capacitor when driven to low. Do not leave this pin floating.
5	PG2	Active high Power-Good (PG) indicator for Channel 2. After power-up or EN2 High, this output is a 1ms delayed Power-Good signal for the Channel 2 output voltage.
6	FB2	The feedback network of the Channel 2 regulator. FB2 is the negative input to the transconductance error amplifier. The output voltage is set by an external resistor divider from VOUT2 connected to FB2. The power-good output and undervoltage lockout protection circuitry uses FB2 to monitor the Channel 1 regulator output voltage.
7	COMP	COMP pin is treated as a No Connect in dual output mode operation, using only the internal compensation. If the SS pin is tied to a soft-start capacitor, external compensation is automatically used. An additional external network across COMP and SGND is required to improve the loop compensation of the amplifier in parallel current sharing operation. Connect an external RC network on COMP pin for parallel mode operation.
8	NC	No connect pin; please tie to GND for thermal relief.
9	FB1	The feedback network of the Channel 1 regulator. FB1 is the negative input to the transconductance error amplifier. The output voltage is set by an external resistor divider from VOUT1 connected to FB1. The power-good output and undervoltage lockout protection circuitry uses FB1 to monitor the Channel 1 regulator output voltage.
10	SGND	System ground.
11	PG1	Active high Power-Good (PG) indicator for Channel 1. After power-up or EN1 High, this output is a 1ms delayed power-good signal for the Channel 1 output voltage.
12	SYNC	Connect to logic high or input voltage VIN. Connect to an external function generator for external synchronization. Negative edge trigger. Do not leave this pin floating. **Do not tie this pin low (or to SGND).**
13	EN1	Regulator Channel 1 enable pin. Enable the output, VOUT1, when driven to high. Shut down VOUT1 and discharge output capacitor when driven to low. Do not leave this pin floating.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
14	SS	SS is used to adjust the soft-start time. When SS pin is tied to VIN, SS time is 1.5ms. SS pin is tied to VIN only in dual output mode operation. SS pin is tied to a soft-start capacitor only in parallel current sharing mode operation. Connect a capacitor from SS to SGND to adjust the soft-start time. C_{SS} should not be larger than 33nF. This capacitor, along with an internal 5µA current source, sets the soft-start interval of the converter, t_{SS}. $C_{SS}[\mu F] = 6.25 \cdot t_{SS}[s]$ (EQ. 1)
15	VDD	Input supply voltage for the logic. VDD to be at the same potential as V_{IN} +0.3/-0.5V.
16, 17 2, 3	VIN1, VIN2	Input supply voltage. Connect 22µF ceramic capacitor to power ground per channel.
18, 19	LX1	Switching node connection for Channel 1.
20, 21	PGND1	Negative supply for the power stage of Channel 1.
22, 23	PGND2	Negative supply for the power stage of Channel 2.
25	PAD	The exposed pad must be connected to the SGND pin for proper electrical performance. Add as many vias as possible to connect the PAD to a ground plane for optimal thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL78236ARZ	782 36ARZ	-40 to +105	24 Ld 4x4 QFN	L24.4x4D
ISL78236DUALEVAL1Z	Evaluation Board			
ISL78236CRSHEVAL1Z	Evaluation Board			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL78236. For more information on MSL, please see tech brief TB363.

Absolute Maximum Ratings (Reference to SGND)

VIN1, VIN2, VDD . . . . . -0.3V to +6.5V
LX1, LX2 (Note 4) . . . . . -0.3V to +6.5V
EN1, EN2, PG1, PG2, SYNC, SS. . . . . -0.3V to +6.5V
FB1, FB2, COMP . . . . . -0.3V to +2.7V
ESD Ratings
Human Body Model (Tested per AEC-Q100-002) 4kV
Machine Model (Tested per AEC-A100-003) 300V
Charged Device Model (Tested per AEC-Q100-011) 2kV
Latch Up (Per JESD-78D; Class 2, Level A; AEC-Q100-004) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld 4x4 QFN (Notes 5, 6)	36	2

Junction Temperature Range . . . . . -55°C to +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Ambient Temperature Range . . . . . -40°C to +105°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

VIN Supply Voltage Range . . . . . +2.85V to +6V
Load Current Range per Channel . . . . . 0A to 3A
Ambient Temperature Range . . . . . -40°C to +105°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Values shown for continuous voltage. Absolute Maximum Rating of 7V for a duration less than 20ms. Absolute Maximum Rating of -1.5V for duration of less than 100ns.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. For θ_{JC}, “case temperature” location is at the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, the typical specifications are measured at the following conditions: T_A = -40°C to +105°C, V_{IN} = 3.6V, EN1 = EN2 = VDD, L = 1.5µH, C1 = C2 = C4 = 2x22µF, I_{OUT1} = I_{OUT2} = 0A to 3A, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
INPUT SUPPLY						
VIN Undervoltage Lockout Threshold	V_{UVLO}	Rising		2.5	**2.85**	V
		Hysteresis	**40**	100		mV
Quiescent Supply Current	I_{VDD}	SYNC = V_{DD}, EN1 = EN2 = VDD, no load at the output		30	**70**	mA
Shutdown Supply Current	I_{SD}	V_{IN} = V_{DD} = 6V, EN1 = EN2 = SGND		8	**35**	µA
OUTPUT REGULATION						
FB1, FB2 Regulation Voltage	V_{FB}		**0.784**	0.8	**0.810**	V
FB1, FB2 Bias Current	I_{FB}	VFB = 0.75V		1		µA
Load Regulation		SYNC = VDD, output load from 0A to 6A		2		mV/A
Line Regulation		V_{IN} = V_O + 0.5V to 6V (minimal 2.85V)		0.1		%/V
Soft-start Ramp Time Cycle		SS = VDD		1.5		ms
Soft-start Charging Current	I_{SS}		**4**	5	**6**	µA
COMPENSATION						
Error Amplifier Trans-Conductance		SS = VDD		20		µA/V
		SS with Capacitor		100		µA/V
Current Sense Amplifier Gain	CSA_GAIN		**0.172**	0.2	**0.228**	V/A
Ch1/Ch2 Amplifier Gain Matching	$GAIN_{MATCH}$		**-0.05**		**+0.05**	V/A
OVERCURRENT PROTECTION						
Dynamic Current Limit ON-time	t_{OCON}			17		Clock pulses
Dynamic Current Limit OFF-time	t_{OCOFF}			8		SS cycle
Positive Peak Overcurrent Limit	I_{poc1}		**4.1**	4.8	**5.5**	A
	I_{poc2}		**4.1**	4.8	**5.5**	A
Negative Peak Overcurrent Limit	I_{noc1}		**-3.5**	-2.5	**-1.5**	A
	I_{noc2}		**-3.5**	-2.5	**-1.5**	A

Electrical Specifications

Unless otherwise noted, the typical specifications are measured at the following conditions: T_A = -40°C to +105°C, V_{IN} = 3.6V, EN1 = EN2 = VDD, L = 1.5µH, C1 = C2 = C4 = 2x22µF, I_{OUT1} = I_{OUT2} = 0A to 3A, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
LX1, LX2						
P-Channel MOSFET ON-Resistance		V_{IN} = 5.5V, I_O = 200mA		50	**75**	mΩ
		V_{IN} = 2.85V, I_O = 200mA		70	**100**	mΩ
N-Channel MOSFET ON-Resistance		V_{IN} = 5.5V, I_O = 200mA		50	**75**	mΩ
		V_{IN} = 2.85V, I_O = 200mA		70	**100**	mΩ
LX_ Maximum Duty Cycle				100		%
PWM Switching Frequency	F_S		**2.15**	2.5	**2.85**	MHz
Synchronization Frequency Range	F_{SYNC}	(Note 8)	**6**		**8**	MHz
Channel 1 to Channel 2 Phase Shift		Rising edge to rising edge timing		180		°
LX Minimum On Time		SYNC = High (PWM mode)			**140**	ns
Soft Discharge Resistance	R_{DIS}	EN = LOW	**80**	100	**120**	Ω
LX Leakage Current		V_{IN} = V_{DD} = 6V		0.1	**1**	µA
PG1, PG2						
Output Low Voltage		Sinking 1mA, VFB = 0.7V			**0.3**	V
PG Pin Leakage Current		PG = V_{IN} = 6V		0.01	**0.1**	µA
Internal PGOOD Low Rising Threshold		Percentage of nominal regulation voltage	**88**	92	**95**	%
Internal PGOOD Low Falling Threshold		Percentage of nominal regulation voltage	**85**	88	**92**	%
Delay Time (Rising Edge)		Time from VOUT_ reached regulation		1		ms
Internal PGOOD Delay Time (Falling Edge)				7	**15**	µs
EN1, EN2, SYNC						
Logic Input Low					**0.4**	V
Logic Input High			**1.5**			V
SYNC Logic Input Leakage Current	I_{SYNC}	V_{IN} = V_{DD} = 6V		0.1	**1**	µA
Enable Logic Input Leakage Current	I_{EN}	V_{IN} = V_{DD} = 6V		0.1	**1**	µA
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				25		°C

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. The operational frequency per switching channel will be half of the SYNC frequency.

Typical Operating Performance for Dual PWM Operation

Unless otherwise noted, operating conditions are: T_A = +25°C; V_{OUT1} = 1.8V; V_{OUT2} = 1.8V; I_{OUT1} = 0A to 3A; I_{OUT2} = 0A to 3A, L1 = L2 = 0.6µH, C_{OUT1} = 2x22µF, C_{OUT2} = 2x22µF, F_{SW} = 2.5MHz.

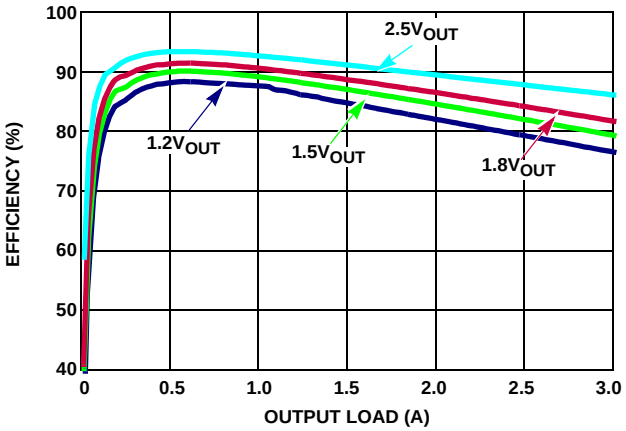


FIGURE 5. EFFICIENCY, V_{IN} = 3.3V, T_A = +25°C

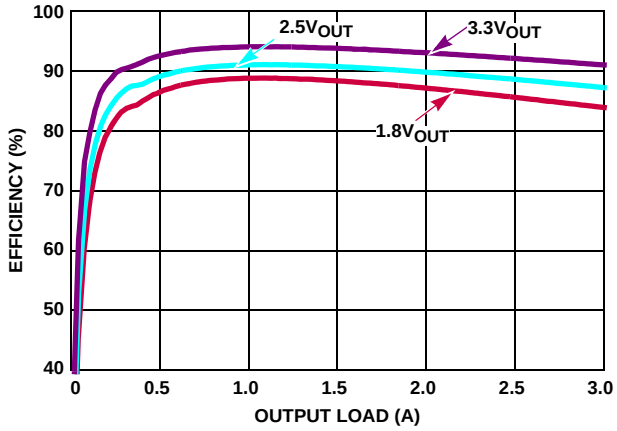


FIGURE 6. EFFICIENCY, V_{IN} = 5V, T_A = +25°C

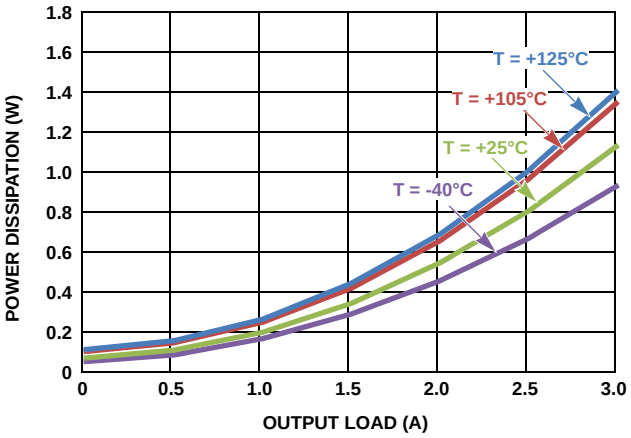


FIGURE 7. POWER DISSIPATION, V_{IN} = 3.3V, V_{OUT} = 1.8V

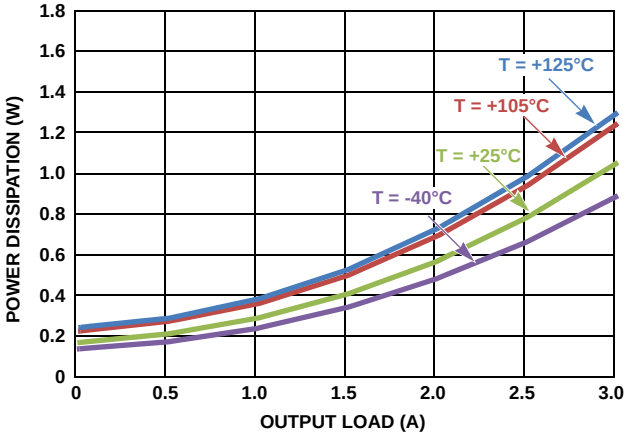


FIGURE 8. POWER DISSIPATION, V_{IN} = 5V, V_{OUT} = 1.8V

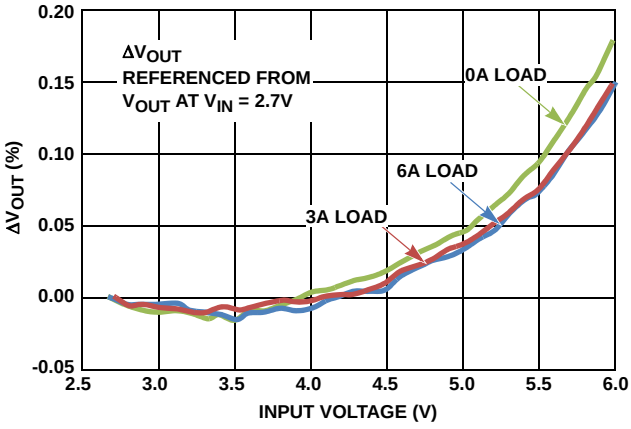


FIGURE 9. LINE REGULATION, V_{OUT} = 1.8V, T_A = +25°C

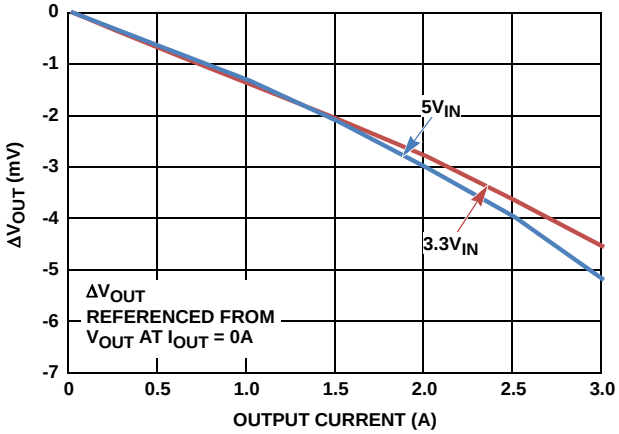


FIGURE 10. LOAD REGULATION, V_{OUT} = 1.8V, T_A = +25°C

Typical Operating Performance for Dual PWM Operation

Unless otherwise noted, operating conditions are: T_A = +25°C; V_{OUT1} = 1.8V; V_{OUT2} = 1.8V; I_{OUT1} = 0A to 3A; I_{OUT2} = 0A to 3A, L1 = L2 = 0.6µH, C_{OUT1} = 2x22µF, C_{OUT2} = 2x22µF, F_{SW} = 2.5MHz. **(Continued)**

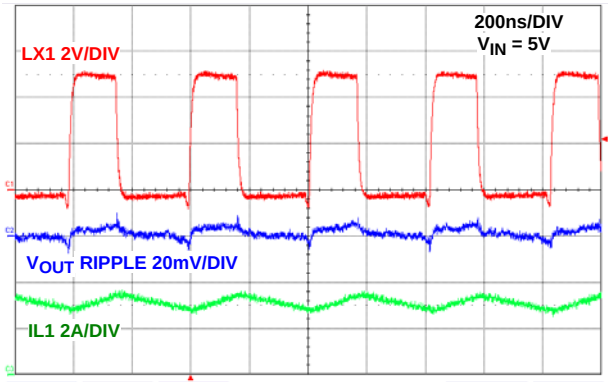


FIGURE 11. STEADY STATE OPERATION AT NO LOAD CHANNEL 1

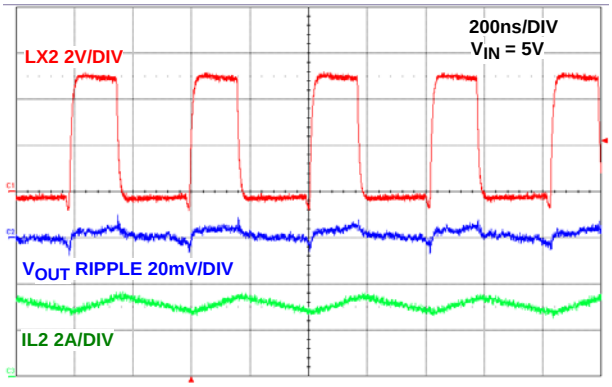


FIGURE 12. STEADY STATE OPERATION AT NO LOAD CHANNEL 2

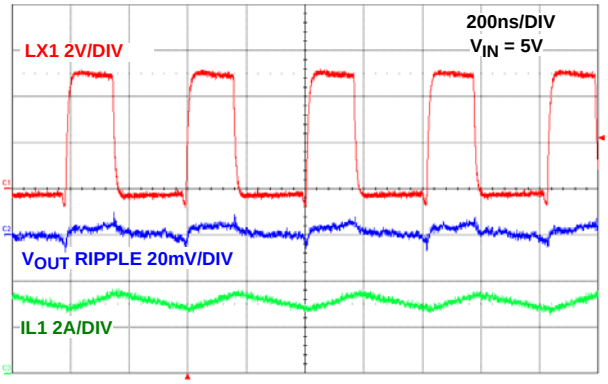


FIGURE 13. STEADY STATE OPERATION AT 3A LOAD CHANNEL 1

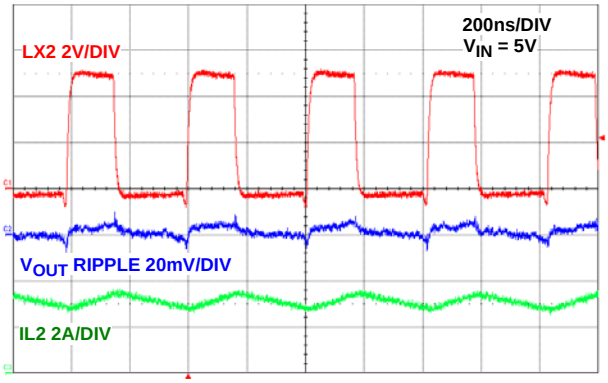


FIGURE 14. STEADY STATE OPERATION AT 3A LOAD CHANNEL 2

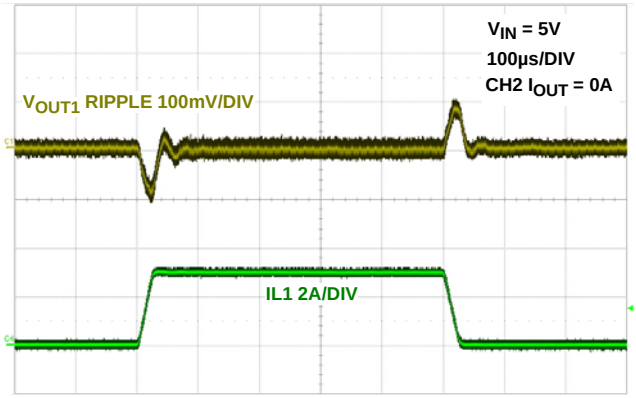


FIGURE 15. LOAD TRANSIENT CHANNEL 1

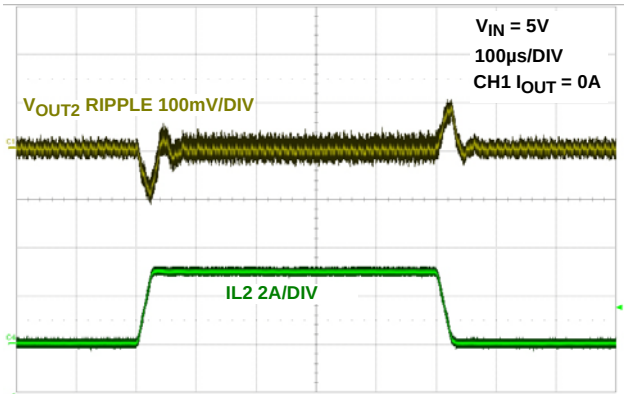


FIGURE 16. LOAD TRANSIENT CHANNEL 2

Typical Operating Performance for Dual PWM Operation

Unless otherwise noted, operating conditions are: T_A = +25°C; V_{OUT1} = 1.8V; V_{OUT2} = 1.8V; I_{OUT1} = 0A to 3A; I_{OUT2} = 0A to 3A, L1 = L2 = 0.6µH, C_{OUT1} = 2x22µF, C_{OUT2} = 2x22µF, F_{SW} = 2.5MHz. **(Continued)**

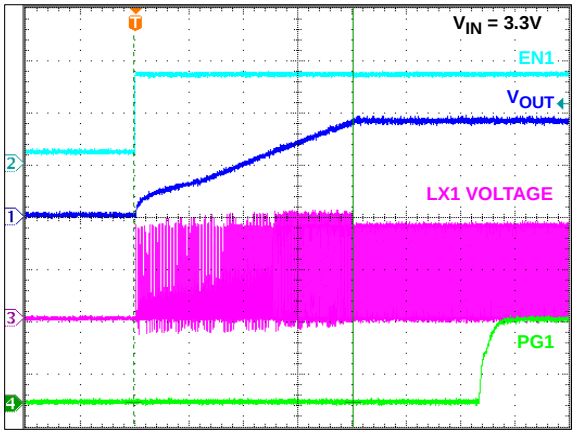


FIGURE 17. SOFT-START WITH NO LOAD CHANNEL 1

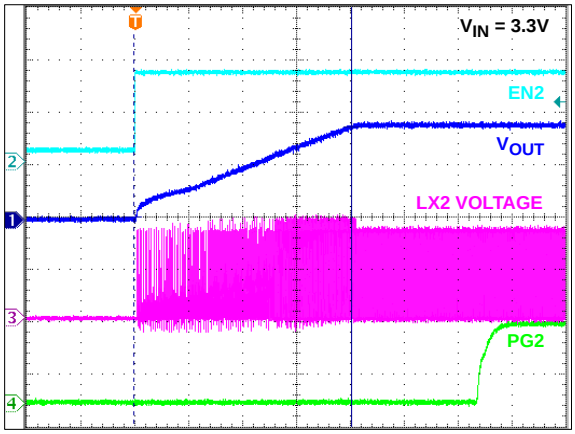


FIGURE 18. SOFT-START WITH NO LOAD CHANNEL 2

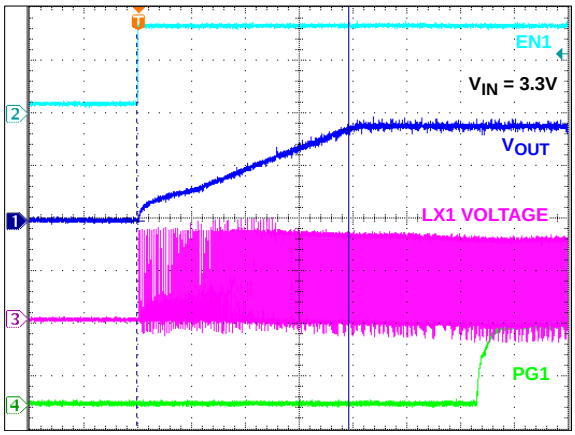


FIGURE 19. SOFT-START AT 3A LOAD CHANNEL 1

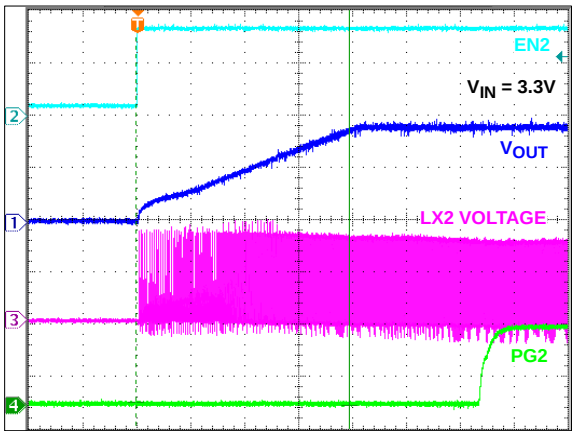


FIGURE 20. SOFT-START AT 3A LOAD CHANNEL 2

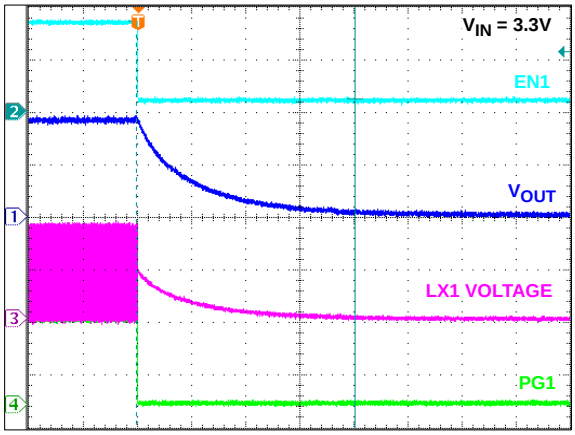


FIGURE 21. SOFT-DISCHARGE SHUTDOWN CHANNEL 1

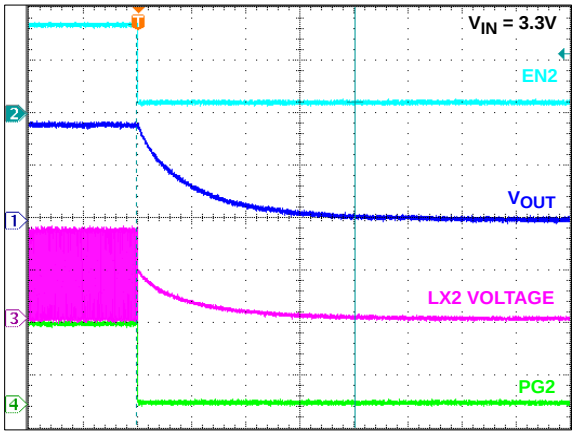


FIGURE 22. SOFT-DISCHARGE SHUTDOWN CHANNEL 2

Typical Operating Performance for Dual PWM Operation

Unless otherwise noted, operating conditions are: T_A = +25°C; V_{OUT1} = 1.8V; V_{OUT2} = 1.8V; I_{OUT1} = 0A to 3A; I_{OUT2} = 0A to 3A, L1 = L2 = 0.6µH, C_{OUT1} = 2x22µF, C_{OUT2} = 2x22µF, F_{SW} = 2.5MHz. **(Continued)**

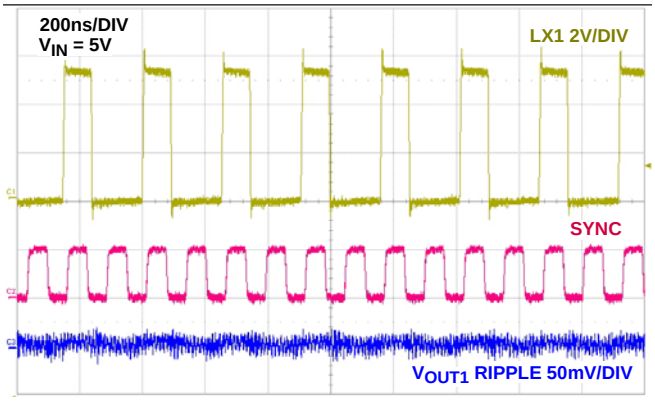


FIGURE 23. STEADY STATE OPERATION CHANNEL 1 AT NO LOAD WITH F_{SW} = 4MHz

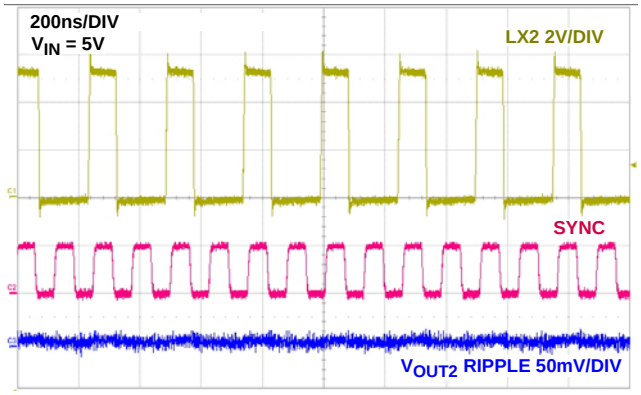


FIGURE 24. STEADY STATE OPERATION CHANNEL 2 AT NO LOAD WITH F_{SW} = 4MHz

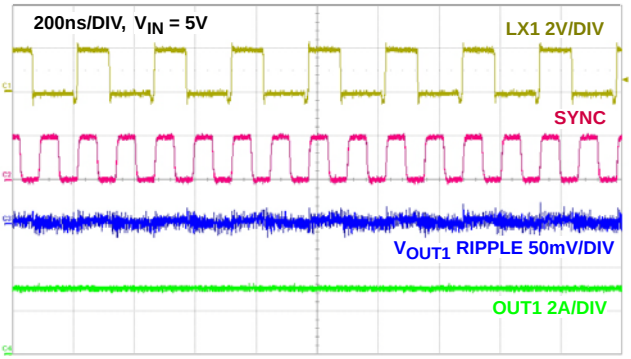


FIGURE 25. STEADY STATE OPERATION CHANNEL1 3A LOAD WITH F_{SW} = 4MHz

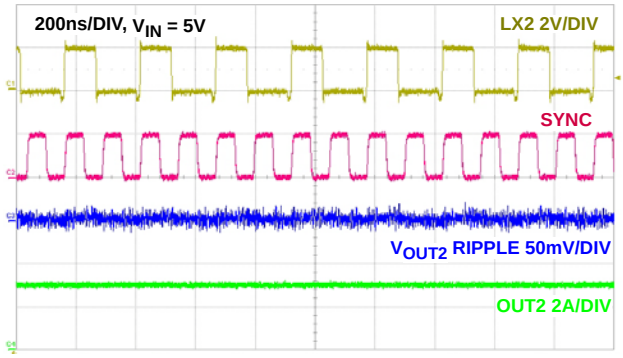


FIGURE 26. STEADY STATE OPERATION CHANNEL2 3A LOAD WITH F_{SW} = 4MHz

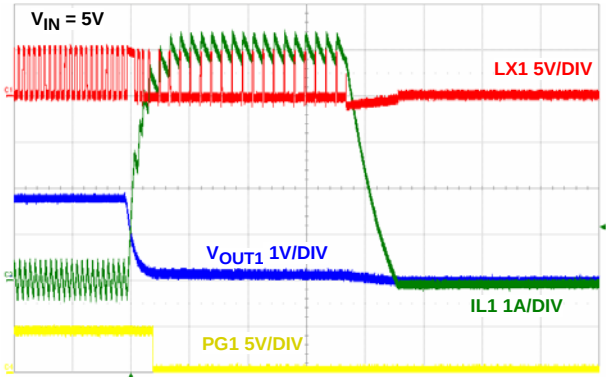


FIGURE 27. OUTPUT SHORT CIRCUIT CHANNEL 1

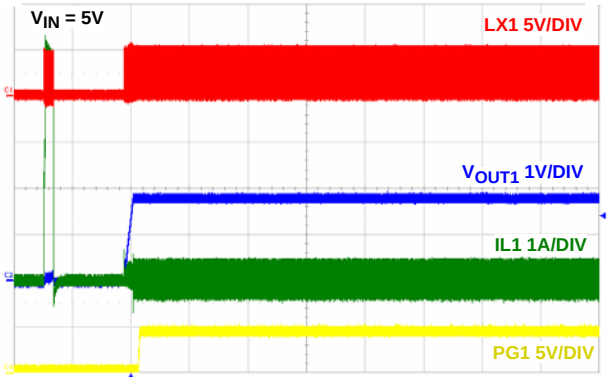


FIGURE 28. OUTPUT SHORT CIRCUIT RECOVERY (FROM HICCUP) CHANNEL 1

Typical Operating Performance for Dual PWM Operation

Unless otherwise noted, operating conditions are: T_A = +25°C; V_{OUT1} = 1.8V; V_{OUT2} = 1.8V; I_{OUT1} = 0A to 3A; I_{OUT2} = 0A to 3A, L1 = L2 = 0.6µH, C_{OUT1} = 2x22µF, C_{OUT2} = 2x22µF, F_{SW} = 2.5MHz. **(Continued)**

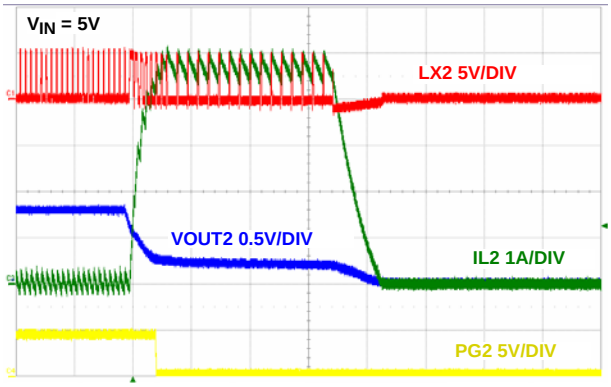


FIGURE 29. OUTPUT SHORT CIRCUIT CHANNEL 2

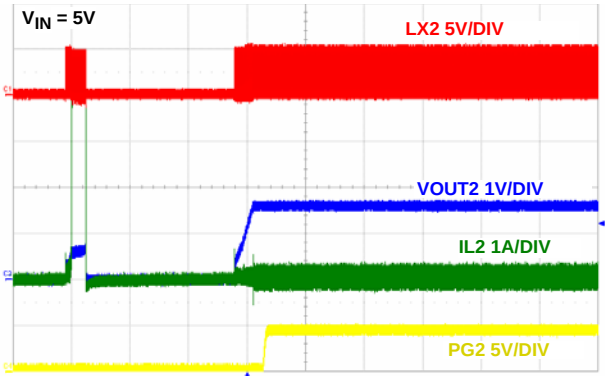


FIGURE 30. OUTPUT SHORT CIRCUIT RECOVERY (FROM HICCUP) CHANNEL 2

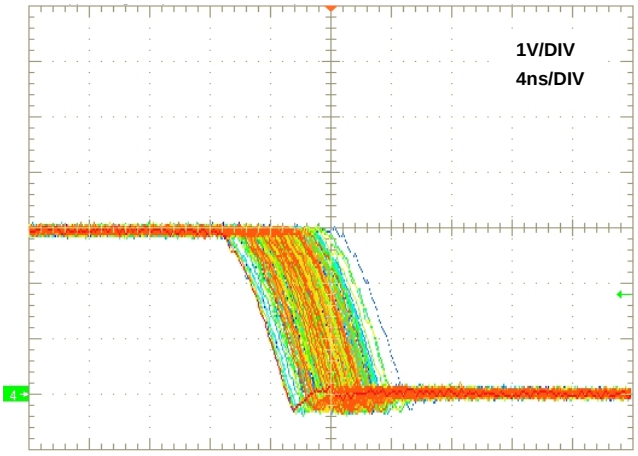


FIGURE 31. LX JITTER AT NO LOAD, V_{IN} = 3V

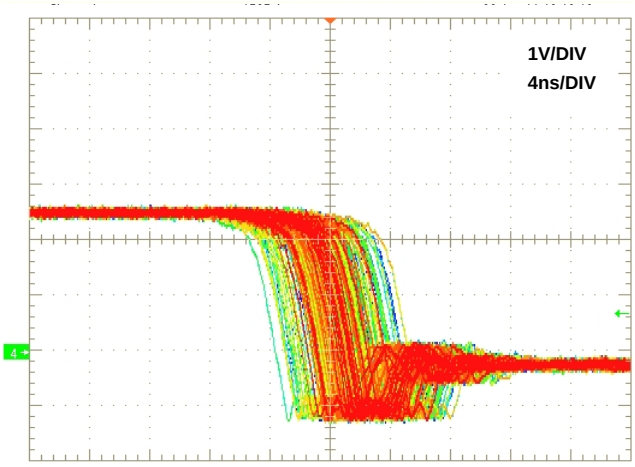


FIGURE 32. LX JITTER AT 3A LOAD, V_{IN} = 3V

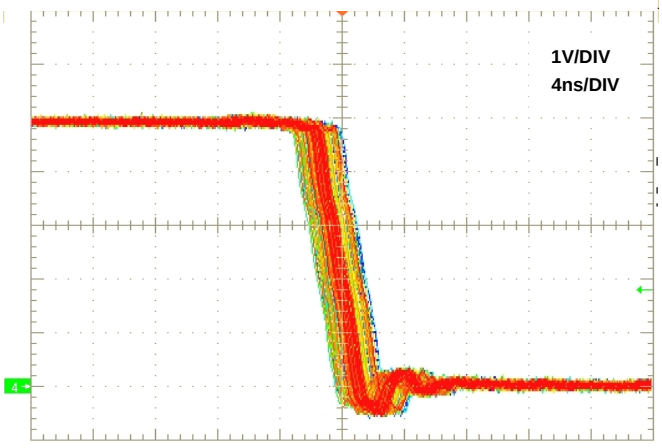


FIGURE 33. LX JITTER AT NO LOAD, V_{IN} = 5V

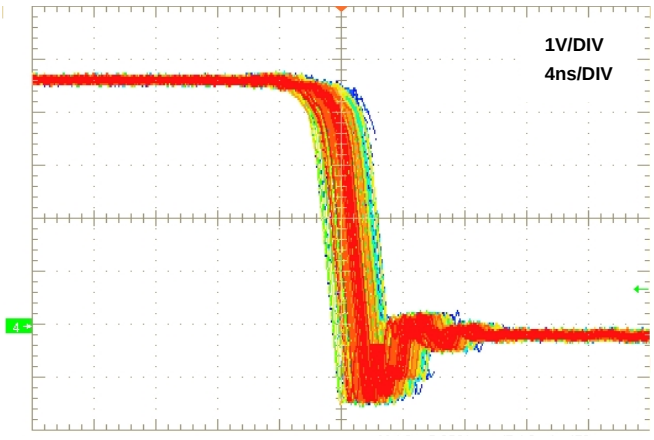


FIGURE 34. LX JITTER AT 3A LOAD, V_{IN} = 5V

Typical Performance for Current Sharing PWM Operation

Unless otherwise noted, operating conditions are: T_A = +25°C; V_{OUT} = 1.8V, I_{OUT1} + I_{OUT2} = 0A to 6A, L1 = L2 = 0.6µH, C_{OUT} = 4x22µF, F_{SW} = 2.5MHz.

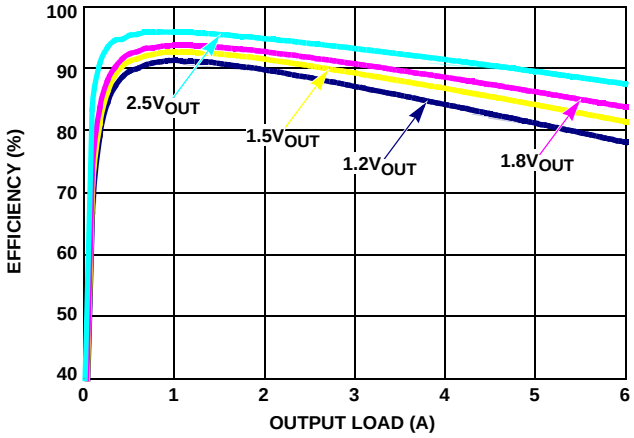


FIGURE 35. EFFICIENCY vs LOAD, V_{IN} = 3.3V, T_A = +25°C

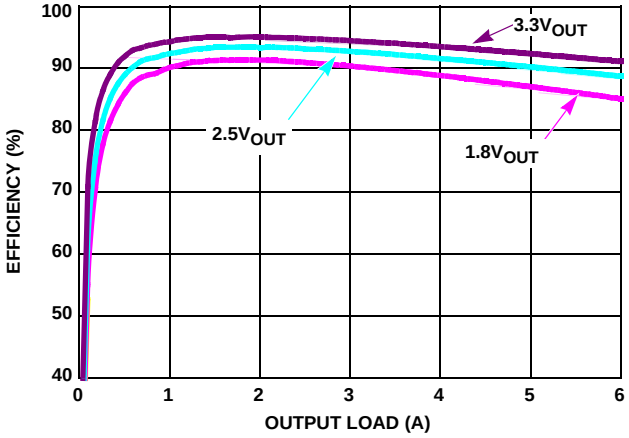


FIGURE 36. EFFICIENCY vs LOAD, V_{IN} = 5V, T_A = +25°C

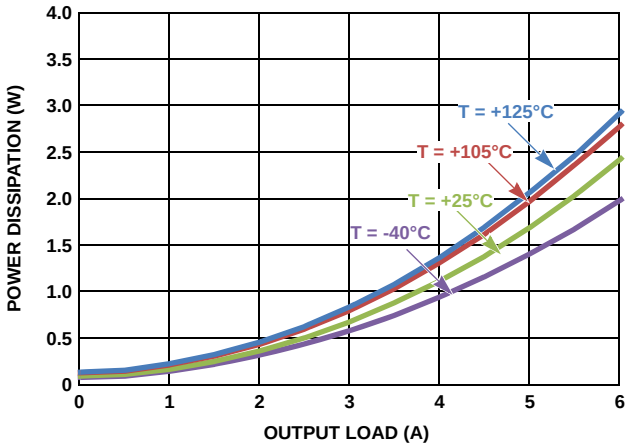


FIGURE 37. POWER DISSIPATION, V_{IN} = 3.3V, V_{OUT} = 1.8V

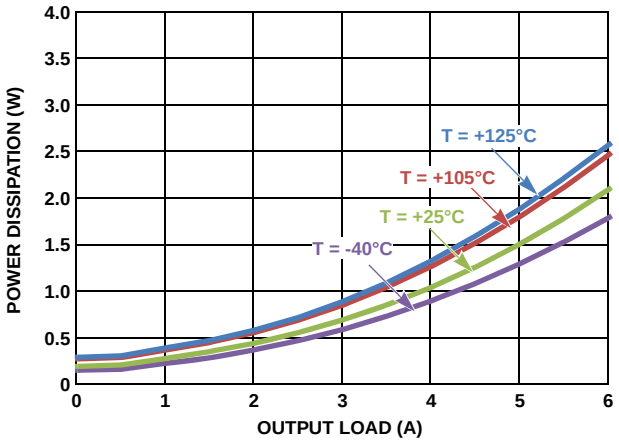


FIGURE 38. POWER DISSIPATION, V_{IN} = 5V, V_{OUT} = 1.8V

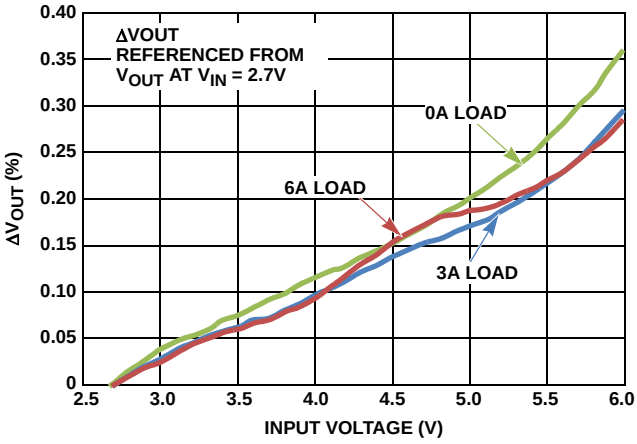


FIGURE 39. LINE REGULATION, V_{OUT} = 1.8V, T_A = +25°C

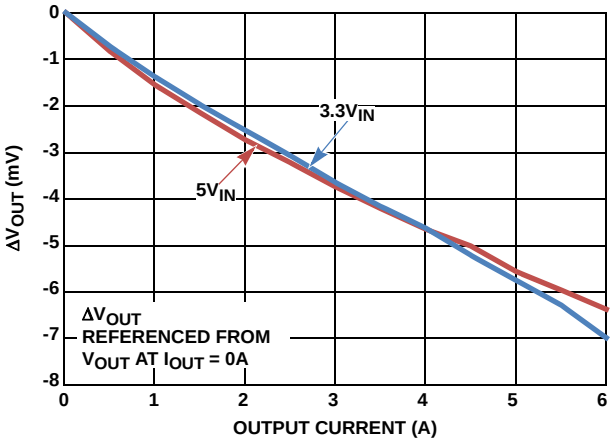


FIGURE 40. LOAD REGULATION, V_{OUT} = 1.8V, T_A = +25°C

Typical Performance for Current Sharing PWM Operation

Unless otherwise noted, operating conditions are: T_A = +25°C; V_{OUT} = 1.8V, I_{OUT1} + I_{OUT2} = 0A to 6A, L1 = L2 = 0.6µH, C_{OUT} = 4x22µF, F_{SW} = 2.5MHz.

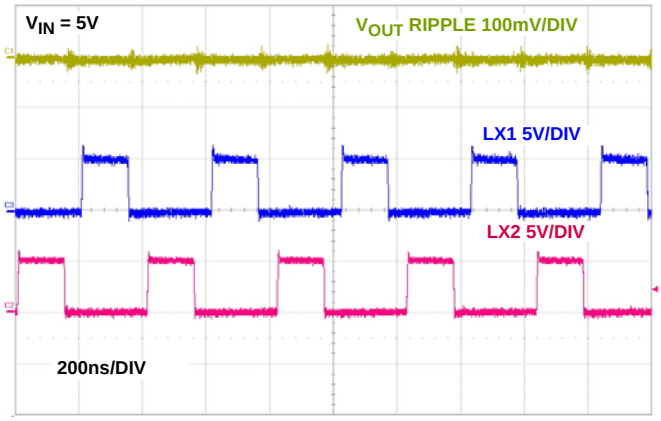


FIGURE 41. STEADY STATE OPERATION AT NO LOAD

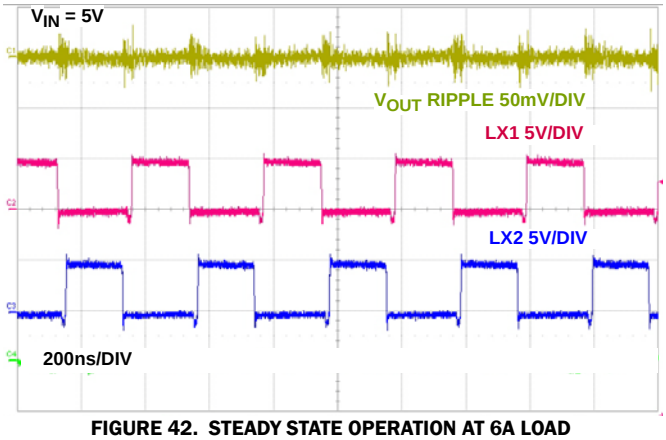


FIGURE 42. STEADY STATE OPERATION AT 6A LOAD

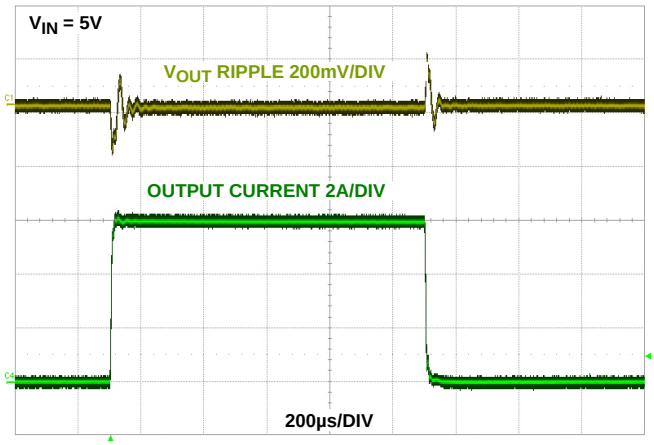


FIGURE 43. LOAD TRANSIENT RESPONSE

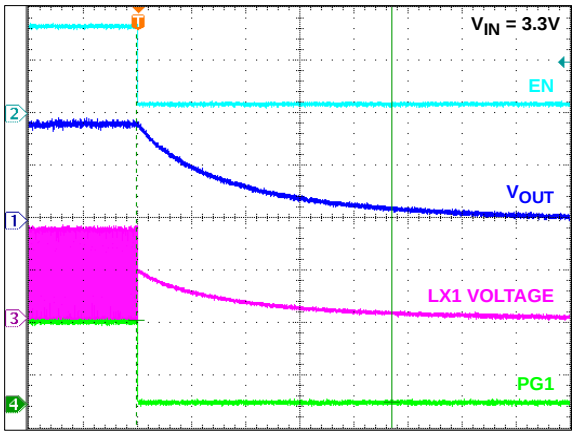


FIGURE 44. SOFT-DISCHARGE SHUTDOWN

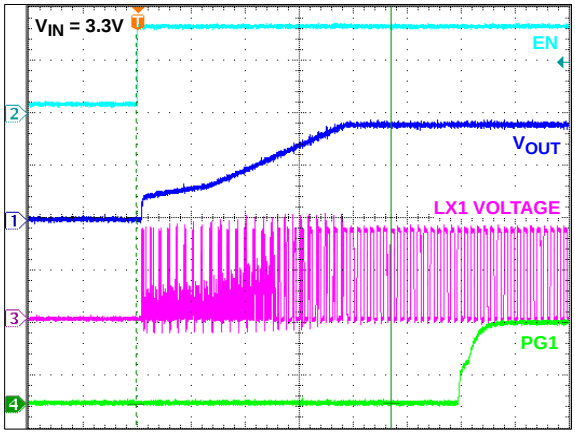


FIGURE 45. SOFT-START AT NO LOAD

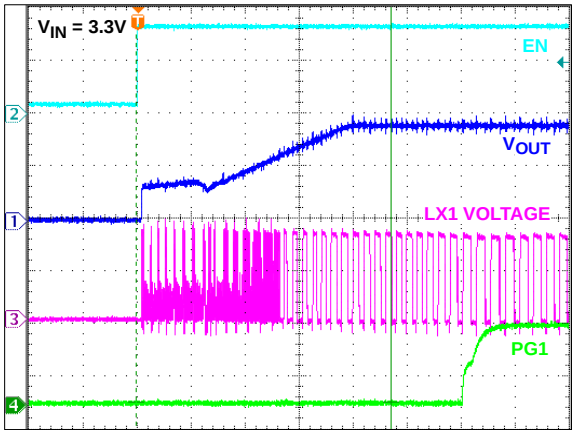


FIGURE 46. SOFT-START AT 6A LOAD

Typical Performance for Current Sharing PWM Operation

Unless otherwise noted, operating conditions are: T_A = +25°C; V_{OUT} = 1.8V, I_{OUT1} + I_{OUT2} = 0A to 6A, L1 = L2 = 0.6µH, C_{OUT} = 4x22µF, F_{SW} = 2.5MHz.

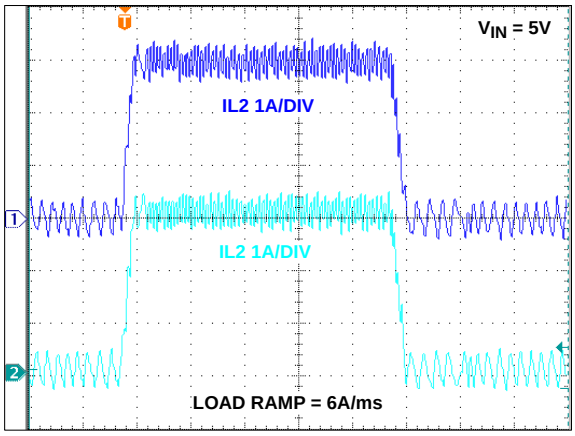


FIGURE 47. CURRENT SHARE BALANCING, 0A TO 6A

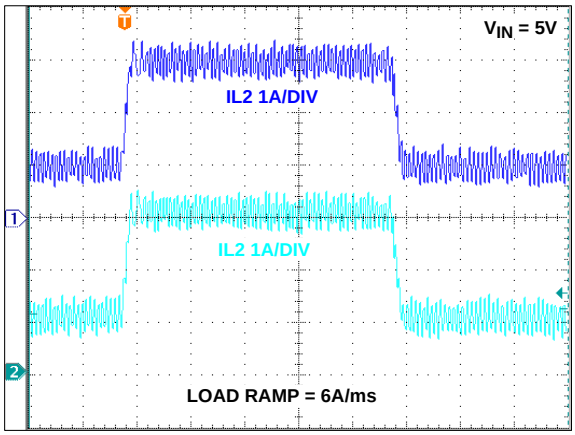


FIGURE 48. CURRENT SHARE BALANCING, 2A TO 6A

Theory of Operation

The ISL78236 is a dual 3A or single current sharing 6A step-down switching regulator optimized for low output ripple point-of-load power in automotive applications. The regulator operates at 2.5MHz internally fixed switching frequency allowing small output filter components while maintaining up to 95% efficiency. The two channels are 180° out-of-phase operation to reduce input ripple currents and EMI. The supply current is typically only 8µA when the regulator is shutdown.

PWM Control Scheme

Pulling the SYNC pin HI (>1.5V) forces the converter into PWM mode in the next switching cycle regardless of output current. Each of the channels of the ISL78236 employ the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting, as shown in the "Block Diagram" on page 5 with waveforms in Figure 49. The current loop consists of the oscillator, the PWM COMP comparator, current sensing circuit, and the slope compensation for the current loop stability. The current sensing circuit consists of the resistance of the P-channel MOSFET when it is turned on and the current sense amplifier CSA. The gain for the current sensing circuit is typically 0.2V/A. The control reference for the current loops comes from the error amplifier, EAMP, of the voltage loop.

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA1 (or CSA2 on Channel 2) and the compensation slope (0.46V/µs) reaches the control reference of the current loop, the PWM COMP comparator sends a signal to the PWM logic to turn off the P-MOSFET and to turn on the N-channel MOSFET. The N-MOSFET stays on until the end of the PWM cycle. Figure 49 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the compensation ramp and the current-sense amplifier CSA_ output.

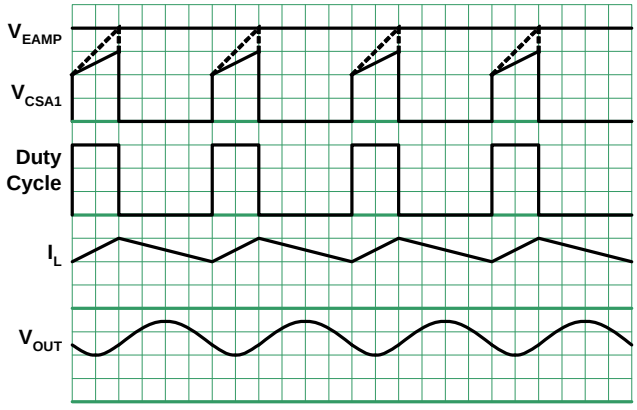


FIGURE 49. PWM OPERATION WAVEFORMS

The output voltage is regulated by controlling the reference voltage to the current loop. The bandgap circuit outputs a 0.8V reference voltage to the voltage control loop. The feedback voltage signal comes from the FB pin. The soft-start block only affects the operation during the start-up and will be discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 27pF and 390kΩ RC network. The maximum EAMP voltage output is precisely clamped to the bandgap voltage (1.172V).

Synchronization Control

The synchronization frequency can be operated to a range of 6MHz to 8MHz by an external signal applied to the SYNC pin. The SYNC pin has logic threshold levels of 0.4V and 1.5V for LOW and HIGH respectively, to allow for external clock signals to be of different magnitude regardless of supply voltage to ISL78236. The 1st falling edge on the SYNC triggers the rising edge of the PWM ON pulse of Channel 1. The 2nd falling edge of the SYNC triggers the rising edge of the PWM ON pulse of Channel 2. Typically, the pulse width of the SYNC signal should be 50% duty cycle, however, it is recommended that the pulse width be in the range of 50ns to 100ns for valid synchronization. This process alternates indefinitely allowing 180° output phase operation between the two channels. It is important to note that this operation makes the switching frequency of each channel 1/2 of the SYNC frequency. Thus, Channel 1 and Channel 2 have a synchronized switching frequency of 3MHz to 4MHz.

Output Current Sharing

The ISL78236 dual outputs are paralleled for multi-phase operation in order to support 6A output. Channel 1 and Channel 2 switches 180° out-of-phase to reduce input ripple currents. In parallel configuration, external soft-start should be used to ensure proper full loading start-up. Connect the FBx pins together and connect a soft-start capacitor from SS pin to GND. External compensation using the COMP pin is required for current sharing operation. Please see Table 2 for recommended values in current sharing mode. The current sharing balancing is dependent on the current sense amplifier matching between the two channels. The matching is internally trimmed and provides excellent balancing of output currents. See Figures 47 and 48 for typical output current matching.

Overcurrent Protection

CSA1 and CSA2 are used to monitor Output 1 and Output 2 channels respectively. The overcurrent protection is realized by monitoring the CSA output with the OCP threshold logic, as shown in the "Block Diagram" on page 5. The current sensing circuit has a gain of 0.2V/A, from the P-MOSFET current to the CSA output. When the CSA output reaches the threshold, the OCP comparator is tripped to turn off the P-MOSFET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFETs.

Upon detection of overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the Overcurrent Fault Counter is set to 1 and the Overcurrent Condition Flag is set from LOW to HIGH. If, on the subsequent cycle, another overcurrent condition is detected, the OC Fault Counter will be incremented. If there are 17 sequential OC fault detections, the regulator will be shut down under an Overcurrent Fault Condition. An Overcurrent Fault Condition will result with the regulator attempting to restart in a hiccup mode with the delay between restarts being 8 soft-start periods. At the

end of the eighth soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away prior to the OC Fault Counter reaching a count of four, the Overcurrent Condition Flag will set back to LOW.

The ISL78236 also features current sense amplifiers on the N-MOSFET for Negative Overcurrent Protection. If the negative output current reaches -2.5A, the part enters Negative OCP. At this point, all switching stops and the part enters tri-state mode while the pull-down FET is discharging the output until it reaches normal regulation voltage, then the IC restarts.

Power-Good (PG)

There are two independent power-good signals. PG1 monitors the Output Channel 1 and PG2 monitors the Output Channel 2. When powering up, the open-collector Power-Good output holds low for about 1ms after the output reaches within 8% of the preset output voltage. The PG pin will pull low under fault conditions when an overcurrent, OTP or UVLO event occurs.

UVLO

When the input voltage is below the undervoltage lockout (UVLO) threshold (2.85V MAX), the regulator is disabled and the PG pin will pull low.

Enable

The enable (ENx) inputs allows the user to control the turning on or off each channel of the regulator for purposes such as low power shutdown or power-up sequencing. When the regulator is enabled, there is typically a 600µs delay for waking up the bandgap reference, afterwards the soft start-up sequence begins.

Soft Start-Up

The soft-start-up eliminates the in-rush current during the start-up. The soft-start block outputs a ramp reference to both the voltage loop and the current loop. The two ramps limit the inductor current rising speed as well as the output voltage speed so that the output voltage rises in a controlled fashion. When the FB voltage is less than 0.2V, the PWM operating frequency is 1/2 of the normal frequency.

When the SS soft-start pin is tied to the VIN pin, the soft start-up time is internally set to 1.5ms. This internal soft-start mode is only for dual output operation. In current sharing mode, for externally programmable soft-start time, connect a capacitor from the SS pin to GND. A 5µA current source charges up the soft-start capacitor and sets the soft-start ramp time. The soft-start capacitor, C_{SS}, should not be larger than 33nF. See Equation 2 for calculating the soft-start ramp time.

It is recommended to operate the internal soft-start ramp time only in Dual Output Mode. In Current Share Mode external soft-start should be used.

$$t_{SS[S]} = \frac{C_{SS[\mu F]}}{6.25} \quad \text{(EQ. 2)}$$

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs, or the input UVLO fault latch is set, the LX pin discharges to PGND through an internal 100Ω switch.

Power MOSFETs

The integrated high-side and low-side power MOSFETs are optimized for best efficiency while delivering up to 3A current. The ON-resistance for the P-MOSFET is typically 50mΩ and the ON-resistance for the N-MOSFET is typical 50mΩ.

100% Duty Cycle

The ISL78236 features 100% duty cycle operation to maximize the battery life in portable applications. When the battery voltage drops to a level that the ISL78236 can no longer maintain the regulation at the output, the regulator completely turns on the P-MOSFET. The maximum dropout voltage under the 100% duty cycle operation is the product of the load current and the ON-resistance of the P-MOSFET.

Thermal Shutdown

The ISL78236 has built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shut down. As the temperature drops to +125°C, the ISL78236 resumes operation by stepping through a soft start-up.

Applications Information

Output Inductor and Capacitor Selection

To consider steady state and transient operation, ISL78236 typically uses a 0.6µH output inductor. Higher or lower inductor value can be used to optimize the total converter system performance. For example applications with output voltage >3.3V, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. The inductor ripple current can be expressed in Equation 3:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_S} \quad \text{(EQ. 3)}$$

The inductor's saturation current rating needs to be larger than the peak current. The ISL78236 overcurrent protection threshold is typically 4.8A. The saturation current needs to be over 4.8A for maximum output current application.

ISL78236 uses an internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R. The recommended minimum output capacitor values for the ISL78236 are shown in Table 3.

TABLE 3. MINIMUM OUTPUT CAPACITOR VALUE vs V_{OUT}

V_{OUT} (V)	C_{OUT} (µF)	L (µH)
1.2	2 x 22	0.5~1.1
1.6	2 x 22	0.5~1.1
1.8	2 x 22	0.5~1.68
2.5	2 x 22	0.5~1.68
3.3	2 x 6.8	0.5~2.2
3.6	10	0.5~2.2

In Table 3, the minimum output capacitor value is given for different output voltages to make sure the converter system is stable.

While ceramic capacitors offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturers data sheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction will generally suffice. The result of these considerations may mean an effective capacitance 50% lower than nominal and this value should be used in all design calculations. Nonetheless, ceramic capacitors are a very good choice in many applications due to their reliability and extremely low ESR.

Equations 4 and 5 allow calculation of the required capacitance to meet a desired ripple voltage level. Additional capacitance may be used.

For the ceramic capacitors (low ESR):

$$V_{OUTripple} = \frac{\Delta I}{8 * F_{SW} * C_{OUT}} \quad \text{(EQ. 4)}$$

where ΔI is the inductor's peak-to-peak ripple current, F_{SW} is the switching frequency and C_{OUT} is the output capacitor.

If using electrolytic capacitors then:

$$V_{OUTripple} = \Delta I * ESR \quad \text{(EQ. 5)}$$

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider, which is used to scale the output voltage relative to the internal reference voltage and feed it back to the inverting input of the error amplifier. Refer to Figures 3 and 4.

The output voltage programming resistor, R_2 (or R_5 in Channel 2), will depend on the desired output voltage of the regulator. The value for the feedback resistor is typically between 50kΩ and 312.5kΩ. Setting R_2 and V_{OUT}, R_3 will be:

$$R_3 = \frac{R_2 x 0.8V}{V_{OUT} - 0.8V} \quad \text{(EQ. 6)}$$

For better performance, add 12pF in parallel with R_2 (or R_5) for faster transient response.

Minimum Output Voltage

The ISL78236 switching frequency F_S (2.5MHz typical, 2.85MHz max) and the minimum LX pin ON Time (140ns, max) sets a minimum duty cycle of the converter under worst case scenario of 0.4 across temperature. Because of this minimum duty cycle, there is an input V_{IN} to output V_{OUT} range the ISL78236 is capable of regulating to. The ratio of output to input (V_{OUT}/V_{IN}) must be higher than 0.4 to maintain output voltage regulation. For example, it is not recommended to regulate below 2.0V for V_{IN} = 5V and below 1.2V for V_{IN} = 3V as the minimum duty cycle limitation will impact output voltage. Note that when external synchronization is used, the switching frequency is higher than 2.85MHz which further restricts the V_{OUT}/V_{IN} range of operation.

Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current flowing back to the battery rail. One 22µF X5R or X7R ceramic capacitor is a good starting point for the input capacitor selection per channel.

Loop Compensation Design

When a soft-start capacitor is connected to the SS pin, the COMP pin is active for external loop compensation. The ISL78236 uses constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant, and the system becomes a single order system. It is much easier to design a type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 50 shows the small signal model of the synchronous buck regulator.

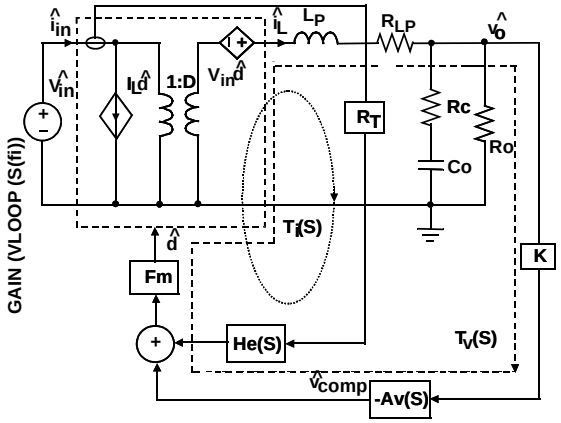


FIGURE 50. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR

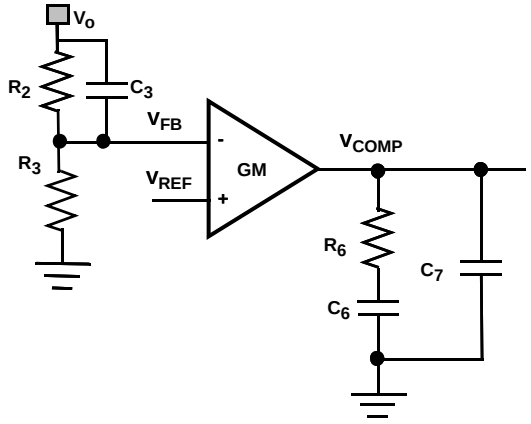


FIGURE 51. TYPE II COMPENSATOR

Figure 51 shows the type II compensator and its transfer function is expressed, as shown in Equation 7:

$$A_V(S) = \frac{\hat{v}_{COMP}}{\hat{v}_{FB}} = \frac{GM \cdot R_3}{(C_6 + C_7) \cdot (R_2 + R_3)} \cdot \frac{\left(1 + \frac{S}{\omega_{cz1}}\right)\left(1 + \frac{S}{\omega_{cz2}}\right)}{S\left(1 + \frac{S}{\omega_{cp1}}\right)\left(1 + \frac{S}{\omega_{cp2}}\right)} \quad \text{(EQ. 7)}$$

where,

$$\omega_{cz1} = \frac{1}{R_6 C_6},\ \omega_{cz2} = \frac{1}{R_2 C_3},\ \omega_{cp1} = \frac{C_6 + C_7}{R_6 C_6 C_7},\ \omega_{cp2} = \frac{R_2 + R_3}{C_3 R_2 R_3}$$

Compensator design goal:

High DC gain

Choose Loop bandwidth f_c 100kHz or below

Gain margin: >10dB

Phase margin: >40°

The compensator design procedure is as follows:

The loop gain at crossover frequency of f_c has a unity gain. Therefore, the compensator resistance R_6 is determined by Equation 8.

$$R_6 = \frac{2\pi f_c V_o C_o R_t}{GM \cdot V_{FB}} = 15.7\times10^3 \cdot f_c V_o C_o \quad \text{(EQ. 8)}$$

Where R_t is the current sense amplifier gain (0.2V/A) and GM is the trans-conductance, g_m, of the voltage error amplifier in each phase (see "Electrical Specification" Table for "Error Amplifier Trans-Conductance" on page 8). Compensator capacitor C_6 and C_7 is then given by Equation 9.

$$C_6 = \frac{R_o C_o}{R_6} = \frac{V_o C_o}{I_o R_6}, C_7 = \max\text{ of }\left(\frac{R_c C_o}{R_6}, \frac{1}{\pi f_s R_6}\right) \quad \text{(EQ. 9)}$$

An optional zero can boost the phase margin. ω_{CZ2} is a zero due to R_2 and C_3.

$$C_3 = \frac{1}{\pi f_c R_2} \quad \text{(EQ. 10)}$$

Example: V_{IN} = 5V, V_O = 1.8V, I_O = 3A, Fs = 2.5MHz, R_2 = 124kΩ, R_3 = 100kΩ, C_o = 2X22µF/3mΩ, L = 0.6µH, f_c = 100kHz, then compensator resistance R_6:

$$R_6 = 15.7\times10^3 \cdot 100\text{kHz} \cdot 1.8\text{V} \cdot 44\mu\text{F} = 124\text{k}\Omega \quad \text{(EQ. 11)}$$

Use a standard 124kΩ 1% tolerance or better resistor.

$$C_6 = \frac{1.8\text{V} \cdot 44\mu\text{F}}{3\text{A} \cdot 124\text{k}\Omega} = 213\text{pF} \quad \text{(EQ. 12)}$$

$$C_7 = \max\left(\frac{3\text{m}\Omega \cdot 44\mu\text{F}}{124\text{k}\Omega}, \frac{1}{\pi \cdot 2.5\text{MHz} \cdot 124\text{k}\Omega}\right) = (1\text{pF}, 1\text{pF}) \quad \text{(EQ. 13)}$$

Use the closest standard values for C_6 and C_7. There is approximately 2pF parasitic capacitance from V_{COMP} to GND; Therefore, C_7 is optional. Use C_6 = 220pF and C_7 = OPEN.

$$C_3 = \frac{1}{\pi \cdot 100\text{kHz} \cdot 124\text{k}\Omega} = 26\text{pF} \quad \text{(EQ. 14)}$$

Use C_3 = 22pF. Note that C_3 may increase the loop bandwidth from previous estimated value.

PCB Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well. For ISL78236, the power loop is composed of the output inductor L's, the output capacitor C_{OUT1} and C_{OUT2}, the LX's pins, and the PGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide. The switching node of the converter, the LX pins, and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The FB network should be as close as possible to its FB pin. SGND should have one single connection to PGND. The input capacitor should be placed as closely as possible to the VIN pin. Also, the ground of the input and output capacitors should be connected as closely as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least 5 vias ground connection within the pad for the best thermal relief.

Thermal Performance

Delivering a full load output current of 6A across the ambient operating temperature is strongly dependent on the thermal characteristic of the PCB layout. The power dissipation of the IC and the thermal impedance of the board will result in a temperature gradient between ambient and junction. Power dissipation curves for typical application can be found in Figures 7 and 8 for dual output operation and Figures 37 and 38 for current sharing operation. If the junction temperature exceeds the +150°C over-temperature protection threshold the regulator will be disabled.

The theta JA (θ_{JA}) spec shown in the "Thermal Information" on page 8 is based upon JEDEC standard JESD51-5. However, real world application boards will differ from the JEDEC standard thus producing different theta JA results. For example, the JESD51-5 specifies the thermal attach pad via only to the top buried layer. Most practical applications will have the via connect to all layers of the PCB board ground plane. JESD51-5 also requires that buried planes use 1 oz. copper while the outer planes use 2 oz. copper. It is recommended to have 2 oz. or greater copper on all layers in application boards.

It is essential to have the package thermal pad connected to a top layer PCB ground pad with the via connecting to additional ground planes. This is where most of the thermal relief will occur. The four PGND pins of the ISL78236 should be connected to the thermal pad also. These connections provide the extra thermal relief to minimize theta JA allowing the ISL78236 to maintain full output current up to +105°C. See Figure 52 for an example layout of the thermal relief pad.

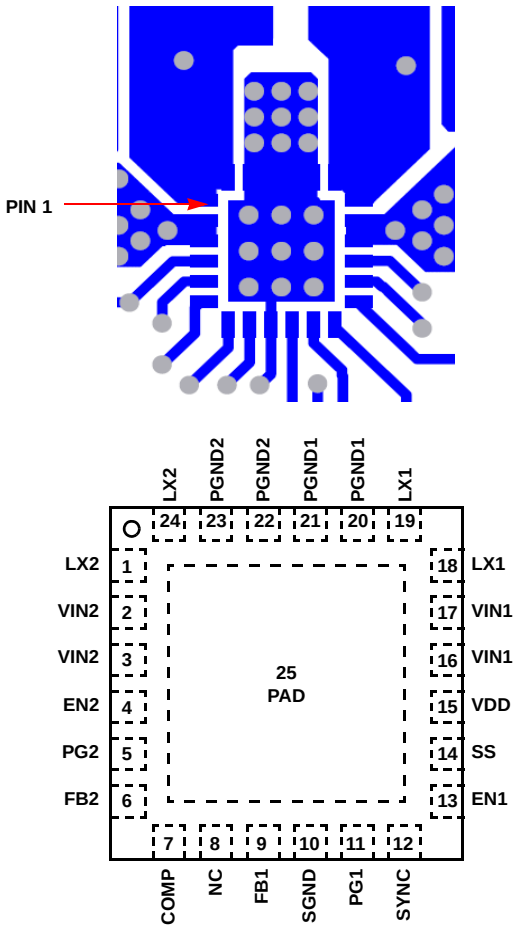


FIGURE 52. RECOMMENDED THERMAL PAD LAYOUT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
April 28, 2014	FN8624.0	Initial Release.

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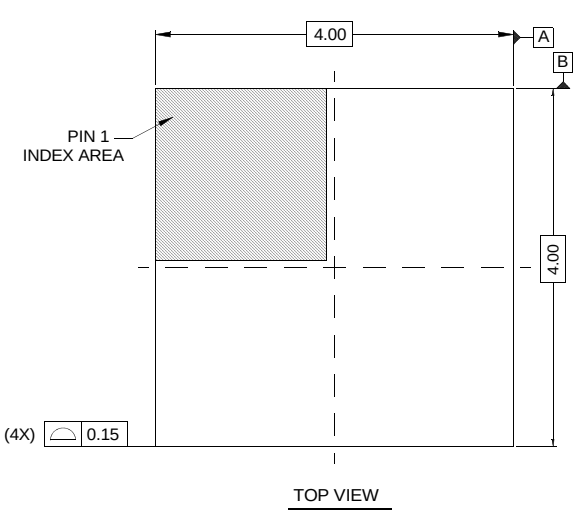
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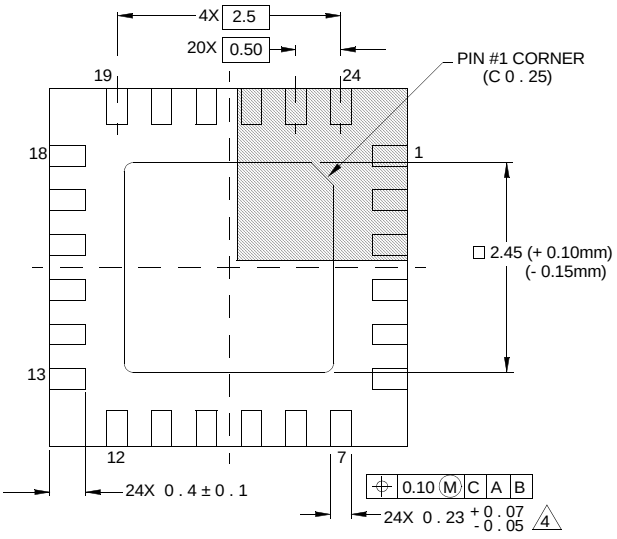
Package Outline Drawing

L24.4x4D

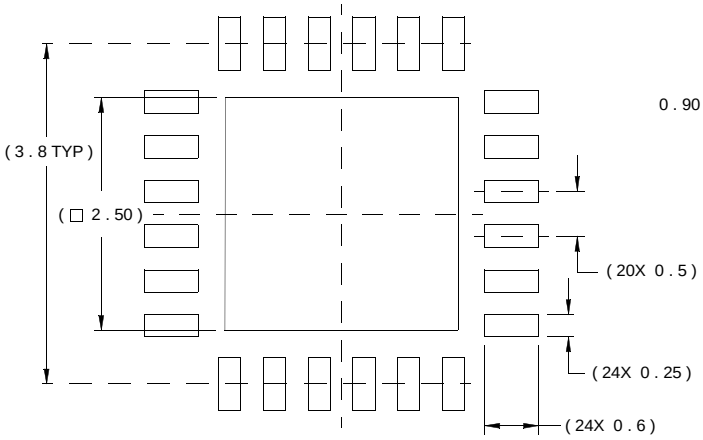
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 3, 11/13



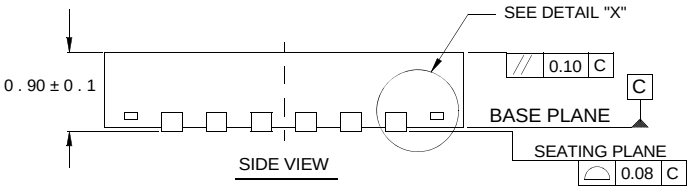
TOP VIEW



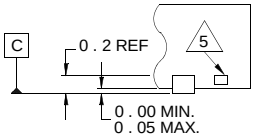
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.